RN6752V1

Data Sheet

1-Channel HD Video Decoder With MIPI CSI2 Output

(Rev. 1.6)

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Revision History

Revision	Date	Notes
1.1	2019-08-13	Initial draft.
1.2	2019-08-22	Modified application diagram and some register description.
1.3	2019-09-16	Modified ordering information
1.4	2019-11-05	Modified ground description
1.5	2019-12-13	Modified product ID
1.6	2020-08-06	Added Digital I/O AC characteristic

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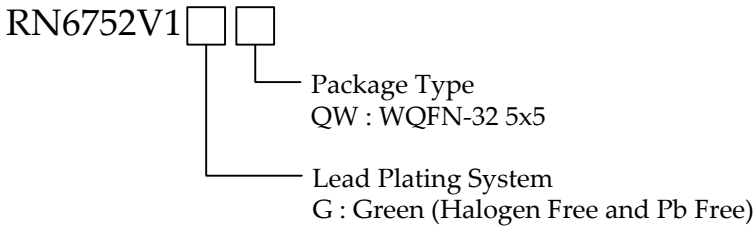
1 General Description

The RN6752V1 is an analog high definition (Analog HD) video decoder IC designed for automotive applications. It integrates all necessary functional blocks: AFE, PLL, Decoding Logic, MIPI and I2C interface, etc., in a small 5mm x 5mm footprint, 32-pin QFN package. The decoder converts composite analog video input of up to full HD (FHD, 1080p) resolution to digital component video format (YCbCr) and sends the data via the MIPI interface to the host controller IC for further processing.

The RN6752V1 supports multiple video formats including most popular formats from products of major camera suppliers. In addition, key format parameters such as resolution, frame rate, aspect ratio, etc. can be customized to meet specific requirements in automotive video. Due to its configurable, feature-rich design, challenges in e-mirror, driver monitoring, surround viewing and many other situations in demanding automotive applications can be effectively addressed. This single-channel decoder IC meets the highest quality and reliability criteria and can operate over temperature range from -40°C to 85°C.

2 Ordering Information



Note:
Richnex products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

3 Contact Information

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4 Features

Video Decoder

- MIPI CSI2 interface supporting 4 data lanes
- Multi-format video decoder, covering FHD (1080p), HD (720p) and D1 (480i) analog video resolution
- Automatic format detection
- I2C interface for control and status registers access
- Video input pins meeting 8KV (HBM) ESD compliance
- Operation temperature range from -40°C to 85°C
- 3.3V and 1.2V power supplies
- Flexible 1.8V to 3.3V I/O interface voltage
- 32pin QFN package (5mm x 5mm)

5 Block Diagram

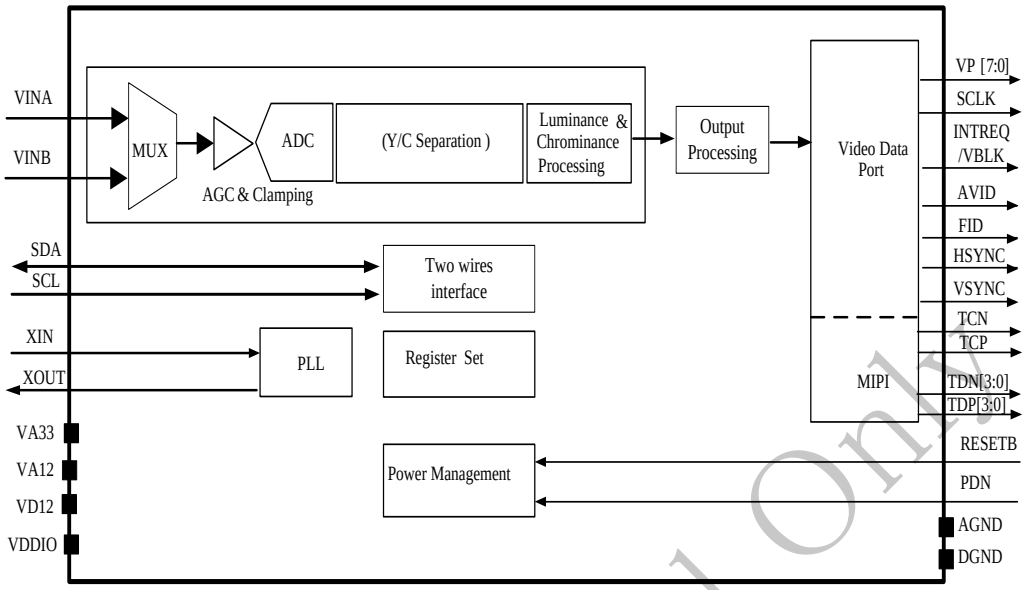


Figure 1: RN6752V1 Functional Block Diagram

6 Pin Diagram

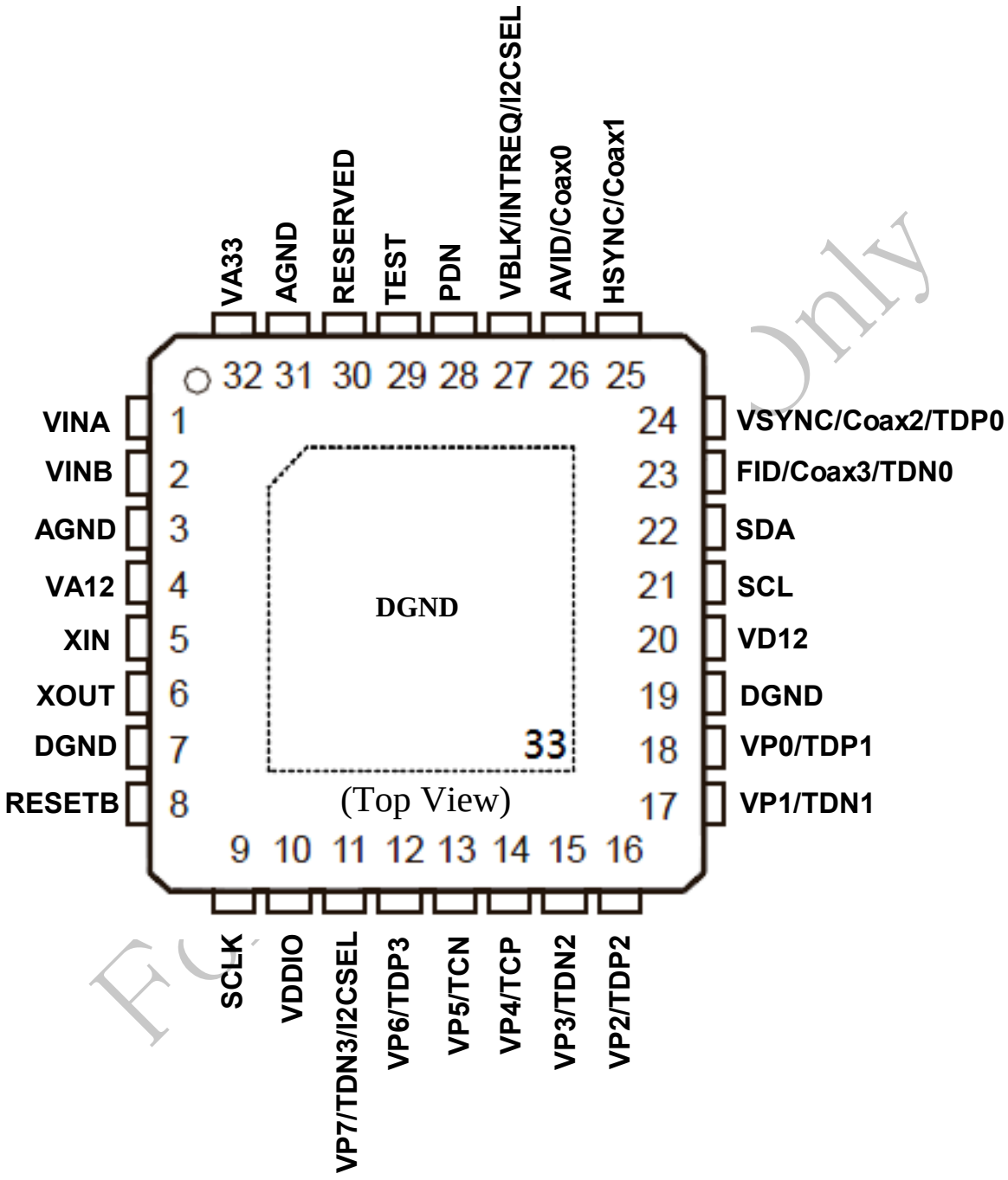


Figure 2: RN6752V1 Pin Diagram

7 Pin Descriptions

Table 1: RN6752V1 Pin Definition

Analog Video Interface

Name	Pin Number	Type	Reset State	Description
VINA	1	A		Analog video input A
VINB	2	A		Analog video input B

Digital Video Interface (shared with MIPI Video Interface)

Name	Pin Number	Type	Reset State	Description
SCLK	9	O	HiZ	Video clock
VP[7:0] I2CSEL	[11,12,13,14,15,16,17,18] 11	O I	HiZ	Video data port I²C select (shared with VP[7])
FID Coax3	23	O IO O	HiZ	Timing signal and status indicator FID also can be programmed as a GPIO pin. Coaxitron control
VSYNC Coax2	24	O IO O	HiZ	Timing signal and status indicator VSYNC also can be programmed as a GPIO pin. Coaxitron control
HSYNC Coax1	25	O IO O	HiZ	Timing signal and status indicator HSYNC also can be programmed as a GPIO pin. Coaxitron control
AVID Coax0	26	O IO O	HiZ	Timing signal and status indicator AVID also can be programmed as a GPIO pin. Coaxitron control
VBLK /INTREQ I2CSEL	27	O IO I	HiZ	Interrupt/Timing signal and status indicator VBLK also can be programmed as a GPIO pin. I²C select (shared with VBLK pin)

MIPI Video Interface (shared with Digital Video Interface)

Name	Pin Number	Type	Reset State	Description
TDN[3:0] TCN	11,13,15, 17,23	O	HiZ	MIPI negative data/clock lane output These pins also can be programmed as a MIPI negative clock/data lane output
TDP[3:0] TCP	12,14,16, 18,24	O	HiZ	MIPI positive data/clock lane output These pins also can be programmed as a MIPI positive clock/dat lane output

System Control

Name	Pin Number	Type	Reset State	Description
SCL	21	I	HiZ	I²C serial clock (pull-up SCL with 4.7K Ohm resistor)
SDA	22	IO	HiZ	I²C serial data (pull-up SDA with 4.7K Ohm resistor)
RESETB	8	I	HiZ	Global chip reset (active low)
PDN	28	I	HiZ	Power down signal (active low)
XIN	5	I	HiZ	External reference clock input or crystal input
XOUT	6	O	HiZ	External crystal output
TEST	29	I	HiZ	Recommend floating
RESERVED	30			Reserved pin (Must be floating)

Power

Name	Pin Number	Type	Reset State	Description
VDDIO	10	P		Internal 1.8V or external 3.3V IO post-driver
VD12	20	P		1.2V digital power
AGND	3,31	P		Analog ground
DGND	7,19, 33 (EP)	P		Digital ground (EP = exposed pad)
VA12	4	P		1.2V analog power.
VA33	32	P		3.3V analog power.

8 I²C address setting

RN6752V1 provides an I²C slave interface for programming internal control registers. After power-on or the external reset has transitioned from low to high, RN6752V1 will capture I2CSEL pin state to determine its I²C device address. User can set their desired device address through weak pull-up/down on this pin. The I²C address can be either 0x2C or 0x2D.

I2CSEL	Pulled up/down	RN6752V1's I²C device address
0	Pulled down or floating: I2CSEL	0x2C
1	Pulled up: I2CSEL	0x2D

9 Register Map

RN6752V1 integrates 1 video decoders and one MIPI CSI-2 links interface in one I²C slave device. The register set is outlined in the following index map. There are 3 sets of indexes, 0x00 to 0x7F, which are used for each individual video decoder control and MIPI interface control. Access to these 3 sets of registers is selectable via RegFF. Index 0x80 to 0xFE registers are used for chip-level control operations.

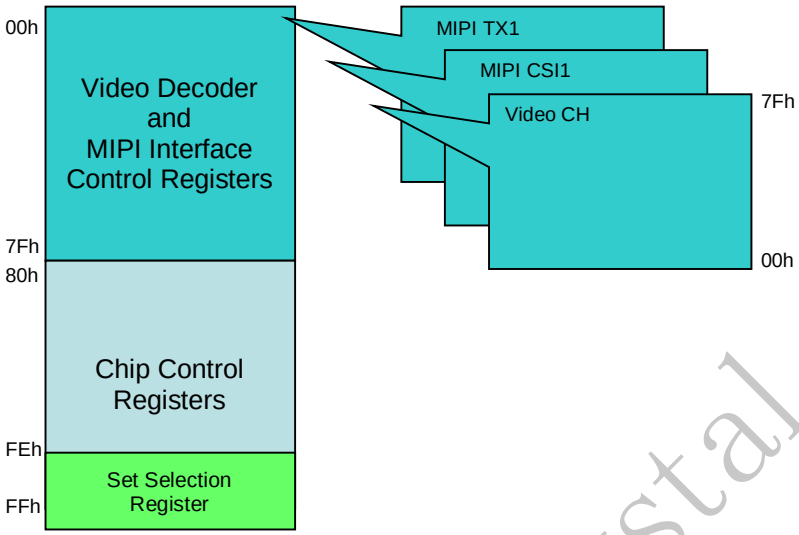


Figure 3: RN6752V1 Register Index Map

The I²C interface supports single or multiple write/read accesses whose register addresses are in sequential order as illustrated in the following two figures. The first figure illustrates the write format for a one-byte write and a multiple-byte write. The second figure describes the transfer format for a single-byte read and a multiple-byte read. In the first byte, after start symbol, the I²C Device Address [6:0] is located at bit 7~1, and bit 0 is for the identification of write (bit0 = 0) or read (bit0 = 1) operation. So the 1st byte after start symbol is 0x58 if users perform the write transfer to the I²C Device Address 0x2C.

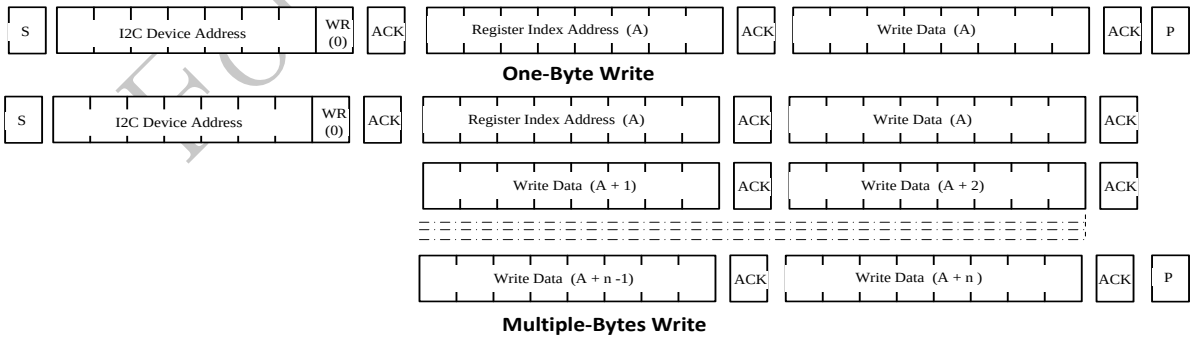


Figure 4: I2C One and Multi-byte Write Operation Sequence

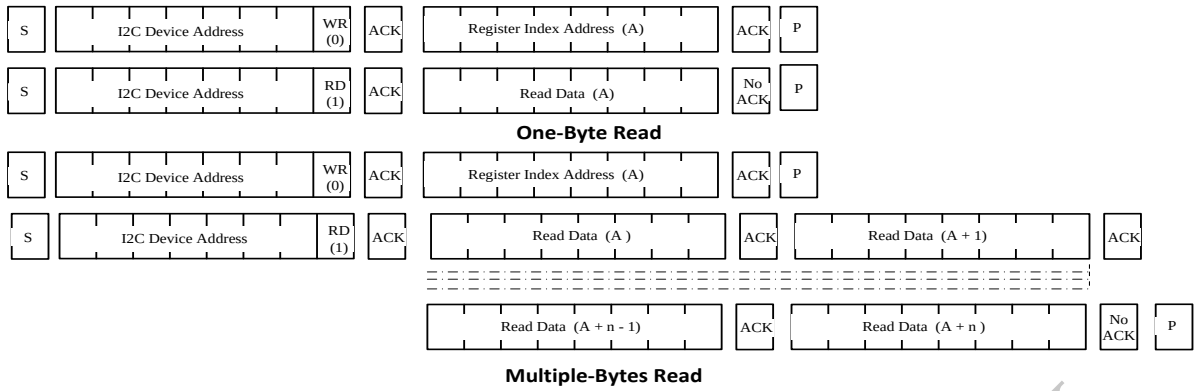


Figure 5: I2C One and Multiple-byte Read Operation Sequence

9.1 Chip Control Registers

9.1.1 Central Control Register

9.1.1.1. Reset / Sleep Control Register

Address: 80h (R/W). Default: 30h.

Bits	Field Name	Description
0	Soft_GRST	Software Global Reset
1	Reserved	Must be 0h.
2	Soft_PWRD	Software Power Down
7:3	Reserved	Must be 6h.

9.1.1.2. Analog Macro Control Register

Address: 81h (R/W). Default: 01h.

Bits	Field Name	Description
0	CH_ON	Channel Enable
7:1	Reserved	Not used.

9.1.2 Video Clock Configuration Register

RN6752V1 supports one independent clock pins, SCLK, which is synchronous with all video data ports. After the power-on/reset sequence has been completed, the SCLK will output 27MHz clock, and the video data port VP[7:0] will be in tri-state.

9.1.2.1. Video Clock Configuration A

SCLK1: Address: 88h (R/W). Default: 01h.

Bits	Field Name	Description
0	EN_SCK	Clock Enable
1	INV_SCK	Clock Invert
5:2	DL_SCK	Clock Output Delay Selection
7:6	DS_SCK	Clock Output Drive Strength

9.1.2.2. Video Clock Configuration B

SCLK1: Address: 89h (R/W). Default: 00h.

Bits	Field Name	Description
2:0	FSEL_SCK	Clock Output Frequency Selection
3	EN960M_SCK	Clock Frequency Base Selection
6:4	PHSEL_SCK	Clock Phase Delay Selection
7	Reserved	N/A

9.1.3 **Video Data Port Configuration Register**

In ITU-R BT.656 format, there is one timing reference codes: one at the beginning of each video data block (start of active video, SAV) and one at the end of each video data block (end of active video, EAV). Each timing reference code consists of a four-word sequence in the following format: (FFh, 00h, 00h, XYh). The first three words are a fixed preamble. The fourth word contains information defining field identification, the state of field blanking, and the state of line blanking.

The data between EAV and SAV is the horizontal blanking code. The data between SAV and EAV is the valid Y/Cb/Cr color component value.

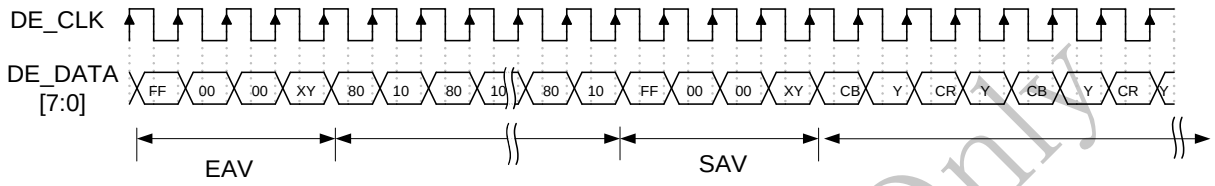


Figure 6: Standard ITU-R BT.656 Format

Like standard ITU-R BT.656 format, RN6752V1 provides a modified ITU-R BT.656 format which inserts decoder information such as channel identification or indicator's status.

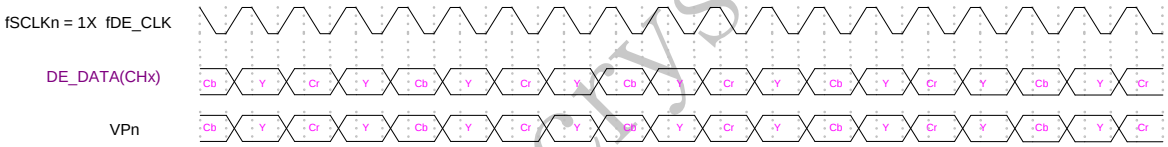


Figure 7: Single Channel Output Format

9.1.3.1. Video Data Port Configuration A

VP[7:0]: Address: 8Dh (R/W). Default: 00h.

Bits	Field Name	Description
0	EN_VP	Video Port Enable
2:1	VP_PRATE	The value of these parameters must be set to 0h.
3	VP_SRC	This bit must be set to 0.
5:4	DS_VP	VP[7:0] : Drive Strength Selection
7:6	VP_DEVSEL	Device Source Selection

9.1.3.2. Video Data Port Configuration B

VP[7:0]: Address: 8Eh (R/W). Default: 04h.

Bits	Field Name	Description
1:0	VP_MODE	VP[7:0] : Output Mode Selection
3:2	VP_CHANSEL	Data Stream Output Selection (only for VP_MODE = 0)

Bits	Field Name	Description
7:4	VP_DDR_PAIR	Reserved

9.1.3.3. Video Data Port Configuration C

VP[7:0]: Address: 8Fh (R/W). Default: 00h.

Bits	Field Name	Description
3:0	DL_VP	VP[7:0] : Output Delay
6:4	VP_PHSEL	VP[7:0] : Output Phase Delay (only for VP_MODE = 0)
7	VP_EN960M	Output Data Source Format Selection

VP[7:0]: Address: A3h (R/W). Default: 00h.

Bits	Name	Description
1:0	Reserved	Must be 0h.
2	EN_HD_OUT	Enable HD Output.
3	VP_ORDER	Pin Order selection
7:4	Reserved	Must be 0h.

9.1.4 GPIO Pin Configuration Register

RN6752V1 provides 5 programmable outputs: VBLK, AVID, FID, VSYNC, and HSYNC. Each of the outputs can be programmed to provide video timing information such as: video blanking, active video, field, vertical sync, or horizontal sync. They can also be used to provide various status information that include: no video detect, PAL/NTSC indicator, VHS detect, color-kill, progressive video detect. Finally, any one of the five outputs can be programmed to transmit Coaxitron protocol data.

In addition to the above functions, users can set *_ENGP as 1 to enable the GPIO function of the video timing pins. When *_GPIO_DIR is 0, the video timing pin is an output pin and the output value is depended on *_GPO. When *_GPIO_DIR is 1, the video timing pin is an input pin, and the input value can be read from Reg98 and Reg9C.

9.1.4.1. Video Timing Pin Enable Register

Address: 96h (R/W). Default: 40h.

Bits	Field Name	Description
0	AVID_ENGP	Video Status and GPIO Function Select
1	VBLK_ENGP	Video Status and GPIO Function Select
2	FID_ENGP	Video Status and GPIO Function Select
3	VSYNC_ENGP	Video Status and GPIO Function Select
5:4	AVID_CHANSEL	Select Indicator Source For AVID Pin (only for AVID_ENGP = 0)
7:6	VBLK_CHANSEL	Select Indicator Source For VBLK Pin (only for VBLK_ENGP = 0)

Address: 9Ah (R/W). Default: 40h.

Bits	Field Name	Description
0	HSYNC_ENGP	Video Status and GPIO Function Select

Bits	Field Name	Description
3:1	Reserved	Not used.
5:4	HSYNC_CHANSEL	Select Indicator Source For HSYNC Pin (only for HSYNC_ENGP = 0)
7:6	Reserved	Not used.

9.1.4.2. Video Timing Pin Direction Control Register

Address: 97h (R/W). Default: E0h.

Bits	Field Name	Description
0	AVID_GPIO_DIR	When AVID_ENGP is 0, AVID_GPIO_DIR's usage is as follows: 1: Enable status indicator output on AVID pin. 0: AVID pin input and output are disabled. When AVID_ENGP is 1, AVID_GPIO_DIR becomes GPIO Direction Control. 1: Set AVID pin to GPIO input. 0: Set AVID pin to GPIO output.
1	VBLK_GPIO_DIR	When VBLK_ENGP is 0, VBLK_GPIO_DIR's usage is as follows: 1: Enable status indicator output on VBLK pin. 0: VBLK pin input and output are disabled. When VBLK_ENGP is 1, VBLK_GPIO_DIR becomes GPIO Direction Control. 1: Set VBLK pin to GPIO input. 0: Set VBLK pin to GPIO output.
2	FID_GPIO_DIR	When FID_ENGP is 0, FID_GPIO_DIR's usage is as follows: 1: Enable status indicator output on FID pin. 0: FID pin input and output are disabled. When FID_ENGP is 1, FID_GPIO_DIR becomes GPIO Direction Control. 1: Set FID pin to GPIO input. 0: Set FID pin to GPIO output.
3	VSYNC_GPIO_DIR	When VSYNC_ENGP is 0, VSYNC_GPIO_DIR's usage is as follows: 1: Enable status indicator output on VSYNC pin. 0: VSYNC pin input and output are disabled. When VSYNC_ENGP is 1, VSYNC_GPIO_DIR becomes GPIO Direction Control. 1: Set VSYNC pin to GPIO input. 0: Set VSYNC pin to GPIO output.
5:4	FID_CHANSEL	Select Indicator Source For FID Pin (only for FID_ENGP = 0)
7:6	VSYNC_CHANSEL	Select Indicator Source For VSYNC Pin (only for VSYNC_ENGP = 0)

Address: 9Bh (R/W). Default: E0h.

Bits	Field Name	Description
0	HSYNC_GPIO_DIR	When HSYNC_ENGP is 0, HSYNC_GPIO_DIR's usage is as follows:

Bits	Field Name	Description
		1: Enable status indicator output on HSYNC pin. 0: HSYNC pin input and output are disabled. When HSYNC_ENGP is 1, HSYNC_GPIO_DIR becomes GPIO Direction Control. 1: Set HSYNC pin to GPIO input. 0: Set HSYNC pin to GPIO output.
7:1	Reserved	Not used.

9.1.4.3. Video Timing Pin GPIO Register

Address: 98h (R/W). Default: 00h.

Bits	Field Name	Description
0	AVID_GPO	Set the AVID GPO value or shows the AVID input value.
1	VBLK_GPO	Set the VBLK GPO value or shows the VBLK input value.
2	FID_GPO	Set the FID GPO value or shows the FID input value.
3	VSYNC_GPO	Set the VSYNC GPO value or shows the VSYNC input value.
4	AVID_SRC	Video Timing or Interrupt Output Select
5	VBLK_SRC	Video Timing or Interrupt Output Select
6	FID_SRC	Video Timing or Video Timing or Interrupt Output Select
7	VSYNC_SRC	Video Timing or Interrupt Output Select

Address: 9Ch (R/W). Default: 00h.

Bits	Field Name	Description
0	HSYNC_GPO	Set the HSYNC GPO value or shows the HSYNC input value.
3:1	Reserved	Not used.
4	HSYNC_SRC	Video Timing or Interrupt Output Select
7:5	Reserved	Not used.

9.1.5 Video ADC MUX Configuration

Address: D3h (R/W). Default: 00h.

Bits	Field Name	Description
1:0	SELV	Video ADC Input Selection
7:2	Reserved	N/A

9.1.6 Video Format Selection Register

Address: DFh (R/W). Default: F0h.

Bits	Field Name	Description
0	VIDEO_CHAN_SEL	FHD/HD/SD Selection
7:1	Reserved	N/A.

Address: F0h (R/W). Default: 1Fh.

Bits	Field Name	Description
5:0	Reserved.	N/A

Bits	Field Name	Description
6	POP144	Enable Top FIFO Output
7	EN_BT144	Enable 144 MHz Decoder Output

9.1.7 **Product ID, Low Byte**

Address: FDh (RO). Default: 01h.

Bits	Field Name	Description
3:0	Chip Package	Product package information
7:4	Reserved	N/A

9.1.8 **Product ID, High Byte**

Address: FEh (RO). Default: 26h.

Bits	Field Name	Description
4:0	Chip PID	The product ID code
7:5	Chip Version	The product revision code

9.1.9 **Register Set Selection**

Address: FFh (R/W). Default: 00h.

Bits	Field Name	Description
7:0	REG_SET_SEL	Register Set Select

9.2 Video Decoder Control Registers

9.2.1 **Mode Control Register**

Address: 00h (WO).

Bits	Field Name	Description
3:0	Reserved	Reserved
5:4	OPM	Decoder Operation Mode Select
7:6	TESTPAT	Test Output Select

Address: 00h (RO).

Bits	Field Name	Description
0	F30	System Input Indicator
2:1	Reserved	Reserved
3	CKill	Color Kill Indicator
4	NoVid	No Video Input Indicator
7:5	VDet	Video Format Detect

Address: 4Bh (RO).Default: 00h.

Bits	Field Name	Description
0	720P_Format	0: Analog HD 1: other public analog HD 720P_Format is valid only when VDet = 1.
7:1	Reserved	Must be 0h.

9.2.2 **Brightness Control Register**

Address: 01h (R/W).Default: 00h.

Bits	Field Name	Description
7:0	Brit	Brightness Control 2's complement form, increases brightness (0~+127) if these bits are positive value. Decrease brightness (-1~ -128) if these bits are negative value.

9.2.3 **Contrast Control Register**

Address: 02h (R/W).Default: 80h.

Bits	Field Name	Description
7:0	Cont	Contrast Control Unsigned form. This 8-bit un-signed value defines the setting for the contrast adjustment. The nominal value is 80h.

9.2.4 **Saturation Control Register**

Address: 03h (R/W).Default: 80h.

Bits	Field Name	Description
7:0	Satu	Saturation Control Unsigned form. This 8-bit un-signed value defines the setting for the saturation adjustment. The nominal value is 80h.

9.2.5 **Hue Control Register**

Address: 04h (R/W).Default: 80h.

Bits	Field Name	Description
7:0	Hue	Hue Control Unsigned form. This 8-bit un-signed value defines the setting for the hue adjustment. The nominal value is 80h.

9.2.6 **Enhancement Control Register**

Address: 05h (R/W).Default: 08h.

Bits	Field Name	Description
6:0	EnhL	Peaking Control for Luma Enhancement. (2's complement form) This value is used to increase the amplitude of high frequency components of luma. A value of zero disables luma enhancement.
7	Reserved	Reserved

9.2.7 **Input Control Register**

Address: 07h (R/W).Default: 23h.

Bits	Field Name	Description
1:0	LOP	NTSC/PAL Operation Control
2	Reserved	Must be 0h.
3	Reserved	Must be 0h.
6:4	Reserved	Must be 2h.
7	Reserved	Reserved

9.2.8 **Output & Decoder Control Register**

Address: 08h (R/W).Default: 02h.

Bits	Field Name	Description
3:0	Reserved	Must be 2h.
4	InvHS	Invert internal HSync signal.
5	InvVS	Invert internal VSync signal.
6	InvF	Invert internal Field signal.
7	Reserved	N/A

Address: 09h (R/W).Default: 08h.

Bits	Field Name	Description
2:0	SwpUV	Swap Color Outputs
3	Reserved	Must be 1h.
4	Reserved	Reserved
5	Reserved	Reserved
6	XCKill	Disable Color Kill detection.
7	AutoEnhL	Enable EQ Feature

9.2.9 **Video Detection Control Register**

Address: 19h (R/W).Default: 00h.

Bits	Field Name	Description
3:0	VDHystS	Video Format Detection Hysteresis Control
7:4	Reserved	Must be 0h.

9.2.10 **Blue Screen Control Register**

Address: 1Ah (R/W).Default: 03h.

Bits	Field Name	Description
6:0	Reserved	Must be 3h.
7	NoBlue	Blue Screen Insertion Disable. If this bit is set, the insertion of blue screen will be disabled when no video is detected at the input.

9.2.11 **Cropping Control Register**

Address	Default	Bits	Field Name	Description
20h	A4h	1:0	HStart[9:8]	Image Cropping setting: {V0Start, V0End} defines field 0 active line range. {V1Start, V1End} defines field 1 active line range. {HStart, HEnd} defines active pixel range. {V0Start, V0End} and {V1Start, V1End} are valid only when VSelCrop = 2 or 3. {HStart, HEnd} is valid only when HSelCrop = 1.
		3:2	HEnd[9:8]	
		4	V0Start[8]	
		5	V0End[8]	
		6	V1Start[8]	
		7	V1End[8]	
21h	43h	7:0	HStart[7:0]	
22h	ACh	7:0	HEnd[7:0]	
23h	16h	7:0	V0Start[7:0]	
24h	05h	7:0	V0End[7:0]	
25h	16h	7:0	V1Start[7:0]	
26h	05h	7:0	V1End[7:0]	
28h	92h	3:0	Reserved	Must be 2h.
		5:4	VSelCrop	0: Reserved 1: • NTSC • PAL • 720p • 1080p/1080N 2, 3: Cropping range from register setting.
		6	HSelCrop	{HStart, HEnd} is valid only when HSelCrop = 1.
		7	Reserved	Reserved
41h	00h	0	HStart[10]	The MSB of HStart, used for HD output.
		4	HEnd[10]	The MSB of HEnd, used for HD output.
42h	00h	1:0	V0Start[10:9]	The MSB of V0Start, used for HD output.
		5:4	V0End[10:9]	The MSB of V0End, used for HD output.

9.2.12 **ID Insertion Control Register**

RN6752V1 supports the channel information insertion option. User can program INST_OBJ_SEL to select the inserted code which can include (1) invalid video indicator and a dark indicator (2) specific channel ID code.

Table 2 shows the case in which Channel Information is inserted in SAV/EAV code.

Table 2: Channel Information Insertion in SAV/EAV Code

CONDITION	FVH VALUE	SAV/EAV CODE

Field	V Time	H Time	F	V	H	1st	2nd	3rd	4th
1	Active	SAV	0	0	0	0xFF	0x00	0x00	{0x8, INST_OBJ[3:0]}
1	Active	EAV	0	0	1	0xFF	0x00	0x00	{0x9, INST_OBJ[3:0]}
1	Blank	SAV	0	1	0	0xFF	0x00	0x00	{0xA, INST_OBJ[3:0]}
1	Blank	EAV	0	1	1	0xFF	0x00	0x00	{0xB, INST_OBJ[3:0]}
2	Active	SAV	1	0	0	0xFF	0x00	0x00	{0xC, INST_OBJ[3:0]}
2	Active	EAV	1	0	1	0xFF	0x00	0x00	{0xD, INST_OBJ[3:0]}
2	Blank	SAV	1	1	0	0xFF	0x00	0x00	{0xE, INST_OBJ[3:0]}
2	Blank	EAV	1	1	1	0xFF	0x00	0x00	{0xF, INST_OBJ[3:0]}

Address: 3Ah (R/W).Default: 00h.

Bits	Field Name	Description
0	EN_MASK_YUV	EN_MASK_YUV = 1, replace Y/Cb/Cr with MaskValue_Y/MaskValue_U/MaskValue_V.
1	INV_AVID	1: Invert the AVID pin output.
2	INV_VBLK	1: Invert the VBLK pin output.
3	EN_NoVid_MASK	EN_NoVid_MASK=1 will enable EN_MASK_YUV when NoVid = 1.
6:4	INST_POS_SEL	Select the Channel Information format
7	Reserved	Must be 0h.

Address	Default	Bits	Field Name	Description
3Bh	10h	7:0	MaskValue_Y	Replace Y/Cb/Cr with (MaskValue_Y+ 0x10)/MaskValue_U/MaskValue_V when EN_MASK_YUV = 1.
3Ch	10h	7:0	MaskValue_U	
3Dh	10h	7:0	MaskValue_V	

Address: 3Eh (R/W).Default: 32h.

Bits	Field Name	Description
3:0	AVID_SEL	AVID_SEL is used to select the desired internal status signals for multiplexing onto the AVID pin output. The following is the mapping table: 0h: VSYNC 1h: HSYNC 2h: AVID 3h: VBLK 4h: Field 0=even, 1=odd. 5h: NoVid 6h: Coaxitron Output 7h: Reserved 8h: Reserved 9h: Reserved Ah: CKill Bh: Progressive mode Ch~Eh: Reserved Fh: Constant 0
7:4	VBLK_SEL	VBLK_SEL is used to select the desired internal status signals for multiplexing onto the VBLK pin output. The following is the mapping table: 0h: VSYNC 1h: HSYNC 2h: AVID 3h: VBLK 4h: Field 0=even, 1=odd. 5h: NoVid 6h: Coaxitron Output 7h: Reserved 8h: Reserved 9h: Reserved Ah: CKill Bh: Progressive mode Ch~Eh: Reserved Fh: Constant 0

Address: 3Fh (R/W).Default: 0001_00XXb.

Bits	Field Name	Description
1:0	CHAN_ID	For Video Decoder N, the default value of this field is N. This field is read/write-able to reassign the channel number.
3:2	Reserved	Must be 0h.
5:4	INST_OBJ_SEL	Select the inserted object format
7:6	Reserved	Reserved

Address: 40h (R/W).Default: 40h.

Bits	Field Name	Description
0	Reserved	Not used.

Bits	Field Name	Description
1	INV_FID	1: Invert the FID output.
2	INV_VSYNC	1: Invert the VSYNC output.
3	INV_HSYNC	1: Invert the HSYNC output.
7:4	FID_SEL	FID_SEL is used to select the desired internal status signals for multiplexing onto the FID pin output. The following is the mapping table: 0h: VSYNC 1h: HSYNC 2h: AVID 3h: VBLK 4h: Field 0=even, 1=odd. 5h: NoVid 6h: Coaxitron Output 7h: Reserved 8h: Reserved 9h: Reserved Ah: CKill Bh: Progressive mode Ch~Eh: Reserved Fh: Constant 0

Address: 46h (R/W).Default: 10h.

Bits	Field Name	Description
3:0	VSYNC_SEL	VSYNC_SEL is used to select the desired internal status signals for multiplexing onto the VSYNC pin output. The following is the mapping table: 0h: VSYNC 1h: HSYNC 2h: AVID 3h: VBLK 4h: Field 0=even, 1=odd. 5h: NoVid 6h: Coaxitron Output 7h: Reserved 8h: Reserved 9h: Reserved Ah: CKill Bh: Progressive mode Ch~Eh: Reserved Fh: Constant 0

Bits	Field Name	Description
7:4	HSYNC_SEL	HSYNC_SEL is used to select the desired internal status signals for multiplexing onto the HSYNC pin output. The following is the mapping table: 0h: VSYNC 1h: HSYNC 2h: AVID 3h: VBLK 4h: Field 0=even, 1=odd. 5h: NoVid 6h: Coaxitron Output 7h: Reserved 8h: Reserved 9h: Reserved Ah: CKill Bh: Progressive mode Ch~Eh: Reserved Fh: Constant 0

Address: 47h (R/W).Default: 00h.

Bits	Field Name	Description
1:0	AVID_DLY	Delay the AVID pin output for AVID_DLY pixel clocks.
3:2	VBLK_DLY	Delay the VBLK pin output for VBLK_DLY pixel clocks.
5:4	VSYNC_DLY	Delay the VSYNC pin output for VSYNC_DLY pixel clocks.
7:6	HSYNC_DLY	Delay the HSYNC pin output for HSYNC_DLY pixel clocks.

Address: 48h (R/W).Default: 03h.

Bits	Field Name	Description
5:0	Reserved	Must be 13h.
7:6	FID_DLY	Delay the FID pin output for FID_DLY pixel clocks.

9.2.13 **BT.656/BT656-like Bus Control Register**

Address: 50h (R/W).Default: 02h.

Bits	Field Name	Description
2:0	VRFmt	Video Resolution Format Select.
3	Reserved	N/A.
4	HRHalf	Horizontal Resolution Half.
7:3	Reserved	Must be 0h.

Address: 56h (R/W).Default:01h.

Bits	Field Name	Description
1:0	BtClk	Selects 54MHz output clock for D1/720p/1080p output format.
2	Bt601	BT.656/BT.656-like output.
7:3	Reserved	Must be 0h.

9.2.14 **HD Mode Control Registers**

The selection of supported HD decoding format is stored in extended register address 0h, and it is accessed through a set of extended control registers. The supported HD decoding formats and the control registers are shown in the following tables.

HD Selection	ExtReg0
720p, 25fps (Analog HD)	8'h42
720p, 30fps(Analog HD)	8'h44
720p, 25fps (other public analog HD)	8'h43
720p, 30fps (other public analog HD)	8'h47
720p, 25fps (other public analog HD)	8'h4A
720p, 30fps (other public analog HD)	8'h4B
1080N, 25fps(Analog HD)	8'h45
1080N, 30fps(Analog HD)	8'h46
1080p, 25fps (Analog HD)	8'h48
1080p, 30fps (Analog HD)	8'h49

ExtendedControlRegister – controls the access of extended register where HD mode selections are stored. Address: 58h (R/W).Default: 00h.

Bits	Field Name	Description
0	ExRegWrEn	This bit enables the write (1) or read access (0) to the extended registers. When set to 1, it enables the data in the *ExtendedDataRegister* to be written into the register defined by *ExtendedAddressRegister*. This bit is self-clearing, i.e. it resets to 0 in the following cycle. When set to 0, it enables the register data defined by *ExtendedAddressRegister* to be updated in *ExtendedDataRegister*.
7:1	Reserved	Must be 0h.

ExtendedAddressRegister – provides the address to select the extended register to be accessed. Address: 59h (R/W).Default: 00h.

Bits	Field Name	Description
7:0	ExRegAddr	This 8-bit value provides the address of the extended register (ExtReg) to be accessed.

ExtendedDataRegister – provides the data for read and write access to the extended register. Address: 5Ah (R/W).Default: 00h.

Bits	Field Name	Description
7:0	ExRegData	This 8-bit value provides the data to be written, when ExRegWrEn is 1, or the read data, when ExRegWrEn is 0, of the register selected by ExRegAddr.

Example of writing data 0x42 to extended register address 0x00 (ExtReg0) to select 720p 25fps mode:

1. Write to *ExtendedAddressRegister* = 00h;

2. Write to *ExtendedDataRegister* = 42h;
3. Write to *ExtendedControlRegister* = 01h;

Example of reading data from extended register address 00h (ExtReg0):

1. Write to *ExtendedAddressRegister* = 00h;
2. Read from *ExtendedDataRegister*;

9.2.15 Black/White Stretch Control

In RN6752V1, the Black/White Stretch function is implemented as a post-decoding process on the luma signal. This non-linear process changes the available resolution that is allotted to the lighter and darker portion of the luma signal. The Black Stretch process assigns more resolution to the darker portion while the White Stretch process assigns more resolution to the lighter portion.

Address: 57h (R/W).Default: 20h.

Bits	Field Name	Description
5:0	Stretch	Black/White Stretch Control This 6-bit control signal is used to control the white stretch function (Stretch > 6'h20), which assigns more resolution to the lighter portion of an input video signal, and black stretch function (Stretch < 6'h20), which assigns more resolution to the darker portion. A value of 6'h20 disables black/white stretch.
7:6	Reserved	Must be 0.

9.2.16 Coaxitron Control Registers

Address: 73h (R/W).Default: 00h.

Bits	Field Name	Description
2:0	Coax_MSel	Coaxitron mode select
3	EnCoaxRx	Enable Coaxitron Receive 0: Coaxitron TX mode. 1: Coaxitron RX mode.
4	CoaxEmpty (RO)	FIFO empty flag
5	CoaxFull (RO)	FIFO full flag
6	CoaxTxWrDone/CoaxRxERR_CLR (WO) CoaxRxERR (RO)	Coaxitron TX FIFO write done (EnCoaxRx = 0) Write 1 to indicate the completion of writing data into FIFO, and the data in the FIFO will be transmitted based on the mode selected by Coax_MSel. This bit is write-only. Coaxitron RX error clear (EnCoaxRx = 1) Write 1 to clear CoaxRxERR status. Coaxitron RX error indication.
7	CoaxFIFO_INIT (WO)	Set 1 to reset FIFO read/write address pointer.

Address: 74h (R/W).Default: 00h.

Bits	Field Name	Description
7:0	CoaxFIFO_DATA	Coaxitron TX data FIFO (EnCoaxRX = 0)

Bits	Field Name	Description
		The data written to this register will be written to the Coaxitron TX data FIFO for transmission. Coaxitron RX data FIFO (EnCoaxRX = 1) Coaxitron RX data in the FIFO can be read from this register whenever CoaxEmpty is 0.

Address: 75h (WO).Default: 0Ah.

Bits	Field Name	Description
3:0	CoaxLine	Select Coaxitron TX line number. Defaults to 4'hA, which is line 18. Using CoaxLine, the TX line number can be selected from a range of 8 to 23.
4	Coax8Bit	Coax8Bit mode enable Instead of using standard Coaxitron 15 or extended 15-bit protocol, setting Coax8Bit will enable 8-bit protocol.
7:5	Reserved	N/A

9.3 MIPI Control Registers

RN6752V1 supports 1 links of MIPI CSI-2 unidirectional output. The low level protocol of MIPI CSI-2 consists of two packets: long packets and short packets. Figure 8 shows an example of the protocol.

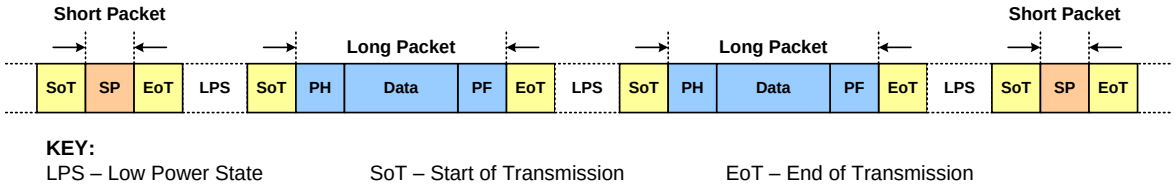


Figure 8: Low Level Protocol of MIPI CSI-2

The data stream is output at a fixed data rate of 648 Mbps per lane. The data stream for each decoder is a virtual channel. These data streams from virtual channels are interleaved. RN6752V1 supports 2-bit programmable virtual channel identifier. The virtual channel identifier is transferred in Data ID for both long packet and short packet. Figure 9, Figure 10 and Figure 11 shows long packet structure, short package structure and data identifier, respectively.

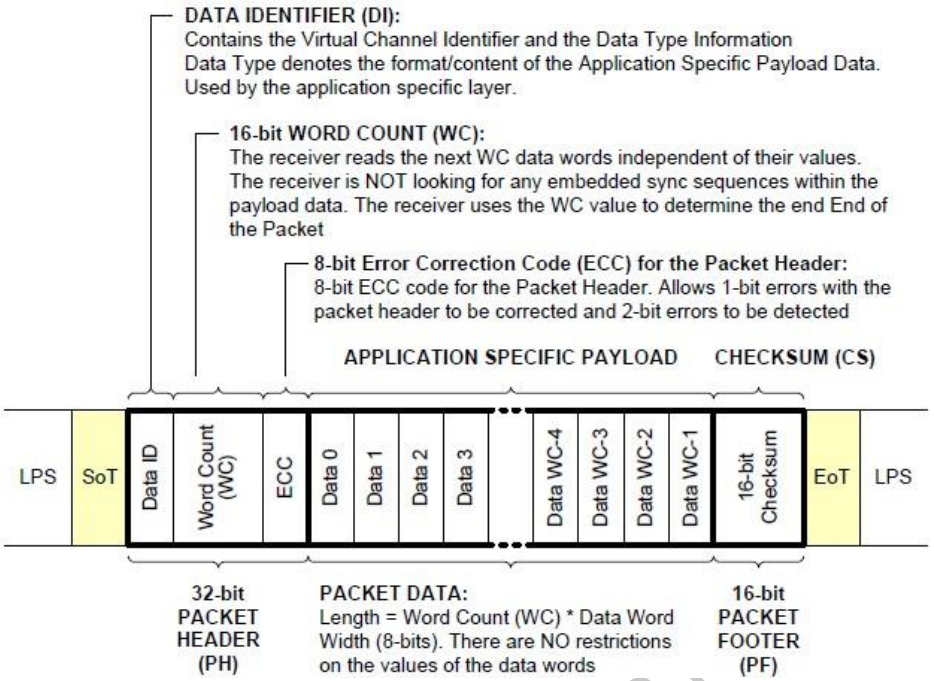


Figure 9: Long Packet Structure

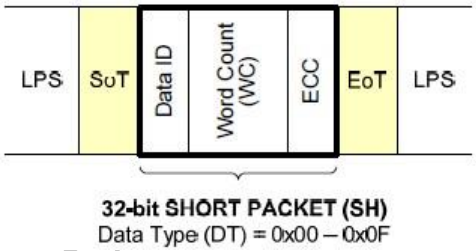


Figure 10: Short Packet Structure

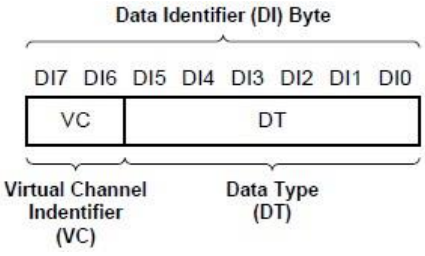


Figure 11: Data Identifier

The following figure shows an example of multi-channel output of RN6752V1.

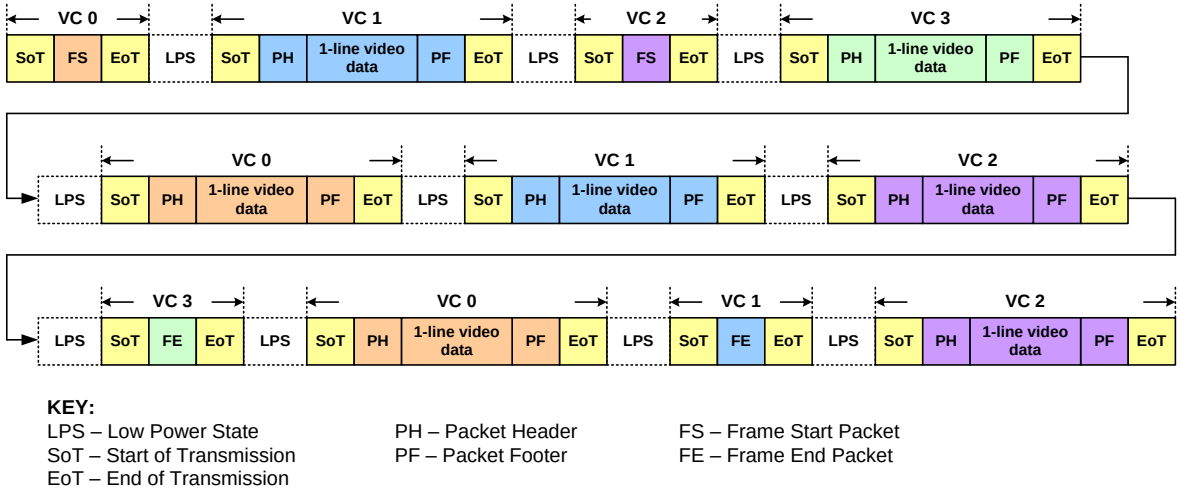


Figure 12: Multi-channel Data Transmission

9.3.1 MIPI CSI-2 Control Registers

Address: 04h (R/W).Default: 00h.

Bits	Field Name	Description
0	CSI_RESET	CSI-2 Controller Software Reset
1	DPHY_RESET	MIPI TX Software Reset
7:2	Reserved	Must be 0h.

Address: 06h (R/W).Default: 40h.

Bits	Field Name	Description
1:0	Reserved	Not used.
5:2	LANE_NUM	Lane Number
7:6	Reserved	Must be 1h.

Address: 07h (R/W).Default: 04h.

Bits	Field Name	Description
0	HSTX_CKLP_EN	Enable non-continuous clock lane.
7:1	Reserved	Must be 2h.

Address: 21h (R/W).Default: 00h.

Bits	Field Name	Description
0	LC_HSTX_EN	Enable clock lane high speed mode.
7:1	Reserved	Must be 0h.

Address: 6Ch (R/W).Default: 0Fh.

Bits	Field Name	Description
3:0	CSI_CH_EN	CSI-2 Channel Enable
4	CSI_CH_RST	CSI-2 Controller Reset
7:5	Reserved	Not used.

Address: 6Dh (R/W).Default: 00h.

Bits	Field Name	Description
1:0	CSI_CH0_FRM_MODE	CSI-2 Frame Mode for Decoder 0
7:6	Reserved	Reserved

Address: 70h (R/W).Default: 01h.

Bits	Field Name	Description
7:0	CSI_CH0_FRM_NUM[7:0]	Bits 7-0 of CSI-2 max. frame number for decoder 0.

Address: 71h (R/W).Default: 00h.

Bits	Field Name	Description
7:0	CSI_CH0_FRM_NUM[15:8]	Bits 15-8 of CSI-2 max. frame number for decoder 0.

Address: 78h (R/W).Default: 80h.

Bits	Field Name	Description
7:0	CSI_CH0_YC_CNT[7:0]	Bits 7-0 of {Cb, Y0, Cr, Y1} counts per line for decoder 0.

Address: 79h (R/W).Default: 02h.

Bits	Field Name	Description
1:0	CSI_CH0_YC_CNT[9:8]	Bits 9-8 of {Cb, Y0, Cr, Y1} counts per line for decoder 0.
7:2	Reserved	Not used.

9.3.2 **MIPI TX Control Registers**

Address: 00h (R/W).Default: 02h.

Bits	Field Name	Description
0	CSI_BIAS_EN	MIPI TX Bias Enable
1	Reserved	Must be 1b.
2	CSI_PHYCK_INV	Invert MIPI TX PHY clock.
7:3	Reserved	Must be 0h.

Address: 02h (R/W).Default: 10h.

Bits	Field Name	Description
0	CSI_LNT0_CKLANE_EN	MIPI TX PHY Lane 0 Clock Mode Enable
1	CSI_LNT1_CKLANE_EN	MIPI TX PHY Lane 1 Clock Mode Enable
2	CSI_LNT2_CKLANE_EN	MIPI TX PHY Lane 2 Clock Mode Enable
3	CSI_LNT3_CKLANE_EN	MIPI TX PHY Lane 3 Clock Mode Enable
4	CSI_LNTC_CKLANE_EN	MIPI TX PHY Lane CK Clock Mode Enable
7:5	Reserved	Not used.

Address: 04h (R/W).Default: 10h.

Bits	Field Name	Description
2:0	MIPI_TX_PHY0_SEL	MIPI TX PHY Lane 0 Selection
3	Reserved	Not used.
6:4	MIPI_TX_PHY1_SEL	MIPI TX PHY Lane 1 Selection
7	Reserved	Not used.

Address: 05h (R/W).Default: 32h.

Bits	Field Name	Description
2:0	MIPI_TX_PHY2_SEL	MIPI TX PHY Lane 2 Selection
3	Reserved	Not used.
6:4	MIPI_TX_PHY3_SEL	MIPI TX PHY Lane 3 Selection
7	Reserved	Not used.

Address: 06h (R/W).Default: 04h.

Bits	Field Name	Description
2:0	MIPI_TX_PHYC_SEL	MIPI TX PHY Lane CK Selection
7:3	Reserved	Not used.

10 Electrical Specifications

10.1 Absolute Maximum Ratings

Description	Symbol	Min	Typ	Max	Units
VA33, 3.3V Analog Power		-0.5		4.5	V
VDDIO Digital Power		-0.5		4.5	V
VD12, 1.2V Digital Power *		-0.5		1.45	V
VA12, 1.2V Analog Power *		-0.5		1.45	V
Voltage on Any Digital Data Pin	V_I	-0.5		4.5	V
Analog Input Voltage for ADC	VIN_M	-0.5		4.5	V
Storage Temperature	T_S	-65		150	°C
Junction Temperature	T_J	-40		125	°C

NOTE: Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

10.2 Recommended Operating Conditions

Description	Symbol	Min	Typ	Max	Units
VA33, 3.3V analog power			3.3		V
VD12, 1.2V digital power *			1.2		V
VA12, 1.2V analog power *			1.2		V
VDDIO			1.8/3.3		V
IO				VDDIO	V
Ambient Operating Temperature	T_A	-40		85	°C

NOTE: The device is not guaranteed to function outside its operating conditions.

10.3 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input high Voltage	V_{IH}	0.8VDDIO			V
Input Low Voltage	V_{IL}			0.2VDDIO	V
Input Leakage Current	I_L			±10u	A
Input Capacitance	C_{IN}		3.5p		F
Digital Outputs					
Output High Voltage	V_{OH}	0.9VDDIO			V
Output Low Voltage	V_{OL}			0.1VDDIO	V
High Level Output Current (@V_{OH}=2.4V)	I_{OH}	8 12			mA
Low Level Output Current (@V_{OL}=0.4V)	I_{OL}	8 12			mA
Tri-state Output Leakage Current	I_{OZ}			±10u	A
Output Capacitance	C_O		3.5p		F

10.4 AC Characteristics

BT656/BT601 I/O Propagation Delay
over recommended ambient operating temperature range, load capacitance = 10pF

VDDIO = 1.8V +/- 0.2V

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay T_{PLH} (High drive)	T_{PLH}	2		5.9	ns
Propagation Delay T_{PHL} (High drive)	T_{PHL}	2		6.1	ns
Propagation Delay T_{PLH} (Low drive)	T_{PLH}	2.2		6.4	ns
Propagation Delay T_{PHL} (Low drive)	T_{PHL}	2.2		6.5	ns

VDDIO = 3.3V +/- 0.3V

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay T_{PLH} (High drive)	T_{PLH}	1.3		2.9	ns
Propagation Delay T_{PHL} (High drive)	T_{PHL}	1.2		2.9	ns
Propagation Delay T_{PLH} (Low drive)	T_{PLH}	1.4		3.2	ns
Propagation Delay T_{PHL} (Low drive)	T_{PHL}	1.3		3.1	ns

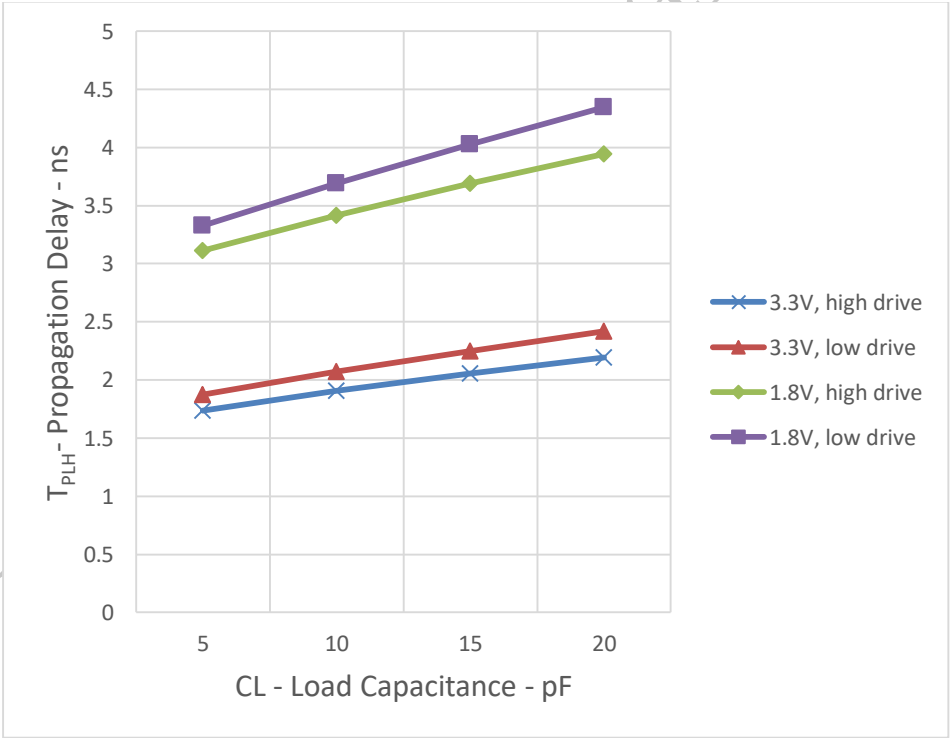


Figure 13: Typical Propagation Delay T_{PLH} vs Load Capacitance (Ta=25°C)

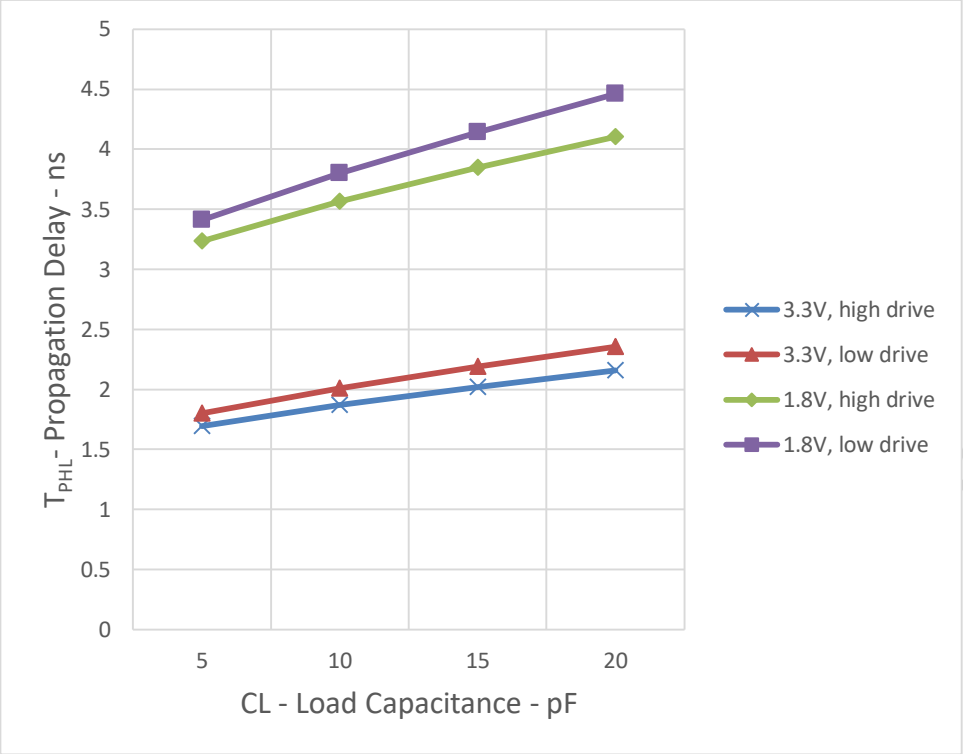


Figure 14: Typical Propagation Delay T_{PHL} vs Load Capacitance (Ta=25°C)

10.5 Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
Analog 3.3V Supply Current [2]	I_{VA33}		TBD		mA
Analog 1.2V Supply Current [2]	I_{VA12}		TBD		mA
Digital 1.2V Supply Current [2]	I_{VD12}		TBD		mA

Measured with normal IO driving strength, 1080p mode.

10.6 Two-wire Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time Between STOP and START	T_{BF}	1.3			us
SDA setup time	T_{SSDAT}	100			ns
SDA hold time	T_{HSDAT}	0		0.9	us
Setup time for START condition	T_{SSTA}	0.6			us
Setup time for STOP condition	T_{SSTP}	0.6			us
Hold time for START condition	T_{HSTA}	0.6			us
Rise time for SCL and SDA	T_R		270		ns
Fall time for SCL and SDA	T_F		2.1		ns
LOW period of SCL	T_{LOW}	0.5			us
HIGH period of SCL	T_{HIGH}	0.5			us
Capacitive load for each bus line	C_{BUS}		25		pF

Parameter	Symbol	Min	Typ	Max	Units
SCL clock frequency	f_{SCLK}			400	KHz

Note: external pull up resistor 4.7K Ohm, rise time, fall time and capacitive load for each bus line are specified by design

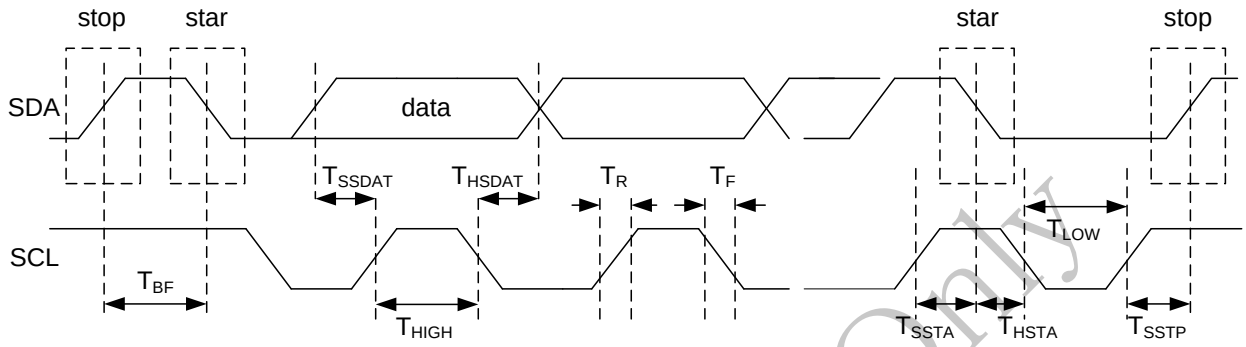


Figure 15: Two-wire Interface Timing

10.7 Analog Video Parameters

Parameter	Symbol	Test conditions	Min	Typ	Max	Units
Analog Front End and ADC						
Input impedance	RIN_{VAD}			500		KOhm
Input capacitance	CIN_{VAD}			10		pF
Full scale input voltage	VIN_{VAD}			1		Vpp

10.8 Oscillator Input

Parameter	Symbol	Min	Typ	Max	Units
nominal frequency			27		MHz
deviation				±50	ppm
duty cycle		45		55	%

11 Application Diagram

Please contact agents for further RN6752V1 applications in detail.

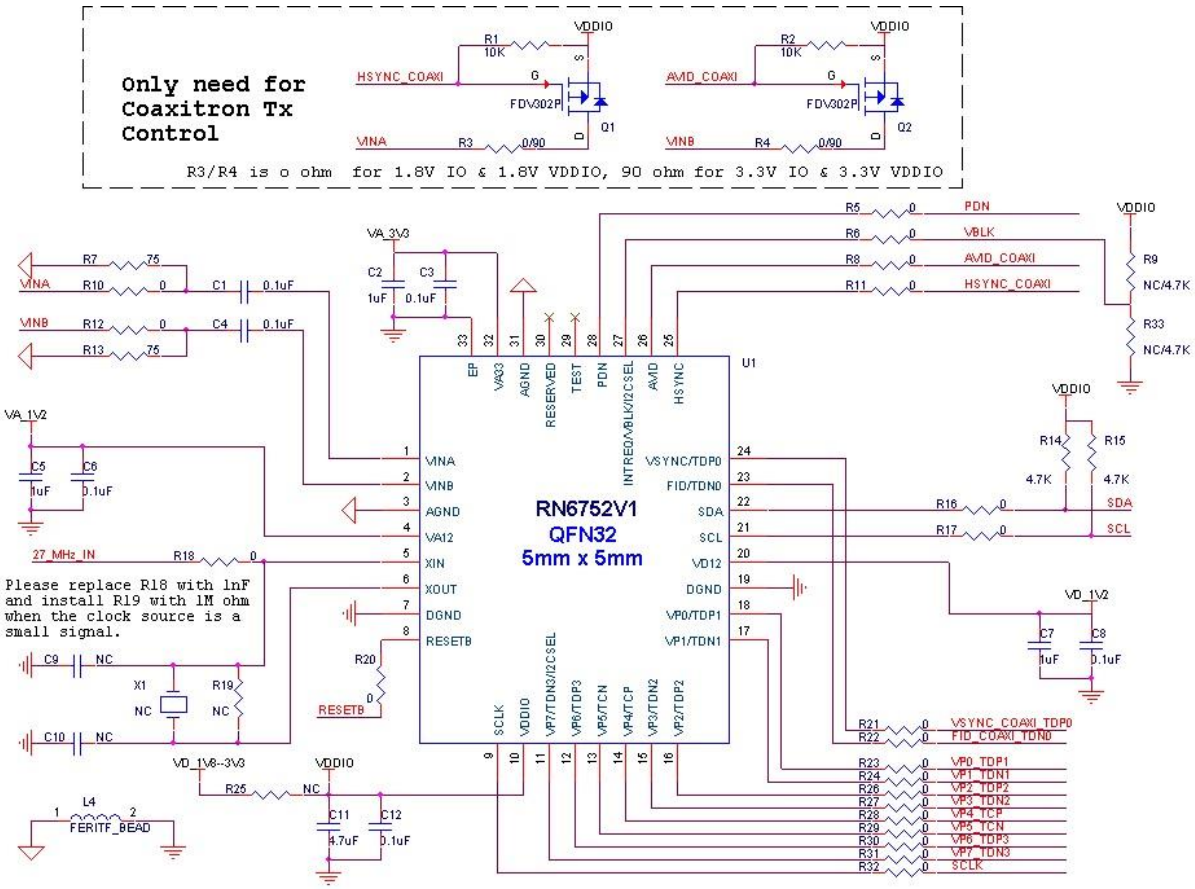
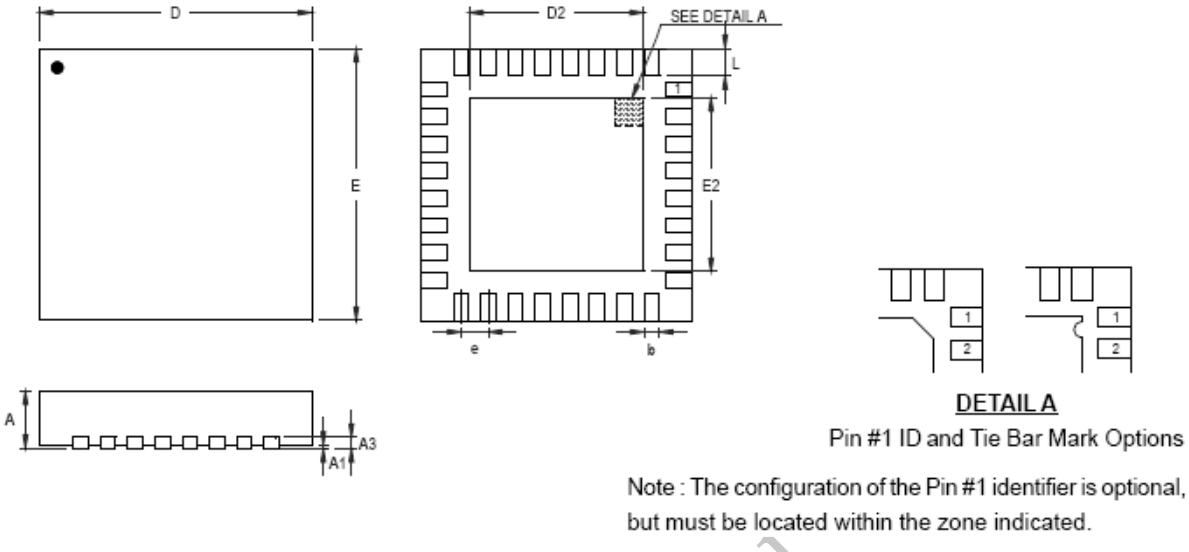


Figure 16: Application schematic

12 Package Outlines



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package

Figure 17: RN6752V1 32-pin QFN Package Information