

# RNA50C27AUS

## CMOS System-Reset IC

REJ03D0834-0100

Preliminary

Rev.1.00

Apr 10, 2006

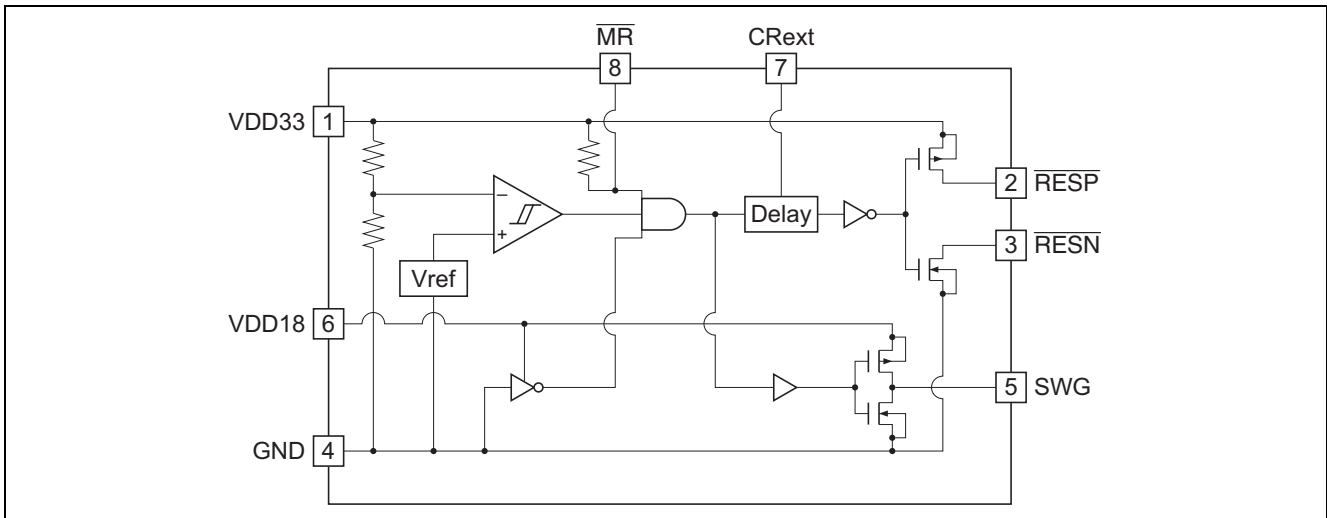
### Description

This IC facilitates complicated power-on and power-monitoring resets of microcomputers that require the 3.3-V and 1.8-V dual power supplies. It also facilitates change of delay time of reset signal by externally setting resistance and capacity for delay time. By employing complementary open-drain output, desired output such as open-drain output and CMOS output can be obtained.

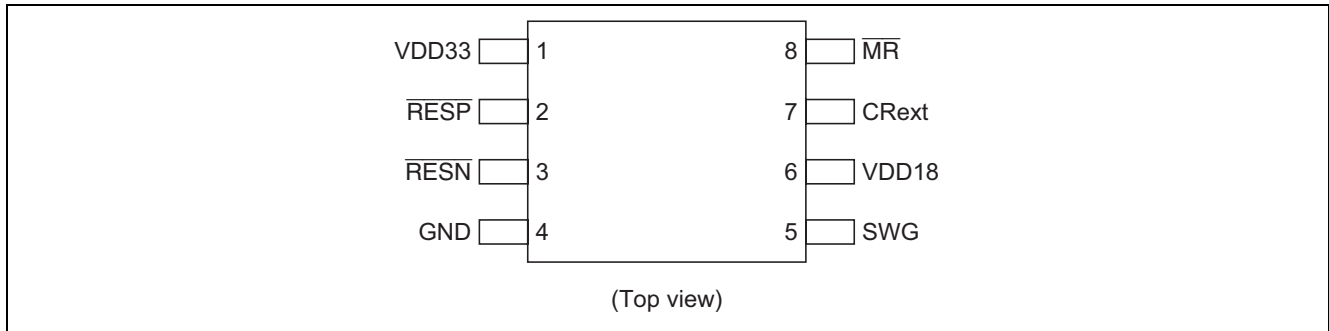
### Functions

- 3.3-V detection voltage : 2.7 V
- Accuracy of 3.3-V detection voltage :  $\pm 1.0\%$
- Hysteresis of 3.3-V detection voltage : 5% Typ.
- Open-drain/CMOS output
- 1.8-V PMOS drive output
- Ultra-small SSOP-8 package

### Block Diagram



## Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
1	VDD33	Input power supply pin for 3.3-V voltage. Recommended operating range is 2.7 to 3.6 V. Set the input voltage to 0.033 V/ $\mu$ s or less when starting up.
2	$\overline{\text{RESP}}$	Active-low reset signal output pin. By connecting to RESN pin, CMOS output can be used. If using open-drain, please connect pull-down resistor.
3	$\overline{\text{RESN}}$	Active-low reset signal output pin. By connecting to RESP pin, CMOS output can be used. If using open-drain, please connect pull-up resistor.
4	GND	GND pin
5	SWG	External PMOS gate control signal to be set between 1.8-V power supply and 1.8-V voltage input of microcomputer.
6	VDD18	Input power supply pin for 1.8-V voltage. Recommended operating range is 1.65 to 3.6 V.
7	CRext	Connecting pin for Rext resistance and Cext capacity that determine the delay time of reset signal. 3.3 k $\Omega$ or more is recommended for resistance. The delay time, $t_{\text{DLY}}$ , is given by the following formula. $t_{\text{DLY}} = \text{Cext} \times \text{Rext} [\text{s}]$
8	$\overline{\text{MR}}$	Pin to provide reset manually. MR pin is pulled-up to VDD33 through internal resistor.

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	VDD33	4.6	V
	VDD18	4.6	
Input voltage	V <sub>I</sub>	-0.3 to VDD33+0.3	V
Output voltage	V <sub>O</sub>	-0.3 to VDD33+0.3	V
Input current	I <sub>I</sub>	20	mA
Output current	I <sub>O</sub>	25	mA
Supply current	I <sub>DD</sub>	25	mA
Power dissipation	P <sub>T</sub>	273	mW
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Supply voltage	VDD33	V <sub>TH33</sub>	—	3.6	V	
	VDD18	1.65	—	VDD33		
Input voltage	V <sub>MR</sub>	0	—	VDD33	V	
Output voltage	V <sub>O</sub>	0	—	VDD33	V	
	V <sub>OSWG</sub>	0	—	VDD18		
External resistor	R <sub>ext</sub>	3.3	—	—	kΩ	VDD33 = 3.3 V
External capacitor	C <sub>ext</sub>	—	No limit	—		
Drivable capacitor	C <sub>L</sub>	—	2200	—	pF	SWG output
Operating temperature	T <sub>a</sub>	-40	—	85	°C	

## Electrical Characteristics

### DC Characteristics

(VDD33 = 3.3 V, VDD18 = 1.8 V, Ta = 25°C, C<sub>Rext:R</sub> = 10 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Quiescent supply current		IDD33	0.75	1.5	4	μA	All outputs are open
		IDD18	0.25	0.5	2		
Detection voltage		VTH33	Typ×0.99	2.7	Typ×1.01	V	
		VTH <sub>H</sub>	1.2	—	—		
		VTH <sub>L</sub>	—	—	0.55		
Detection voltage temperature dependency		$\frac{\Delta V_{th33}}{V_{th} \cdot \Delta T_a}$	—	±100	—	ppm/°C	
Detection voltage hysteresis		V <sub>HYS</sub>	VTH33×3%	VTH33×5%	VTH33×8%	V	
MR	Low-level input voltage	V <sub>IL</sub>	—	—	VTH33×0.25	V	
	High-level input voltage	V <sub>IH</sub>	VTH33×0.75	—	—	V	
	internal pull-up resistance	R <sub>MR</sub>	—	T.B.D.	—	kΩ	
CMOS *1	Low-level output current	I <sub>OL</sub>	7.5	15	30	mA	V <sub>O</sub> = 0.5 V
	High-level output current	I <sub>OH</sub>	5	10	20		V <sub>O</sub> = VDD33 – 0.5 V
RESP	Output leakage current	I <sub>LEAK</sub>	—	—	0.1	μA	RESN off
RESN	Output leakage current	I <sub>LEAK</sub>	—	—	0.1	μA	RESP off
SWG	High-level output voltage	V <sub>OH</sub>	1.7	—	—	V	V <sub>O</sub> = open
	Output source current	I <sub>OH</sub>	1.5	3	6	mA	V <sub>O</sub> = VDD33 – 0.5 V
	Low-level output voltage	V <sub>OL</sub>	—	—	0.1	V	V <sub>O</sub> = open
	Output sink current	I <sub>OL</sub>	0.2	0.35	0.55	mA	V <sub>O</sub> = 0.5 V

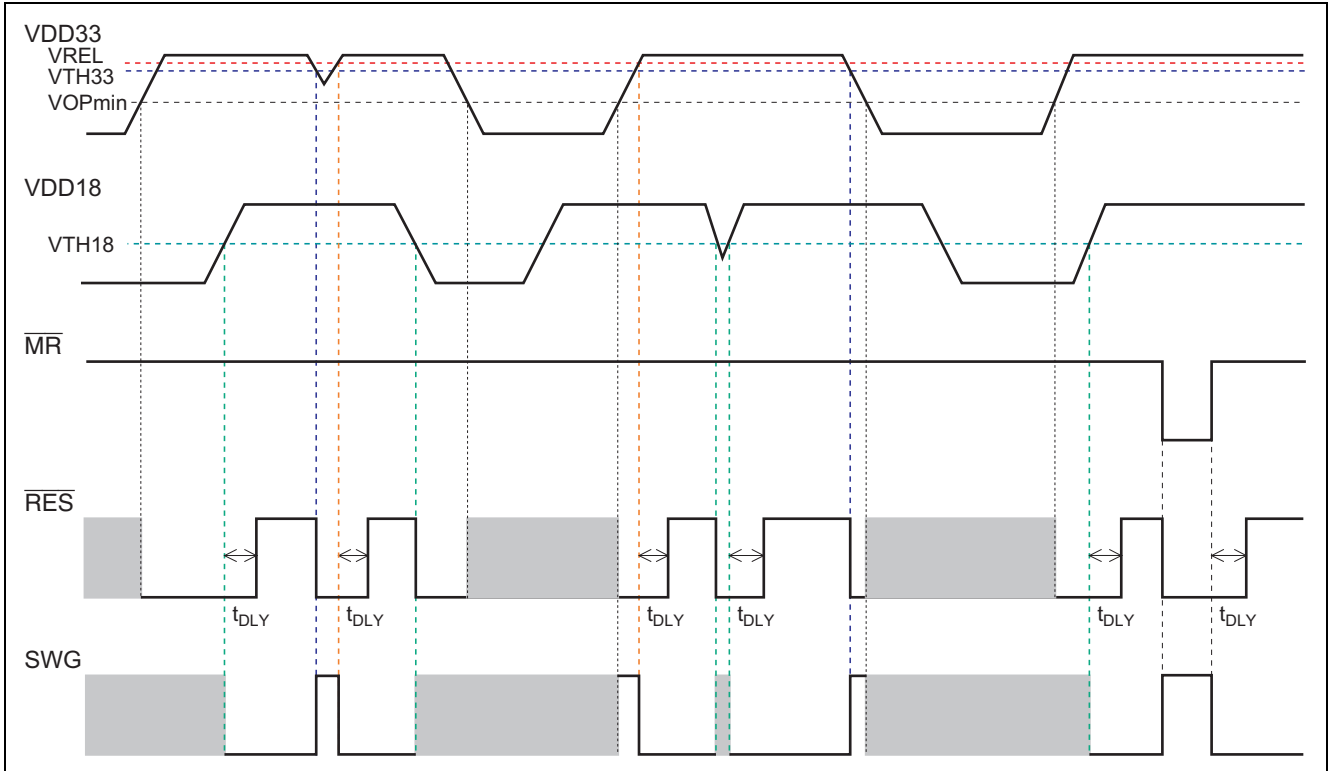
Note: When the voltage within  $V_{IL} < V_{IN} < V_{IH}$  is applied to MR and VDD18 input by DC, oscillation may occur.

1. When RESP output and RESN short out and CMOS output is used.

### AC Characteristics

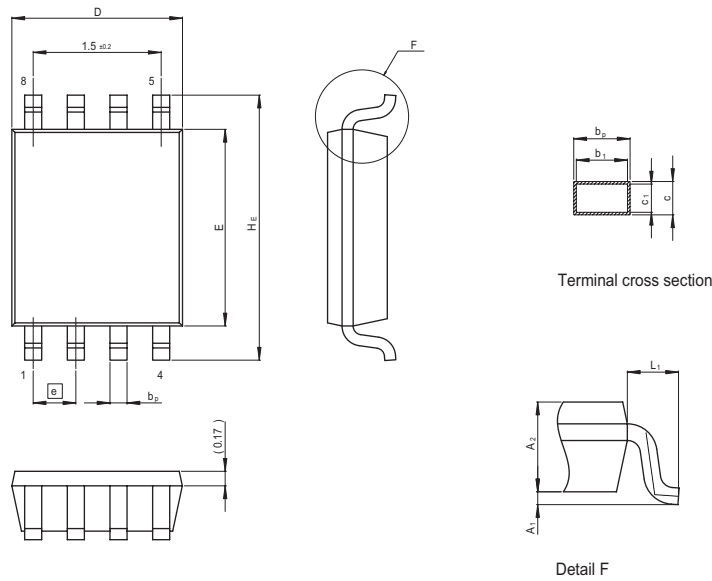
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
RESP	Propagation delay time	t <sub>PLH</sub>	—	50	400	μs	C <sub>L</sub> = 15 pF, C <sub>Rext:C</sub> = open
		t <sub>PHL</sub>	—	5	T.B.D.		
	Response time	t <sub>r</sub>	—	5	T.B.D.	ns	C <sub>L</sub> = 15 pF
		t <sub>f</sub>	—	5	T.B.D.		
RESN	Propagation delay time	t <sub>PLH</sub>	—	50	400	μs	C <sub>L</sub> = 15 pF, C <sub>Rext:C</sub> = open
		t <sub>PHL</sub>	—	1.5	T.B.D.		
	Response time	t <sub>r</sub>	—	5	T.B.D.	μs	C <sub>L</sub> = 15 pF
		t <sub>f</sub>	—	5	T.B.D.		
SWG	Propagation delay time	t <sub>PLH</sub>	—	50	400	μs	C <sub>L</sub> = 2200 pF
		t <sub>PHL</sub>	T.B.D.	1.5	T.B.D.		
	Response time	t <sub>r</sub>	T.B.D.	1.0	T.B.D.	μs	
		t <sub>f</sub>	T.B.D.	7.6	T.B.D.		
Delay time		t <sub>DLY</sub>	—	93	—	ms	C <sub>Rext:C</sub> = 0.1 μF, R = 1 MΩ

Timing Chart



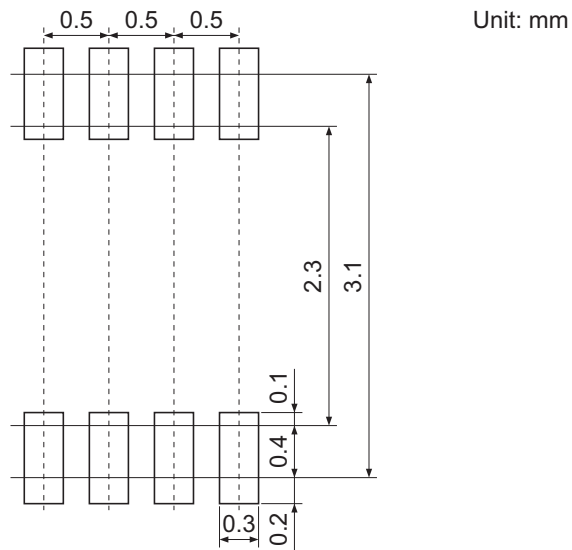
### Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VSSOP8-2.3x2-0.50	PVSP0008KA-A	TTP-8DB/TTP-8DBV	0.010g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	1.8	2.0	2.2
E	2.2	2.3	2.4
A <sub>2</sub>	0.6	0.7	0.8
A <sub>1</sub>	0	—	0.1
A	—	—	—
b <sub>p</sub>	0.15	0.22	0.3
b <sub>1</sub>	—	0.20	—
c	0.08	0.13	0.23
c <sub>1</sub>	—	0.11	—
θ	—	—	—
H <sub>E</sub>	2.8	3.1	3.4
ⓐ	—	(0.5)	—
x	—	—	—
y	—	—	—
Z	—	—	—
L	—	—	—
L <sub>1</sub>	—	(0.4)	—

### Footprint



SSOP-8 Footprint Example

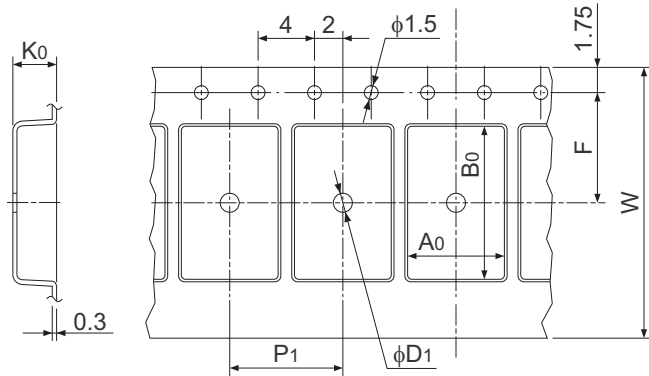
Note: These numbers on the diagram are reference values.  
Please adjust size, space, and other area of footprint as needed.

Taping and Reel Specifications

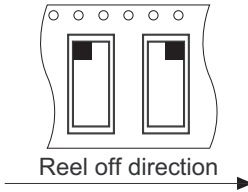
[Taping]

Unit: mm

W	P <sub>1</sub>	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	F	D <sub>1</sub>	Maximum Storage No.	Reel Type	Packing Form
8	4	2.25	3.4	1.0	3.5	1.05	3,000 IC/Reel	C	Non dry pack



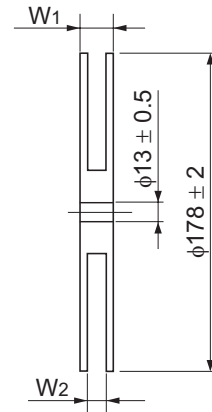
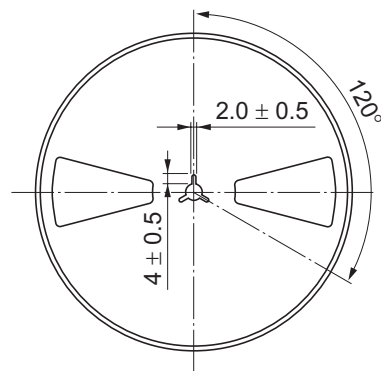
The pin1 is located in the hatching portion



[Reel]

Tape width: W	W <sub>1</sub>	W <sub>2</sub>
8	13.0	9.0

Reel type: C



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