STANDARD MICROSYSTEMS CORPORATION

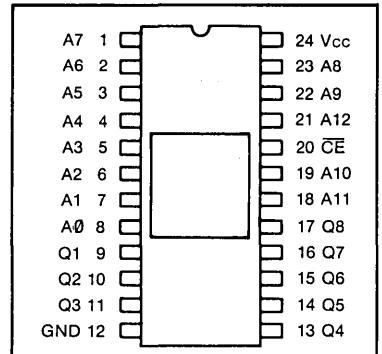
ROM 36000*
μPC FAMILY

8192 X 8-Bit Static Read-Only Memory
64K ROM

FEATURES

- ☐ 8192 X 8 Organization
- ☐ All Inputs and Outputs TTL-Compatible
- ☐ Edge Activated**
- ☐ Single +5V±10% Power Supply
- ☐ Maximum Access Time...250ns
- ☐ Minimum Cycle Time...375ns
- ☐ Low Power Consumption...220mW max active
- ☐ Low Standby Power Dissipation...35mW typical
- ☐ Three-State Outputs for Wire-OR Expansion
- ☐ Industry Standard 24 Pin DIP Pin Out
- ☐ Pin Compatible with MOSTEK MK36000-4
- ☐ On-Chip Address Latches
- ☐ Outputs drive 2 TTL loads and 100pf
- ☐ COPLAMOS® N-Channel MOS Technology

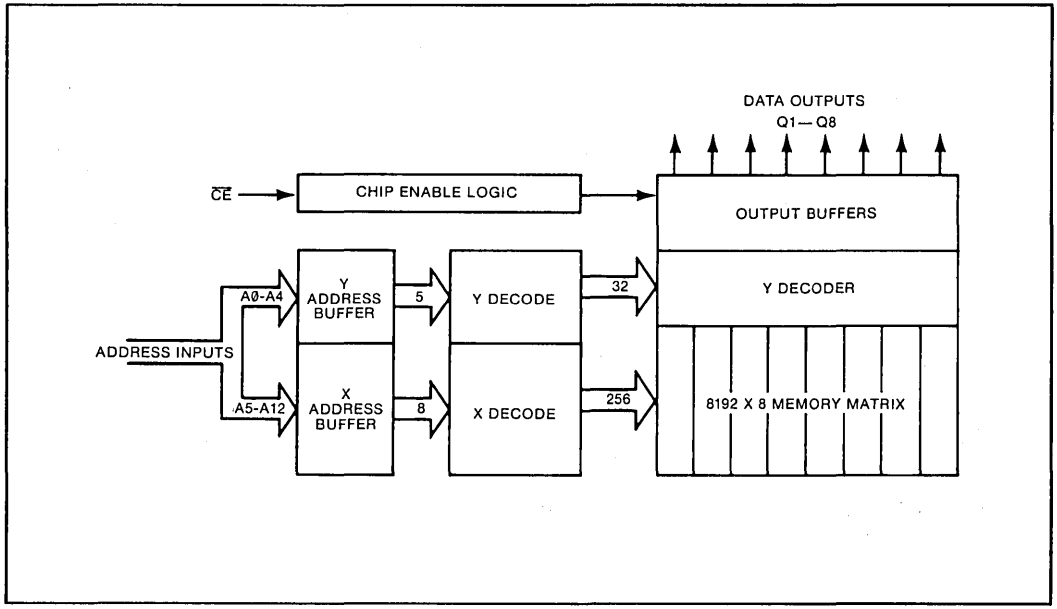
PIN CONFIGURATION



PACKAGE: 24-pin D.I.P.

SECTION VI

BLOCK DIAGRAM



*FOR FUTURE RELEASE

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GENERAL DESCRIPTION

The ROM 36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the ROM 36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

The ROM 36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The ROM 36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire- 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The ROM 36000 operates from a single +5 volt power supply with a wide ±10% tolerance, providing the widest operating margins available. The ROM 36000 is packaged in the industry standard 24 pin DIP.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... —0.5V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... —65°C to +150°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted)

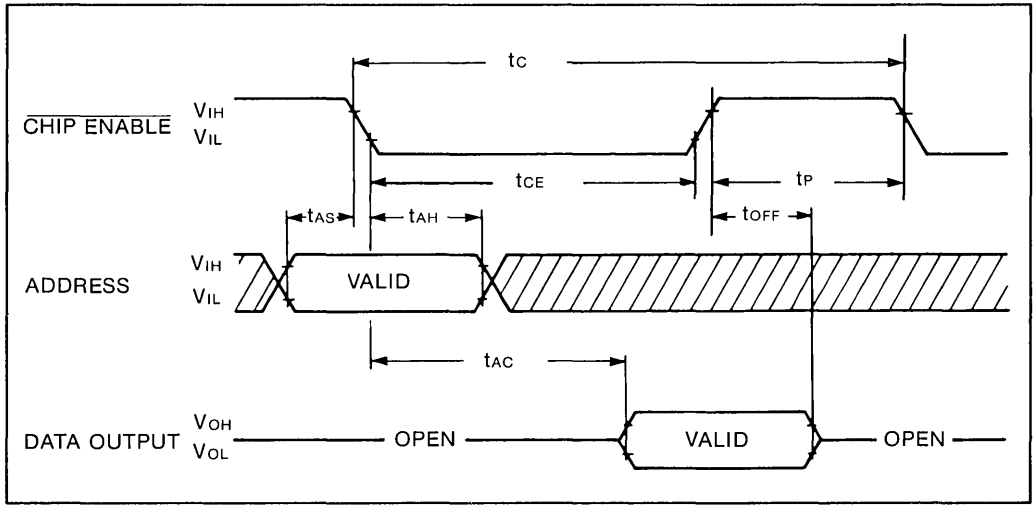
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	6
Input Logic 0 Voltage	V_{IL}	—0.5		0.8	Volts	
Input Logic 1 Voltage	V_{IH}	2.0		V_{CC}	Volts	
DC ELECTRICAL CHARACTERISTICS						
V_{CC} Power Supply Current (Active)	I_{CC1}			40	mA	1
V_{CC} Power Supply Current (Standby)	I_{CC2}		7		mA	7
Input Leakage Current	$I_{I(L)}$	—10		10	μA	2
Output Leakage Current	$I_{O(L)}$	—10		10	μA	3
Output Logic "0" Voltage @ I_{OUT} = 3.3mA	V_{OL}			0.4	Volts	
Output Logic "1" Voltage @ I_{OUT} = —220μA	V_{OH}	2.4			Volts	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
AC ELECTRICAL CHARACTERISTICS						
Cycle Time	tC	375			ns	4
$\overline{CE}$ Pulse Width	tCE	250				4
$\overline{CE}$ Access Time	tAC			250	ns	4
Output Turn Off Delay	tOFF			60	ns	4
Address Hold Time Referenced to $\overline{CE}$	tAH	60			ns	
Address Setup Time Referenced to $\overline{CE}$	tAS	0			ns	
CE Precharge Time	tP	125			ns	
CAPACITANCE						
Input Capacitance	CI		5		pF	5
Output Capacitance	CO		7		pF	5

NOTES:

1. Current is proportional to cycle rate. ICCI is measured at the specified minimum cycle time.
2. VIN = 0V to 5.5V.
3. Device unselected; VOUT = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with $\Delta V = 3$ volts
6. A minimum 100μs time delay is required after the application of VCC (+5) before proper device operation is achieved.
7. $\overline{CE}$ high.

TIMING DIAGRAM



OPERATION

The ROM 36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

PROGRAMMING

Standard Microsystems Corporation will accept data input in the form of 8K, 16K, 32K and 64K EPROMS and 8K, 16K, 32K and 64K ROMS. If other programming media is preferable, please consult the factory.