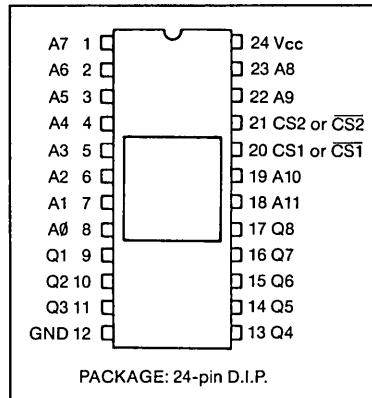


4096 X 8-Bit Static Read-Only Memory 32K ROM

FEATURES

- 4096 x 8 Organization
- All Inputs and Outputs TTL-Compatible
- Fully Static (No Clocks, No Refresh)
- Single +5v Power Supply
- Maximum Access Time...450ns
- Minimum Cycle Time...450ns
- Typical Power Dissipation...580mW
- Three-State Outputs for Wire-OR Expansion
- Industry Standard 24 pin DIP Pin Out
- Pin Compatible with TMS 4732, TMS 4700, TMS 2708 and Intel 2316E
- Two programmable chip select inputs for Chip Select Flexibility
- Automated Custom Programming—Formats—Media
- COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

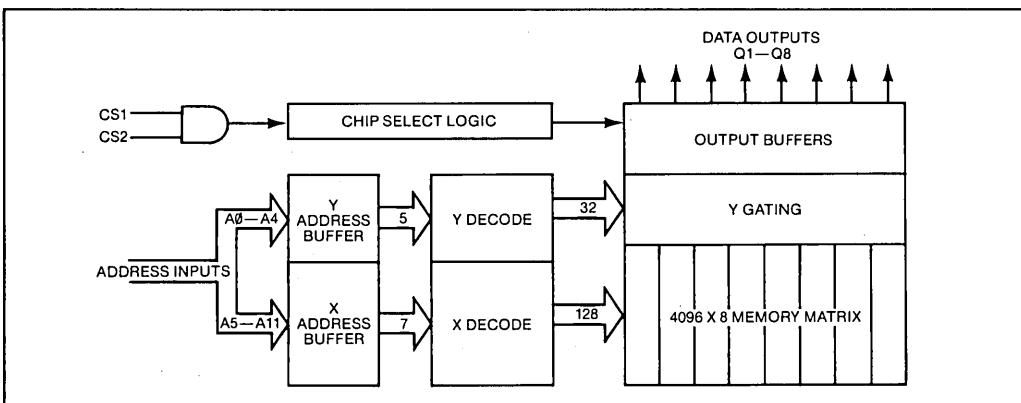
The ROM 4732 is a 32,768-bit read-only memory organized as 4096 words of 8-bit length. This makes the ROM 4732 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any external pull-up resistor. Each output can drive one Series 74 or 74S load without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus, facilitating easy memory expansion. Two chip select controls allow data to be read.

These controls are programmable, providing additional system decode flexibility allowing four 32K ROMs to be OR-tied without external decoding. The data is always available, it is not dependent on external CE clocking.

The ROM 4732 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. Systems utilizing 1024 x 8-bit ROMs or 1024 x 8-bit EPROMs can expand to the 4096 x 8-bit ROM 4732 with changes only to pins 18, 19, and 21. To upgrade from the 2316E, simply replace CS2 with A11 on pin 18.

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+7.0V
Negative Voltage on any Pin, with respect to ground	-0.3V

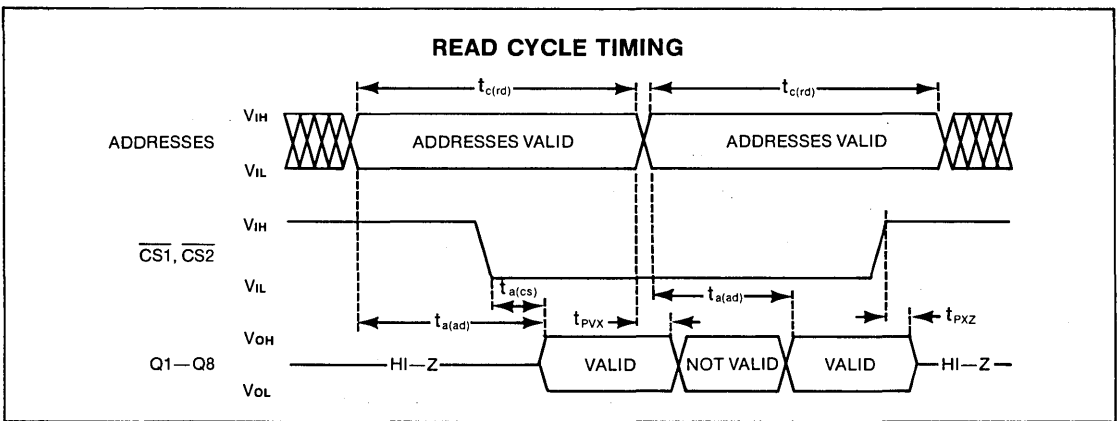
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V _{IL}			0.65	V	
High-level, V _{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low-level, V _{OL}			0.4	V	I _{OL} = 2.0mA
High-level, V _{OH}	2.4			V	I _{OH} = -200µA
INPUT CURRENT					
Low-level, I _{IL}			10	µA	0V ≤ V _{IN} ≤ V _{CC}
OUTPUT CURRENT					
I _{OL}			±10	µA	Chip Deselected
INPUT CAPACITANCE					
All inputs, C _{IN}			7	pF	
OUTPUT CAPACITANCE					
All Outputs, C _{OUT}			10	pF	
POWER SUPPLY CURRENT					
I _{CC}			150	mA	
A.C. CHARACTERISTICS					
Read cycle time, t _{c(rd)}	450			ns	1 Series 74 TTL load, C _L = 100 pF
Access time from address, t _{a(ad)}			450	ns	
Access time from chip select, t _{a(cs)}			200	ns	
Previous output data valid after address change, t _{PVX}			450	ns	
Output disable time from chip select, t _{PXZ}			200	ns	



Description of Pin Functions

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 18, 19, 22, 23	A7, A6, A5, A4, A3, A2, A1, A0, A11, A10, A9, A8	Addresses	I	The 12-bit positive-logic address is decoded on-chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least significant bit and A11 the most significant bit of the word address. The address valid interval determines the device cycle time.
9, 10, 11, 13, 14, 15, 16, 17	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	Data Outputs	0	The eight outputs must be enabled by both chip select controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least significant bit, Q8 the most significant bit. The outputs will drive TTL circuits without external components.
12	GND	Ground	GND	Ground
20, 21	CS1, CS2	Chip Select	I	Each chip select control can be programmed during mask fabrication to be active with either a high or a low level input. When both chip select signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either chip select is not active, all eight outputs are in a high-impedance state.
24	Vcc	Power Supply	PS	+5 volt power supply

PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The ROM 4732 is a fixed program memory in which the programming is performed via computer aided techniques by SMC at the factory during the manufacturing cycle to the specific customer inputs supplied in the punched computer card format below. The device is organized as 4096 8-bit words with address locations numbered 0 to 4095. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, A0 is least significant bit and A11 is the most significant bit.

Every card should include the SMC Custom Device Number in the form ROXXXX (4 digit number to be assigned by SMC) in column 75 through 80.

PROGRAMMABLE CHIP SELECTS: The chip select inputs shall be programmed according to the data punched in columns 73 and 74. Every card should include in column 73 a 1 if the output is to be enabled with a high level at CS2 or a 0 (zero) to enable the output with a low level at CS2. The column 74 entry is the same for programming CS1.

PROGRAMMED DATA FORMAT: The format for the cards to be supplied to SMC to specify that data to be programmed is provided below. The card deck for each device consists of 128 cards with each card containing data for 32 memory locations.

CARD COLUMN

HEXADECIMAL FORMAT

1 to 3	Hexadecimal address of first word on the card
4	Blank
5 to 68	Data. Each 8-bit memory byte is represented by two ASCII characters to represent a hexadecimal value of '00' or 'FF'.
69, 70	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from column 1 to 68, evaluate modulo 256 (carry from high order bit ignored). (For purposes of calculating the checksum, the value of Column 4 is defined to be zero.) Adding together, modulo 256, all 8-bit bytes from Column 1 to 68 (Column 4 = 0), then adding the checksum, results in zero.
71, 72	Blank
73	One (1) or zero (0) for CS2
74	One (1) or zero (0) for CS1
75, 76	RO
77 to 80	XXXX (4 digit number assigned by SMC)

ALTERNATIVE INPUT MEDIA

In addition to the preferred 80 column "IBM Card," customers may submit their ROM bit patterns on 9-track 800-BPI mag tape, 8-channel perforated paper tape, EPROM, ROM, etc. Where one of several nationwide time sharing services is mutually available, arrangements may be made with the factory to communicate the ROM definition data directly through the service computer. Format requirements and other information required to use alternative input media may be obtained through SMC sales personnel.

ALTERNATIVE DATA FILE FORMATS

In addition to the standard SMC format, it is possible to furnish data to SMC in other formats if prearranged with the factory. Non-standard formats may be acceptable. Contact SMC sales personnel.

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