

1.5V Drive Pch MOSFET

RP1A090ZP

● Structure

Silicon P-channel MOSFET

● Features

- 1) Low Voltage Drive(1.5V drive).
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (MPT6).

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	1000
RP1A090ZP		O

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	-12	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	Continuous	I_D	±9	A
	Pulsed	I_{DP} *1	±36	A
Source current (Body Diode)	Continuous	I_S	-1.6	A
	Pulsed	I_{SP} *1	-36	A
Power dissipation		P_D *2	2.0	W
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	-55 to +150	°C

 *1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

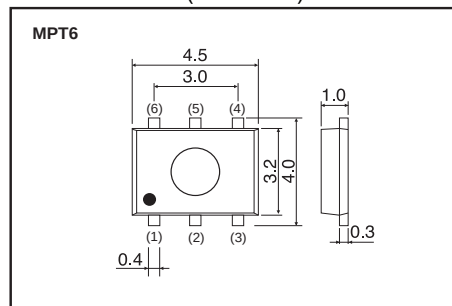
*2 Mounted on a ceramic board.

● Thermal resistance

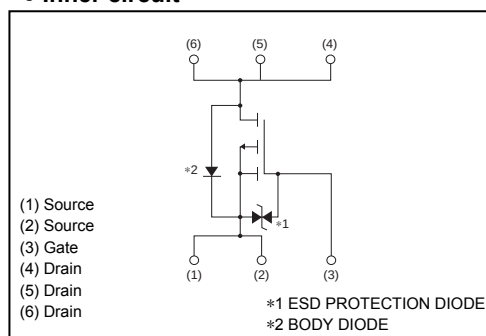
Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-a)*	62.5	°C / W

*Mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS} = \pm 10V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-12	-	-	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	-	-	-1	μA	$V_{DS} = -12V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS} = -6V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	8	12	m Ω	$I_D = -9A, V_{GS} = -4.5V$
		-	11	16		$I_D = -4.5A, V_{GS} = -2.5V$
		-	15	23		$I_D = -4.5A, V_{GS} = -1.8V$
		-	19	38		$I_D = -1.8A, V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} ^*$	12	-	-	S	$I_D = -9A, V_{DS} = -6V$
Input capacitance	C_{iss}	-	7400	-	pF	$V_{DS} = -6V$
Output capacitance	C_{oss}	-	800	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	-	750	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	35	-	ns	$I_D = -4.5A, V_{DD} = -6V$
Rise time	t_r^*	-	120	-	ns	$V_{GS} = -4.5V$
Turn-off delay time	$t_{d(off)}^*$	-	350	-	ns	$R_L = 1.3\Omega$
Fall time	t_f^*	-	170	-	ns	$R_G = 10\Omega$
Total gate charge	Q_g^*	-	59	-	nC	$I_D = -9A,$
Gate-source charge	Q_{gs}^*	-	11	-	nC	$V_{GS} = -4.5V$
Gate-drain charge	Q_{gd}^*	-	9	-	nC	$V_{DD} = -6V$

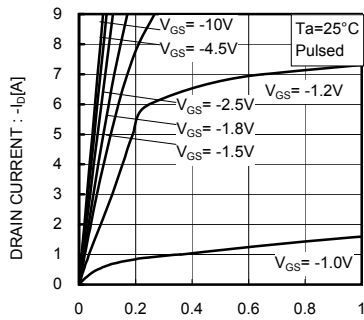
*Pulsed

● Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	-1.2	V	$I_s = -9A, V_{GS} = 0V$

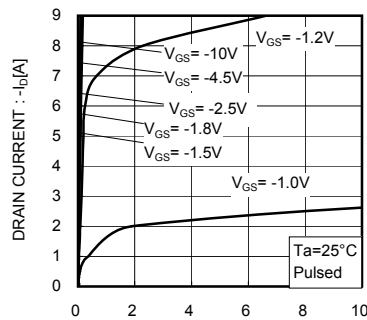
*Pulsed

● Electrical characteristic curves



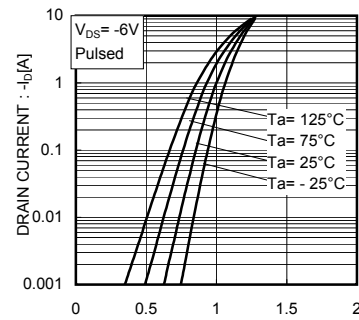
DRAIN-SOURCE VOLTAGE : $-V_{DS}$ [V]

Fig.1 Typical output characteristics(I)



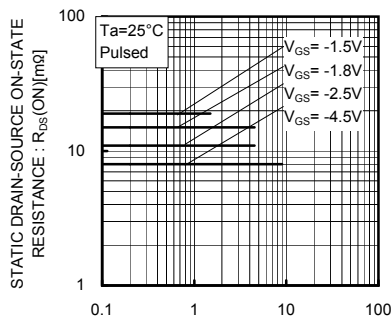
DRAIN-SOURCE VOLTAGE : $-V_{DS}$ [V]

Fig.2 Typical output characteristics(II)



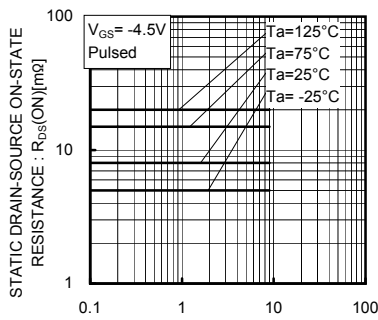
GATE-SOURCE VOLTAGE : $-V_{GS}$ [V]

Fig.3 Typical Transfer Characteristics



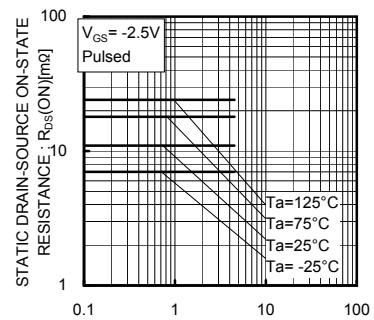
DRAIN-CURRENT : I_D [A]

Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)



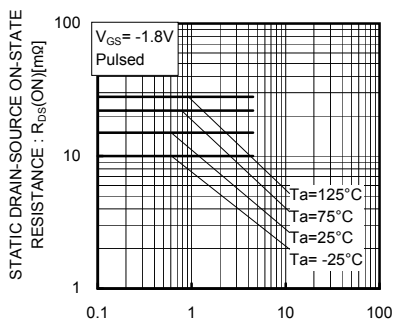
DRAIN-CURRENT : I_D [A]

Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)



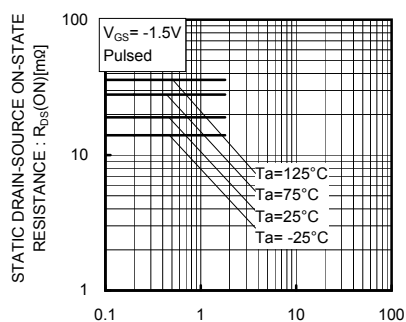
DRAIN-CURRENT : I_D [A]

Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)



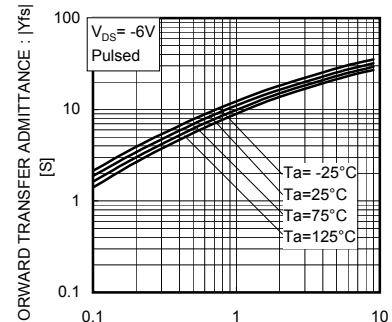
DRAIN-CURRENT : I_D [A]

Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)



DRAIN-CURRENT : I_D [A]

Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)



DRAIN-CURRENT : I_D [A]

Fig.9 Forward Transfer Admittance vs. Drain Current

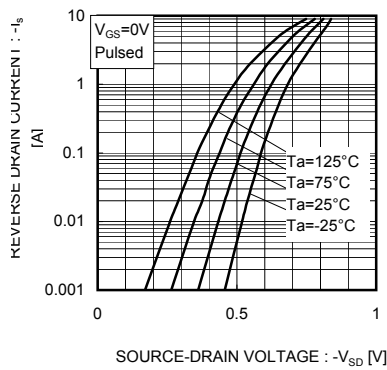


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

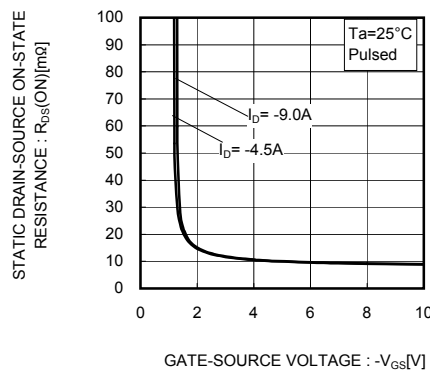


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

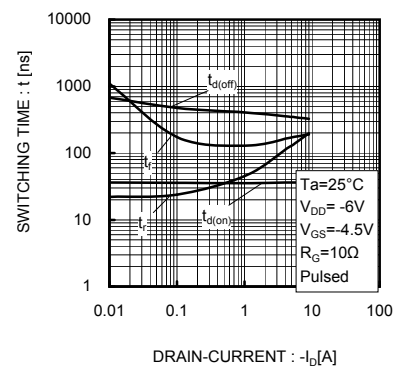


Fig.12 Switching Characteristics

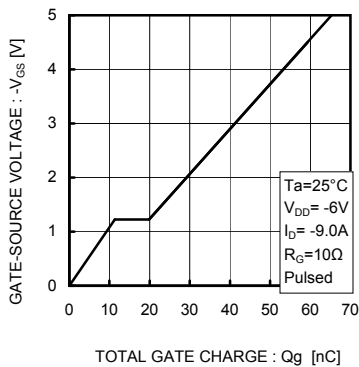


Fig.13 Dynamic Input Characteristics

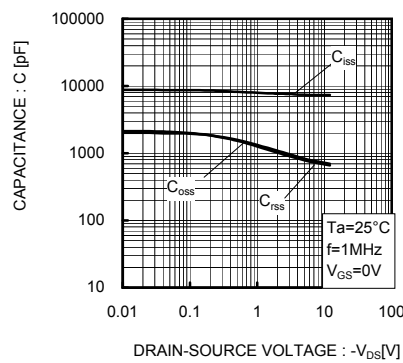


Fig.14 Typical Capacitance vs. Drain-Source Voltage

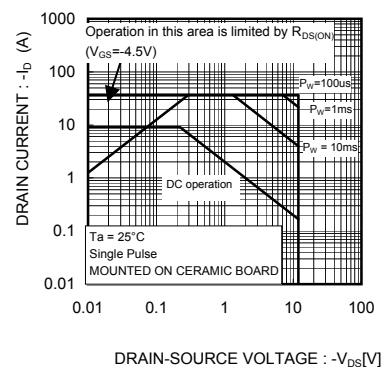


Fig.15 Maximum Safe Operating Area

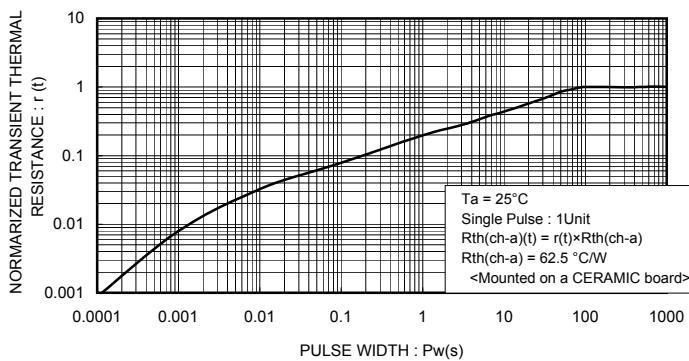


Fig.16 Normalized Transient Thermal Resistance vs. Pulse Width

● Measurement circuits

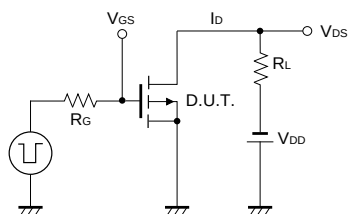


Fig.1-1 Switching Time Measurement Circuit

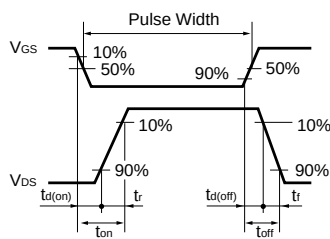


Fig.1-2 Switching Waveforms

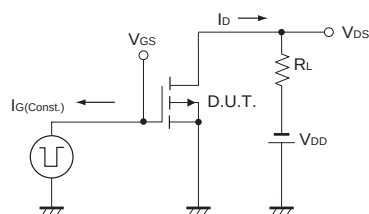


Fig.2-1 Gate charge measurement circuit

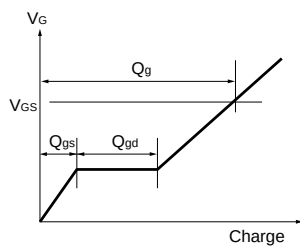


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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