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RPLIS-2048-EX 2048 x 1 Linear Image Sensor Datasheet

Key Features

- **High resolution**
  - Linear sensor with 2048 pixels, including 12 optical black pixels
  - 4 µm X 32 µm pixels on a 4 µm pixel pitch
  - 32 µm X 8192 µm imaging area
  - Fill factor >99%
- **Special Features**
  - On-chip Auto Dynamic Threshold™ * (ADT) with digital output – eliminates external ADC
  - Full frame electronic shutter
  - On-chip correlated double sampling
  - Black pixel clamping removes global pixel offsets
  - Dynamic Power Control™ ** minimizes power consumption for each operating mode
- **High sensitivity and dynamic range**
  - 12/24 µV/electron programmable conversion gain
  - 1.7V full scale range
  - 65 dB dynamic range
- **Ease of application**
  - Single 3.0 V supply voltage
  - Only a clock and a start pulse needed for operation
  - Programmable setup register for device mode selection
- **Multiple operating modes**
  - Analog video output
  - Digital comparator output
  - ADT™ digital output and analog output
  - Ultra low-power standby mode
  - Short and Normal exposure modes

P/N RPLIS-2048-EX B-LG
Packaged Imager Photo
Actual Size

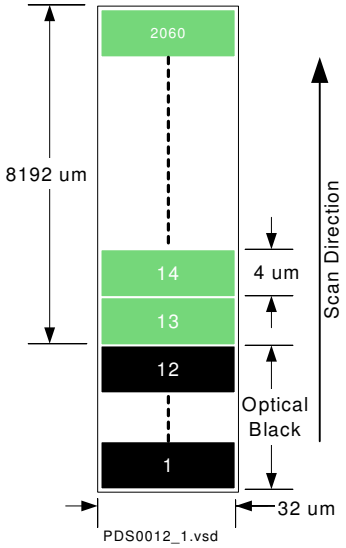


Figure 1: Pixel Structure Drawing

* Auto Dynamic Thresholding™ (ADT) is a trademark of Panavision Imaging, LLC

** Dynamic Power Control™ is a trademark of Panavision Imaging, LLC

ACS® is a registered trademark of Panavision Imaging, LLC

Description

The RPLIS-2048-EX image sensor is an ideal sensor for a broad range of applications requiring wide dynamic range and a large aspect ratio pixel, such as bar code reading, position measurement, laser triangulation, etc. The design incorporates many on-chip features that lower the overall system cost compared to multi-chip systems using CCD's. The RPLIS-2048-EX sensor includes full-frame snapshot shutter operation, with adjustable exposure time and programmable gain to handle varying light conditions. The video port has line driving capability further reducing system costs. The output is user selectable as analog video output, or Panavision Imaging's exclusive on-chip ADT with digital 1 bit comparator output. This circuit pre-processes the video signal by dynamically adjusting the threshold to compensate for lighting and optical variations. On-chip analog pre-processing prior to comparator output often eliminates the need for an expensive external Analog-to-Digital converter. An easy to use programmable register is provided to allow for easy setup and operation.

The RPLIS-2048-EX image sensor uses several Panavision Imaging's patented*, patent pending, and proprietary technologies.
*Note: This product covered under Patent # 6,084,229 and other patents pending.

Applications
- Bar Code Reading
- Text Scanning / OCR
- Edge Detection
- Position Encoding
- Laser Triangulation
- Distance Measurement

Table 1: Array Data

Pixel Type	Active Column Sensor (ACS®) Pixel
Array Size	12 optical black + 2048 video pixels
Pixel Size / Pitch	4 µm by 32 µm on a 4 µm pitch
Fill Factor	>99%
Imaging Area	Imaging sub-array: 32 µm by 8.192 mm Optical black sub-array: 32 µm by 48 µm
Output	Analog and Digital

Table 2: Electro-Optical Specifications

Unless otherwise specified: T_A = 25°C, VDD = 3.3V, CLK = 1.0MHz @ 50% duty cycle, t_{int} = 2.4ms, Analog Video Load C_{LOAD} = 20pF, Collimated Light Source = 3200K

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD		2.8	3.0	3.3	V
Supply Current	I_{DD}			3		mA
Power Dissipation	P_W	Normal mode		9		mW
Power Dissipation	P_{SB}	Standby mode			100	µW
Logic Input, High	V_{IH}		V_{DD}-0.6V			V
Logic Input, Low	V_{IL}				0.8	V
Pixel/Clock Frequency	F_{CLK}		0.1		2.5	MHz
Video Dark Level	V_{Dark}			1.46		V
Video Saturation Level	V_{Sat}			3.16		V
Output Voltage Swing, Full Scale [1]	V_{FS}			1.70		V
Temporal Noise [2]	e_n			1.0		mVrms
Dynamic Range [3]	DR			67		dB
Photo-Response Non-Uniformity [4]	PRNU	At 50% of SE		1		$\%V_{FS}$
Dark Signal Non-Uniformity [5]	DSNU			1		$\%V_{FS}$
Clock Feed Through [6]	CFT			50	120	mV
Linearity [7]	L			+/- 1		$\%V_{FS}$
Saturation Exposure [8]	SE			0.076		lx-s
Sensitivity	R	1x gain		22.3		V/lx-s
Conversion Gain	G_C	1x gain		12.3		$\mu V/e^-$
Full Well Capacity	FW			138k		e^-
Total Transfer Efficiency [9]	TTE			100		%
Image Lag	IL			1		$\%V_{FS}$
Spectral Response			200		1100	nm

Notes:

1. $V_{FS} \equiv V_{SAT} - V_{DARK}$, where V_{SAT} is the output voltage at saturation and V_{DARK} is the output voltage in the dark.
2. Temporal noise, e_n measured at dark with a 1.25MHz video filter applied. V_{rmse} is equivalent to one sigma of standard deviation. This noise is independent of PRNU, DSNU and CFT. V_{rmse} of N samples is calculated as:
$$V_{rmse} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[V_i - \hat{V}\right]^2}$$
3. DR ≡ V_{FS} / e_n , measured at dark.
4. PRNU is defined as the peak variation from the average when the imager is illuminated to 50% of SE (typ). PRNU is measured when the photosensitive surface is illuminated with light of uniform intensity and uniform color temperature. PRNU is defined by the expression: $PRNU = (\Delta V_{MAX}\text{-}V_{AVE})/ V_{FS} \times 100(\%)$.
5. DSNU is defined as the peak variation from the average when the imager is at dark. DSNU is defined by the expression: $DSNU = (\Delta V_{MAX}\text{-}V_{AVE})/ V_{FS} \times 100(\%)$.
6. Clock feed through noise is similar to Register Imbalance in CCD's and is described as uncompensated DC offsets in the video signal that is repeatable and can be subtracted.
7. Pixel average response measured from 5% to 70% of saturation. Linearity error is reported as a deviation in the response relative to the 'best fit' straight line and is given as a percentage of full scale.
8. Definition of SE: SE = V_{FS}/R .
9. No charge transfer loss during readout.

Table 3: Signal Labels and Definitions

Signal Name	Pin Name	Signal Type	Pin No.	Function
Analog Supply	AVDD	Bias	4	Supplies 3.0V to the internal analog circuitry. Bypass externally to AGND
Analog Ground	AGND		5	Distributes common ground node (0V) to the internal analog circuitry.
Digital Supply	DVDD		13	Supplies 3.0V to the internal digital circuitry. Bypass externally to DGND
Digital Ground	DGND		12	Distributes common ground node (0V) to the internal digital circuitry.
Comparator Threshold	THR	Analog In/Out	7	Mode Dependant Pin: Mode 0 – not used do not connect; Mode 1 – Internal DAC voltage output; Mode 2 - Analog input with user supplied Threshold; Mode 3 - ADT threshold analog output, tie to AGND with filter per the application circuit in figure 12.
Analog Test Input	ATI	Analog In	8	Connect directly to AGND.
Analog Video	Vout	Analog Outputs	6	Analog video output, 1 pixel per clock cycle.
Clock	CLK	Digital Inputs	16	Master clock input at the pixel rate – 50% duty cycle.
Start	STRT		15	Line initialization. Rising edge initiates readout and end exposure time.
Low Power Mode	LPM		2	High active input enables low-power standby mode.
Setup Clock	SCLK		9	Programmable Setup Register data clock.
Setup Data	SDIN		10	Programmable Setup Register data input.
Setup Enable	SEN		11	Programmable Setup Register data enable, loads setup data when high.
Data Valid	DVAL	Digital Outputs	14	Active high signal indicates that valid video is available at the output.
Comparator Output	/Dout		3	Comparator digital output for Modes 1, 2, and 3 - 1 bit per pixel per clock cycle. Not used in Mode 0.
Test Mode	TM		1	Internal use only, leave unconnected.

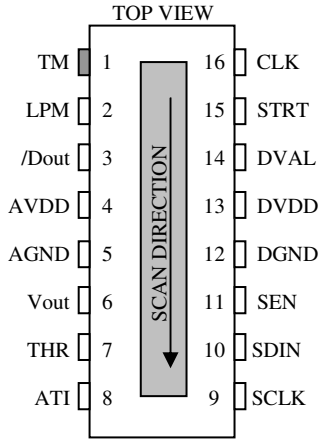


Figure 2: Pin-out diagram, top view

Absolute Maximum and Environmental Specifications

Table 4. Absolute Maximum Specifications

Supply voltage range, V_{DD} [1]	0 V to 6.0 V
Digital input current range, I_{IN}	–4 mA to 4 mA
Digital output current range, I_{OUT}	–4 mA to 4 mA

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated above, is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

Notes:

1. Voltage values are with respect to the device GND terminal.

Table 5. Environment Specifications

Operating case temperature range, T_{CASE} [1]	–10°C to 70°C
Operating free-air temperature range, T_A	–10°C to 50°C
Storage temperature range	–20°C to 85°C
Humidity range, R_H	0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 45 seconds	240°C

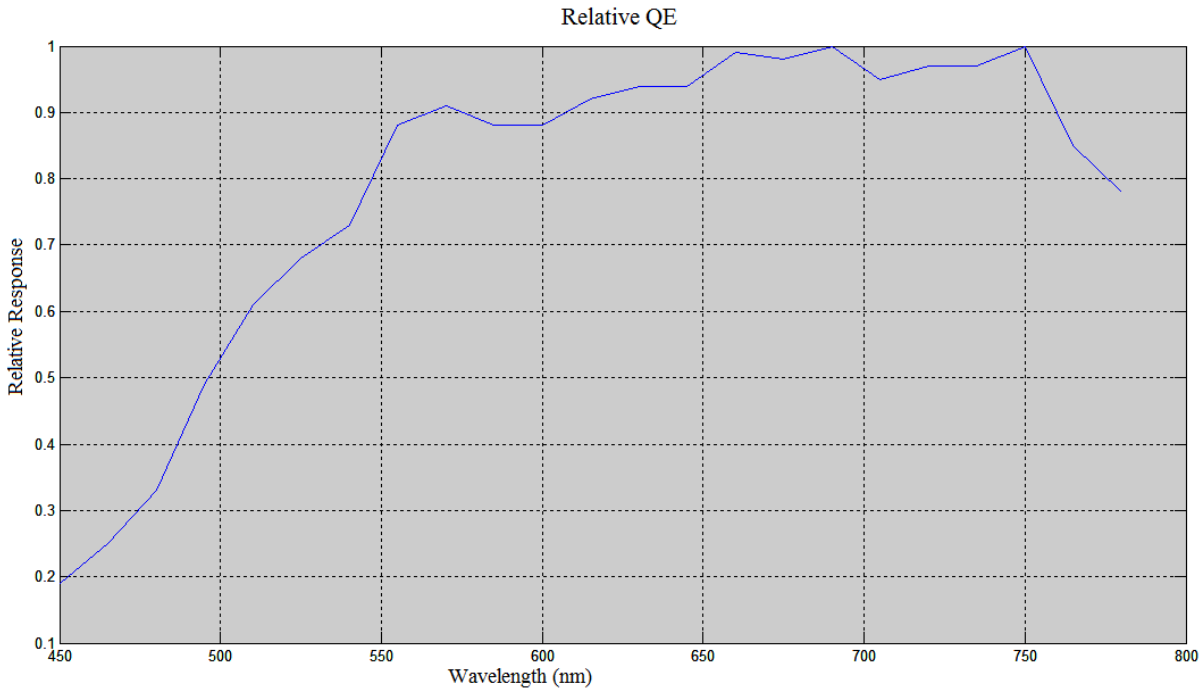


Figure 3: Relative Quantum Efficiency

Application Data

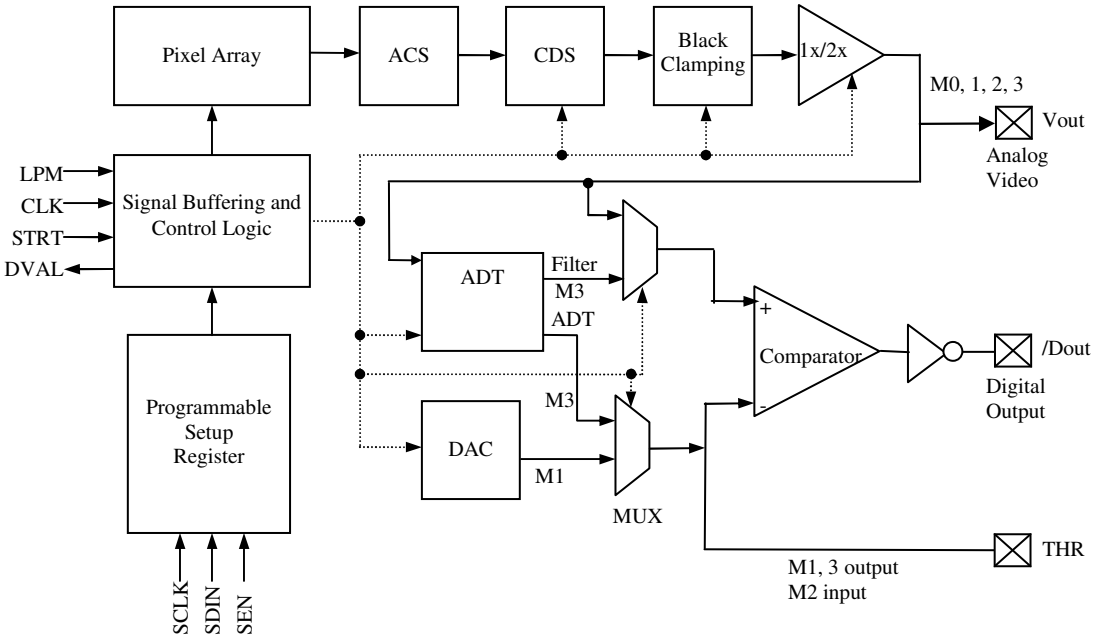


Figure 4: Simplified Block Diagram. Mx numbers indicate output mode that path is active – see table 5.

Theory of Operation

Overview

A simplified functional block diagram of the RPLIS-2048-EX imager is shown in Figure 4. The pixel array represents the 12 optical black pixels, 2048 video pixels, serial scanning shift register and pixel selection circuitry. All global and line initialization functions are generated by the control logic. One of the four device operating modes, along with other device options are set by programming the desired bits into the programmable setup register which then switches the mode in the control logic. The four available operating modes are: 0-Analog video output only, 1-Analog and Digital output with internal DAC used as comparator reference, 2-Analog and Digital output with external input used as comparator reference and Analog, 3-Digital and ADT output. During readout the pixel reset and video levels are buffered by the ACS amplifier and the CDS samples the difference between the two signals. At the start of each frame the Black Clamping circuit removes the offset from a reference pixel and subtracts it from each of the subsequent pixels in the frame. For all pixels other than the reference pixel the Black Clamping circuit behaves as a Unity Gain Amplifier (UGA) that drives the output amplifier. The output amplifier is a Programmable Gain Amplifier (PGA) that has 1x/2x selectable gain to adjust for varying light conditions. The multiple operating modes and device settings are selected using the programmable setup register.

The RPLIS-2048-EX has special on-chip features that increase design flexibility and reduce the number of external devices. A comparator is available to provide a digital output stream corresponding to the analog video output. The reference for the comparator can be selected as the on-chip DAC output or from an external user input. An Auto Dynamic Thresholding (ADT) analog signal processor is also included on-chip to eliminate external ADC's and signal processing in most applications. If desired, and external A/D can be added to either the raw analog video and/or to the ADT generated dynamic threshold. The ADT digital output is specifically designed for barcode or other binary imaging applications to generate a bit stream identifying which pixels are "white" and which are "black". The ADT can process analog video signals that are only a few hundred millivolts in amplitude and in conditions where the profile of the light source is not uniform across the pixel array. By controlling the exposure time and gain, the

user can control the signal amplitude applied to the ADT. Additionally the user can control the response time of the ADT via external capacitor. See the Application circuit for more details.

Dynamic Power Control: When one of the four modes is selected the on-chip control logic disables the circuits that are not being used to minimize the power consumption. A Low-power Standby mode is also available to disable the entire imager when it is not in use. During normal operation in any mode the amplifiers in the analog video readout path are dynamically enabled and disabled to further reduce power. When the imager is not actively outputting video the ACS, CDS and Black Clamping/UGA amplifiers are disabled but the output amplifier remains active and drives the black video level. When a new line readout is initiated the disabled amplifiers are enabled to process the video signal until the end of the frame where they are disabled again until the next frame readout. When using any of the special on-chip features the dynamic power control is also implemented. As a result, the DAC, ADT and comparator are only active while video is being generated and disabled otherwise.

Device Operation & Timing

General

The operation of the RPLIS-2048-EX is very simple, only a clock and start pulse are needed in a minimal configuration. With the clock running, readout is initiated when STRT is sampled high on the rising edge of clock. This event triggers the line initialization sequence. Line initialization consists of transferring the photo-generated charge from each pixel to the storage node for readout, enabling the amplifiers and starting up internal timing circuits. This sequence is always 16 clock cycles long. After the line initialization is complete DVAL goes high indicating that the first optical black pixel is valid. Once the last video pixel has been readout DVAL goes low indicating the end of the frame.

Feature Selection

The RPLIS-2048-EX has multiple operating modes and operating features that are selected using the programmable setup register. The programmable features are discussed below and summarized in the table at the end of this section.

Video Output Modes [Bits10:9]

The unique design of the RPLIS-2048-EX on-chip video signal processing offers the user a choice of four video output modes, the output mode is set by bits 10 & 9 in the programmable setup register:

- Mode 0: Raw Analog Video only output on the Vout pin with the ADT processor, DAC and comparator disabled. This mode is used if only raw analog output is needed for input to an external analog to digital converter or comparator.
- Mode 1: Raw Analog Video output on Vout pin AND 1-bit Digital output on /Dout pin from the internal comparator. The internal user programmable DAC is used as threshold reference for the comparator digital output. The DAC voltage is output on the THR pin. This mode is ideal to provide both a raw analog output and a binary digital output using a preset threshold.
- Mode 2: Raw Analog video is output on Vout pin AND 1-bit Digital output on /Dout pin from the internal comparator. User inputs threshold voltage on THR pin. Same as Mode 1 except user provides external threshold voltage to THR pin. Note that the user can supply a set DC level or an externally generated analog signal as the threshold.
- Mode 3: Raw Analog Video output on Vout pin AND 1-bit Digital output on /Dout pin AND the Automatic Dynamic Threshold is output on the THR pin. The on-chip ADT circuit generates an adaptive threshold (Automatic Dynamic Threshold) voltage for the on-chip comparator digital output. The user can adjust the ADT rate of change by varying the capacitor that is connected to the THR pin. See the application circuit for more detail. *Note that the first few pixel values may not be valid due to the time delay of the ADT circuit.*

Auto Dynamic Threshold (ADT) is a form of analog video signal processing that detects a varying video signal that is superimposed on a non-uniform DC level. Localized signal processing is performed within a window of pixels to determine whether or not the video level is above or below the average of all pixels within the window. This calculated 'moving average' becomes the dynamic threshold. The user can select the moving window size as 3, 6, or 9 pixels as well as select the amount of hysteresis within that window 20mV or 118mV.

Selectable Gain [Bit8]

During low light conditions the gain of the analog video amplifier can be increased to 2x for increased sensitivity by setting bit 8.

DAC Output Selection [Bits7-4]

In the standard comparator mode, the comparator threshold can be supplied by the on-chip DAC or by the user via the THR pin. The DAC will supply threshold voltages in the video signal range between the black level and VDD, see the equation below for more details. In all three digital output modes, the data rate is 2048 bits per frame (one bit per pixel). The power-up default setting is 0000.

V_{DAC}=Black level + (DAC[3:0])/16*(VDD - Black level)

Table 4: DAC Output Values.

Bits [7:4]	DAC Out	Bits [7:4]	DAC Out	Bits [7:4]	DAC Out	Bits [7:4]	DAC Out
0000	0.32V	0100	0.98V	1000	1.65V	1100	2.32V
0001	0.48V	0101	1.14V	1001	1.81V	1101	2.48V
0010	0.64V	0110	1.31V	1010	1.98V	1110	2.65V
0011	0.81V	0111	1.48V	1011	2.15V	1111	2.81V

*Table represents nominal expected values for a Black Level of 0.32V and a VDD of 3.0V. 0000 is default setting for bits 7-4.

ADT Pixel Delay [Bits3:2]

This is used only when operating the device in Mode 3. The video signal is delayed by the ADT and compared with the filtered video signal. The amount of delay is selectable to be 3 (default), 6 or 9 pixels to allow flexibility when using the ADT processor. Note that the digital output /Dout, is delayed from the corresponding analog output (Vout) by the value of this setting.

Comparator Hysteresis Select [Bit 1]

This is used only when operating the device in Mode 3. The hysteresis of the comparator is selectable to increase the noise immunity. The default hysteresis setting is 20mV but can be increased to 118mV.

Exposure Time [Bit0]

In default mode [normal exposure] the user will get a minimum of 2074 clocks for a minimum exposure time. To get short exposure time the user needs to program the bit to 1, using serial interface logic. In the short exposure mode the user will get a minimum of 11 clocks for minimum exposure time.

Table 5: Programmable Setup Register Bit Definitions.

Bit #	Description (* power-up default settings)
10:9	Output Mode Select bits 00* = Mode 0 - Analog Output Only (ADT, DAC & Comparator disabled) 01 = Mode 1 - Digital Output Enabled with DAC Output used for Comparator Threshold 10 = Mode 2 - Digital Output Enabled with "THR" used for Comparator Threshold 11 = Mode 3 - Digital Output Enabled with ADT processing AND ADT processed Analog
8	Gain Select 0* = 1x Gain 1 = 2x Gain
7-4	DAC Output Select See Table 4
3-2	ADT Pixel Delay [Mode 3 only] 00* = 3 Pixel Delay 01 = 6 Pixel Delay 1x = 9 Pixel Delay
1	ADT Hysteresis Select [Mode 3 only] 0* = 20mV [Subject to change] 1 = 118mV [subject to change]
0	0* = Normal Exposure Time 1 = Short Exposure Time

Low Power Standby Mode

When the device is not in use it can be placed into a low-power standby mode to conserve power. In this mode all analog circuitry is disabled and the digital timing controller is held in reset. The programmable setup

register remains active to retain device settings and to allow new settings to be programmed while the device is not in use. As long as SCLK is not running the programmable setup register will not consume any additional power. The master input clock can be stopped during standby for ultra-low dissipation and should not start until after returning to normal mode of operation.

Readout Timing – Short Exposure

Short exposure is set with a logic "1" in bit "0" of the Programmable Setup Register for Short Exposure. The Clock signal ("CLK") is a free-running 50% duty-cycle clock. The start pulse ("STRT") goes high before a rising "CLK" edge to end the short exposure time and the line initialization sequence followed by the black pixel and video pixel readout. Integration starts when "DVAL" output goes low, and ends 9 clocks after "STRT" goes high. The minimum integration is 11 clocks.

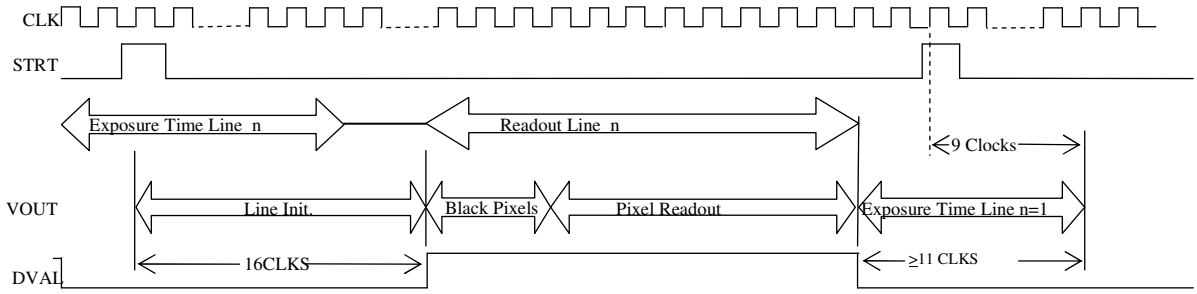


Figure 5a: Short Exposure Time.

Readout Timing – Normal Exposure

Normal Exposure is the default exposure method with logic "0" set in bit "0" of the Programmable Setup Register. To program the Programmable Setup Register see Figure # 9. The Clock signal ("CLK") is a free-running 50% duty-cycle clock. The start pulse ("STRT") goes high before a rising "CLK" edge to end the normal exposure time and the line initialization sequence followed by the black pixel and video pixel readout. The "DVAL" output goes high when the line initialization has completed after 16 clocks of "STRT" high and goes low when the last pixel has been read out. The normal exposure time is determined by the period of "STRT" signal (Fig. 5b), which is equal to period of STRT – 2 clocks. The "STRT" can only be triggered after all pixels have been read out. The initialization sequence always takes 16 clock cycles to complete (see below) and is followed by the black pixel readout sequence indicated by the rising edge of the "DVAL" output. So, the minimum STRT period is 2060+16 =2076 clocks, and the minimum exposure time is 2074 clocks.

Comparator Readout Timing

The readout timing when in one of the two standard comparator modes (Mode 1 with internal DAC reference or Mode 2 with externally applied reference) is similar to the standard timing (Fig. 6). Additionally, the digital output is also present on the /Dout pad concurrently with the analog video. Every clock cycle a valid digital signal and analog value is available and the output is only valid while DVAL is high.

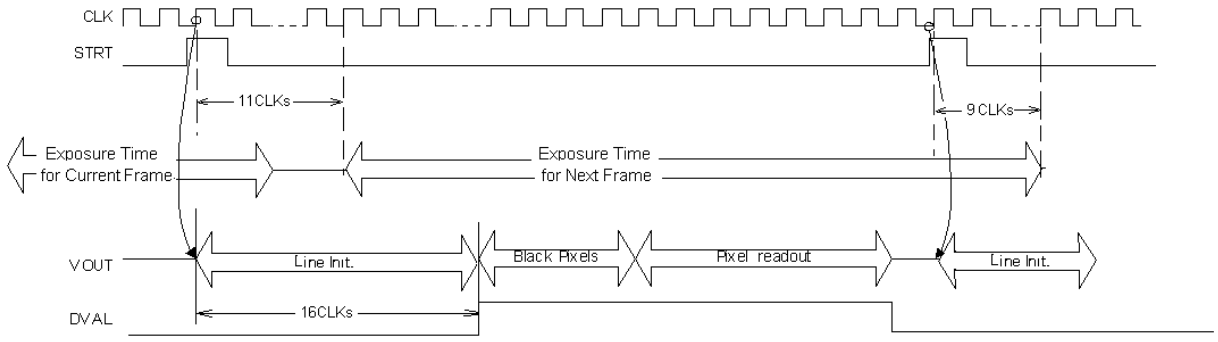


Figure 5b: Normal Exposure Time.

ADT Readout Timing

The readout timing in ADT mode (Mode 3) is similar to comparator mode except that there is a delay in the digital output with respect to DVAL (Fig. 7). The first digital bit is valid 3, 6 or 9 clock cycles after DVAL goes high. The number of delayed clock cycles is programmable and is set through the programmable setup register. The default is 3 clock cycles. The delay at the start of the line is also translated to the end so that the last digital bit is valid 3, 6, or 9 clock cycles after DVAL goes low.

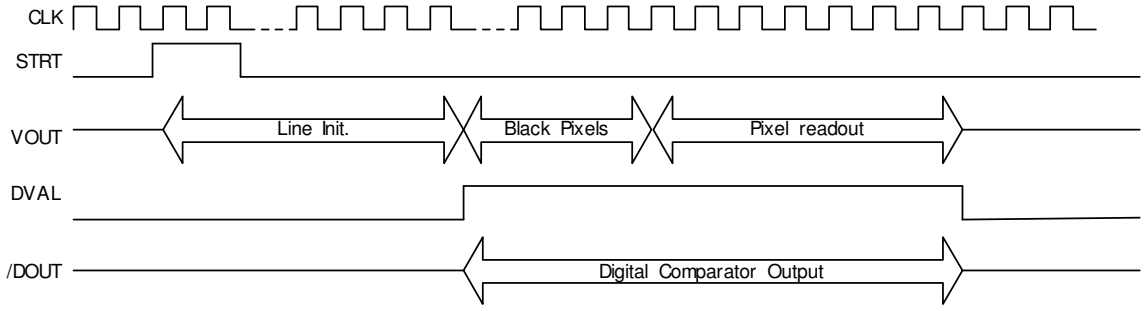


Figure 6: Comparator Readout Timing.

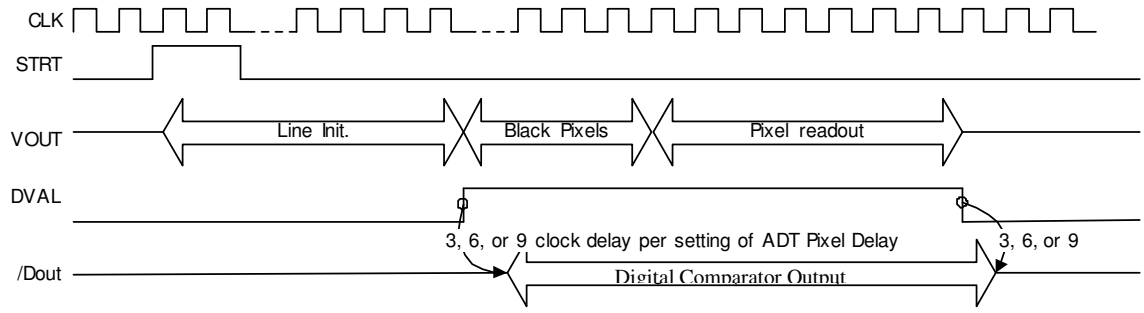


Figure 7: ADT Readout Timing.

Note that /Dout is delayed from Vout and Dval by the ADT pixel delay setting. Also note that the first few pixel data output on /Dout may not be valid due to the ADT delay.

Line Initialization Detail

Line initialization is 16 clock cycles after STRT has been sampled as a rising edge. It is used for frame storage transfers to ACS bus transfer and pixel to frame storage and other internal operations.

Actual exposure time stops at the first clock cycle after STRT has been sampled as a rising edge and the next exposure begins on the next falling edge of DVAL.

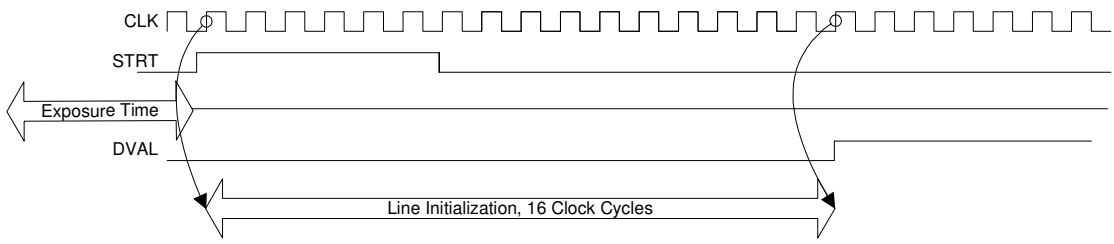


Figure 8: Line Initialization Timing

Programmable Setup Register

A programmable setup register is used to set device operating parameters and for mode selection. The 3 signals required for the programmable setup register include a Setup Clock (SCLK), Setup Data Input (SDIN) and a Setup Enable (SEN) that latches the data once all bits are shifted in. Programmable setup register timing is illustrated below.

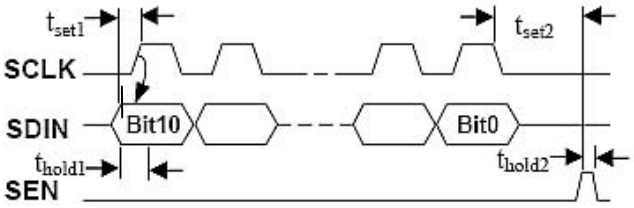


Figure 9: Programmable Setup Register Timing.

When loading bits into the programmable setup register the data bit must be stable on "SDIN" before the rising edge of "SCLK". Once the data bit has been sampled and stored on the rising edge of "SCLK" the next bit can be put on "SDIN". After all bits have been shifted in, "SCLK" must be kept low and "SEN" must be pulsed to transfer the data bits in parallel to a storage register. When the programmable setup register is not in use both "SCLK" and "SEN" should remain low. If the device is put into Low Power Mode (LPM) the settings are retained. Minimal timing: t_{set1}=4ns, t_{hold1}=12ns, t_{set2}= 1 period of SCLK, and t_{hold2}=4ns.

Pixel Timing Detail

The video output sequence is shown in Figure 10 below. A new pixel appears on rising edges of the clock signal.

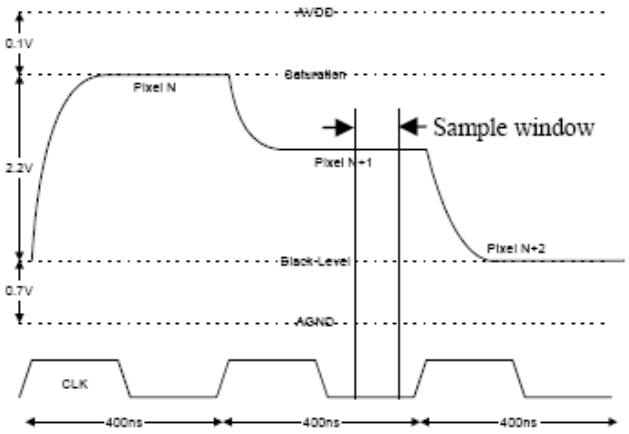


Figure 10: Detailed Pixel Timing.

Note: Clock input to be 50% duty cycle. Overshoot and undershoot to 5% or 0.16Volts from DGND or DVDD. Trise and Tfall <<5ns.

RPLIS-2048-EX Typical Application Circuit

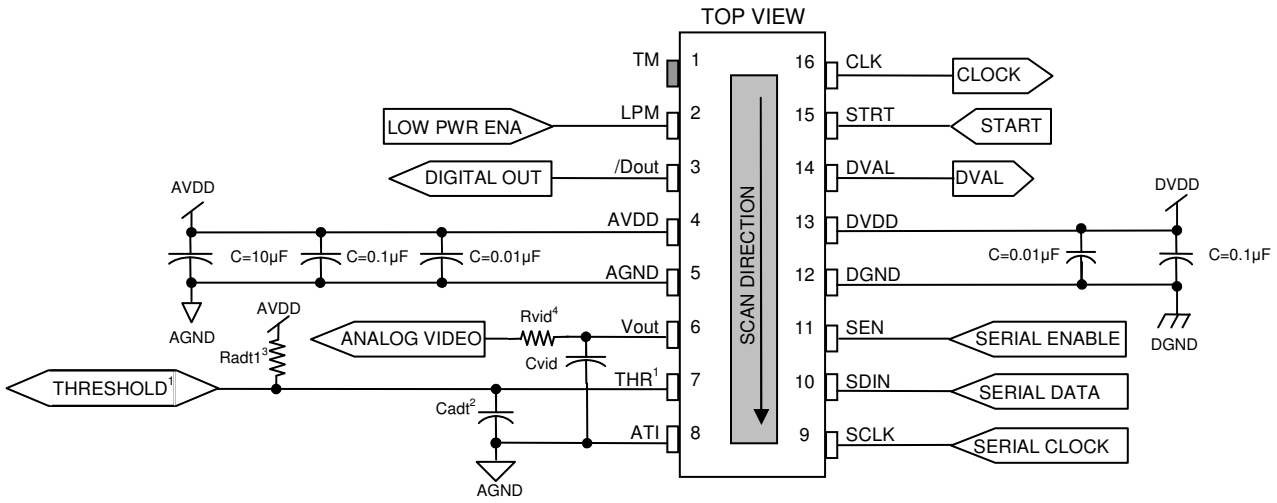


Figure 11: Application Circuit

Notes:

1. THR pin not used in Mode 0 and should not be connected. Mode 1 THR pin is an analog output with value of the internal DAC as set by the user. Mode 2 THR is an analog input. Mode 3 THR is an analog output which is the internally generated dynamic threshold.

2. Cadt is mode dependant as follows: Mode 0, 1, and 2 - not needed; Mode 3 - Cadt determines the rate of change or the slew rate of the dynamic threshold. Table 6 lists suggested values but the user can choose the best value that suits the application.

3. Radt1 is only used for Mode 3, and therefore not populated for Modes 0, 1, and 2. Table 6 lists suggested valued for Radt for various operating speeds.

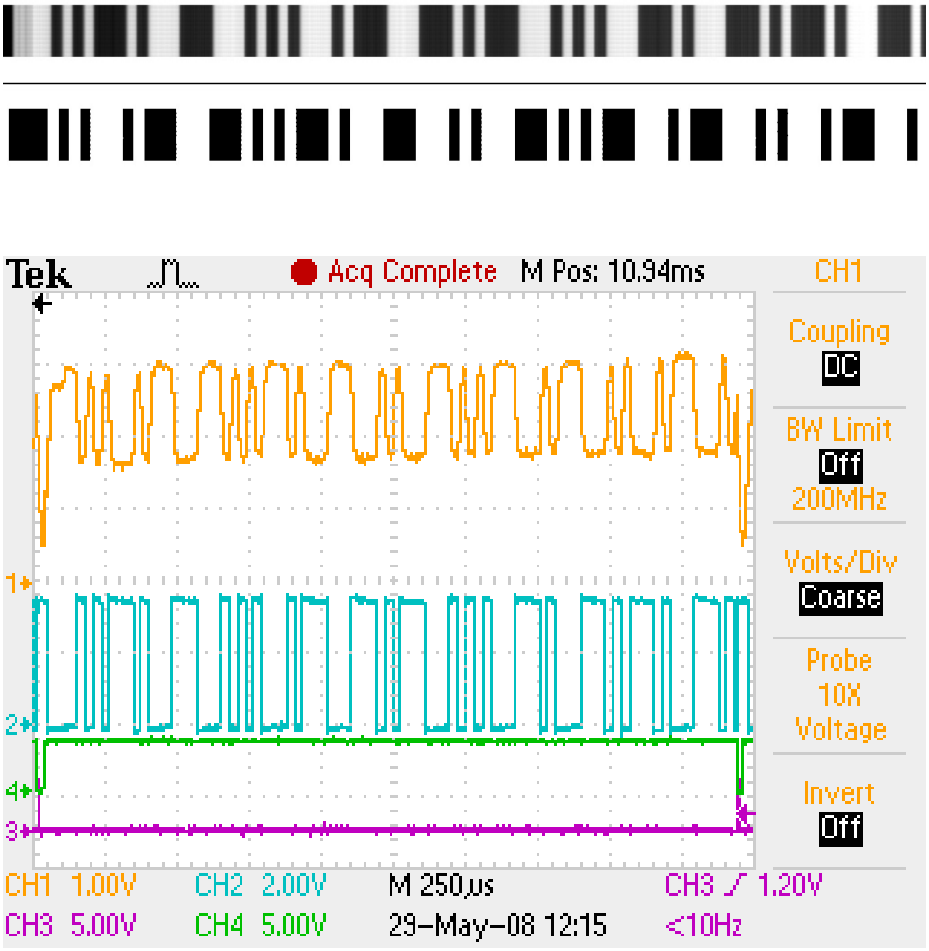
4. If using the analog video in modes 0, 1, and 2, a simple RC filter can be applied to the video prior to the user-supplied A/D. R & C should be set to provide a bandwidth filter one-half of the clock rate. For example at 1.25MHz, a 2000kΩ resistor and a 4700pF capacitor are sufficient. For Mode 3, Rvid not needed and Cvid can be populated with a small capacitance to provide filtering of the analog video to reduce or eliminate unwanted transients on the Digital output (/Dout).

5. /Dout (modes 1,2,3) has inverted polarity compared to Analog Out.

6. In mode 3, /Dout signal polarity is depend on reference signal's DC level for comparator. This reference signal is internally generated (Automatic Dynamic Threshold) but user can adjust the DC level of reference signal by varying the capacitor that is connected to "THR" pin. Please see application circuit for more details.

Speed	100KHz	500KHz	1Mhz-2.5MHz
THR - ADT Capacitor (Cadt)	.22 uF	6800pF	4700pF
THR - ADT Pull Up Resistor (Radt1)	2 Meg ohm	2 Meg ohm	2Meg ohm

Table 6: Cadt and Radt suggested values at nominal clock frequencies.



Example : Mode 3 (ADT), 1.0MHz Clock, 1X Gain, 9 Pixel Delay, 20mV Hysteresis

Top Bar Code-Analog Video

Bottom Bar Code – Digital Out

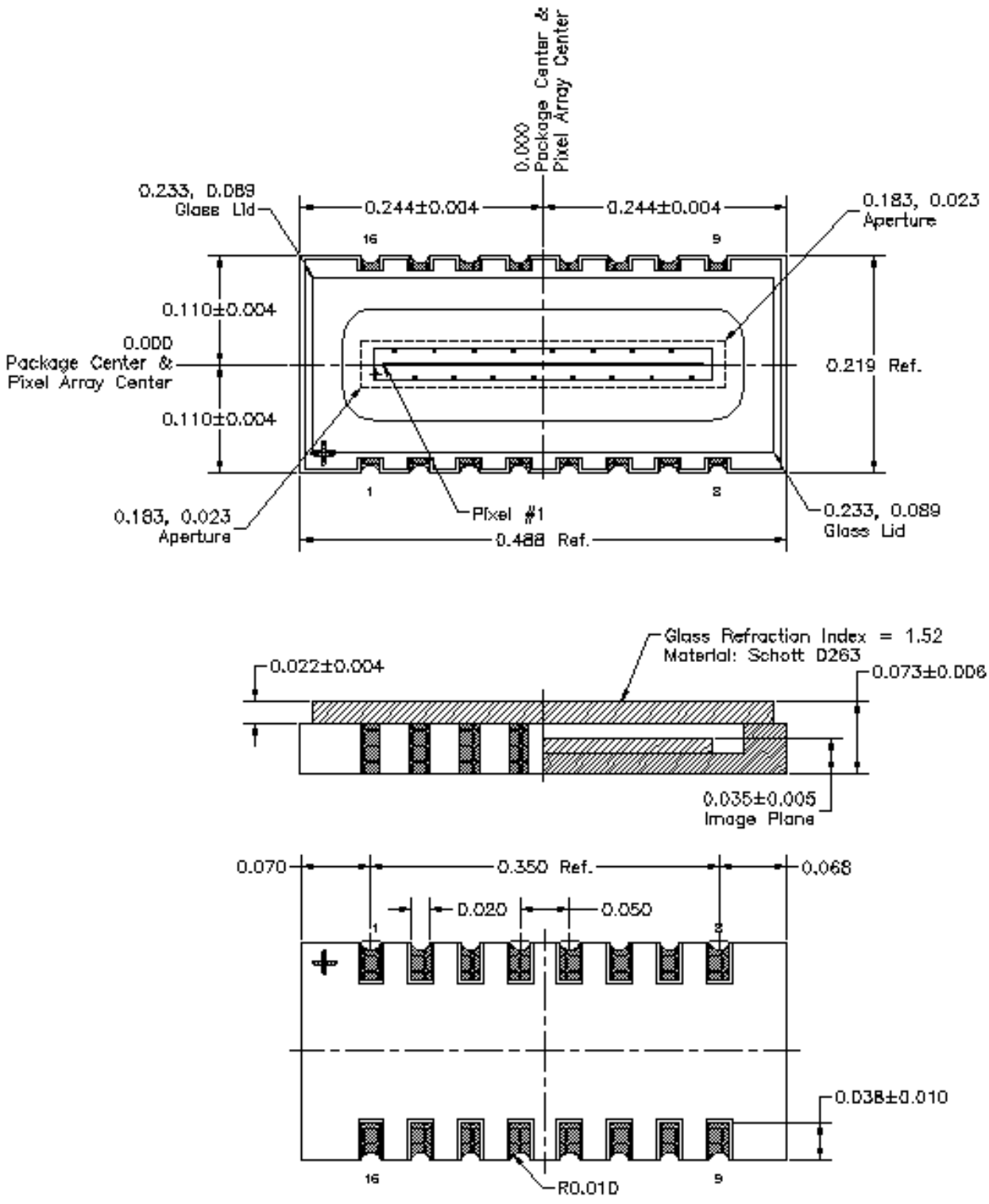
Scope Trace 1-Analog Video

Scope Trace 2 - Digital Out

Scope Trace 3 - STRT

Scope Trace 4 - DVAL

Package Data



Units are in inches unless otherwise noted

Characterization Criteria

Characterization measurements are guaranteed by design and are not tested for production parts. Unless otherwise specified, the measurements described herein are characterization measurements.

Full Well

Full well (or Saturation Exposure) is the maximum number of photon-generated and/or dark current-generated electrons a pixel can hold. Full well is based on the capacitance of the pixel at a given bias. Full well is determined by measuring the capacitance of all pixels for the operational bias. In reality, the column circuitry will limit the signal swing on the pixel, so full well is defined as the number of electrons that will bring the output to the specified saturation voltage.

Quantum Efficiency

Quantum Efficiency is a measurement of the pixel ability to capture photon-generated charge as a function of wavelength. This is measured at 25nm increments over the wavelength range of 300 to 1100 nm. Measurements are taken using a stable light source that is filtered using a monochromator. The exiting light from the monochromator is collimated to provide a uniform flux that overfills a portion of the sensor area. The flux at a given wavelength is measured using a calibrated radiometer and then the device under test is substituted and its response measured.

Linearity

Linearity is an equal corresponding output signal of the sensor for a given amount of photons incident on the pixel active area. Linearity is measured numerous ways. The most straightforward method is plotting the saturation exposure measurement from 5% to 70% of full well and applying a “best fit” straight-line plot and finding the greatest deviation (error) in terms of percent of full well.

Dark Signal

The ‘dark signal’ is the voltage proportional to the accumulated electrons for a given exposure period, that were not photon generated. There are a few sources in CMOS circuits for the dark current and the dark current levels will vary even for a given process. Dark signal is measured for a 10 millisecond exposure time at T_A = 25°C.

Read Noise

Read noise is the temporal or time variant noise in the analog signal. Read noise does not include Fixed Pattern Noise (FPN) or dark signal. FPN and dark signal are fixed levels per pixel for a given temperature, illumination and pixel. Read noise will be measured at the output of the imager with proper loading and bandwidth limitations applied. Two successive frames of image data will be collected and subtracted from each other to determine the combined noise of the imager and test jig. A second pair of frames are captured with a low noise d.c. source substituted for the imager. Again these two frames are subtracted to determine the noise of the test jig. Since noise sources add in quadrature, the noise of the imager is calculated by subtracting the second measurement from the first in a root-mean-square fashion.

Image Lag

Image lag is the amount of residual signal in terms of percent of full well on the current frame of video after injecting the previous frame of video. Image lag is measured by illuminating a number of pixels (TBD) to 50% of saturation for one frame and then rereading those pixels for the next and subsequent frames without light exposure. Any remaining residual signal will be measured and recorded in terms of percent of full well.

Dynamic Range

Dynamic range is normally calculated by dividing the full-scale output voltage swing by the root mean squared (rms) temporal read noise voltage and expressing the result in decibels.

$$DR = 20\log\left[V_{FS} \Big/ e_n\right]$$

Part number info

RPLIS-2KEXB-LG, 16-pin LCC glass lidded package.

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