

RQJ0304DQDQA

Silicon P Channel MOS FET
Power Switching

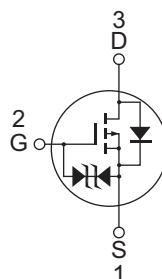
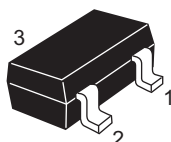
R07DS0296EJ0300
Rev.3.00
Jan 10, 2014

Features

- Low gate drive
 V_{DSS} : -30 V and 2.5 V gate drive
- Low drive current
- High speed switching
- Small traditional package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Notes: Marking is "DQ".

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	+8 / -12	V
Drain current	I_D	-1.8	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-8	A
Body - drain diode reverse drain current	I_{DR}	1.8	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, Duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

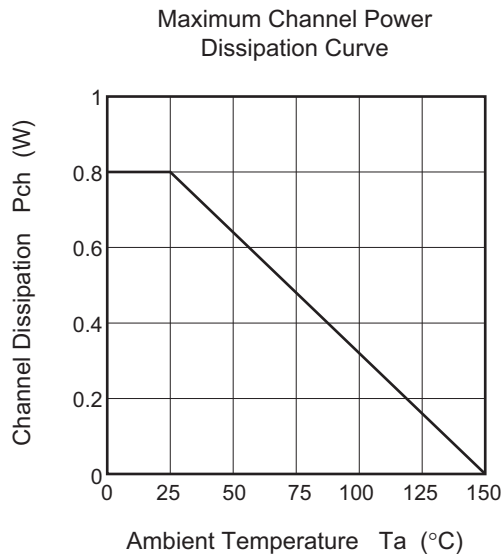
Electrical Characteristics

(Ta = 25°C)

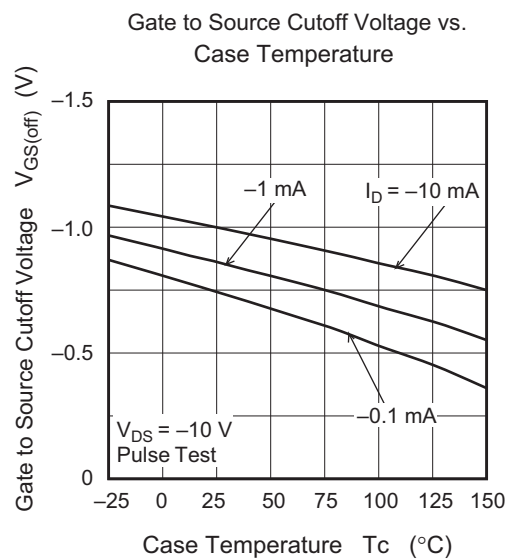
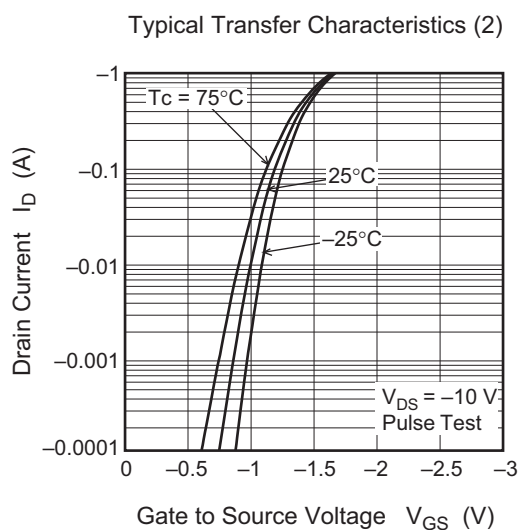
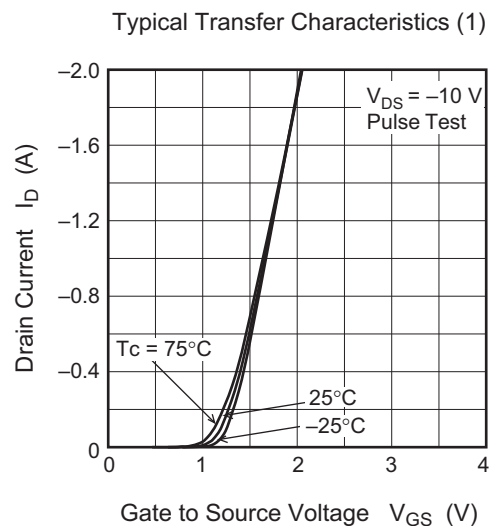
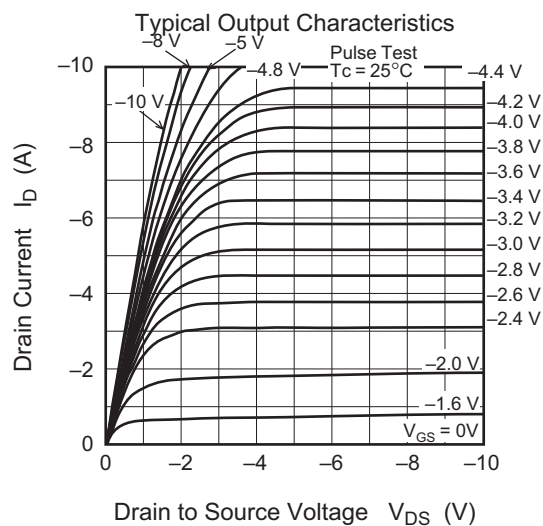
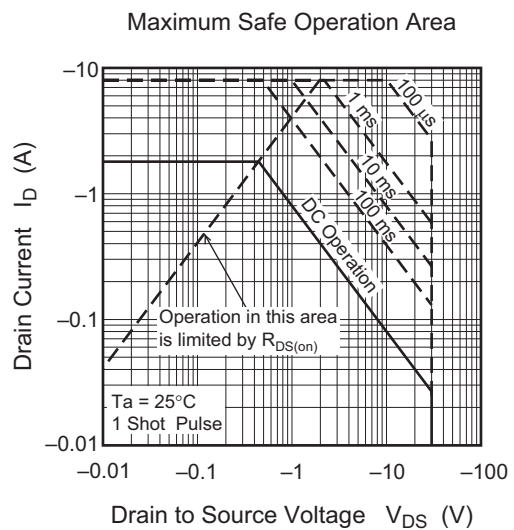
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8	—	—	V	$I_G = +100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +6 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	195	245	$\text{m}\Omega$	$I_D = -1.0 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
Drain to source on state resistance	$R_{DS(on)}$	—	300	420	$\text{m}\Omega$	$I_D = -1.0 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	1.8	2.5	—	S	$I_D = -1.0 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	185	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	45	—	pF	
Reverse transfer capacitance	C_{rss}	—	25	—	pF	
Turn - on delay time	$t_{d(on)}$	—	18	—	ns	$I_D = -1.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}$ $R_L = 10 \text{ } \Omega$ $R_g = 4.7 \text{ } \Omega$
Rise time	t_r	—	33	—	ns	
Turn - off delay time	$t_{d(off)}$	—	22	—	ns	
Fall time	t_f	—	5	—	ns	
Total gate charge	Q_g	—	1.9	—	nC	$V_{DD} = -10 \text{ V}$
Gate to Source charge	Q_{gs}	—	0.4	—	nC	$V_{GS} = -4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	0.7	—	nC	$I_D = -2.0 \text{ A}$
Body - drain diode forward voltage	V_{DF}	—	-0.9	-1.3	V	$I_F = -2.0 \text{ A}$, $V_{GS} = 0$ ^{Note3}

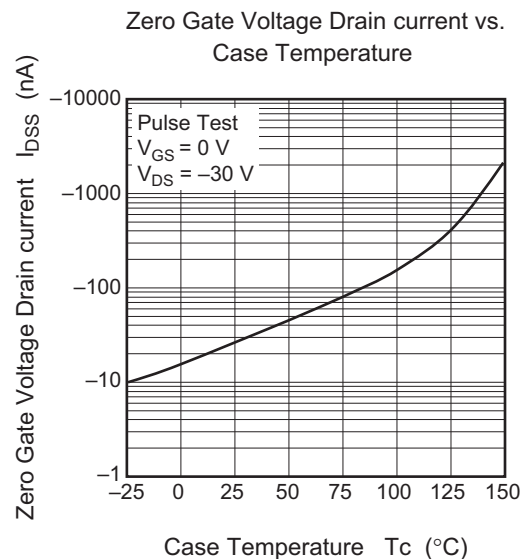
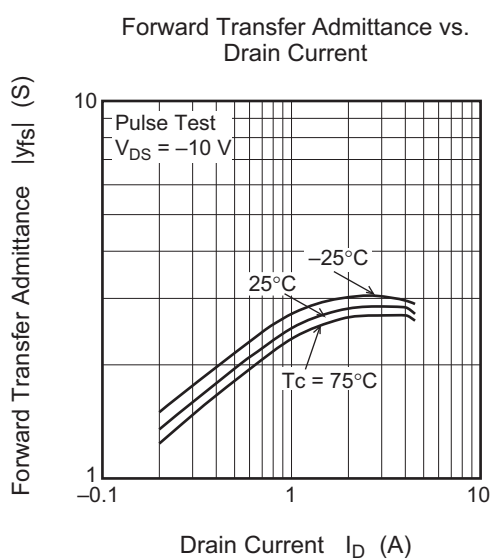
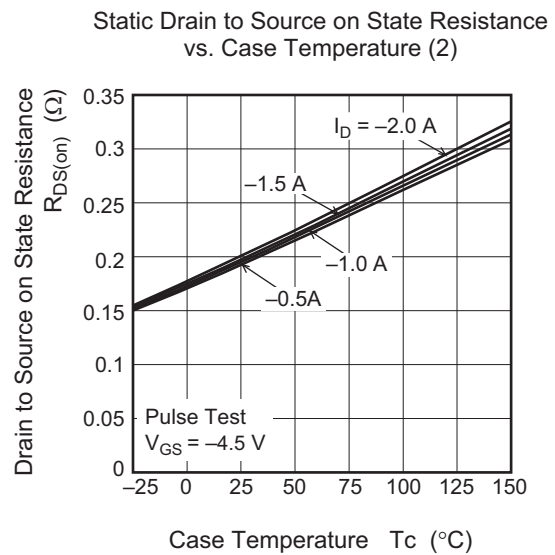
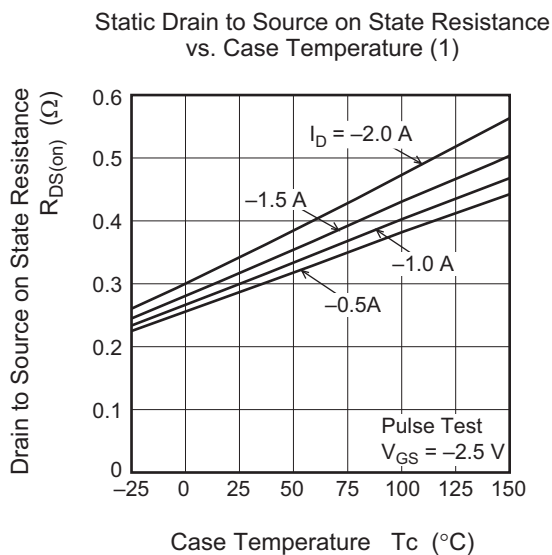
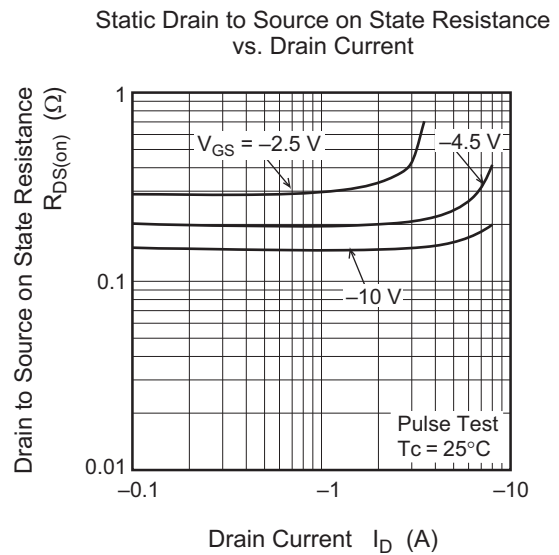
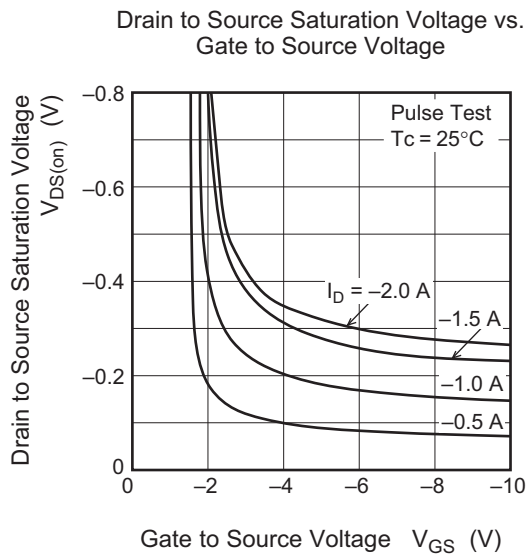
Notes: 3. Pulse test

Main Characteristics

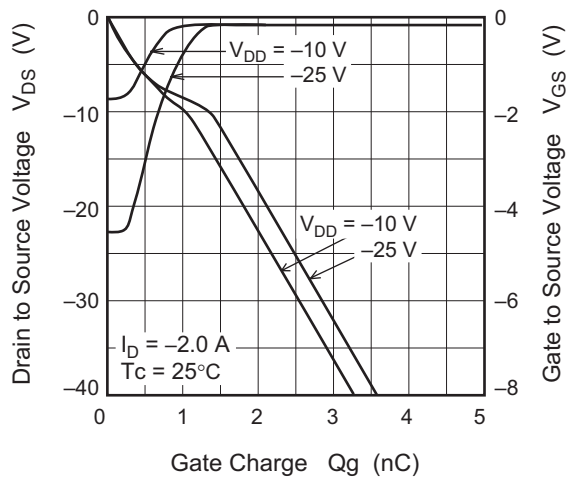


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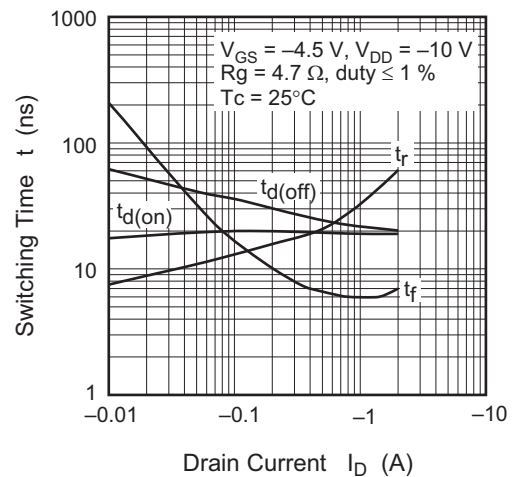




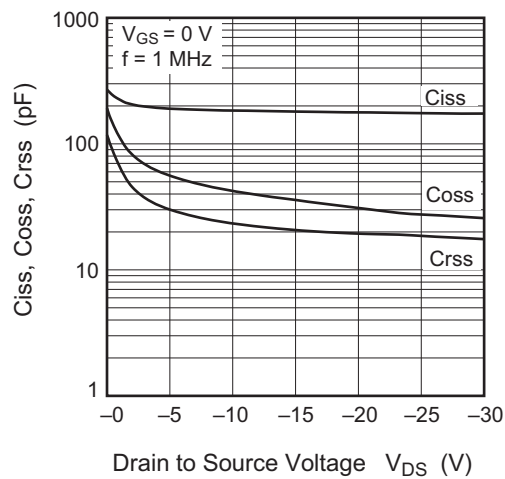
Dynamic Input Characteristics



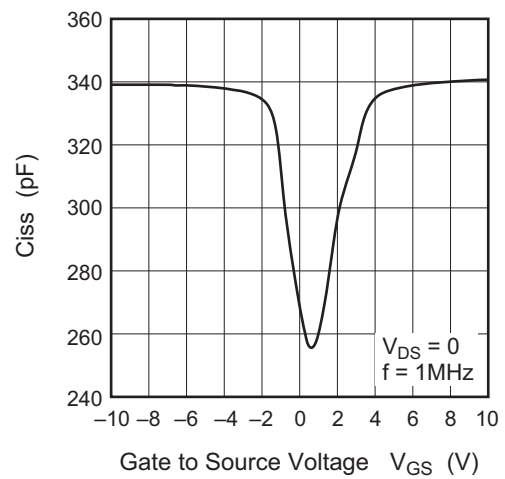
Switching Characteristics



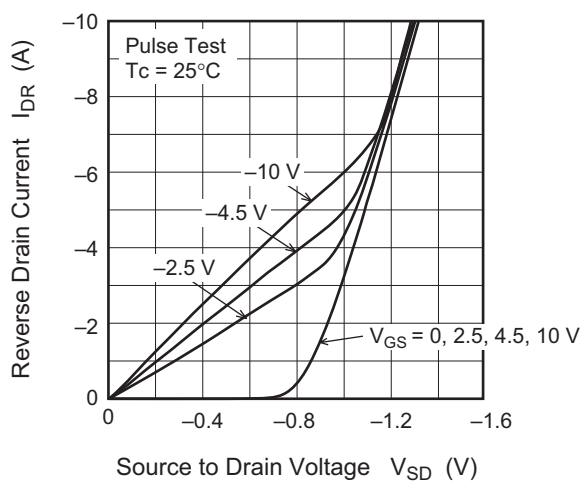
Typical Capacitance vs. Drain to Source Voltage



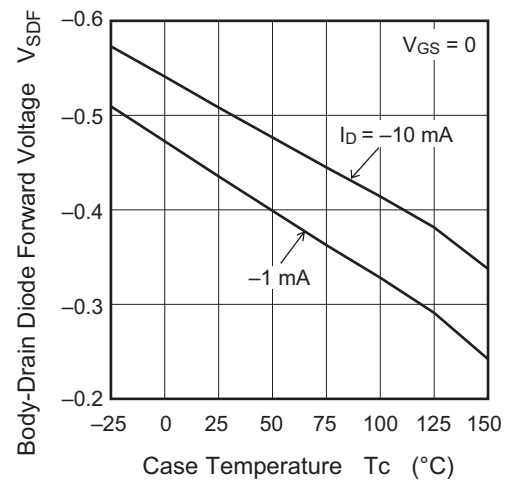
Input Capacitance vs. Gate to Source Voltage



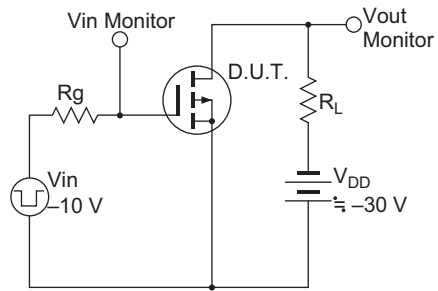
Reverse Drain Current vs. Source to Drain Voltage



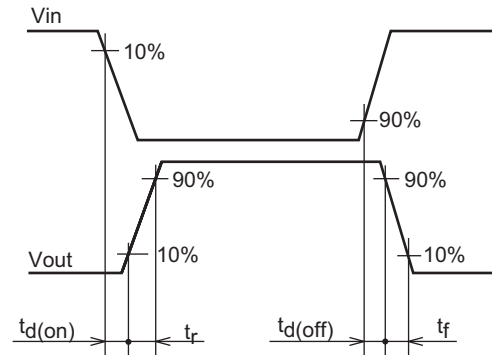
Body-Drain Diode Forward Voltage vs. Case Temperature



Switching Time Test Circuit

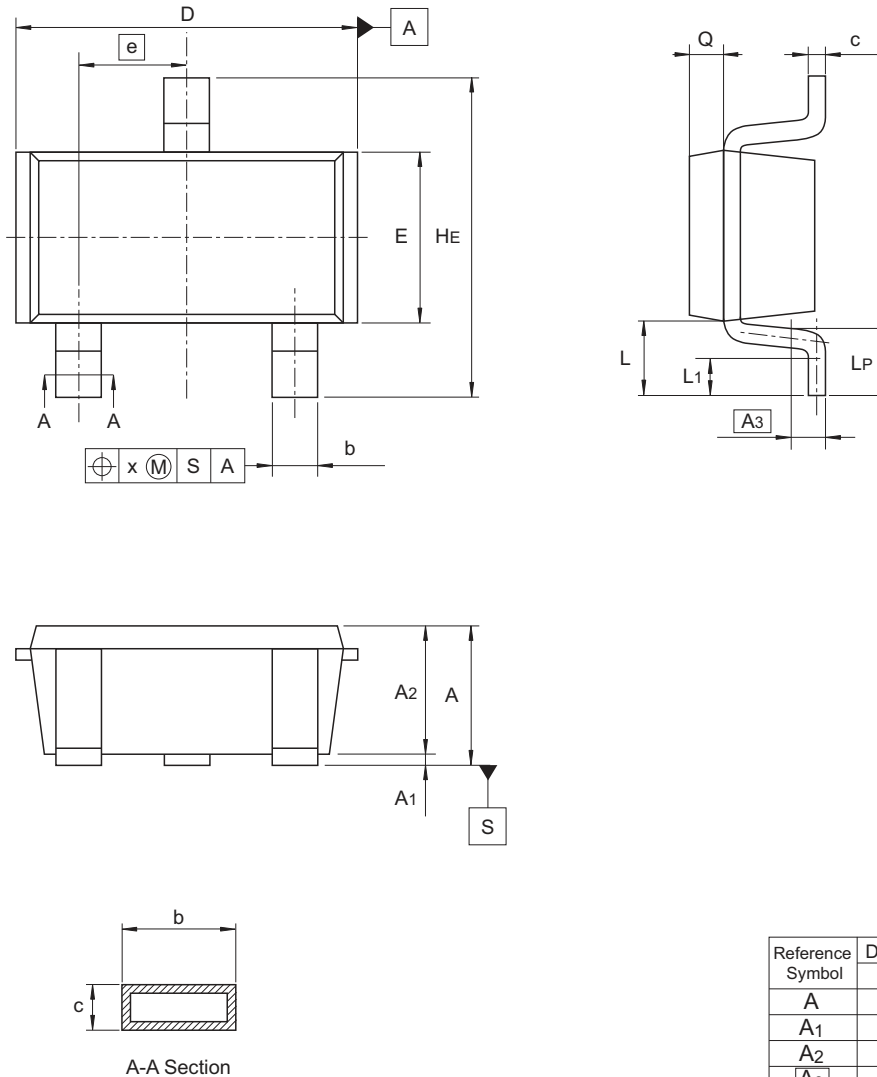


Switching Time Waveform



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A ₁	0	—	0.1
A ₂	1.0	1.1	1.2
A ₃	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
e	—	0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L ₁	0.15	—	0.55
LP	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

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Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQJ0304DQDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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