

RQJ0602EGDQA

Silicon P Channel MOS FET
Power Switching

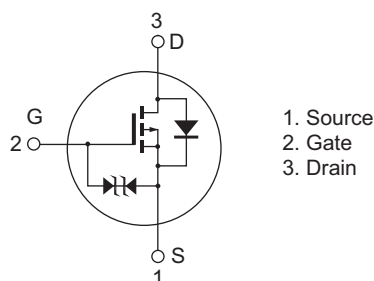
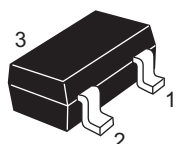
R07DS0299EJ0600
Rev.6.00
Jan 10, 2014

Features

- Low on-resistance
 $R_{DS(on)} = 490 \text{ m}\Omega$ typ ($V_{GS} = -10 \text{ V}$, $I_D = -0.55 \text{ A}$)
- Low drive current
- High speed switching
- 4.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



Note: Marking is "EG".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	+10 / -20	V
Drain current	I_D	-1.1	A
Drain peak current	$I_{D(Pulse)}$ ^{Note1}	-3	A
Body - drain diode reverse drain current	I_{DR}	-1.1	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4: $40 \times 40 \times 1 \text{ mm}$)

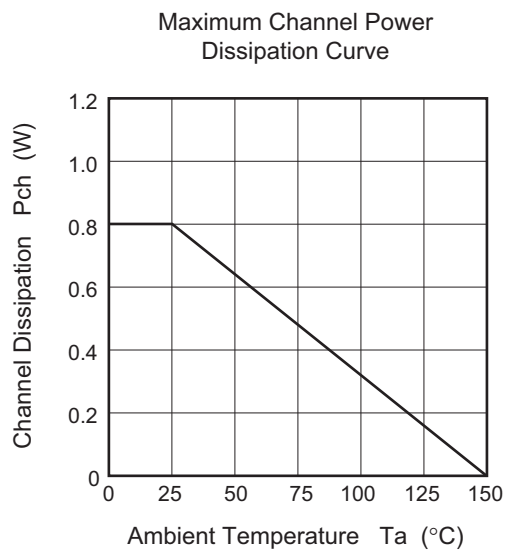
Electrical Characteristics

(Ta = 25°C)

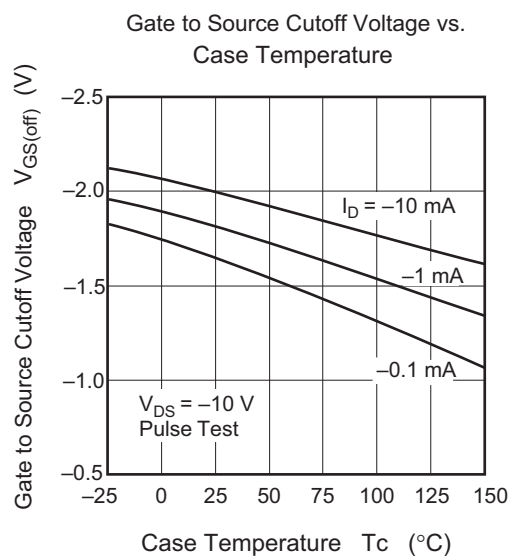
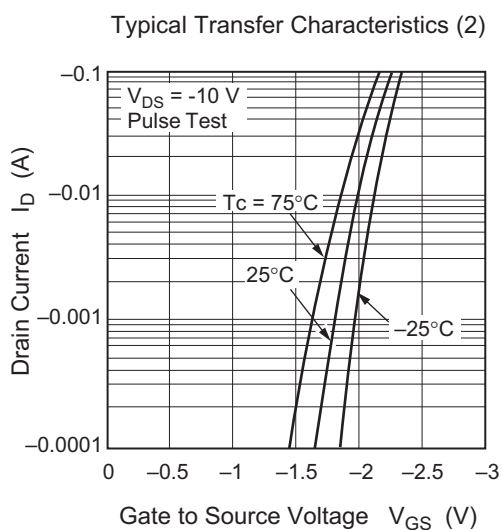
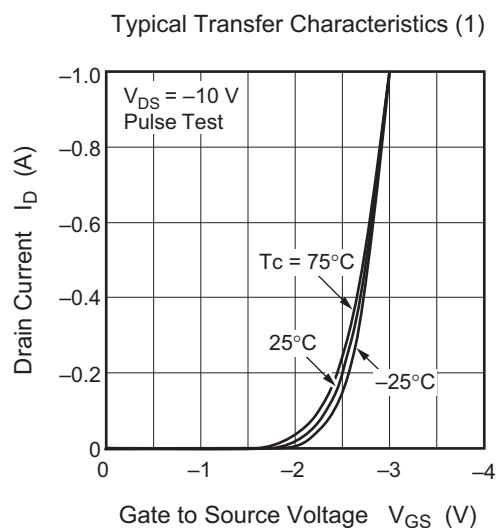
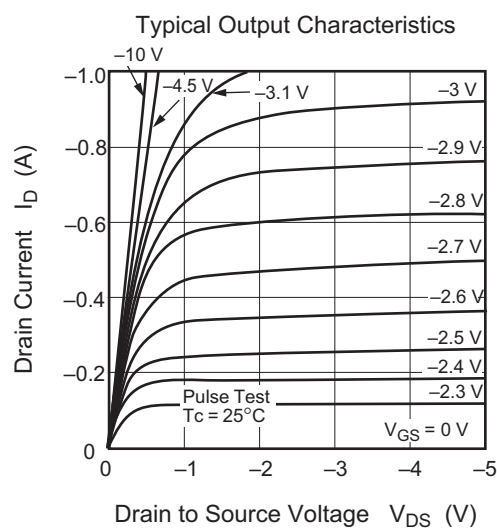
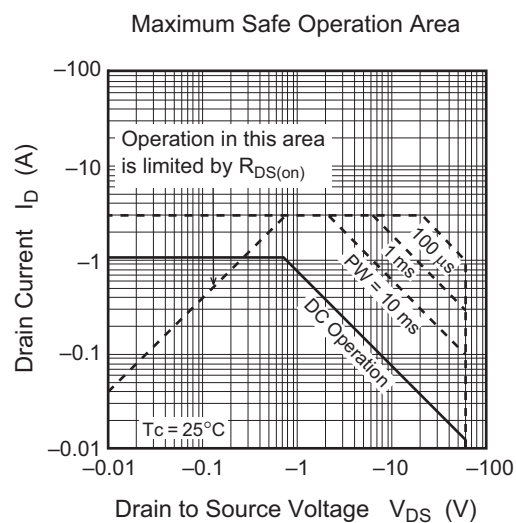
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+10	—	—	V	$I_G = +100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-20	—	—	V	$I_G = -100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +8 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -16 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	490	613	$\text{m}\Omega$	$I_D = -0.55 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	613	854	$\text{m}\Omega$	$I_D = -0.55 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	0.7	1.2	—	S	$I_D = -0.55 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	145	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	24	—	pF	
Reverse transfer capacitance	C_{rss}	—	11	—	pF	
Turn - on delay time	$t_{d(on)}$	—	23	—	ns	$I_D = -0.5 \text{ A}$, $V_{GS} = -10 \text{ V}$, $R_L = 20 \text{ } \Omega$, $R_g = 4.7 \text{ } \Omega$
Rise time	t_r	—	24	—	ns	
Turn - off delay time	$t_{d(off)}$	—	28	—	ns	
Fall time	t_f	—	19	—	ns	
Total gate charge	Q_g	—	3.0	—	nC	$V_{DD} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -1.1 \text{ A}$
Gate to source charge	Q_{gs}	—	0.5	—	nC	
Gate to drain charge	Q_{gd}	—	0.6	—	nC	
Body - drain diode forward voltage	V_{DF}	—	-0.9	—	V	$I_F = -1.5 \text{ A}$, $V_{GS} = 0$ ^{Note3}

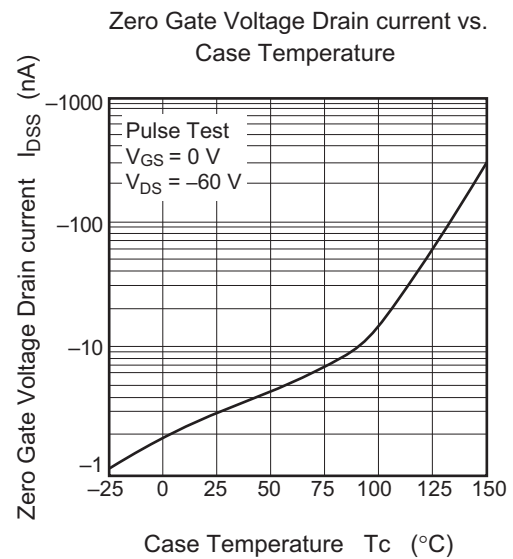
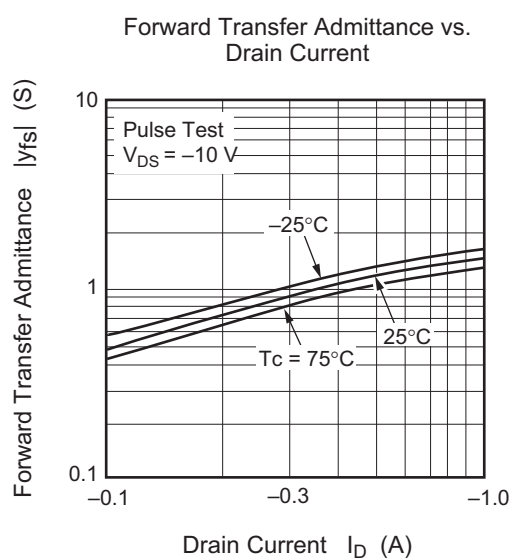
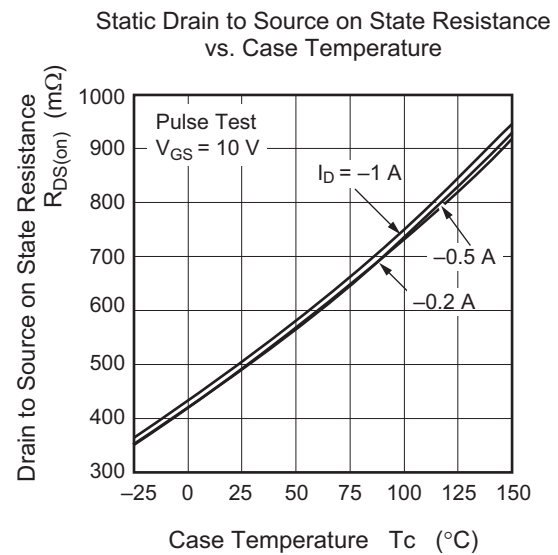
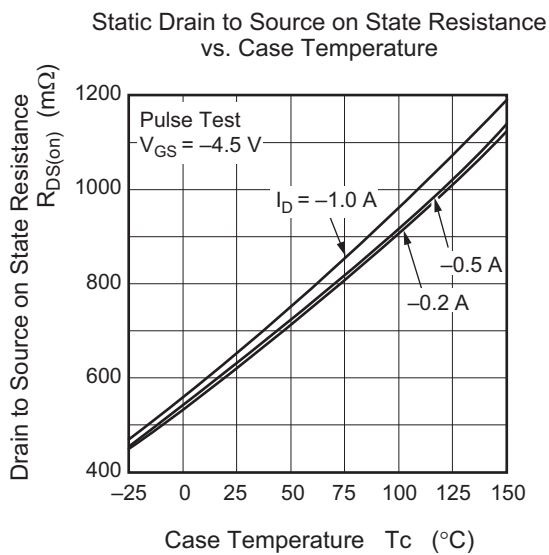
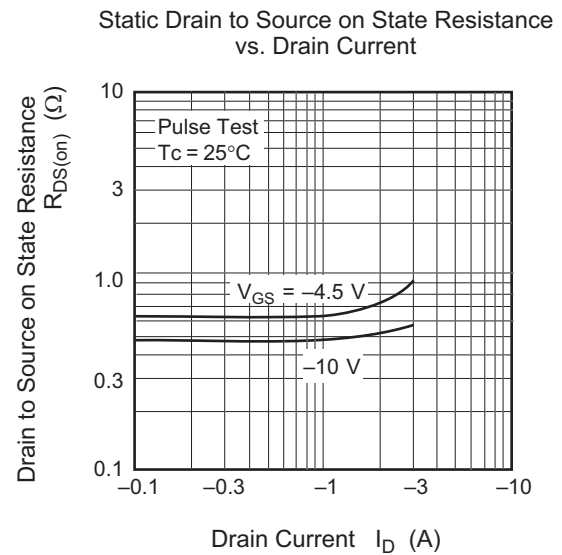
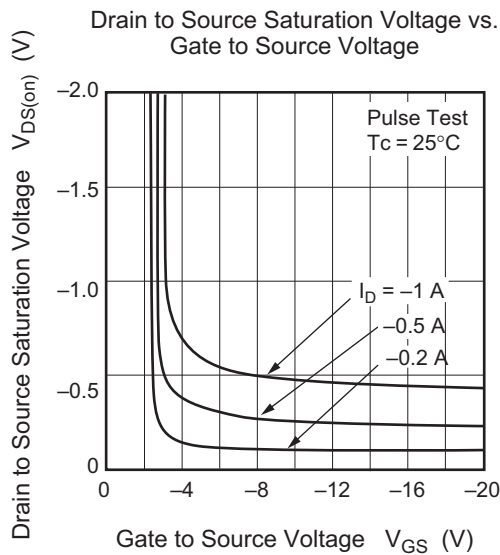
Notes: 3. Pulse test

Main Characteristics

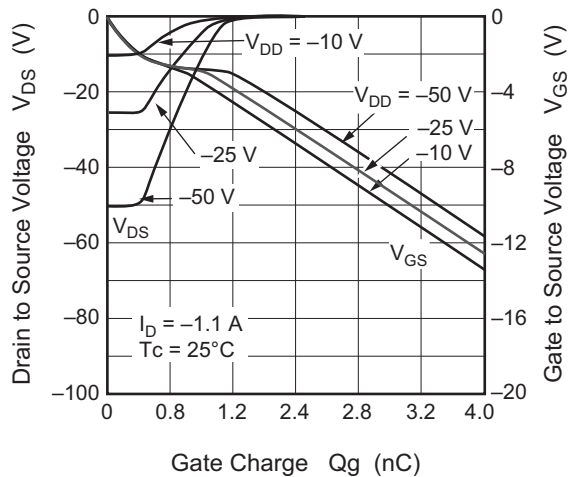


*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

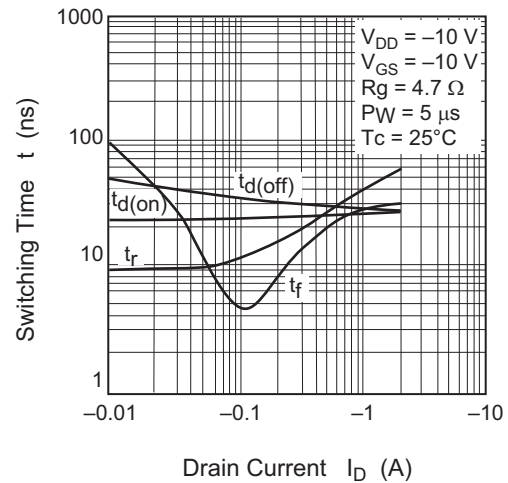




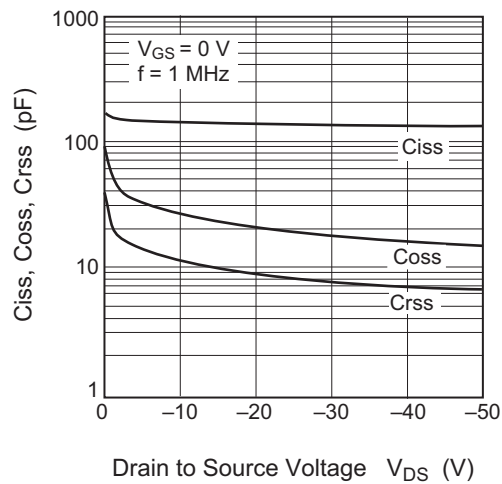
Dynamic Input Characteristics



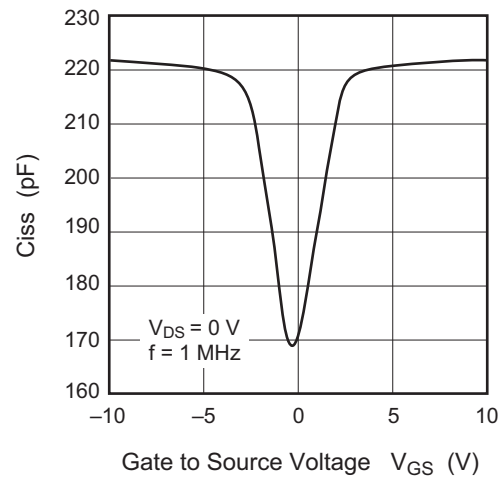
Switching Characteristics



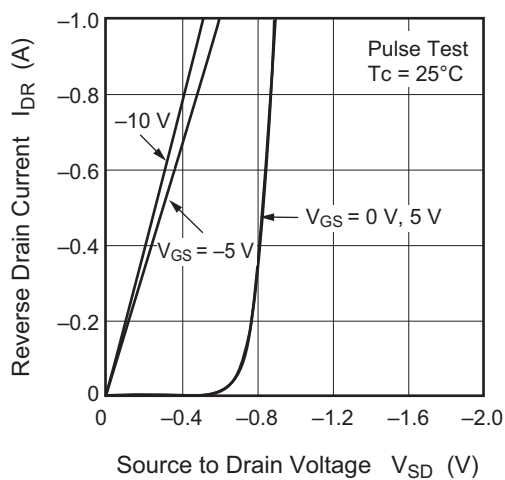
Typical Capacitance vs. Drain to Source Voltage



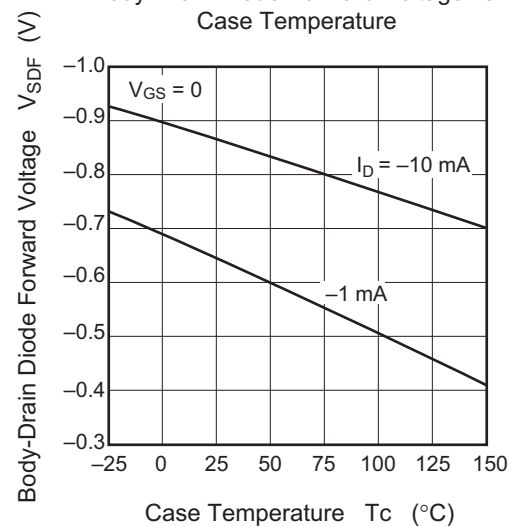
Input Capacitance vs. Gate to Source Voltage



Reverse Drain Current vs. Source to Drain Voltage

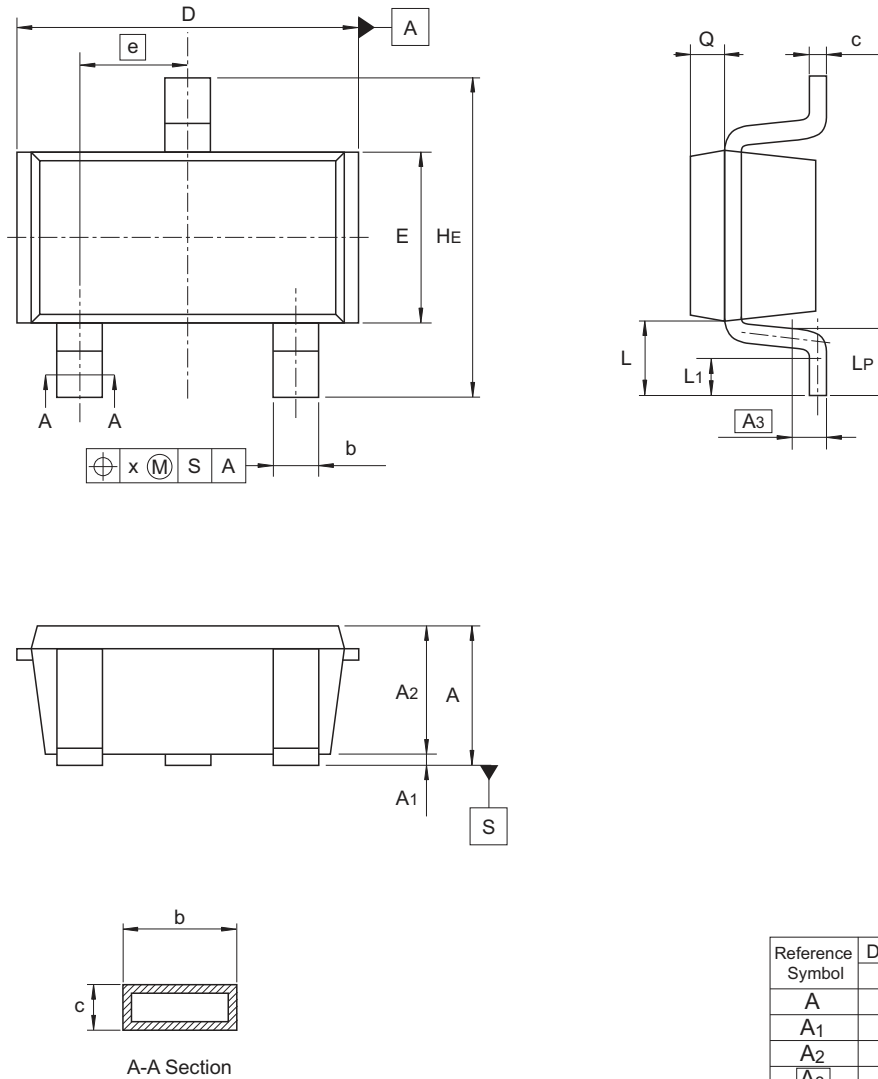


Body-Drain Diode Forward Voltage vs. Case Temperature



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A ₁	0	—	0.1
A ₂	1.0	1.1	1.2
A ₃	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
e	—	0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L ₁	0.15	—	0.55
LP	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

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Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQJ0602EGDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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