RQK0203SGDQA

Silicon N Channel MOS FET
Power Switching

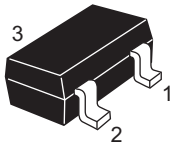
R07DS0303EJ0500
Rev.5.00
Jan 10, 2014

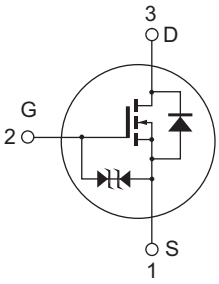
Features

- Low on-resistance
  $R_{DS(on)}$ = 68 mΩ typ (V_{GS} = 4.5 V, I_D = 1.5 A)
- Low drive current
- High speed switching
- 2.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)





1. Source
2. Gate
3. Drain

Note: Marking is “SG”.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±12	V
Drain current	I_D	2.9	A
Drain peak current	$I_{D(pulse)}$ Note1	10	A
Body - drain diode reverse drain current	I_{DR}	2.9	A
Channel dissipation	Pch Note2	0.8	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)

Electrical Characteristics

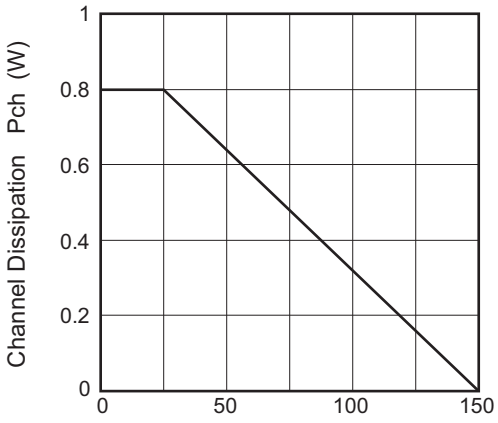
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±12	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±10 V, V_{DS} = 0
Drain to source leak current	I_{DSS}	—	—	1	µA	V_{DS} = 20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	V_{DS} = 10 V, I_D = 1 mA
Drain to source on state resistance	$R_{DS(on)}$	—	68	90	mΩ	I_D = 1.5 A, V_{GS} = 4.5 V[Note3]
	$R_{DS(on)}$	—	105	150	mΩ	I_D = 1.5 A, V_{GS} = 2.5 V[Note3]
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 1.5 A, V_{DS} = 10 V[Note3]
Input capacitance	Ciss	—	159	—	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	48	—	pF	
Reverse transfer capacitance	Crss	—	20	—	pF	
Turn - on delay time	$t_{d(on)}$	—	11	—	ns	I_D = 1.5 A V_{GS} = 4.5 V R_L = 6.6 Ω Rg = 4.7 Ω
Rise time	t_r	—	81	—	ns	
Turn - off delay time	$t_{d(off)}$	—	27	—	ns	
Fall time	t_f	—	8	—	ns	
Total gate charge	Qg	—	1.9	—	nC	V_{DD} = 10 V V_{GS} = 4.5 V I_D = 2.9A
Gate to source charge	Qgs	—	0.4	—	nC	
Gate to drain charge	Qgd	—	0.5	—	nC	
Body - drain diode forward voltage	V_{DF}	—	0.85	1.1	V	I_F = 2.9 A, V_{GS} = 0 [Note3]

Notes: 3. Pulse test

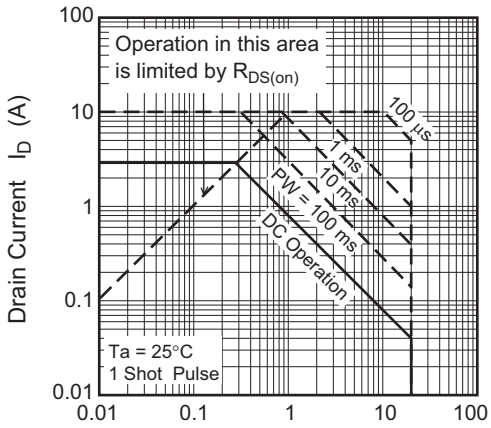
Main Characteristics

Maximum Channel Power Dissipation Curve

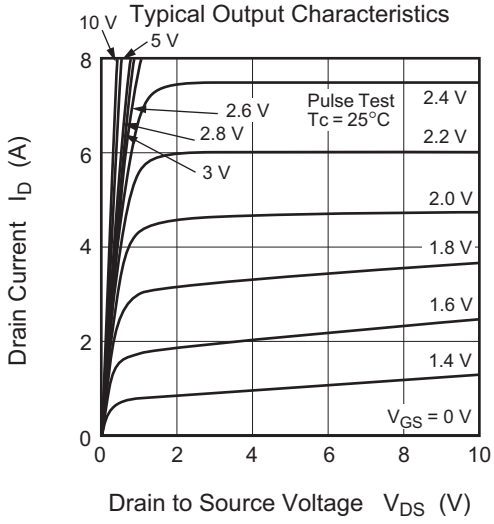


*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

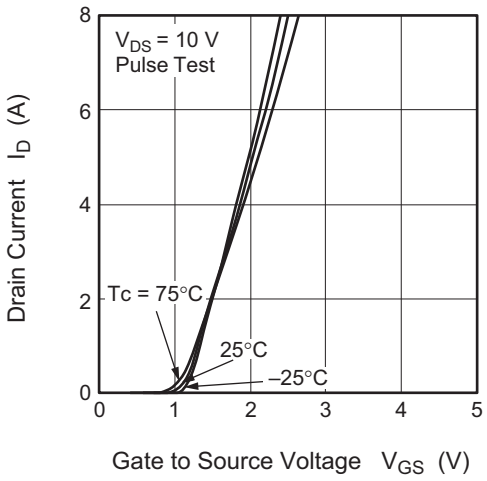
Maximum Safe Operation Area



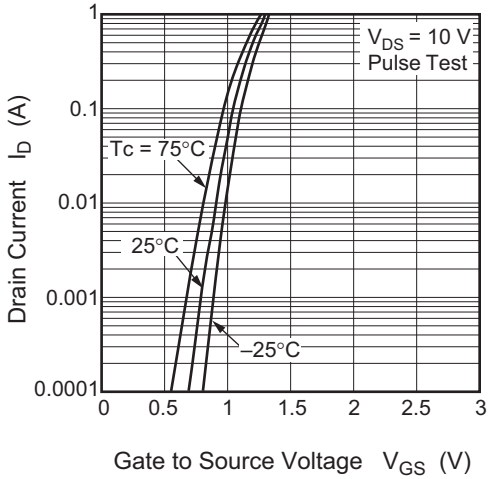
Typical Output Characteristics



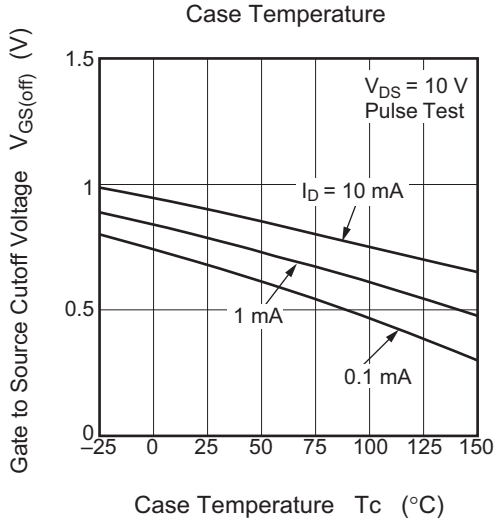
Typical Transfer Characteristics (1)



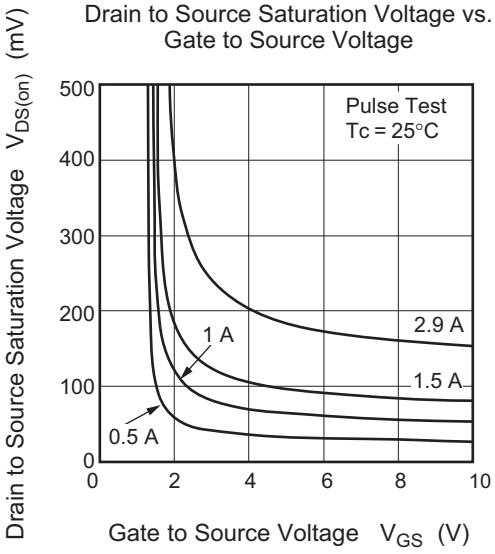
Typical Transfer Characteristics (2)



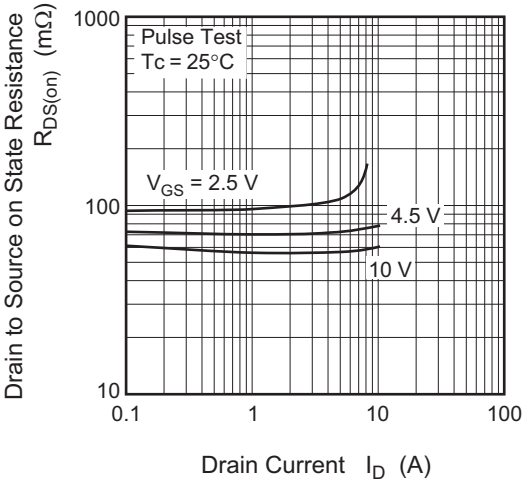
Gate to Source Cutoff Voltage vs. Case Temperature



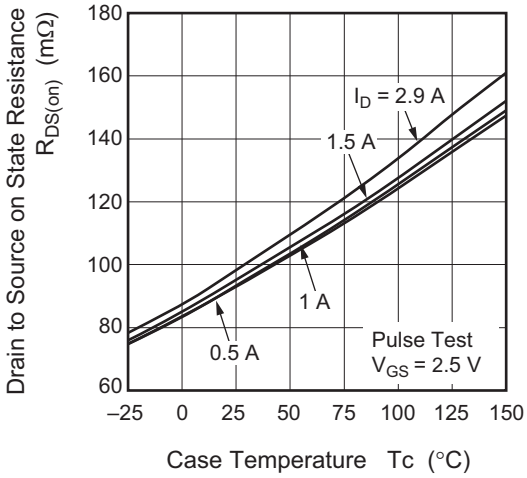
Drain to Source Saturation Voltage vs. Gate to Source Voltage



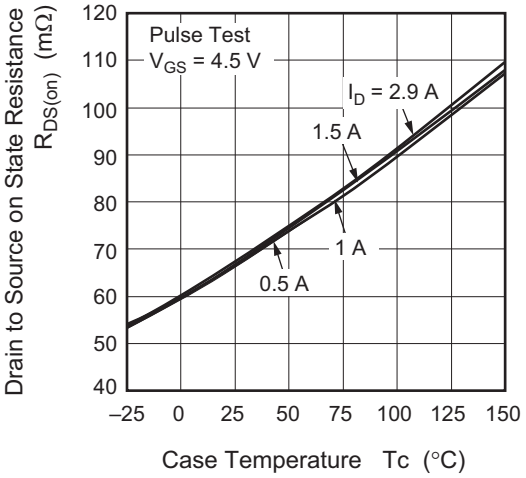
Static Drain to Source on State Resistance vs. Drain Current



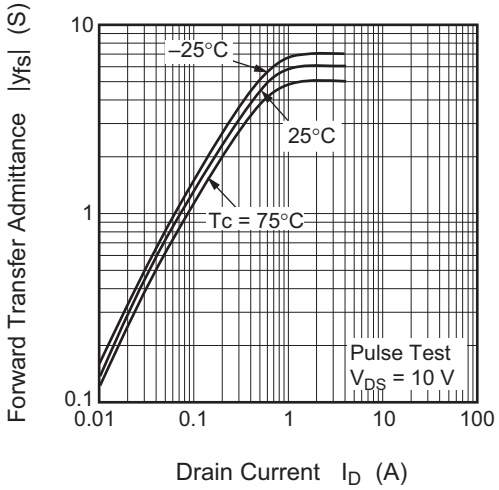
Static Drain to Source on State Resistance vs. Case Temperature



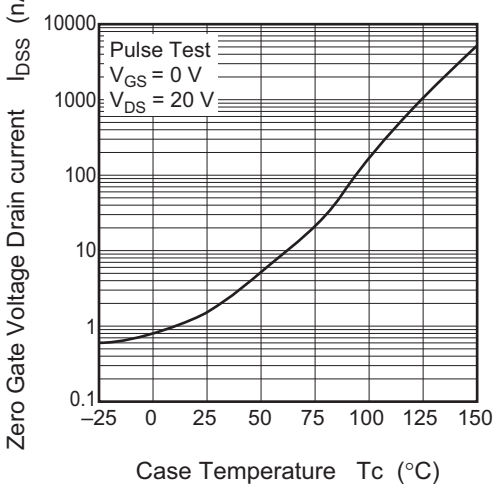
Static Drain to Source on State Resistance vs. Case Temperature



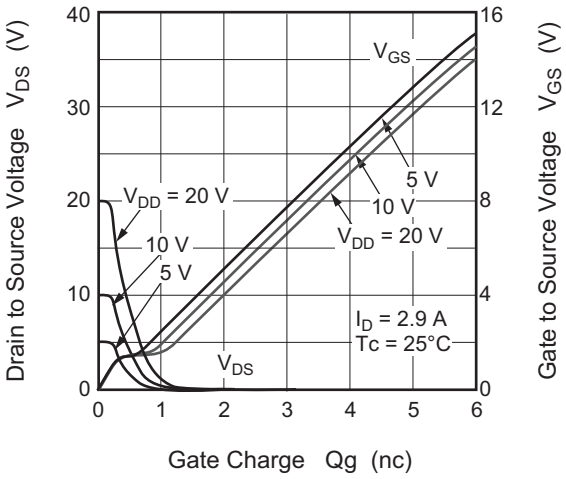
Forward Transfer Admittance vs. Drain Current



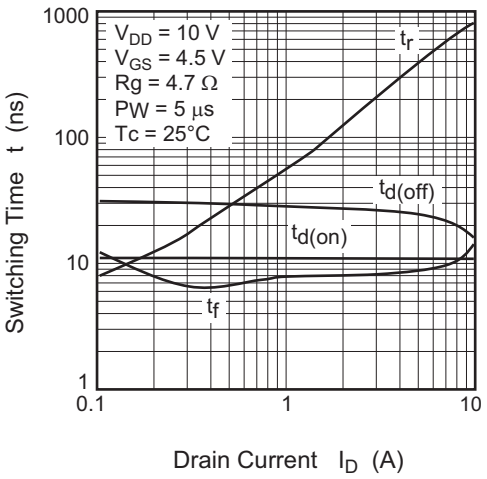
Zero Gate Voltage Drain current vs. Case Temperature



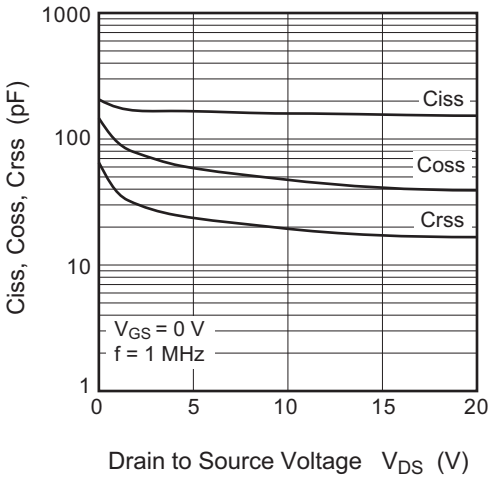
Dynamic Input Characteristics



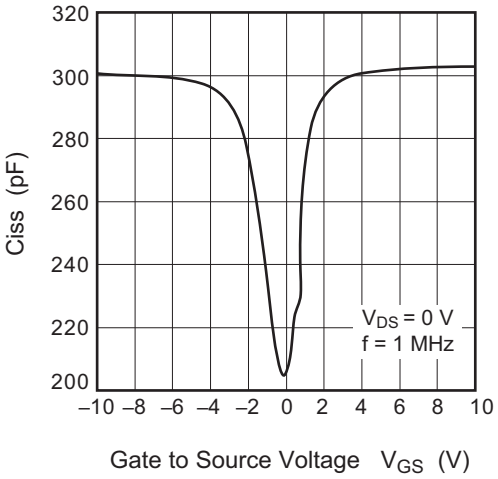
Switching Characteristics



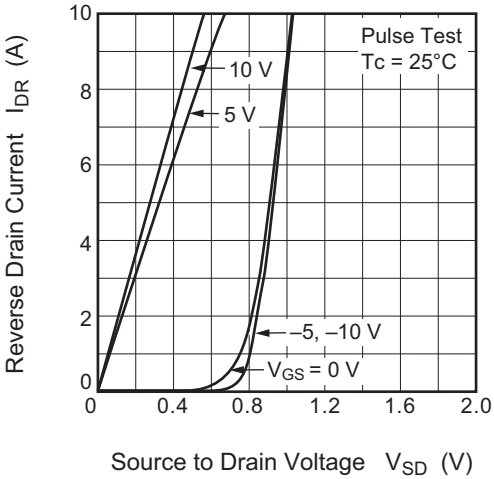
Typical Capacitance vs.
Drain to Source Voltage



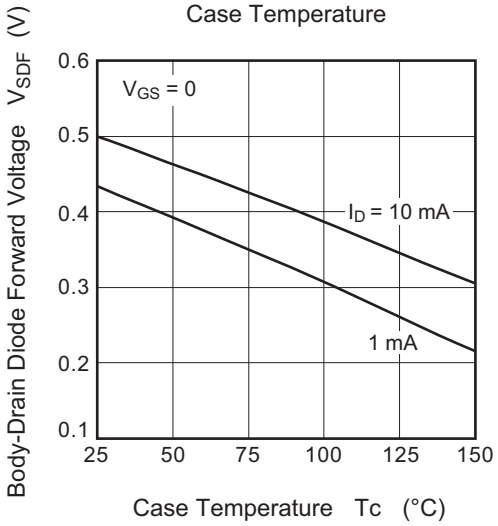
Input Capacitance vs.
Gate to Source Voltage



Reverse Drain Current vs.
Source to Drain Voltage

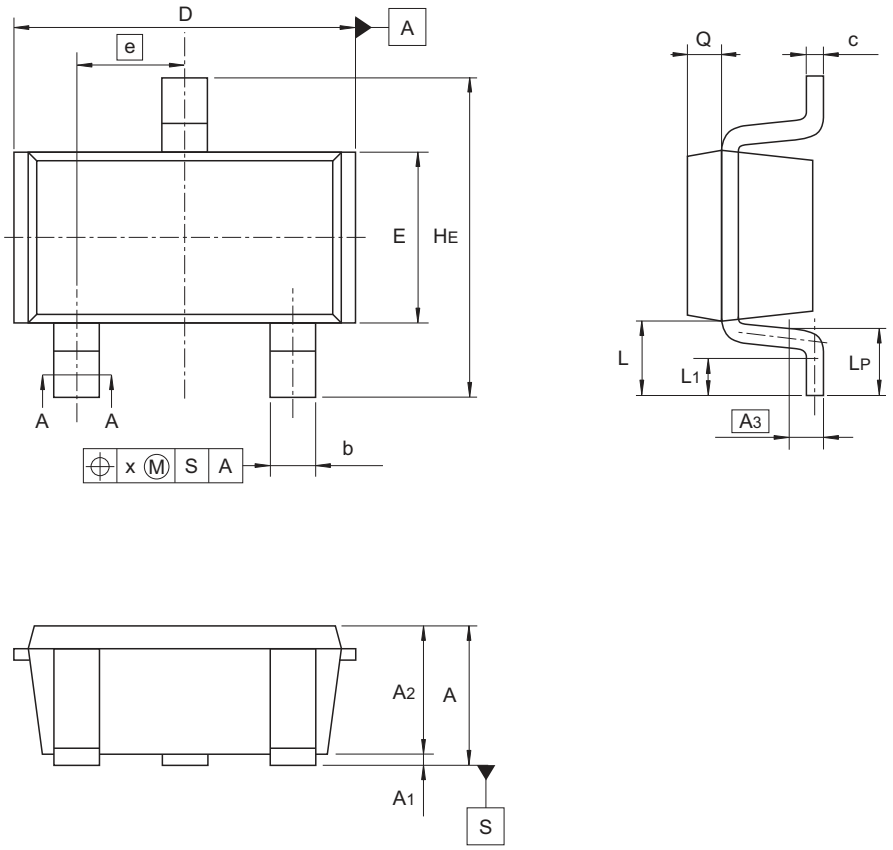


Body-Drain Diode Forward Voltage vs.
Case Temperature



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A_1	0	—	0.1
A_2	1.0	1.1	1.2
$\boxed{A_3}$	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
$\boxed{e}$	—	0.95	—
H_E	2.2	2.8	3.0
L	0.35	—	0.75
L_1	0.15	—	0.55
L_P	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQK0203SGDQATL-H	3000 pcs.	ϕ178 mm reel, 8 mm Emboss taping

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