REAL-TIME CLOCK

RP/RF/RS5C62

APPLICATION MANUAL

RICOH

ELECTRONIC DEVICES DIVISION

NO.EA-012-9803

NOTICE

1. The products and the product specifications described in this application manual are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to Ricoh sales representatives for the latest information thereon.

2. This application manual may not be copied or otherwise reproduced in whole or in part without prior written consent of Ricoh.

3. Please be sure to take any necessary formalities under relevant laws or regulations before exporting or otherwise taking out of your country the products or the technical information described herein.

4. The technical information described in this application manual shows typical characteristics of and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under Ricoh's or any third party's intellectual property rights or any other rights.

5. The products listed in this document are intended and designed for use as general electronic components in standard applications (office equipment, computer equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or misoperation of the product could result in human injury or death (aircraft, spacevehicle, nuclear reactor control system, traffic control system, automotive and transportation equipment, combustion equipment, safety devices, life support system etc.) should first contact us.

6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire-containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.

7. Anti-radiation design is not implemented in the products described in this application manual.

8. Please contact Ricoh sales representatives should you have any questions or comments concerning the products or the technical information.

June 1995

RP/RF/RS5C62

APPLICATION MANUAL

CONTENTS

RP/RF/RS5C62

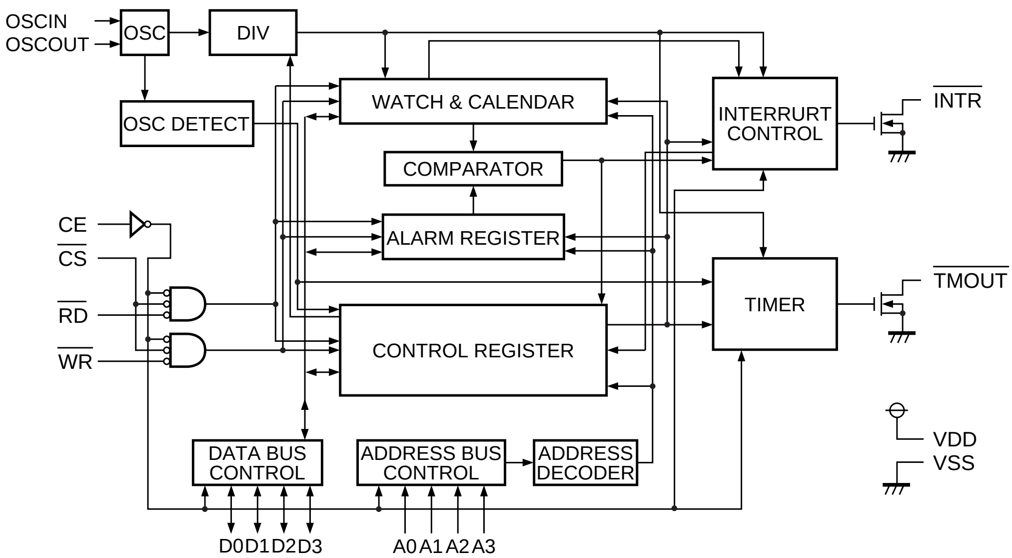
OUTLINE

The RP/RF/RS5C62 are CMOS LSIs which serve microcomputers as real-time clocks providing time, calendar, and alarm functions in direct coupling with the data buses of CPUs such as 8086 and 68000. A built-in timer counter acts as a watchdog timer or interrupt timer. They are available in three different types of packages: the DIP type, the SOP type, and the SSOP type.

FEATURES

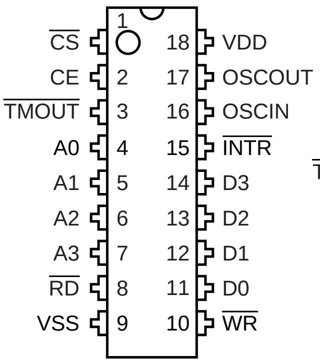
- Directly connected to CPU, enabling fast access.
- 4bit bidirectional data bus, and 4bit address bus.
- The oscillator is driven by a constant voltage, so the oscillation frequency is stable even when the power supply voltage fluctuates.
- Built-in timer counter using internal clock.
- Generates cyclic CPU interrupts, and generates alarm-match interrupts.
- Interrupt flag and interrupt inhibit.
- Clock (hour, minute, second), calendar (leap year, year, month, day, day-of-the-week), alarm (hour, minute).
- 12-or 24-hour mode is selectable.
- Recognizes leap years automatically.
- All clock and alarm data expressed in BCD codes.
- ±30 seconds adjustment function.
- Determines whether clock data is valid or invalid.
- Consumes very low power due to CMOS technology, so it can be backed up by batteries.
- Power supply voltage between 3.0 to 5.0V.
- Time keeping supply voltage between 2.0 to 6.0V.
- Package : 18pin DIP for RP5C62, 18pin SOP for RF5C62, 20pin SSOP for RS5C62.

BLOCK DIAGRAM

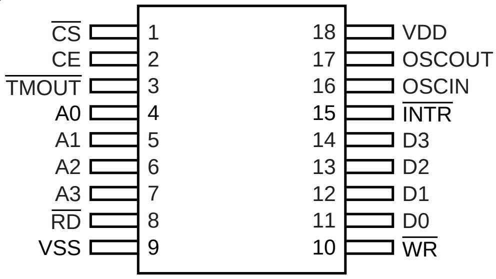


PIN CONFIGURATION

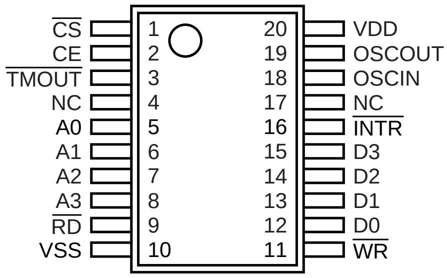
• **RP5C62 (18pin DIP)**



• **RF5C62 (18pin SOP)**



• **RS5C62 (20pin SSOP)**



PIN DESCRIPTION

Pin No.	Symbol	Name	Function
1 2	$\overline{CS}$ CE	Chip select input Chip enable input	$\overline{CS}$ and CE are used when interfacing external devices. They may be accessed when $\overline{CS}$ is low and CE is high. CE is connected to an output of power down detector on the system power supply side, and $\overline{CS}$ is connected to the microcomputer address bus.
3	$\overline{TMOUT}$	Timer output	Timer output may be used as an interrupt free-run timer or watchdog timer. When CE is low (running on battery backup), operation stops (there is no output). It is N-ch open drain output.
4–7	A0–A3	Address input	Address input is connected to the CPU address bus. It is gated internally with CE.
8	$\overline{RD}$	Read control input	When $\overline{RD}$ falls from high to low, the contents of the counters or registers specified by A0 to A3 are output to D0 to D3. It is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
10	$\overline{WR}$	Write control input	When $\overline{WR}$ falls from high to low or rises from low to high, the contents of D0 to D3 are written to registers or counters specified by A0 to A3. $\overline{WR}$ is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
11–14	D0–D3	Bi-directional data bus	D0 to D3 are connected to the CPU data bus. The input section is gated internally with CE. It is CMOS input/output.
15	$\overline{INTR}$	Interrupt output	$\overline{INTR}$ outputs cyclic interrupts or alarm interrupts to CPU. It also operates when CE is low (at battery backup). It is N-ch open drain output.
16 17	OSCIN OSCOUT	Oscillator circuit input/output	Crystal oscillator of 32.768kHz must be connected between OSCIN and OSCOUT. Capacitance is connected externally between VDD and OSCIN and VDD and OSCOUT, forming the oscillator circuit.
18 9	VDD VSS	Power supply	VDD connects to +5V or +3V and VSS to ground.

*) The pin numbers marked in the above table indicate the pins on the 18pin packages.

ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Symbol	Item	Conditions	Ratings	Unit
V_{DD}	Supply Voltage		–0.3 to +7.0	V
V_I	Input Voltage		–0.3 to +V_{DD}+0.3	V
V_O	Output Voltage 1	$\overline{INTR}$, $\overline{TMOUT}$	–0.3 to +12.0	V
	Output Voltage 2	Except $\overline{INTR}$, $\overline{TMOUT}$	–0.3 to +V_{DD}+0.3	V
P_D	Maximum Power Dissipation	TA=25˚C	300	mW
Topt	Operating Temperature		–20 to +70	˚C
Tstg	Storage Temperature		–40 to +125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITION

V_{SS}=0V, Topt=–20 to +70˚C

Symbol	Item	Conditions	Limits			Unit
			MIN.	TYP.	MAX.	
V_{DD}	Supply Voltage		2.7	5.0	6.0	V
V_{CLK}	Time Keeping Supply voltage		2.0		6.0	V
f_{XT}	Crystal Oscillation Frequency			32.768		kHz
V_{PUP}	Pull-up Voltage for $\overline{INTR}$, $\overline{TMOUT}$ pin	$\overline{INTR}$, $\overline{TMOUT}$			10	V

DC ELECTRICAL CHARACTERISTICS

Unless Noted, V_{SS}=0V, V_{DD}=5V±10%, Topt=–20 to +70°C, X'tal=32.768kHz, (R_1≤35kΩ), C_G=10pF, C_D=10pF

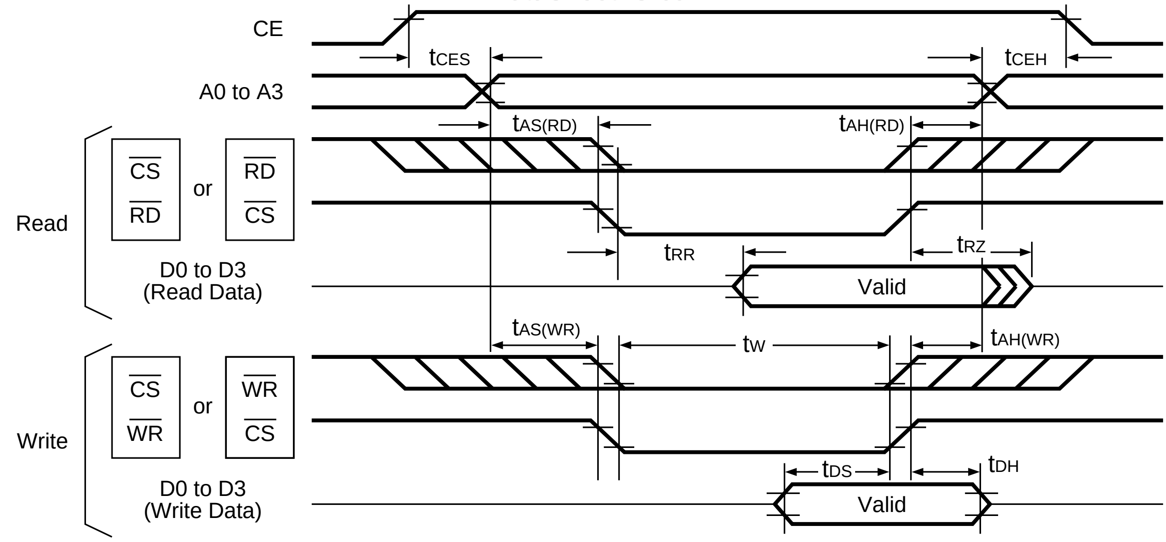
Symbol	Item	Pin Name	Conditions	Limits			Unit
				MIN.	TYP.	MAX.	
V_{IH1}	"H" input voltage	A0 to A3, D0 to D3 $\overline{CS}$, $\overline{RD}$, $\overline{WR}$		2.2		V_{DD}+0.3	V
V_{IL1}	"L" input voltage			–0.3		0.8	V
V_{IH2}	"H" input voltage	CE		0.8×V_{DD}		V_{DD}+0.3	V
V_{IL2}	"L" input voltage			–0.3		0.2×V_{DD}	V
V_{OH1}	"H" output voltage	D0 to D3	I_{OH1}=–400μA	2.4			V
V_{OL1}	"L" output voltage		I_{OL1}=2mA			0.4	V
V_{OL2}	"L" output voltage	$\overline{INTR}$, $\overline{TMOUT}$	I_{OL2}=2mA			0.4	V
I_{ILK}	Input leak current	A0 to A3, CE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$	V_{ILK}=V_{DD} or V_{SS}	–1		1	μA
I_{OZ1}	Output off leak current	D0 to D3	V_{OZ1}=V_{DD} or V_{SS}	–5		5	μA
I_{OZ2}		$\overline{INTR}$, $\overline{TMOUT}$	V_{OZ2}=V_{DD}	–2		2	μA
I_{OZ3}		$\overline{INTR}$, $\overline{TMOUT}$	V_{OZ3}=10V	–5		5	μA
I_{DD1}	Consumption current for back-up	V_{DD}	V_{DD}=2.5V, CE=L Others : OPEN			3	μA
I_{DD2}	Consumption current for stand-by	V_{DD}	V_{DD}=5.5V, CE=H, $\overline{CS}$=H, Output : OPEN Input : V_{DD} or V_{SS}			8	μA
∂f	Oscillation frequency drift for voltage drift	OSCIN OSCOUT	V_{DD}=2.5 to 5.5V Topt=25°C	–1		1	ppm

AC ELECTRICAL CHARACTERISTICS

V_{SS}=0V, Topt=–20 to +70°C

Symbol	Item	V_{DD}=5V±10%		V_{DD}=3V±10%		V_{DD}=5V±20%		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{CES}	CE Setup Time	500		1,000		500		ns
t_{CEH}	CE Hold Time	500		1,000		500		ns
t_{AS} (RD)	Address Setup Time (For Read)	20		20		20		ns
t_{AS} (WR)	Address Setup Time (For Write)	20		20		20		ns
t_{AH} (RD)	Address Hold Time (For Read)	10		10		10		ns
t_{AH} (WR)	Address Hold Time (For Write)	10		10		10		ns
t_{RR}	Output Data Delay Time (C_L=100pF)		120		295		150	ns
t_{RZ}	Output Data Floating Time		70		95		75	ns
t_W	Write Pulse Width	120		195		150		ns
t_{DS}	Input Data Setup Time	60		95		75		ns
t_{DH}	Input Data Hold Time	10		10		10		ns

TIMING CHART



*) The diagonally shaded sections marked in the above timing chart indicate the allowable high or low levels of the $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ pin inputs.

Input/Output Conditions

(V_{DD}= 5V±10%)	(V_{DD}= 3V±10%)	(V_{DD}= 5V±20%)
V_{IH} = 2.2V	V_{IH} = 0.8 × V_{DD}	V_{IH} = 2.4V
V_{IL} = 0.8V	V_{IL} = 0.2 × V_{DD}	V_{IL} = 0.4V
V_{OH}= 2.2V	V_{OH}= 0.8 × V_{DD}	V_{OH}= 2.4V
V_{OL} = 0.8V	V_{OL} = 0.2 × V_{DD}	V_{OL} = 0.4V

FUNCTIONAL DESCRIPTION

1. Addressing

	Address Bus				BANK 0 (BANK=0)						BANK 1 (BANK=1)					
	A3	A2	A1	A0	Description		D3	D2	D1	D0	Description		D3	D2	D1	D0
0	0	0	0	0	1 sec. Counter	R/W	S_8	S_4	S_2	S_1	Cyclic interrupt select Reg.	W/O	CT_3	CT_2	CT_1	CT_0
1	0	0	0	1	10 sec. Counter	R/W		S_{40}	S_{20}	S_{10}	Adust Reg.	W/O				ADJ
2	0	0	1	0	1 min. Counter	R/W	M_8	M_4	M_2	M_1	1 min. alarm Reg.	R/W	AM_8	AM_4	AM_2	AM_1
3	0	0	1	1	10 min. Counter	R/W		M_{40}	M_{20}	M_{10}	10 min. alarm Reg.	R/W		AM_{40}	AM_{20}	AM_{10}
4	0	1	0	0	1 hour Counter	R/W	H_8	H_4	H_2	H_1	1 hour alarm Reg.	R/W	AH_8	AH_4	AH_2	AH_1
5	0	1	0	1	10 hour Counter	R/W			P/$\overline{A}$ or H_{20}	H_{10}	10 hour alarm Reg.	R/W			AP/$\overline{A}$ or AH_{20}	AH_{10}
6	0	1	1	0	day-of-the-week Counter	R/W		W_4	W_2	W_1						
7	0	1	1	1	1 day Counter	R/W	D_8	D_4	D_2	D_1						
8	1	0	0	0	10 day Counter	R/W			D_{20}	D_{10}						
9	1	0	0	1	1 month Counter	R/W	MO_8	MO_4	MO_2	MO_1						
A	1	0	1	0	10 month Counter	R/W				MO_{10}	$\overline{12}$/24 select Reg.	W/O				$\overline{12}$/24
B	1	0	1	1	1 year Counter	R/W	Y_8	Y_4	Y_2	Y_1	Leap Year Reg.	R/O R/W		$\overline{LYE}$	LY_1	LY_0
C	1	1	0	0	10 year Counter	R/W	Y_{80}	Y_{40}	Y_{20}	Y_{10}	Timer Clock Select Reg.	W/O R/W R/O	TM_3	TM_2	TM_1	TM_0 TMFG
D	1	1	0	1	Control Reg. 1	W/O	WTEN	ALEN	TMR	BANK	Control Reg. 1	W/O	WTEN	ALEN	TMR	BANK
E	1	1	1	0	Control Reg. 2	R/O R/W	BSY	CTFG	ALFG	XSTP	Control Reg. 2	R/O R/W	BSY	CTFG	ALFG	XSTP
F	1	1	1	1	Control Reg. 3	W/O	$\overline{TSTA}$	$\overline{TSTB}$	WTRST		Control Reg. 3	W/O	$\overline{TSTA}$	$\overline{TSTB}$	WTRST	

*1) R/W bits can be read and written. R/O bits can only be read. W/O bits can only be written.
*2) It is no problem to attempt writing to R/O bits and blank bits, but the attempt will fail.
*3) If W/O bits and blank bits are read, the returned value is 0.
*4) The control registers 1, 2, and 3 have the same address assignment for BANK0 and BANK1.

2. Functions of Registers

2.1 Control Register 1 (Bank0/1 at “Dh”)

D3	D2	D1	D0	
WTEN	ALEN	TMR	BANK	(For write operation)
0	0	0	0	(For read operation) *1

Bank switching bit

BANK	Function
0	Specifies selection of BANK0 in the address table.
1	Specifies selection of BANK1 in the address table.

Timer resetting bit *2

TMR	Function
0	Specifies no change.
1	Specifies resetting of the timer conditional on restart.

Alarm operation setting bit *3

ALEN	Function
0	Disables an alarm interrupt.
1	Enables an alarm interrupt.

Time count operation setting bit *4

WTEN	Function
0	Disables a carry to the 1-second time digit.
1	Enables a carry to the 1-second time digit.

*1) The BANK bit is intended for only write operation and always read as “0”.

*2) The timer frequency can be set by the timer clock selection register.

*3) Setting the ALEN bit to “0” during output of an alarm interrupt from the $\overline{\text{INTR}}$ pin (while it is held low) turns off the $\overline{\text{INTR}}$ pin.
Setting the ALEN bit to “1” in matching between clock time and alarm time drives the $\overline{\text{INTR}}$ pin low within a maximum of 61.1µs.

*4) A 1-second carry with the WTEN bit set to “0” increments the second digit by 1 upon setting of the WTEN bit to “1”. This bit will automatically be set to “1” upon driving low the CE pin.

2.2 Control Register 2 (BANK0/1 at "Eh")

D3	D2	D1	D0	
*[*1]	CTFG	ALFG	XSTP	(For write operation)
BSY	CTFG	ALFG	XSTP	(For read operation)

Oscillation stop detection bit [*2]

XSTP	Function
0	Indicates the progress of oscillation. Intended for setting to "0".
1	Indicates the stop of oscillation. Not intended for setting to "1".

Alarm time match indication bit [*3]

ALFG	Function
0	Indicates an alarm interrupt is disabled or indicates mismatching between clock time and alarm time (upon turning off the $\overline{\text{INTR}}$ pin). Intended for setting to "0".
1	Indicates matching between clock time and alarm time (upon driving low the $\overline{\text{INTR}}$ pin). Not intended for setting to "0".

Cyclic interrupt indication bit [*4]

CTFG	Function
0	Indicates that the $\overline{\text{INTR}}$ pin is turned off. Intended for setting to "0" in the level mode.
1	Indicates that the $\overline{\text{INTR}}$ pin is driven low. Not intended for setting to "0".

Time/calendar counter state indication bit [*5]

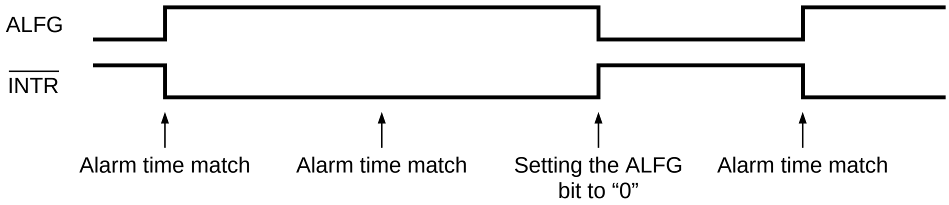
BSY	Function
0	Indicates the normal state of the time and calendar counters (no carry or no reset pulse).
1	Indicates the busy state of the time and calendar counters (a carry or a reset pulse generated).

*1) The BSY bit is intended for only read operation and is not intended for write operation.

*2) The XSTP bit is used to detect the stop of the crystal oscillator. The XSTP bit is set to "1" upon the stop of oscillation and held at "1" after the restart of oscillation. Upon detection of the stop of oscillation, the built-in timer counter is reset (because the TM_3 bit in the timer clock selection register is reset).

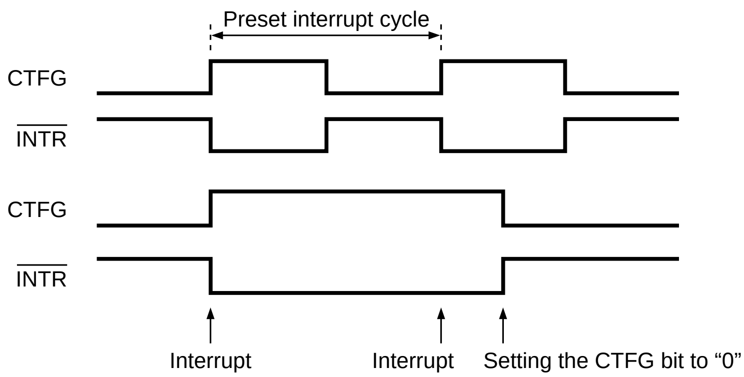
*3) When the ALEN bit is set to "1", the ALFG bit is also set to "1" upon output of an alarm interrupt from the $\overline{\text{INTR}}$ pin (while it is held low).

RICOH



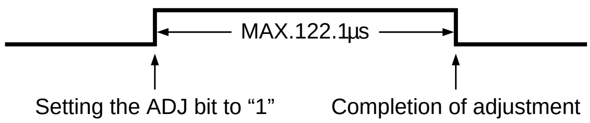
*4) The CTFG bit is set to "1" upon output of a cyclic interrupt from the $\overline{\text{INTR}}$ pin (while it is held low). (A cyclic interrupt may occur in the pulse mode and the level mode.)

- Pulse mode
  (The CT3 bit is set to "0".)
  (The CTFG bit is not intended for write operation.)
- Level mode
  (The CT3 bit is set to "1".)
  (The CTFG bit is intended for setting to "0" only.)

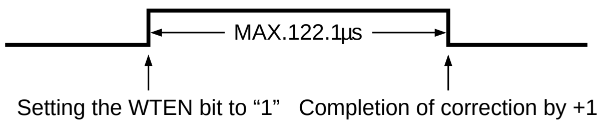


*5) When the BSY bit is set to "1", write operation must not be performed upon the time and calendar counters which are being updated. Normally, read operation must be performed from the counters upon setting the BSY bit to "0". Reading from them without checking the BSY bit requires separate software for preventing reading errors. The BSY bit is set to "1" in the four cases below:

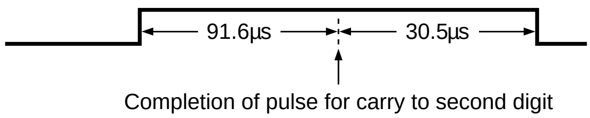
(I) Adjustment by ±30 seconds



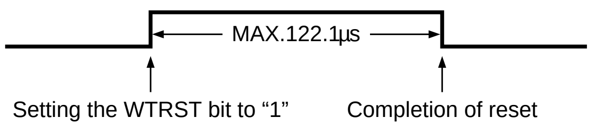
(II) Correction by +1
(when there is a 1-second carry in transition of the WTEN bit from "0" to "1")



(III) Normal 1-second carry



(IV) Counter resetting (setting of WTRST bit)
(Resetting the 1 to 8Hz dividers)



2.3 Control Register 3 (BANK0/1 at “Fh”)

D3	D2	D1	D0	
$\overline{\text{TSTA}}$	$\overline{\text{TSTB}}$	WTRST	∗*1	(For write operation)
0	0	0	0	(For read operation) *2

Bit for resetting lower-order counter than the second counter. *3

WTRST	Function
0	Specifies normal operation.
1	Specifies resetting of 1- to 8-Hz dividers conditional on restart.

Test mode setting bits *4

$\overline{\text{TSTA}}$,$\overline{\text{TSTB}}$	Function
0	Specifies setting of the test mode.
1	Specifies setting of normal operation.

∗1) The bit marked with “∗” is not intended for write operation.

∗2) This bit is intended for only write operation and always read as “0”.

∗3) When set to “1”, the WTRST bit specifies resetting of the lower-order counter than the 1 second counter ranging from 8Hz and 4Hz to 2Hz and 1Hz conditional on restart. The WTRST bit is used to adjust the lower-order counter than the 1 second counter. After the WTRST bit is set to “1”, the BSY bit is set to “1” for a maximum of 122.1µs.

∗4) Both the $\overline{\text{TSTA}}$ and $\overline{\text{TSTB}}$ bits must be set to “1” to specify normal operation and will automatically be set to “1” upon driving low the CE pin.

2.4 Adjustment Register (BANK1 at “1h”)

D3	D2	D1	D0	
∗*1	∗	∗	ADJ	(For write operation)
0	0	0	0	(For read operation) *2

Second digit adjustment bit *3

ADJ	Function
0	Specifies normal operation.
1	Specifies adjustment of second digit.

∗1) The bits marked with “∗” are not intended for write operation.

∗2) This bit is intended for only write operation and always read as “0”.

∗3) The ADJ bit is used to correct the second digit. When set to “1”, the ADJ bit functions as follows:

1) For digits ranging from 00 seconds to 29 seconds → Resets the lower-order counter than the 1 second counter (in the same manner as the WTRST bit) and sets the second digit to “00”.

2) For digits ranging from 30 seconds to 59 seconds → Resets the second and lower-order counters (in the same manner as the WTRST bit), sets the second digit to “00” and increments the minute digit by 1. The BSY bit is set to “1” for a maximum of 122.1µs after the ADJ bit is set to “1”.

2.5 Interrupt Cycle Selection Register (BANK1 at "0h")

D3	D2	D1	D0	
CT_3	CT_2	CT_1	CT_0	(For write operation)
0	0	0	0	(For read operation) *1

Interrupt cycle/output mode selection bits *2

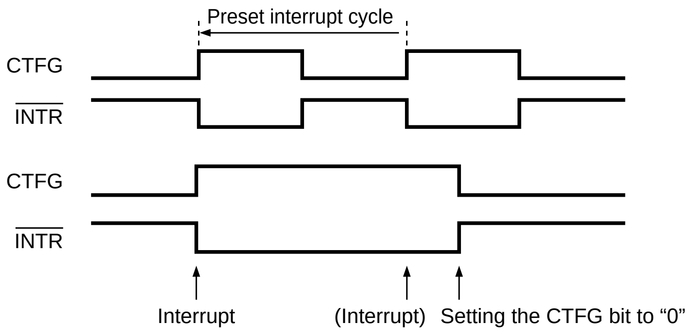
*1) These bits are intended for only write operation and always read as "0".
*2) The CT_3 to CT_0 bits are used to set interrupt cycles and output modes as shown in the table below:

CT3	CT2	CT1	CT0	$\overline{\text{INTR}}$	Remarks
*	0	0	0	"OFF"	Disable a cyclic interrupt.
*	0	0	1	2048Hz	Specify a cycle (T) of 0.488ms (1/2048Hz).
*	0	1	0	1024Hz	Specify a cycle (T) of 0.977ms (1/1024Hz).
*	0	1	1	128Hz	Specify a cycle (T) of 7.813ms (1/128Hz).
*	1	0	0	16Hz	Specify a cycle (T) of 62.5ms (1/16Hz).
*	1	0	1	1Hz	Specify a cycle (T) of 1s (1/1Hz).
*	1	1	0	1/60Hz	Specify a cycle (T) of 60s (1/1/60Hz).
*	1	1	1	"ON"	Specify the fixed low level of the $\overline{\text{INTR}}$ pin output.
0	*	*	*	Pulse mode	Specify a duty cycle of 50%. See below.
1	*	*	*	Level mode	See below.

) The bits marked with "" are set to "0" or "1".

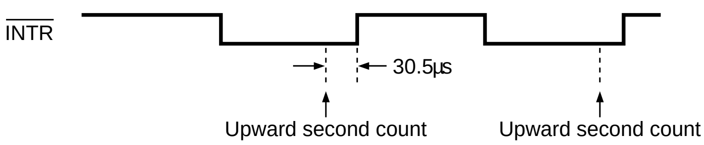
- Pulse mode
  (The CT_3 bit is set to "0".)
  (The CTFG bit is not intended for write operation.)

- Level mode
  (The CT_3 bit is set to "1".)
  (The CTFG bit is intended for setting to "0" only.)

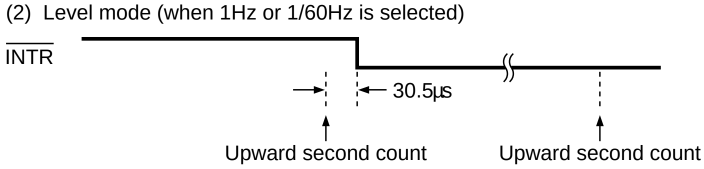


- Relationship between $\overline{\text{INTR}}$ pin output and upward second count

(1) Pulse mode (when 1Hz or 1/60Hz is selected)



(2) Level mode (when 1Hz or 1/60Hz is selected)



2.6 Alarm Register (1-minute, 10-minute, 1-hour, and 10-hour) (BANK1 at “2h to 5h”)

D3	D2	D1	D0	
AM_8	AM_4	AM_2	AM_1	(For read and write operations) 1-minute alarm digit (at“2h”)
*	AM_{40}	AM_{20}	AM_{10}	(For read and write operations) 10-minute alarm digit (at“3h”)
AH_8	AH_4	AH_2	AH_1	(For read and write operations) 1-hour alarm digit (at“4h”)
*	*	$AP/\overline{A}$ or AH_{20}	AH_{10}	(For read and write operations) 10-hour alarm digit (at“5h”)

1) The bits marked with “” are always read as “0” and not intended for write operation.
*2) When enabling an alarm interrupt, non-existent minute and hour alarm digits must not be left (to prevent mismatching between clock time and alarm time).
*3) Alarm minute and hour settings are exemplified in the table below:

Alarm minute and hour setting	12-hour time scale				24-hour time scale			
	10-hour digit	1-hour digit	10-minute digit	1-minute digit	10-hour digit	1-hour digit	10-minute digit	1-minute digit
0 : 00 a.m.	1	2	0	0	0	0	0	0
1 : 30 a.m.	0	1	3	0	0	1	3	0
11 : 59 a.m.	1	1	5	9	1	1	5	9
0 : 00 p.m.	3	2	0	0	1	2	0	0
1 : 30 p.m.	2	1	3	0	1	3	3	0
11 : 59 p.m.	3	1	5	9	2	3	5	9

*4) In the the 12-hour time scale, the hour digits of 12 and 32 indicate 0 o'clock a.m. and 0 o'clock p.m., respectively.

2.7 $\overline{12}$/24-hour Time Scale Selection Register (BANK1 at “Ah”)

D3	D2	D1	D0	
** 1	*	*	$\overline{12}$/24	(For write operation)
0	0	0	0	(For read operation) *2

$\overline{12}$/24-hour time scale selection bit *3,4

$\overline{12}$/24	Function
0	Selects the 12-hour time scale with a.m. and p.m. indications.
1	Selects the 24-hour time scale.

1) The bits marked with “” are not intended for write operation.
*2) These bits are intended for only write operation and always read as “0”.
*3) The time digits are indicated in binary-coded decimal (BCD) notation as shown in the table below:

24-hour time scale	12-hour time scale	12-hour time scale	24-hour time scale
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

*4) The 12-hour or 24-hour time scale must be selected before time of day adjustment or alarm time setting (e.g. at the time of initialization after power-on from 0V)

2.8 Leap Year Indication Register (BANK1 at "Bh")

D3	D2	D1	D0	
*[*1]	$\overline{LYE}$	*	*	(For write operation)
0	$\overline{LYE}$	LY_1	LY_0	(For read operation)

Leap year indication bits (intended for only read operation) *[2]

(LY_1,LY_0)	Function
(0,0)	Specifies leap year indication (including February 29) (when the $\overline{LYE}$ bit is set to "0".
Any other value	Specifies normal year indication (not including February 29).

Leap year indication selection bit *[3,4]

$\overline{LYE}$	Function
0	Enables leap year indication.
1	Disables leap year indication.

1) The bits marked with "" are not intended for write operation.
*2) The LY1 and LY0 bits cycle from "00" via "01" and "10" to "11" with the passage of years.
*3) Upon setting the $\overline{LYE}$ bit to "0", automatic correction is made for leap years in the years 1901 to 2099 (e.g. 1992, 1996, and 2000).
Upon setting the $\overline{LYE}$ bit to "1", leap year indication is disabled (counting up to February 28).
*4) Writing to the 1-year or 10-year counter enables leap year indication (sets the $\overline{LYE}$ bit to "0").

2.9 Timer Clock Selection Register (BANK1 at “Ch”)

D3	D2	D1	D0	
TM_3	TM_2	TM_1	TM_0	(For write operation)
TM_3	0	0	TMFG	(For read operation) *1

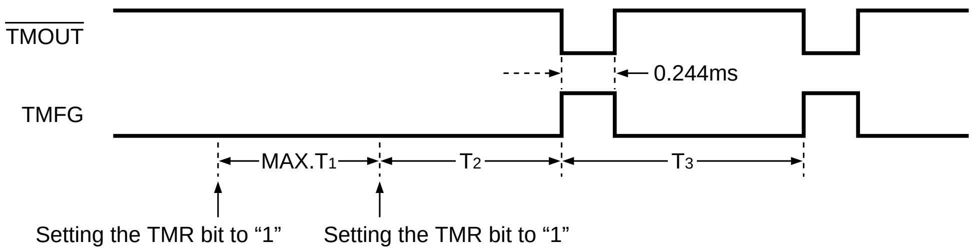
Timer counter cycle setting bit (TM_3 to TM_0) *2
Timer output indication bit (TMFG) *3

*1) Only the TM_3 bit is intended for read operation. The D0 bit is always read as “TMFG”. The D2 and D1 bits are always read as “0”.
*2) The TM_3 to TM_0 bits are used to set cycles for the counters as shown in the table below.

TM_3	TM_2	TM_1	TM_0	T1 (Watchdog timer cycle)	T2 (Output time after timer resetting)	T3 (Free-running timer cycle)
0	*	*	*	Timer output disabled ($\overline{\text{TMOUT}}$ pin output turned off)	Timer output disabled ($\overline{\text{TMOUT}}$ pin output turned off)	Timer output disabled ($\overline{\text{TMOUT}}$ pin output turned off)
1	0	0	0	562ms	562 to 626ms	625ms
1	0	0	1	281ms	281 to 313ms	312.5ms
1	0	1	0	140ms	140 to 157ms	156.3ms
1	0	1	1	70.3ms	70.3 to 78.2ms	78.13ms
1	1	0	0	35.1ms	35.1 to 39.1ms	39.06ms
1	1	0	1	17.5ms	17.5 to 19.6ms	19.53ms
1	1	1	0	8.78ms	8.78 to 9.77ms	9.766ms
1	1	1	1	4.39ms	4.39 to 4.89ms	4.883ms

T1 : Maximum time during which timer output is disabled after timer resetting.
(Timer reset occurs upon setting the TMR bit to “1” in the control register 1.)
(Timer output occurs upon driving low the $\overline{\text{TMOUT}}$ pin output.)
T2 : Time between timer output and cycle setting during timer resetting (upon setting the TM_3 bit to “0”), or timer resetting, or transition of the CE pin input from its low to high levels.
T3 : Timer output cycle without timer reset.

*3) Relationship between TMFG Bit and $\overline{\text{TMOUT}}$ pin output



*4) The timer is stopped (the $\overline{\text{TMOUT}}$ pin output is turned off) upon driving low the CE pin input, but restarted upon driving high the CE pin input.

*5) Timer output is disabled (the $\overline{\text{TMOUT}}$ pin output is turned off) upon resetting the TM_3 bit to "0" when the stop of oscillation is detected (setting the XSTP bit to "1").

*6) Timer output is turned off (the $\overline{\text{TMOUT}}$ pin output is turned off) upon setting the TMR bit to "1" in the control register 1 during timer output (while the $\overline{\text{TMOUT}}$ pin is held low).

3. Functions of Counters

3.1 Time Counter (BANK0 at "0h to 5h")

D3	D2	D1	D0		
S_8	S_4	S_2	S_1	(For read and write operations)	1-second time digit (at "0h")
*	S_{40}	S_{20}	S_{10}	(For read and write operations)	10-second time digit (at "1h")
M_8	M_4	M_2	M_1	(For read and write operations)	1-minute time digit (at "2h")
*	M_{40}	M_{20}	M_{10}	(For read and write operations)	10-minute time digit (at "3h")
H_8	H_4	H_2	H_1	(For read and write operations)	1-hour time digit (at "4h")
*	*	$P/\overline{A}$ or H_{20}	H_{10}	(For read and write operations)	10-hour time digit (at "5h")

1) The bits marked with "" are always read as "0" and not intended for write operation.

*2) Upon setting the WTEN bit to "0" in the control register 1, a carry to the 1-second time digit from the second counter is disabled.

*3) The time digits are indicated in BCD notation as shown below:

Second digit: Ranges from 00 to 59 and carried to the minute digit in transition from 59 to 00.

Minute digit: Ranges from 00 to 59 and carried to the hour digit in transition from 59 to 00.

Hour digit: Ranges as shown in "2. 7 $\overline{12}$/24-hour Time Scale Selection Register" and carried to the day or day-of-the-week digit in transition from 11 p.m. to 12 a.m. or from 23 to 00.

*4) A carry from any non-existent time digit must be avoided because it may cause malfunction in the time counter.

3.2 Day-of-the-week Counter (BANK0 at "6h")

D3	D2	D1	D0	
*	W_4	W_2	W_1	(For read and write operations) Day-of-the-week counter

1) The bits marked with "" are always read as "0" and not intended for write operation.
*2) The day-of-the-week counter is incremented by 1 in a carry to the 1-day calendar digit.
*3) Days of the week written to the W_4, W_2, and W_1 bits are counted up in septimal notation as shown below :
(000)→(001)→ ····· →(110)→(000)
The correspondence between days of the week and readings of the day-of-the-week counter is user-definable (e.g. Sunday=000)
*4) The W_4, W_2, and W_1 bits must not be all set to 1.

3.3 Calendar Counter (BANK0 at "7h" to "Ch")

D3	D2	D1	D0	
D_8	D_4	D_2	D_1	(For read and write operations) 1-day calendar digit (at "7h")
*[*1]	*	D_{20}	D_{10}	(For read and write operations) 10-day calendar digit (at "8h")
MO_8	MO_4	MO_2	MO_1	(For read and write operations) 1-month calendar digit (at "9h")
*	*	*	MO_{10}	(For read and write operations) 10-month calendar digit (at "Ah")
Y_8	Y_4	Y_2	Y_1	(For read and write operations) 1-year calendar digit (at "Bh")
Y_{80}	Y_{40}	Y_{20}	Y_{10}	(For read and write operations) 10-year calendar digit (at "Ch")

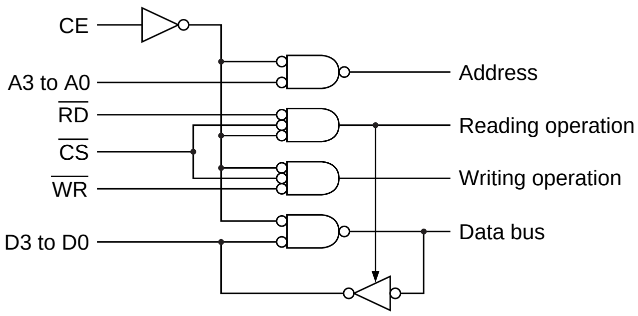
1) The bits marked with "" are always read as "0" and not intended for write operation.
*2) The calendar digits are indicated in BCD notation by the automatic calendar function as shown below:

Day digit : Ranges from 1 to 31 (in January, March, May, July, August, October, and December)
Ranges from 1 to 30 (in April, June, September, and November)
Ranges from 1 to 29 (in February in leap years)
Ranges from 1 to 28 (in February in normal years)
Carried to the month digit in transition back to 1.
Month digit : Ranges from 1 to 12 carried to the year digit in transition back to 1.
Year digit : Ranges from 00 to 99 including leap years of 00, 04, 08, - - - - - -, 92, and 96 (when leap year indication is enabled by setting the $\overline{LYE}$ bit in the leap year indication register to "0").

*3) A carry from any non-existent calendar digit must be avoided because it may cause malfunction in the calendar counter.

USAGE

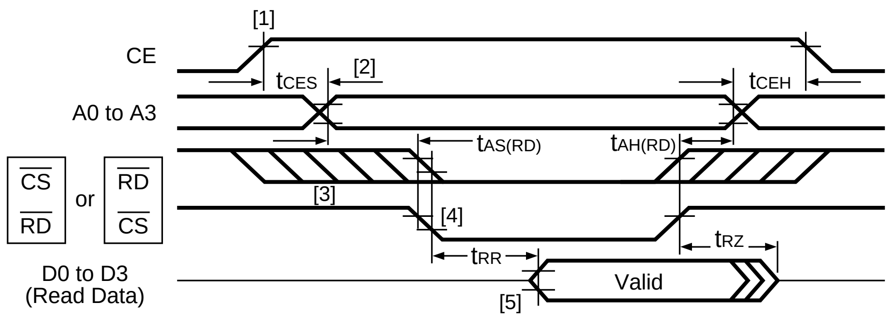
1. Reading and Writing Operations



Upon driving high the CE pin, the interfacing input/output pins are enabled, establishing equivalence in logic between the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pin inputs during read operation and between the $\overline{\text{WR}}$ and $\overline{\text{CS}}$ pin inputs during write operation. Upon driving low the CE pin, the interfacing input/output pins are disabled, preventing occurrence of invalid leak current due to their floating. The CE pin must always be driven either high or low and must never be left floating.

1.1 Reading Operation

The requirements for reading data from the internal registers and counters are: [1] holding the CE pin high, [2] performing the process of addressing through the A3 to A0 pin inputs, then [3] driving low the $\overline{\text{CS}}$ pin, [4] causing the $\overline{\text{RD}}$ pin to transition from its high to low levels, and thereby [5] causing the D3 to D0 pins to output read data. The reading timing is shown in the chart below.



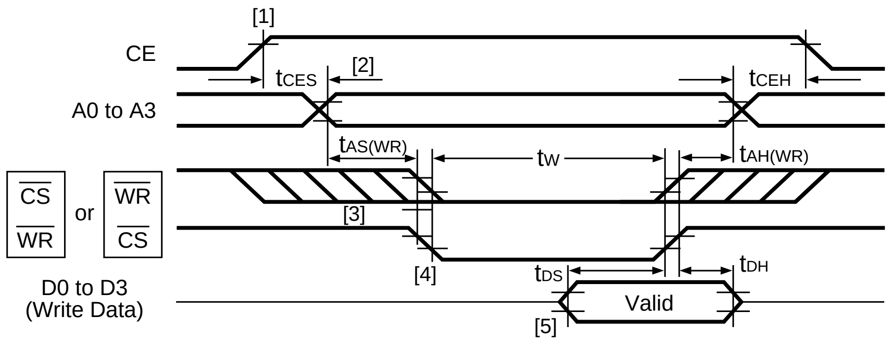
*1) The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pin inputs are interchangeable. The diagonally shaded sections marked in the above timing chart may be set to both high and low levels. (Consequently, the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pin inputs may be caused to transition from their high to low levels before the process of addressing.)

*2) "t_{AS} (RD)" indicates the time required to perform the process of addressing before the start of read operation at which both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pin inputs are driven low.

*3) "t_{AH} (RD)"indicates the time required to maintain the result of addressing after the completion of read operation at which either the $\overline{\text{RD}}$ or $\overline{\text{CS}}$ pin input is driven high.

1.2 Writing Operation

The requirements for writing data to the internal registers and counters are: [1] holding the CE pin high, [2] performing the process of addressing through the A3 to A0 pin inputs, then [3] driving low the $\overline{CS}$ pin, [4] causing the $\overline{WR}$ pin to transition from its high to low to high levels, and thereby [5] causing the D3 to D0 pins to input data to be written. The writing timing is shown in the chart below.



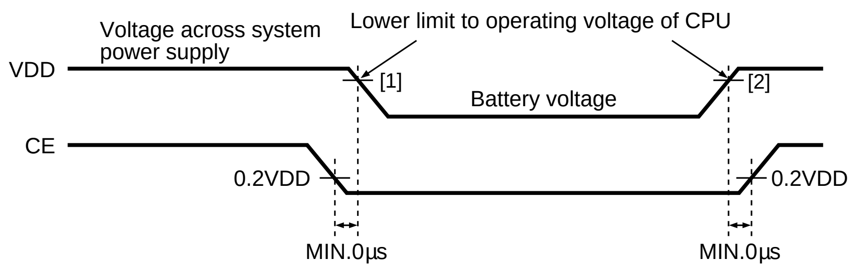
*1) The $\overline{CS}$ and $\overline{WR}$ pin inputs are interchangeable. The diagonally shaded sections marked in the above timing chart may be set to both high and low levels. (Consequently, the $\overline{CS}$ and $\overline{WR}$ pin inputs may be caused to transition from their high to low levels before the process of addressing.)

*2) "t_{AS} (WR)" indicates the time required to perform the process of addressing before the start of write operation at which both the $\overline{WR}$ and $\overline{CS}$ pin inputs are driven low.

*3) "t_{AH} (WR)" indicates the time required to maintain the result of addressing after the completion of write operation at which either the $\overline{WR}$ or $\overline{CS}$ pin input is driven high.

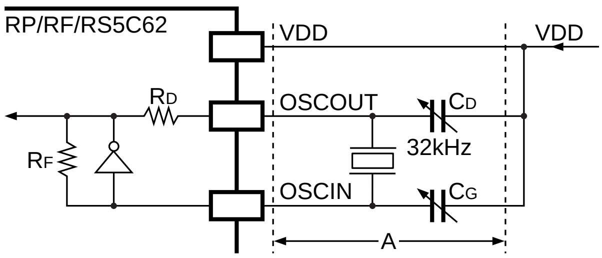
2. Handling of CE Pin

Normally, the CE pin is connected to the supply voltage detection circuit of the system power supply. In switching the system power supply (see the typical power supply circuit), the CE pin must be driven low before the voltage across the system power supply drops below the lower limit to the operating voltage of the CPU (at the point ([1]) in the timing chart below) and then driven high after the supply voltage rises above the lower limit to the operating voltage of the CPU (at the point ([2]) in the timing chart below).



*) The CE pin must be driven as low as the V_{SS} pin whenever possible in order to minimize battery consumption in battery backup (while the CE pin is held low).

3. Configuration of Oscillatory Circuit



Typical external components:

X'tal : 32.768 kHz

$R_1 \leq 35k\Omega$

C_G=5pF to 35pF

C_D=5pF to 35pF

Standard values of internal elements:

R_F=12MΩ

R_D=60kΩ

In the oscillatory circuit, which is driven by a constant voltage of about 2V relative to the VDD pin, either one end of the oscillatory capacitors C_G and C_D must be connected to the VDD pin without exception.

Reference
When either one end of the oscillatory capacitors C_G and C_D is connected to the VSS pin instead of the VDD pin, the oscillatory circuit is still operational but subject directly to fluctuations in the voltage of the system power supply. Under sharp fluctuations between 5V and battery voltage in particular, the oscillatory circuit may be brought to a temporary stop. Thus, it is not recommendable to connect either one end of the oscillatory capacitors C_G and C_D to the VSS pin.

< Considerations in Installing Components Surrounding Oscillatory Circuit >

1) Install the oscillatory capacitors C_G and C_D in the closest possible proximity to the IC.
2) Avoid laying any signal or power line in the proximity of the oscillatory circuit (particularly in the area marked with "←A→" in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN or OSCOUT pin and the printed circuit board (PCB).
4) Avoid using any long parallel line to wire the OSCIN and OSCOUT pin.
5) Take extreme care not to cause condensation, which leads to various problems such as failure of the crystal oscillators.

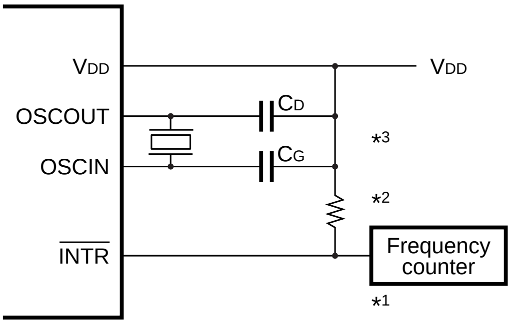
< Other Relevant Considerations >

1) When applying an external input of clock pulses (32.768kHz) to the OSCIN pin:
   DC coupling ···········Prohibited due to mismatching input levels.
   AC coupling ···········Permissible except that unpredictable results may occur upon detection of the stop of oscillation if any error occurs in such detection due to such factors as noises. Timer operation is prohibited upon detection of the stop of oscillation.
2) Avoid using the oscillator output of the RP/RF/RS5C62 (from the OSCOUT pin) to drive any other IC for the purpose of ensuring stable oscillation characteristics.

4. Adjustment of Oscillation Frequencies

4.1 Measurement of Oscillation Frequency

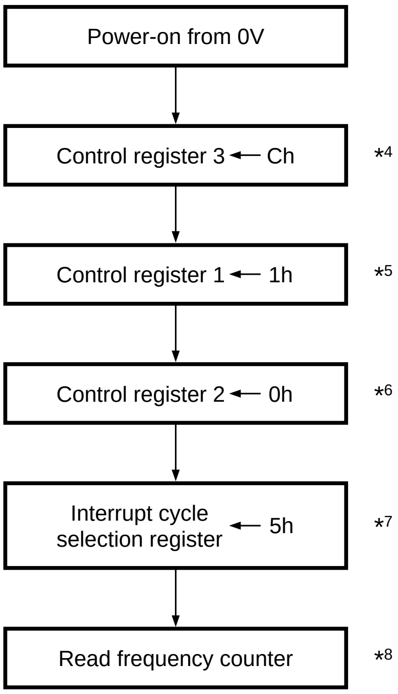
The oscillation frequency can be measured by using the $\overline{\text{INTR}}$ pin output (a cyclic interrupt). Note that its measurement is affected by and cannot therefore be obtained with accuracy by the OSCIN pin input and the OSCOUT pin output, which are directly measured by such means as a probe.



*1) Use a frequency counter with 6 or more readout digits in order to ensure an accuracy on the order of ±1ppm.

*2) Pull up the $\overline{\text{INTR}}$ pin to the V_{DD} and set the CE pin to high.

*3) Connect either one end of the oscillatory capacitors C_G and C_D to the V_{DD} pin.



*4) Set both the $\overline{\text{TSTA}}$ and $\overline{\text{TSTB}}$ bits to "1" in the control register 3 to disable the test circuit.

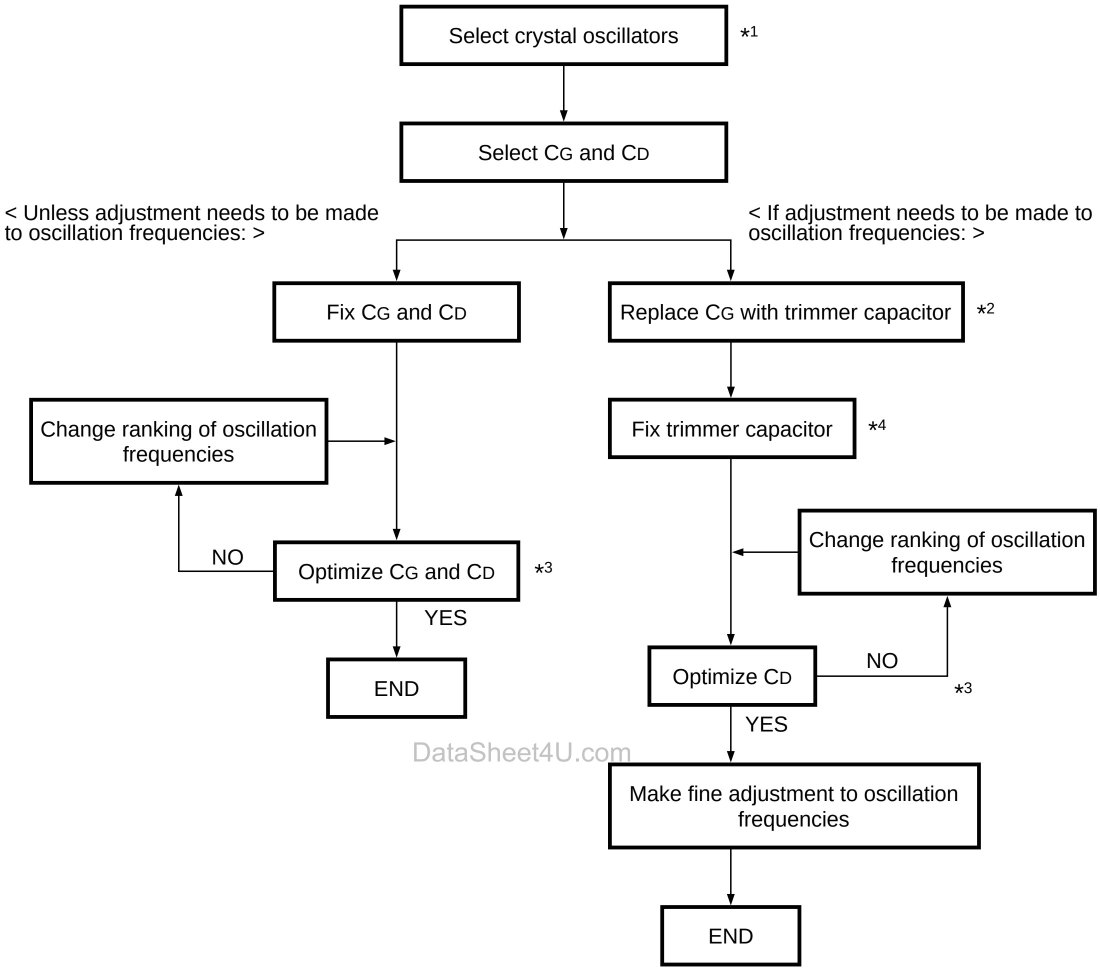
*5) Set the ALEN bit to "0" and the BANK bit to "1" in the control register 1 to disable an alarm interrupt.

*6) Set both the CTFG and ALFG bits to "0" in the control register 2 to disable an alarm interrupt and a cyclic interrupt.

*7) Set a cyclic interrupt to 1Hz (or any other cycle) in the pulse mode.

*8) An error of ±1ppm for every 1Hz amounts to a time lag of approximately 2.6 seconds per month.
[Example of monthly time lag calculation given an error of ±1ppm for every 1Hz.
±1ppm x 60 seconds x 60 minutes x 24 hours x 30 days = 2.592
= approx. 2.6 seconds per month]

4.2 Adjustment of Oscillation Frequencies



*1) In selecting crystal oscillators, inquire of their suppliers. Check how the selected crystal oscillators match the RP/RF/RS 5C62 and determine the ranking of oscillation frequencies (load capacitance (C_L) in general and equivalent series resistance (R1).)

*2) The oscillatory capacitor C_D can be replaced with a trimmer capacitor to adjust oscillation frequencies.

*3) Optimize the oscillatory capacitors C_G and C_D to adjust oscillation frequencies to desired values (on the actual PCB in consideration of possible influences by floating capacitance). Note that the greater capacitance of the oscillatory capacitors C_G and C_D tend to result in increased current consumption and prolonged oscillation start time. As a guide, their recommendable capacitance ranges from 5 pF to 20 pF (10 pF to 10-odd pF in particular). (See the typical characteristic measurement.)

*4) Set the rotational angle of the trimmer capacitor slightly below the central value in its adjustment range (to ensure matching between the central values of the rotational angle and oscillation frequencies in consideration of the fact that smaller capacitance lead to greater frequency variations).

Oscillation frequencies are subject to variations due to possible fluctuations in ambient temperature and supply voltage (see "Typical Characteristics").

Reference
A 32kHz crystal oscillator causes a clock delay above or below the central temperature range of 20˚C to 25˚C. It is therefore recommended to adjust or set oscillation frequencies in such a manner as to become slightly high in room temperature.

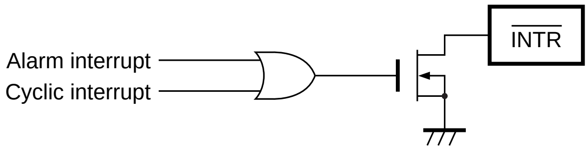
RICOH

5. Interrupts

Interrupts are available in the following two types:

1) Alarm interrupt: Requested upon driving low (turning on) the $\overline{\text{INTR}}$ pin in matching between preset alarm time (in minutes and hours) and time indicated by the time counter (in minutes and hours).
2) Cyclic interrupt: Requested upon driving low (turning on) the $\overline{\text{INTR}}$ pin with a preset cycle.

To output an alarm interrupt and a cyclic interrupt, the $\overline{\text{INTR}}$ pin is configured as shown in the figure below:



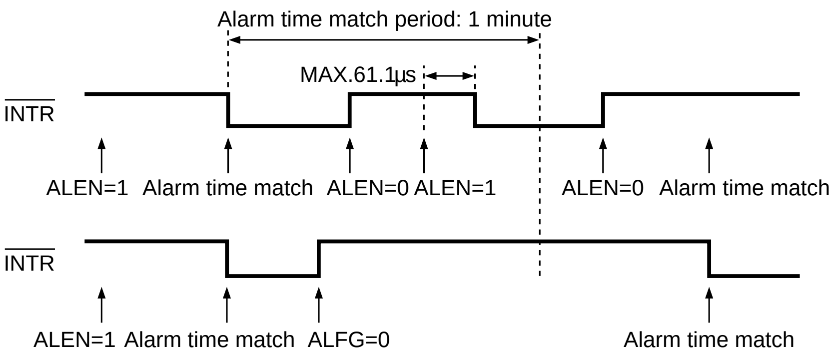
*1) When an alarm interrupt and a cyclic interrupt are generated in combination, their logical sum (OR) is output from the $\overline{\text{INTR}}$ pin. In this event, they can be distinguished from each other by reading the ALFG and CTFG bits of the control register 2.
*2) The $\overline{\text{INTR}}$ pin output has indefinite states at power-on from 0V.
*3) An alarm interrupt and a cyclic interrupt are both enabled whether the CE pin input is held high or low.

Interrupt Registers

Alarm-time················	Alarm register	(See "2. 6 Alarm Register".)
	ALEN bi	(See "2. 1 Control Register 1".)
	ALFG bit	(See "2. 2 Control Register 2".)
Cyclic ······················	Cyclic interrupt select register	(See "2. 5 Control Register 2".)
	CTFG bit	(See "2. 2 Control Register 2".)

5.1 Alarm Interrupt

Desired alarm time (in minutes and hours) can be preset in the alarm digits of the alarm register with the ALEN bit set to "0" and then to "1" in the control register 1. Upon matching between the preset alarm time and the time indicated by the time counter, the $\overline{\text{INTR}}$ pin is driven low (turned on) to output a request for an alarm interrupt. The $\overline{\text{INTR}}$ pin output can be controlled by using the ALEN bit in the control register 1 and the ALFG bit in the control register 2.



*1) The above figure assumes that an alarm interrupt occurs in the absence of a cyclic interrupt.
*2) The ALFG bit has an inverse logic from that of the $\overline{\text{INTR}}$ pin output.

RICOH

5.2 Cyclic Interrupt

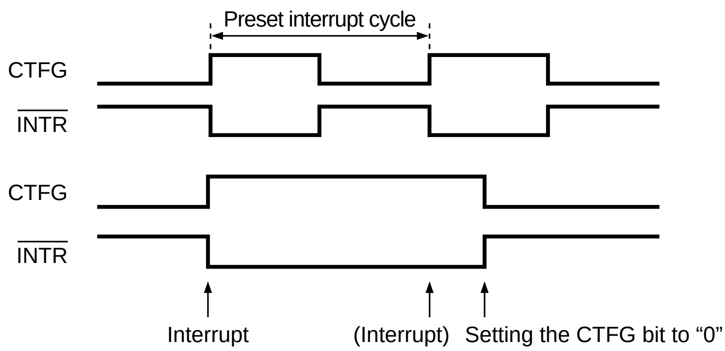
A desired interrupt cycle can be preset in the bits in the interrupt cycle selection register. With the preset interrupt cycle, the $\overline{\text{INTR}}$ pin is driven low (turned on) to output an request for a cyclic interrupt. A cyclic interrupt can be output from the $\overline{\text{INTR}}$ pin in the pulse mode and the level mode. In the level mode in particular, a cyclic interrupt can be disabled by setting the CTFG bit to “0” in the control register 2.

Available interrupt cycles: 6 types (0.488ms, 0.977ms, 7.813ms, 62.5ms, 1s, and 60s)

Available output modes: 2 types (pulse mode and level mode)

- Pulse mode
  (The CT_3 bit is set to “0”.)
  (The CTFG bit is not intended for write operation.)

- Level mode
  (The CT_3 bit is set to “1”.)
  (The CTFG bit is intended for setting to “0” only.)



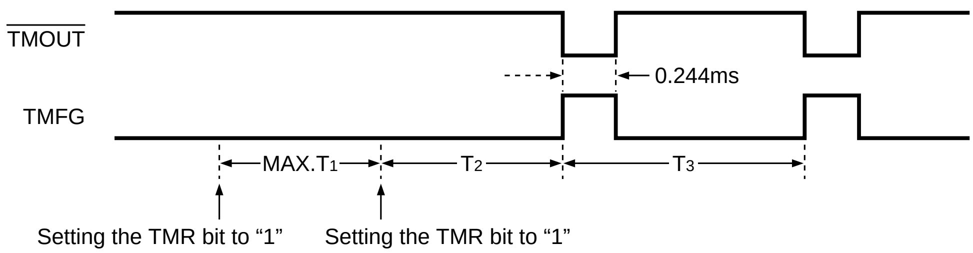
*1) A preset interrupt cycle can be canceled by setting the bits to “0” in the interrupt cycle selection register.
*2) The above figure assumes that a cyclic interrupt occurs in the absence of an alarm interrupt.
*3) The CTFG bit has an inverse logic from that of the $\overline{\text{INTR}}$ pin output.

Cyclic Interrupt

Interrupt cycle selection register	(See “2.5 Interrupt Cycle Selection Register”)
CTFG bit	(See “2.2 Control Register 2”)

6. Timer

Upon lapse of time preset in the timer clock selection register, cyclic pulses are output from the $\overline{\text{TMOUT}}$ pin. The timer counter can be reset conditional on restart by setting the TMR bit to “1” in the control register 1. (It can act as a watchdog timer.)



*1) The timer is stopped upon driving low the CE pin input, but restarted upon driving high the CE pin input.
*2) Timer output is disabled upon resetting the TM_3 bit to “0” when the stop of oscillation is detected.
*3) The T3 to T1 bits are described in “2. 9 Timer Clock Selection Register”.
*4) Timer output is turned off upon setting the TMR bit to “1” in the control register 1 during timer output.

Reference

It is recommended to update the settings of the timer clock selection register at regular time intervals to improve the stability of timer operation.

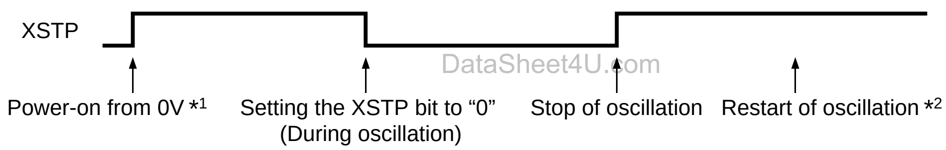
Elements Involved in Timer

Timer clock selection register and TMFG bit	(See “2.9 Timer Clock Selection Register”)
TMR bit	(See “2.1 Control Register 1”)

7. Detection of Stop of Oscillation

The stop of oscillation can be detected by monitoring the XSTP bit in the control register 2. Namely, the XSTP bit is switched from “0” to “1” upon detection of the stop of oscillation. This principle can be used to check the validity of time data.

(The stop of oscillation can also be detected by using the software-controlled processes described in 11.1.2 Initialization Subject to Setting of XSTP Bit. “Initialization at Power-on”.)



*1) The XSTP bit is set to “1” at power-on from 0V. Note that the XSTP bit may be locked at instantaneous power disconnection.

*2) Once the stop of oscillation has been detected, the XSTP bit is kept at “1” even after the restart of oscillation.

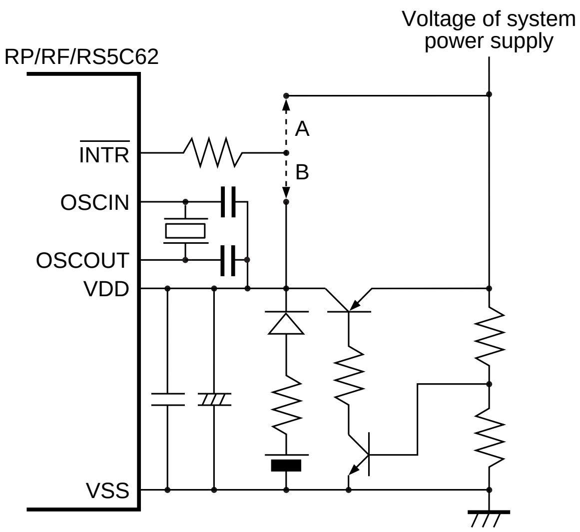
Considerations in Using XSTP Bit

Ensure error-free detection of the stop of oscillation by:

1) Preventing the VDD pin input from making instantaneous power disconnection.
2) Preventing the crystal oscillators causing condensation.
3) Preventing the crystal oscillators from causing noises on the PCB.
4) Preventing the individual pins from being impressed with voltage exceeding the maximum rating.

RICOH

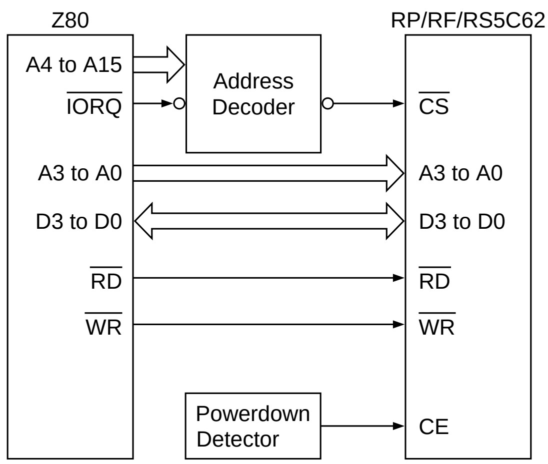
8. Typical Power Supply Circuit



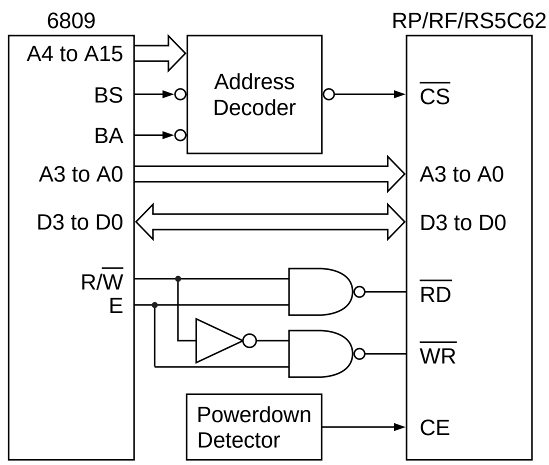
1) Connect either one end of the oscillatory capacitors C_G and C_D to the VDD pin.
2) Install the by-pass capacitors for both high and low frequencies in close proximity to the IC in such a manner as to form a parallel arrangement.
3) Connect the pull-up resistor of the $\overline{\text{INTR}}$ pin to different points depending on whether it is used while the CE pin is held low (in battery backup).
   (I) Connect the pull-up resistor to Point A in the left circuit diagram unless it is used while the CE pin is held low.
   (II) Connect the pull-up resistor to Point B in the left circuit diagram if it is used while the CE pin is held low.

9. Typical Connection between RP/RF/RS5C62 and CPU

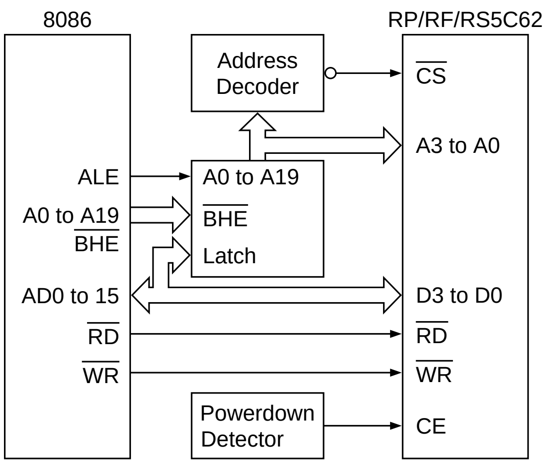
RP/RF/RS5C62 and CPU Z80



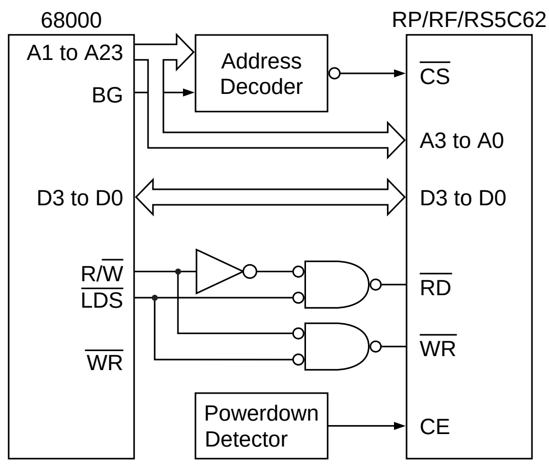
RP/RF/RS5C62 and CPU 6809



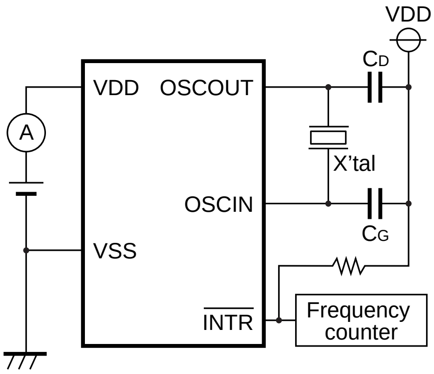
RP/RF/RS5C62 and CPU 8086



RP/RF/RS5C62 and CPU 68000

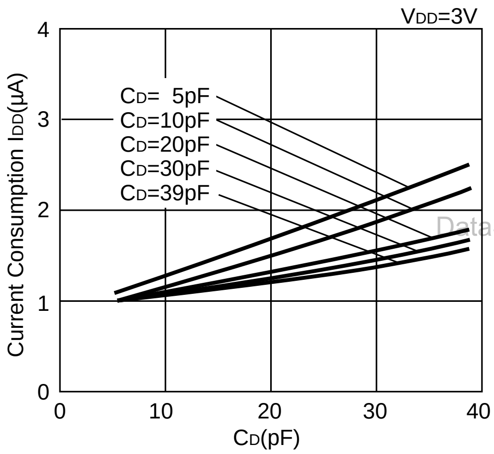


10. Typical Characteristics

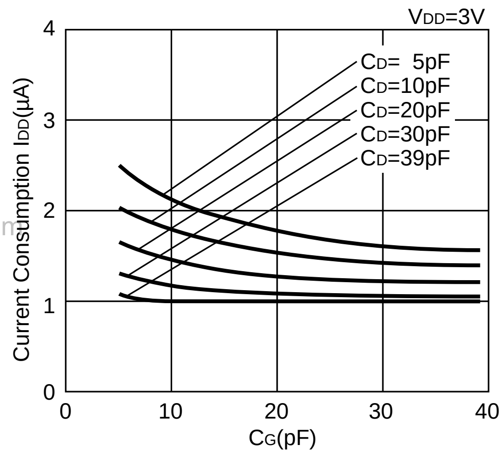


C_D=10pF, C_G=10pF
X'tal : $R_L \leq 35k\Omega$
Topt=25˚C
Input pin : VDD or VSS
Output pin : Open

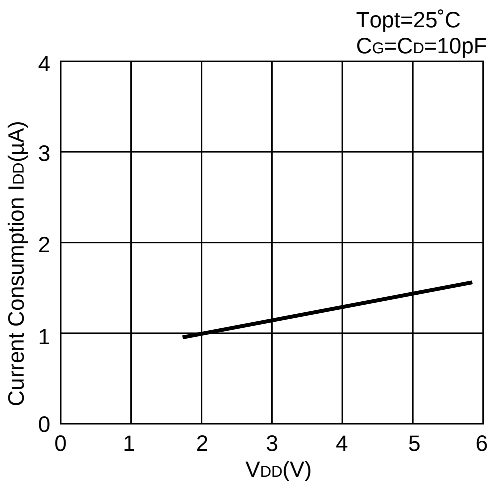
10.1 Current Consumption vs. CD



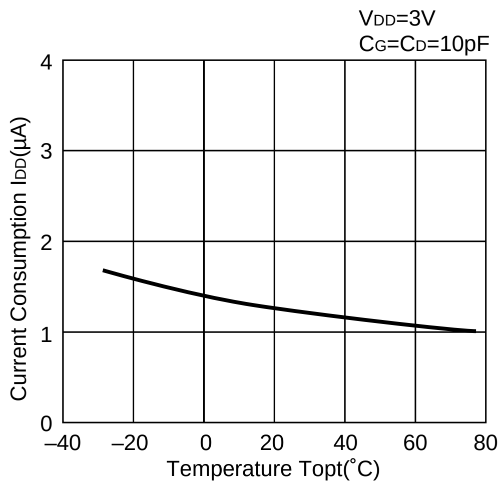
10.2 Current Consumption vs. CG



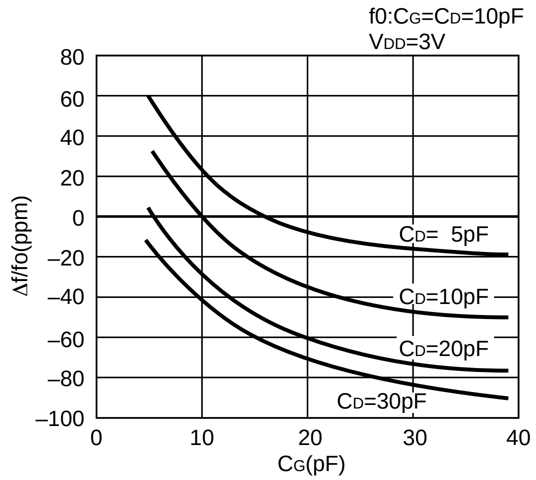
10.3 Current Consumption vs. VDD



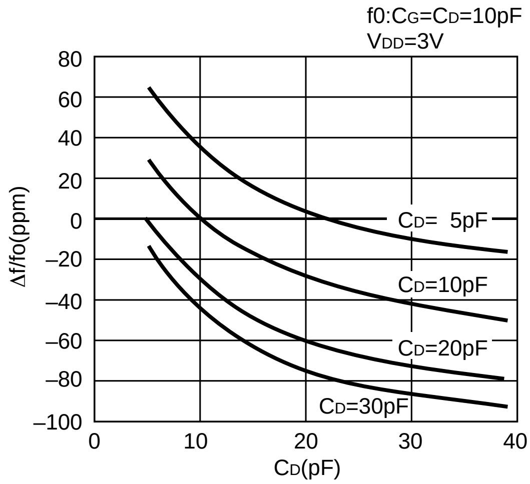
10.4 Current Consumption vs. Temperature



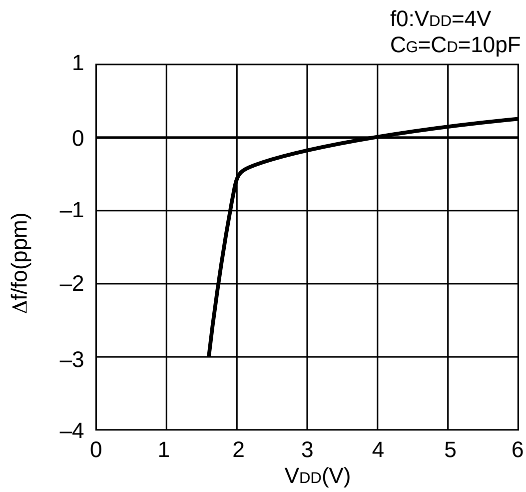
10.5 Oscillation Frequency vs. CG



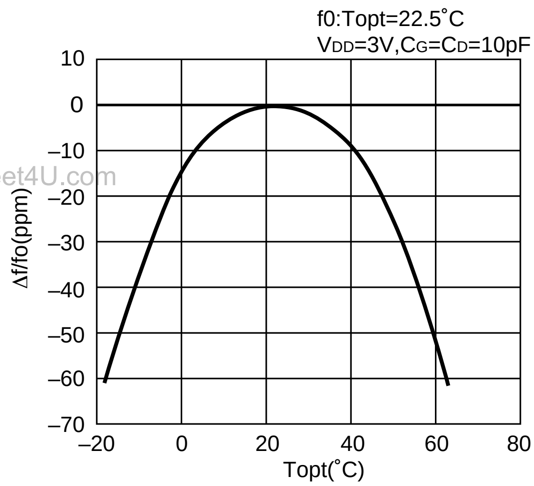
10.6 Oscillation Frequency vs. CD



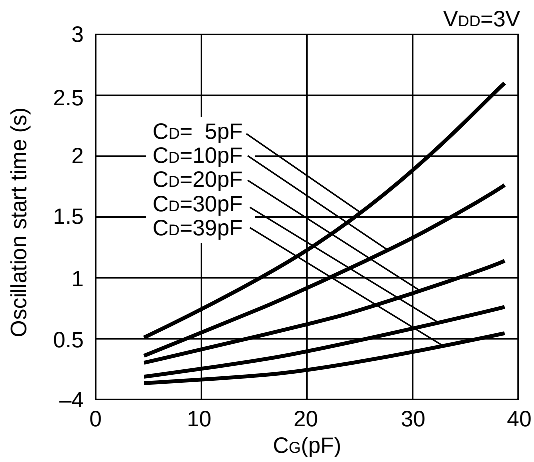
10.7 Oscillation Frequency vs. VDD



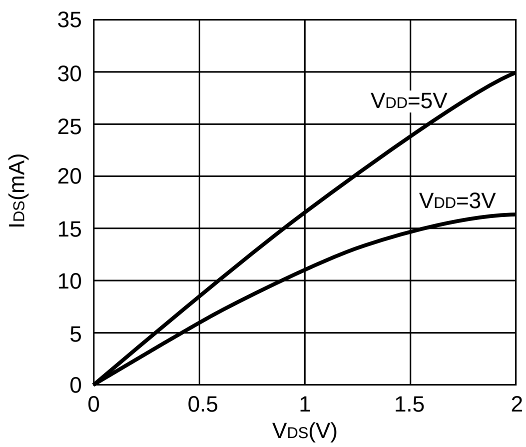
10.8 Oscillation Frequency vs. Temperature



10.9 Oscillation Start Time vs. CG



10.10 Nch Open Drain Output IDS vs.VDS

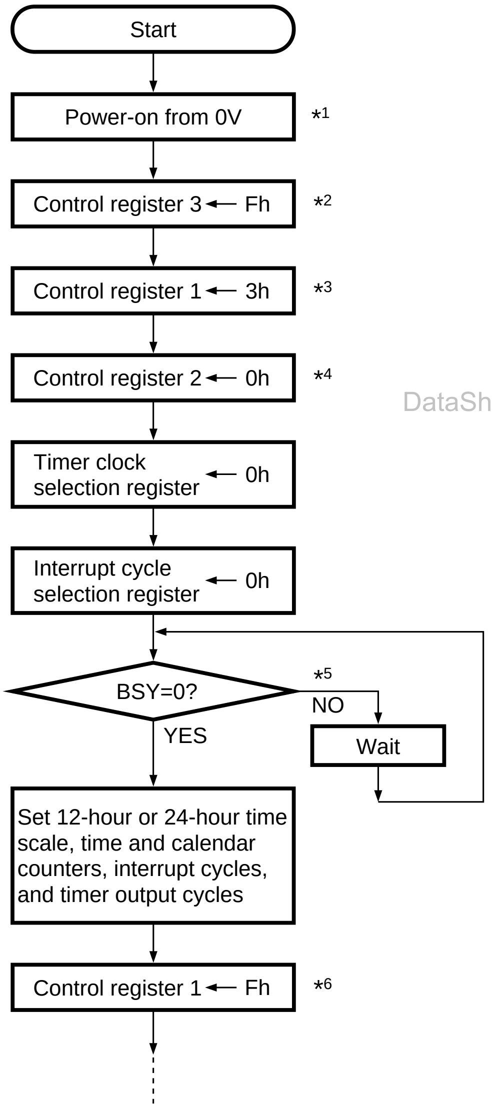


11. Typical Software-controlled Processes

11.1 Initialization at Power-on

At power-on from 0V, the internal registers and the output pins have indefinite states and therefore require initialization. The process of initialization differs as exemplified below depending on whether the XSTP bit (oscillation stop detection bit) is set in the control register 2. In the latter typical process of initialization below, the XSTP bit is used to check the validity of internal time data and the presence or absence of the initial routine.

11.1-1 Initialization Subject to No Setting of XSTP Bit



*1) At power-on from 0V, the internal registers and the output pins have indefinite states.

*2) Set both the $\overline{\text{TSTA}}$ and $\overline{\text{TSTB}}$ bits and the WTRST bit to “1” in the control register 3 and thereby set the BSY bit to“1” in the control register 2.

*3) Set the WTEN bit to “0” (clock operation disabled), the ALEN bit to “0” and TMR bit to “1” (turn off the output pins) and the BANK bit to “1” in the control register 1.

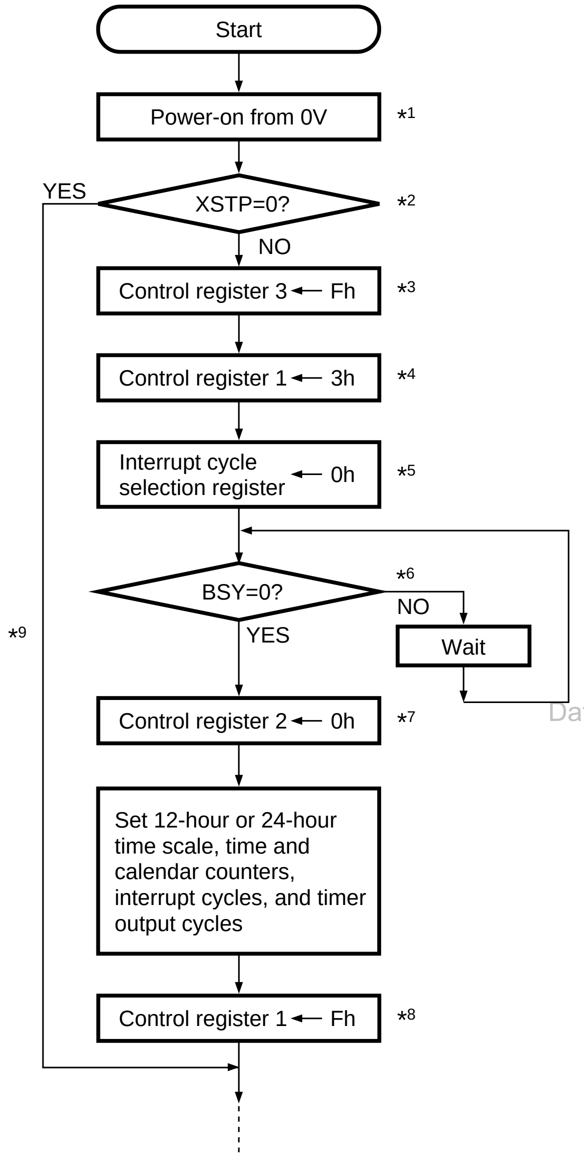
*4) Drive high (turn off) the $\overline{\text{INTR}}$ and $\overline{\text{TMOUT}}$ pin outputs.

*5) Check the BSY bit in the control register 2 for the dual purpose of confirming the absence of a carry and confirming the start of oscillation. This requires additional time to wait for the start of the crystal oscillators. Further, assign a time-out period to exit from the loop for checking the BSY bit.

*6) Start both the clock and alarm functions.

*7) This typical process of initialization is applied at power-on from 0V and not required at start-up from the backup battery.

11.1-2 Initialization Subject to Setting of XSTP Bit



*1) At power-on from 0V, the internal registers and the output pins have indefinite states.

*2) Check the validity of internal time data.
In using the XSTP bit, ensure error-free detection of the stop of oscillation by:
1) Preventing the crystal oscillators causing condensation.
2) Preventing the VDD pin input from making instantaneous power disconnection.
3) Preventing the crystal oscillators from causing noises on the PCB (by such means as signal line isolation).
4) Preventing the individual pins from being impressed with voltage exceeding the maximum rating.

*3) Set both the $\overline{TSTA}$ and $\overline{TSTB}$ bits and the WTRST bit to "1" in the control register 3 and thereby set the BSY bit to "1" in the control register 2.

*4) Set the WTEN bit to "0" (clock operation disabled), the ALEN bit to "0" and TMR bit to "1" (turn off the output pins) and the BANK bit to "1" in the control register 1.

*5) Drive high (turn off) the $\overline{INTR}$ pin output.

*6) Wait for the start of the crystal oscillators to confirm the start of oscillation as well as the absence of a carry. Further, assign a time-out period to exit from the loop for checking the BSY bit.

*7) Set the XSTP bit to "0" in the control register 2.

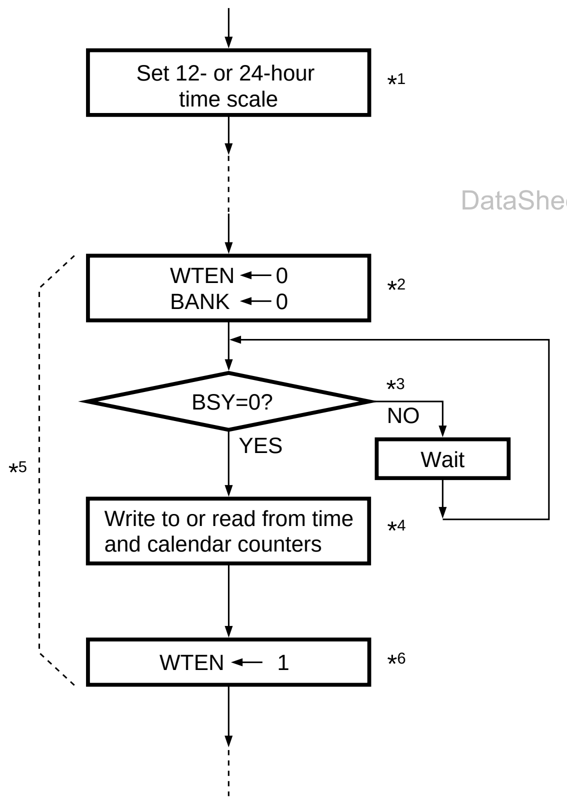
*8) Start both the clock and alarm functions.

*9) This route is applied at start-up from the backup battery when the process of initialization is omitted, assuming no internal time data destruction.

11.2 Writing to or Reading from Time and Calendar Counters

Writing to the time and calendar counters must be performed in the absence of a carry. In particular, correct writing to the time and calendar counters requires stopping time count operation (by setting that the WTEN bit to "0" in the control register 1) and confirming the absence of a carry (by checking that the BSY bit to "0" in the control register 2). On the other hand, reading from the time and calendar counters may be performed by stopping time count operation, generating a cyclic interrupt, or dual reading.

11.2-1 Writing to or Reading from Time and Calendar Counters by Stopping Time Count Operation (by Setting WTEN and checking BSY bits)



*1) Set the 12- or 24-hour time scale once before writing to the time and calendar counters (at the time of initialization after power-on from 0V).

*2) Set the WTEN bit to "0" in the control register 1 to stop the second and higher-order digits.

*3) When the BSY bit is set to "1" in the control register 2, continue reading from the time and calendar counters until it is set to "0" or wait for 122.1 μs or more. When the BSY bit is set to "0", it is kept at "0" until the WTEN bit is set to "1" again in the control register 1.

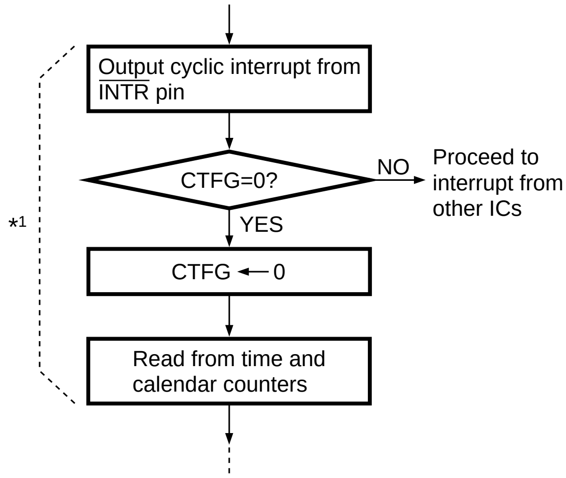
*4) Writing to the 1-year or 10-year counter automatically enables leap year indication. To disable leap year indication, write "4h" (set the $\overline{\text{LYE}}$ bit to "1") in the leap year indication register after setting the time and calendar counters. Note that leap year indication is continued without correction until the year 2099.

*5) When reading from the time and calendar counters, ensure that this route lasts within 1 second. If this route lasts within 1 second, the 1-second digit is incremented by 1 to correct a 1-second carry occurring during read operation upon setting the WTEN bit to "1" again in the control register 1. Note that the 1-second digit is also incremented by 1 to correct more than one 1-second carry while the WTEN bit is kept at "0", resulting in a clock delay.

*6) Restart time count operation. (The WTEN bit will automatically be set to "1" in the control register 1 upon driving low the CE pin.)

*7) When writing to the time and calendar counters, be sure to check the BSY bit in the control register 2 by disabling a carry (by setting the WTEN bit to "0").

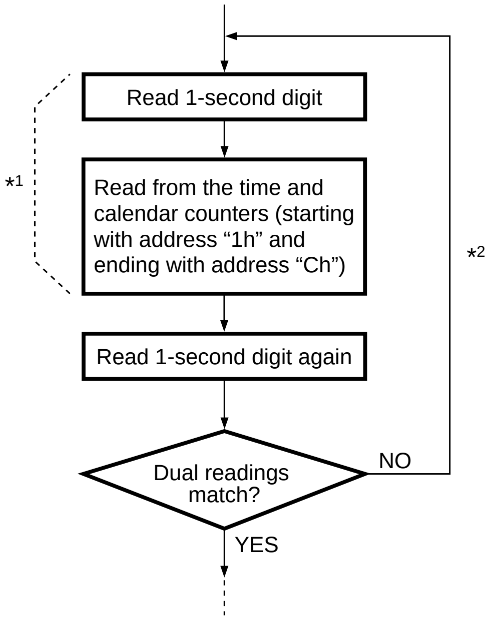
11.2-2 Reading from Time and Calendar Counters by Generating Cyclic Interrupt



This typical process of reading from the time and calendar counters is applied on the conditions below:

1) The $\overline{\text{INTR}}$ pin is set to the level mode (upon setting the CT_3 to "1" in the interrupt cycle selection register).
2) The route marked with "*1" lasts within the time equivalent to a preset cycle minus 30.5µs (for the purpose of preventing occurrence of an error due to a carry during reading from the time and calendar counters).

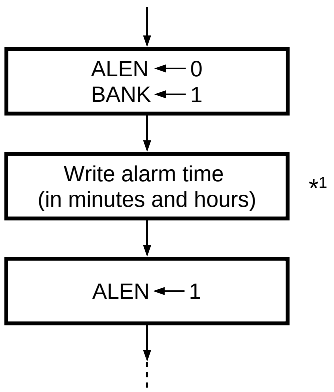
11.2-3 Reading from Time and Calendar Counters by Dual Reading



*1) A carry from the second digit starts with 1 second via 10 seconds,---and 1 year, and ends with 10 years. Consequently, reading from the time and calendar counters must also start with the 10-second digit (at address "1h") and end with the 10-year digit (at address "Ch").

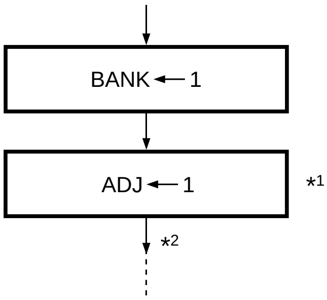
*2) This route assumes that an error occurs due to a carry during reading from the time and calendar counters.

11.3 Writing Alarm Time to Alarm Registers

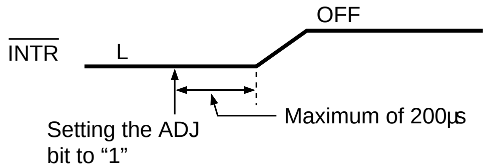


*1) Non-existent alarm time may be set in the alarm register, provided that an alarm interrupt is disabled. To enable an alarm interrupt, existent alarm time must be set in the alarm register.

11.4 Adjusting Second Digit by ±30 Seconds

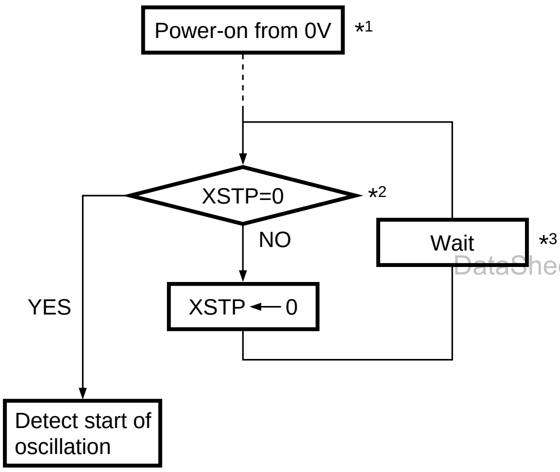


*1) Upon setting the ADJ bit to "1" in the adjustment register, the second and lower-order 1 to 8Hz dividers are reset conditional on restart. At this time, when the $\overline{\text{INTR}}$ pin is held low for output of a cyclic interrupt with a cycle of 1 second or 60 seconds in the pulse mode, the $\overline{\text{INTR}}$ pin is turned off with the timing shown below:



*2) Adjustment of the second digit by ±30 seconds requires a maximum of 122.1µs, during which the BSY bit is kept at "1" in the control register 2.

11.5 Detecting Start of Oscillation



*1) This typical process of detecting the start of oscillation is applied at power-on from 0V.

*2) At power-on from 0V, the XSTP bit is set to "1" in the control register 2.

*3) Note that the start of oscillation normally requires a time period (oscillation start time) on the order of 0.1 to 2 seconds. Further, assign a time-out period to exit from loop for checking the XSTP bit in the control register 2.

Notice
In using the XSTP bit, ensure error-free detection of the stop of oscillation by: 1) Preventing the crystal oscillators causing condensation. 2) Preventing the VDD pin input from making instantaneous power disconnection. 3) Preventing the crystal oscillators from causing noises on the PCB (by such means as signal line isolation). 4) Preventing the individual pins from being impressed with voltage exceeding the maximum rating.

QUESTIONS AND ANSWERS ON USE

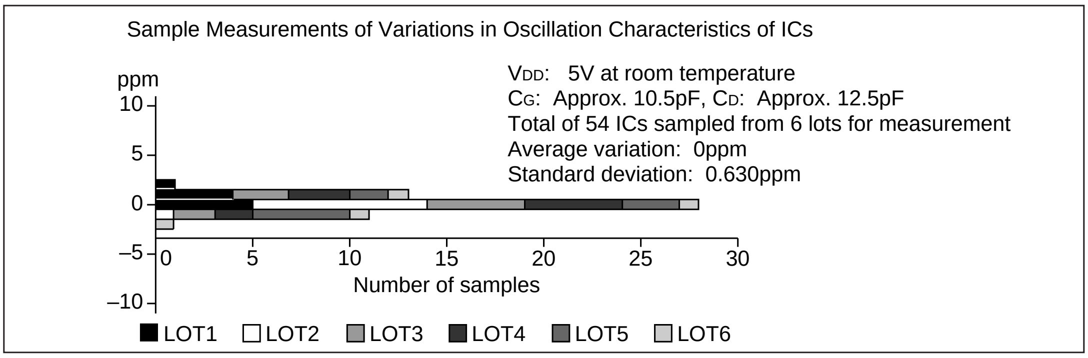
Below are listed questions and answers on using the RP/RF/RS5C62 under the following four categories:

1) Crystal oscillators
2) Hardware
3) Software
4) AC/DC electrical characteristics and others

Category	Questions and Answers
1) Crystal oscillators	Question 1 : What are the causes of failure in adjustment of oscillation frequencies? (Subject to use of variable capacitors and adjustment of oscillation frequencies) Answer 1: For capacitance variations of about 5 to 30pF, oscillation frequency variations measure a little more than about 60ppm in real terms (see the graphs in 10.5 and 10.6 of "10. Typical Characteristics"). The possible causes of failure in adjustment of oscillation frequencies are: 1. Variations in the crystals, the capacitors, and the ICs outside the range of adjustment of capacitance variations, and 2. Mismatching between the central value of variations in these elements and that of the range of variations of variable capacitors. The possible corrective measures for the causes 1. and 2. above are : 1. Reviewing variations in the individual elements. (For reference, measurements of variations in the ICs are shown in Answer 3 below.), and 2. Adjusting oscillation frequencies according to the directions described in "4. Adjustment of Oscillation Frequencies" in "USAGE". Question 2 : What are the causes of inaccurate time count operation? (Subject to use of fixed capacitors and no adjustment of oscillation frequencies) Answer 2: The possible causes of inaccurate time count operation are : 1. Mismatching between the capacitance of the oscillatory capacitors C_G and C_D and that of the crystals and the ICs, and 2. Too great floating capacitance present on the actual PCB to be neglected for the oscillatory capacitors C_G and C_D, which are adapted to the ICs and the ranking of oscillation frequencies (load capacitance (C_L)). The possible corrective measures for the causes 1. and 2. above are : 1. Adjusting oscillation frequencies according to the directions described in "4. Adjustment of Oscillation Frequencies" in "USAGE", and 2. Reduce the capacitance of the oscillatory capacitors C_G and C_D by the equivalent of floating capacitance, which seems to vary from 1 to several pF depending on the layout of the PCB, or mount them on the actual PCB for final fixing.

Category	Questions and Answers
	Question 3 : How many variation factors should be considered? (Subject to use of fixed capacitors and no adjustment of oscillation frequencies) 1. The possible factors behind oscillation frequency variations are : 1-1. Variations in frequencies of crystals, 1-2. Variations in oscillation characteristics of the ICs, 1-3. Variations in the external oscillatory capacitors C_G and C_D, and 1-4. Variations in floating capacitance present on the actual PCB. 2. On the other hand, the possible factors behind surrounding environment variations are : 2-1. Variations in ambient temperature, and 2-2. Variations in supply voltage. Variations in 1 - 1 to 1 - 4 are listed in the order of decreasing degree. The individual variations are described below : 1-1. Most crystals seem to have variations in their frequencies on the order of ±20ppm while some crystals may have smaller variations. For variations in frequencies of individual crystals, inquire of their suppliers. 1-2. Sample measurements of variations in oscillation characteristics of the ICs are shown graphically on the next page. Note that these measurements are not guaranteed ones and are therefore intended for reference use only. 1-3. Variations in oscillation frequencies differ slightly depending on the capacitance of external oscillatory capacitors C_G and C_D. More specifically, the smaller the capacitance of C_G and C_D, the greater the variations in oscillation frequencies. Subject to no adjustment of oscillation frequencies, they should have small variations relative to their capacitance (see the graphs in 10.5 and 10.6 of "10. Typical Characteristics"). 1-4. Normally, variations in floating capacitance present on the actual PCB seem to be small enough to be negligible. 2-1. Variations in ambient temperature are dominantly affected by the temperature characteristics of fork-shaped crystal oscillators (forming an upward-facing quadratic curve) (see the graph in 10.8 of "10. Typical Characteristics"). 2-2. Because the oscillatory circuit inside the ICs is driven by constant voltage, Variations in oscillation frequencies due to variations in supply voltage measure±0.5ppm or less on real terms at room temperature with the VDD pin input ranging from 2.5V to 5.5V (see the graph in 10.7 of "10. Typical Characteristics").

Category	Questions and Answers

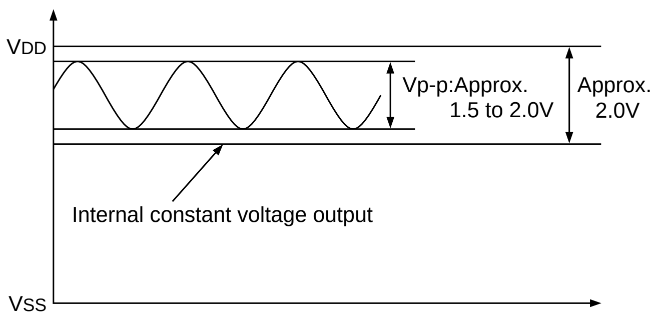


Question 4 : Why should you avoid connecting either end of the oscillatory capacitors C_G and C_D to the VSS pin instead of the VDD pin?

Answer 4: Because the oscillatory circuit is driven by a constant voltage of 2V relative to the VDD pin, either one end of the oscillatory capacitors C_G and C_D must be connected to the VDD pin without exception. When either one end of the oscillatory capacitors C_G and C_D is connected to the VSS pin instead of the VDD pin, the oscillatory circuit is still operational but subject directly to fluctuations in the voltage of the system power supply. Under sharp fluctuations between 5V and battery voltage in particular, the oscillatory circuit may be brought to a temporary stop. Thus, it is not recommendable to connect either one end of the oscillatory capacitors C_G and C_D to the VSS pin.

Question 5 : Synchroscopic observation of the OSCOUT pin output shows that it has an oscillatory waveform having a small amplitude or approximating to the VDD pin input. What is the cause of this phenomenon?

Answer 5: To reduce power consumption, the oscillatory circuit is driven by a constant voltage of about 2V relative to the VDD pin, so that the OSCOUT pin output has an oscillatory waveform shown in the figure below. Its amplitude will vary slightly depending on the capacitance of the oscillatory capacitor C_D. Note that the oscillatory waveform measurements on the OSCOUT pin cannot be directly applied to adjustment of oscillation frequencies, which are shifted by use of a probe. (For how to adjust oscillation frequencies, see “4. Adjustment of Oscillation Frequencies” in “USAGE”.)



Category	Questions and Answers
2) Software	Question 1 : In the typical software-controlled process of initialization at power-on from 0V, the BSY bit is checked to find that it fails to be switched from "1" to "0". What is the cause of this failure? Answer 1 : In the typical software-controller process of initialization at power-on from 0V, the BSY bit is set to "1" in the control register 2 by setting the WTRST bit to "1" in the control register 3 for the dual purpose of confirming the absence of a carry and confirming the start of oscillation. After power-on from 0V, the start of oscillation normally requires a time period (oscillation start time) on the order of 0.1 to 2 seconds, which, in turn, requires additional time to wait for the start of the crystal oscillators. It seems most likely, therefore, that the BSY bit fails to be switched from "1" to "0" due to prolonged oscillation start time. Further, another possibility is that the start of oscillation may be hindered by some trouble (e.g. condensation) with the crystal oscillators. It is necessary, therefore, to assign a time-out period to exit from the loop for checking the BSY bit in the control register 2. Question 2 : How is it possible to read from the time and calendar counters without setting the WTEN and BSY bits? Answer 2 : As described in "11. 2. 1. Writing to or Reading from Time and Calendar Counters by Stopping Time Count Operation (by Setting WTEN and BSY Bits)", the WTEN bit in the control register 1 and the BSY bit in the control register 2 are used to read from the time and calendar counters in such a manner as to prevent occurrence of an error due to a carry during read operation. If the BSY bit is found to be "1", however, this typical software-controlled process involves additional time to wait for setting of the BSY bit to "0". To save such wait time, an alternative action can be taken to read the 1-second digit twice without setting the WTEN and BSY bits as shown in "11. 2. 3. Reading from Time and Calendar Counters by Dual Reading". This process features dual reading from the 1-second digit in anticipation of an error which may occur due to a carry during read operation from the time and calendar counters in case of mismatching between the dual readings. Question 3 : How can the $\overline{\text{INTR}}$ pin output be used? Answer 3 : The $\overline{\text{INTR}}$ pin outputs an alarm interrupt and a cyclic interrupt. For details on these two types of interrupts, see "5. Interrupts" in "USAGE". Question 4 : An attempt to disable an alarm interrupt by setting the ALFG bit to "0" in the control register 2 results in holding the $\overline{\text{INTR}}$ pin output low. What is the cause of this phenomenon? Answer 4 : The $\overline{\text{INTR}}$ pin outputs the logical sum (OR) of an alarm interrupt and a cyclic interrupt when they are generated in combination. Consequently, an attempt to disable an alarm interrupt by setting the ALFG bit to "0" may result in holding the $\overline{\text{INTR}}$ pin low when it outputs a cyclic interrupt as well.

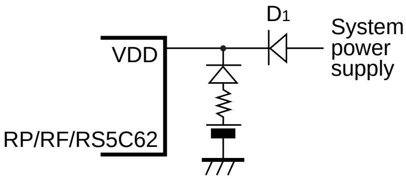
Category	Questions and Answers
	Question 5 : An attempt to disable a cyclic interrupt by setting the CTFG bit to "0" in the control register 2 results in holding the $\overline{\text{INTR}}$ pin output low. What is the cause of this phenomenon? Answer 5 : As in Answer 4 above, this phenomenon may occur when an alarm interrupt and a cyclic interrupt are simultaneously output from the $\overline{\text{INTR}}$ pin. Question 6 : What will happen if non-existent time is set? Answer 6 : Time or alarm digits which are non-existent or indicated in non-BCD notation can be set in the time counter or the alarm register without causing any trouble. If such invalid digits are left, however, they may cause faulty time count operation in case of a carry or mismatching between clock time and alarm time. Question 7 : How can an alarm interrupt be used in battery backup? (Why is an alarm interrupt not output in battery backup?) Answer 7 : An alarm interrupt is normally output from the $\overline{\text{INTR}}$ pin in battery backup (while the CE pin is held low). Its output is most likely to fail, therefore, when the other end of the pull-up resistor of the $\overline{\text{INTR}}$ pin is connected to any power supply which may be turned off. To prevent this problem, confirm that the other end of the pull-up resistor of the $\overline{\text{INTR}}$ pin is connected to the backup battery. Question 8 : How can an alarm interrupt be output on a monthly basis? Answer 8 : The RP/RF/RS5C62 are configured to issue a daily alarm and cannot be reconfigured to generate an alarm interrupt on a monthly basis. Considering that they are designed to reduce current consumption as described in "Note" below, an advisable alternative action is to generate an alarm interrupt to the CPU on a daily basis and keep track of alarm dates in a software-controlled process. Note : The RP/RF/RS5C62 are designed to reduce current consumption (ensure typical current consumption on the order of 1µA for 3V). Daily current consumption can be calculated as follows : Assuming, for example, that an alarm interrupt to the CPU is generated on a daily basis as the CPU is operating for a period of 0.5seconds with peak current consumption of 20mA, daily current consumption can be calculated from the equation : $0.5s \times 20mA / 60 \times 60 \times 24 = 0.115\mu A$. This means a total base current of a little more than 1µA, a slight increase in current consumption.

Category	Questions and Answers
3) Hardware	Question 1 : Can the $\overline{CS}$ pin input be used as it is held low? Answer 1 : The $\overline{CS}$ pin input can be used as it is held low, provided that the $\overline{RD}$ and $\overline{WR}$ pin inputs are caused to transition from their high to low to high levels to enable read and write operations, respectively. Question 2 : May the $\overline{CS}$ pin input be driven low before or during the process of addressing? Answer 2 : The $\overline{CS}$ pin input may be driven low before, during, or even after the process of addressing. Addressing time (t_{AS}) indicates the time required to perform the process of addressing before the start of read or write operation at which both the $\overline{RD}$ and $\overline{CS}$ pin inputs or both the $\overline{WR}$ and $\overline{CS}$ pin inputs are driven low. For more details, see "1. Reading and Writing Operations" in "USAGE". Question 3 : At power-on from 0V, the $\overline{INTR}$ pin is driven low to output interrupts. What is the cause of this phenomenon? Answer 3 : At power-on from 0V, the internal registers and counters have indefinite states, causing the $\overline{INTR}$ pin to have indefinite states as well. It is necessary, therefore, to provide temporary masking for interrupts output from the $\overline{INTR}$ pin and initialize the internal registers and counters by following the typical software-controlled processes of initialization at power-on (see "11. 1 Initialization at Power-on"). (At power-on from 0V, when the XSTP bit is set to "1" to indicate the start of oscillation, the $\overline{TMOUT}$ pin output is turned off.) Question 4 : As the N-channel open drain pins, may the $\overline{INTR}$ and $\overline{TMOUT}$ pins be impressed with higher voltage than the VDD pin? Answer 4 : As the N-channel open drain pins, the $\overline{INTR}$ and $\overline{TMOUT}$ pins, neither of which incorporates a protective diode for the VDD pin, may be impressed with higher voltage than the VDD pin as long as it does not exceed the maximum absolute rating of 12V. Their on-state resistance typically ranges from a few dozen ohms to one hundred ohms (see the graph in 10.10 of "10. Typical Characteristics"). Their on-state current should preferably range from 10mA to 20mA or less and must not exceed the maximum current consumption for the package.

Category	Questions and Answers

Question 5 : Is it possible to configure a power switching circuit containing a diode?

Answer 5: It is not recommendable to configure a power switching circuit containing a diode, which causes a voltage drop as shown in the right circuit diagram (where "D_1" represents a diode). (The maximum absolute ratings of the input and output pins range from –0.3V to the V_{DD} plus 0.3V.)



Question 6 : To what test modes can the $\overline{\text{TSTA}}$ and $\overline{\text{TSTB}}$ bits be applied as test bits?

Answer 6: The $\overline{\text{TSTA}}$ and $\overline{\text{TSTB}}$ bits are intended for IC selection and not for general users. (These test bits should be kept at "1" in normal operation and will automatically be set to "1" upon driving low the CE pin.)

Question 7 : What are the possible causes of any changes which may occur to internal time data?

Answer 7: The possible causes of such changes include :

1. Occurrence of writing errors due to such factors as noises caused below the operating voltage of the CPU at the time of switching from the power supply to the backup battery,
2. Occurrence of instantaneous power disconnection, and
3. Writing to other addresses than are allocated originally due to shortage of addressing time (t_{AS}).

   To cope with the cause 1. , see "2. Handling of CE Pin" in "USAGE". To solve the cause 2. , check the power supply system to prevent instantaneous power disconnection from occurring. To overcome the cause 3. , secure sufficient addressing time (t_{AS}).

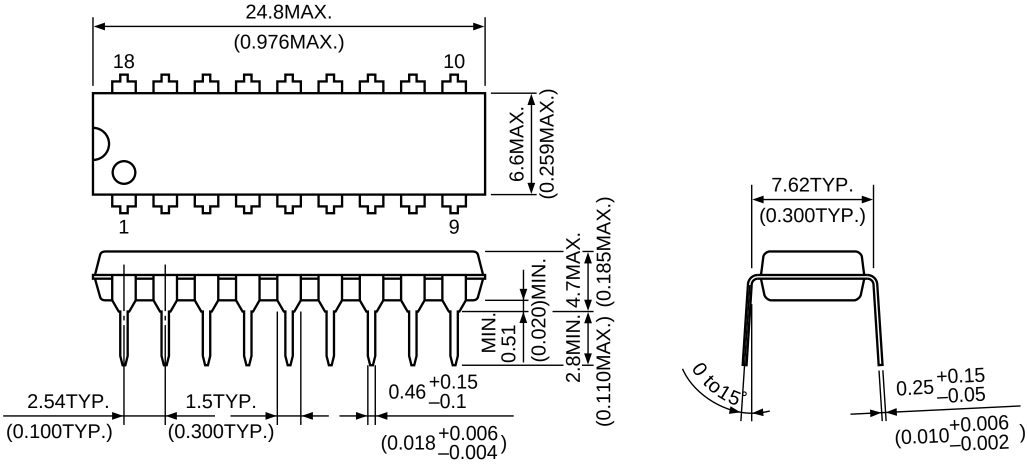
Question 8 : What are the ranges of operating voltages?

Answer 8: Range of operating voltage of crystal oscillators only for time count operation: 2.0V to 6.0V.
Range of operating voltage having any access to the CPU : 2.7V to 6.0V
Incidentally, AC timing is available in three ratings : 3V±10%, 5V±10%, and 5V±20%.

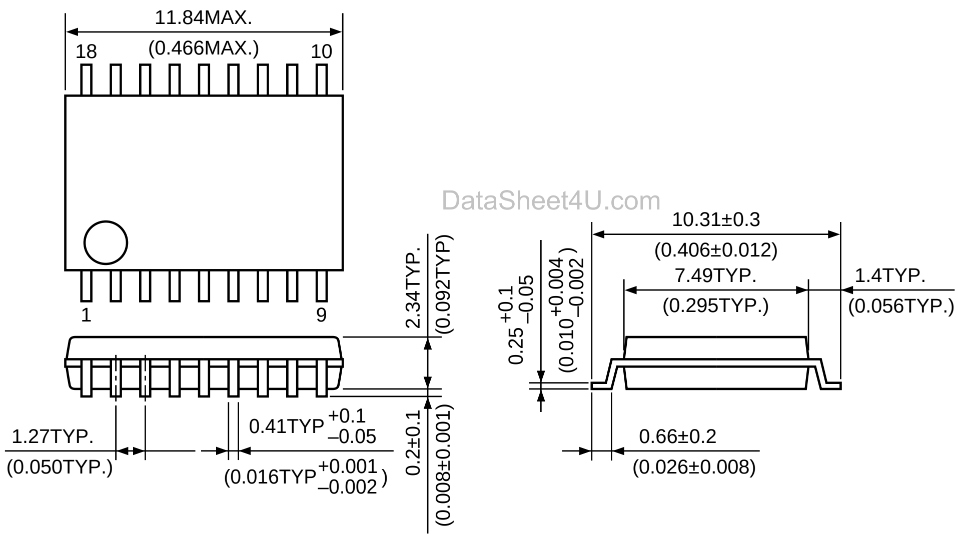
Category	Questions and Answers
4) AC/DC electric character-istics and others	Question 1: What is the difference between backup current consumption and standby current consumption? Answer 1: Backup current consumption is defined as current consumption in battery backup with the CE pin held low (connected to the VSS input) and the other pins opened (the term "opened" also refers to "impressed with intermediate voltage"). On the other hand, standby current consumption is defined as current consumption in the absence of access from the CPU with the CE and $\overline{CS}$ pins held high (connected to the VDD pin input) and the other input pins connected to the VDD or VSS pin input and the other output pins opened. The VDD pin input is set to 2.5V for backup current consumption and 5.5V for standby current consumption. Question 2: How is it possible to know typical backup current consumption and temperature characteristics in determining the battery capacity? Answer 2: For typical backup current consumption and temperature characteristics, see the graphs in 10. 1 to 10.4 in "10. Typical Characteristics". Question 3: What is the cause of partial mismatching of AC timing with the high-speed CPU? Answer 3: AC timing is designed to secure margins including variations and therefore difficult to change in principle, provided that it is susceptible to change, as the case may be, upon request. Question 4: Is it possible to extend the operating temperature range of –20°C to +70°C? Answer 4: As in Answer 3 above, the operating temperature range is difficult to change in principle, provided that it is susceptible to change, as the case may be, upon request.

PACKAGE DIMENSIONS (Unit: mm/(inch))

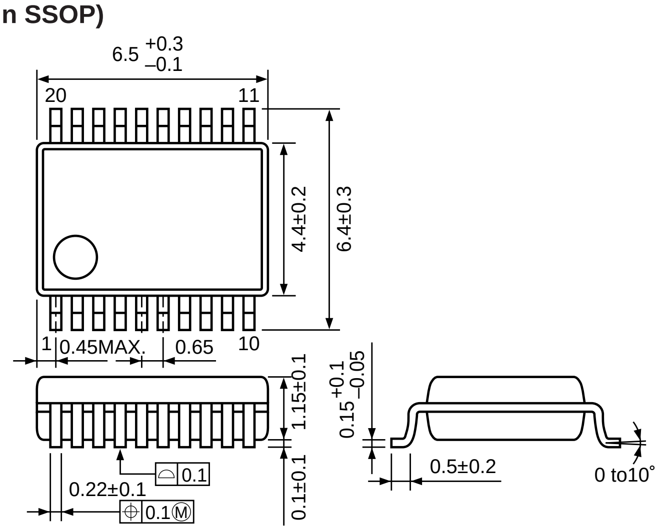
• **RP5C62 (18pin DIP)**



• **RF5C62 (18pin SOP)**

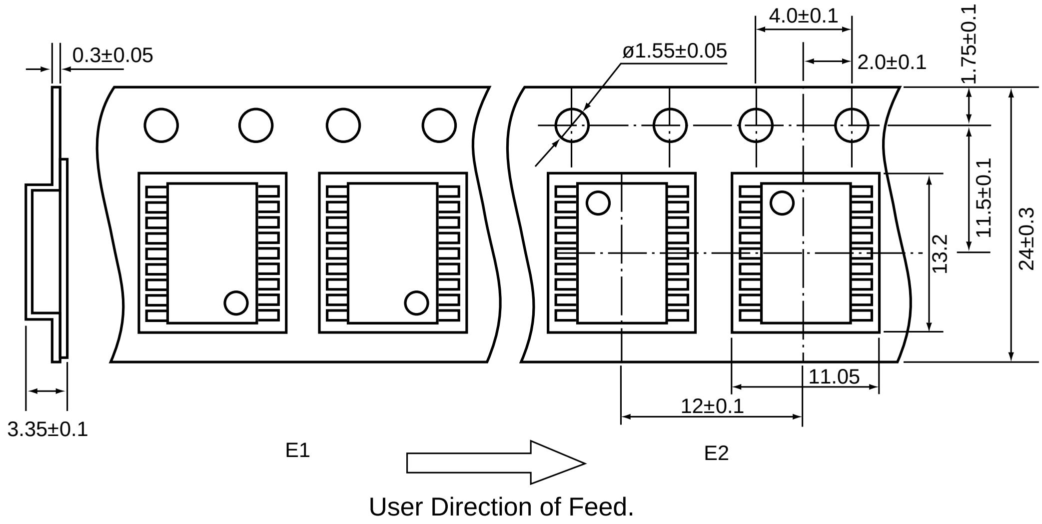


• **RS5C62 (20pin SSOP)**

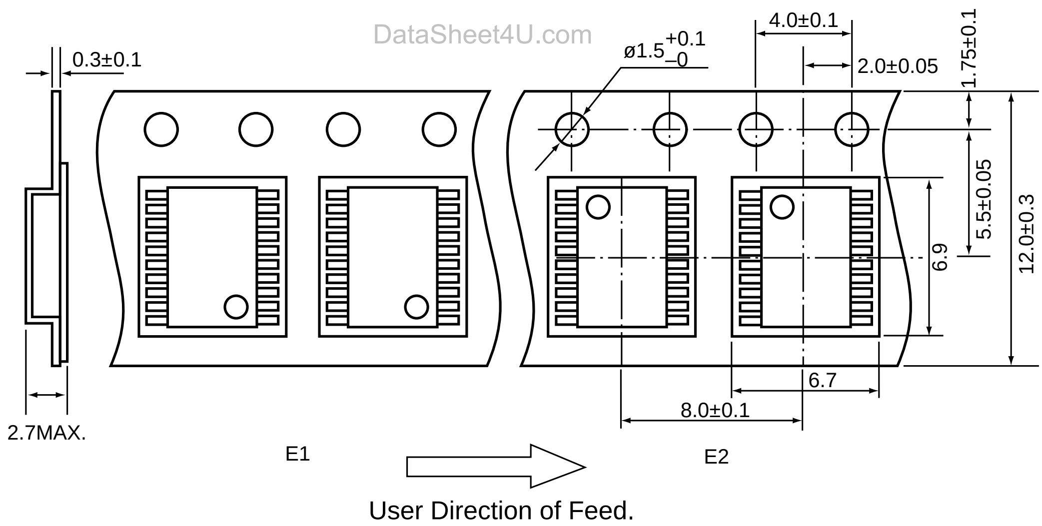


TAPING SPECIFICATIONS (Unit: mm)

• RF5C62 (18pin SOP)



• RS5C62 (20pin SSOP)



RICOH COMPANY, LTD.
ELECTRONIC DEVICES DIVISION

HEADQUARTERS
13-1, Himemuro-cho, Ikeda City, Osaka 563-8501, JAPAN
Phone 81-727-53-1111   Fax 81-727-53-6011

YOKOHAMA OFFICE (International Sales)
3-2-3, Shin-Yokohama, Kohoku-ku, Yokohama City, Kanagawa 222-8530, JAPAN
Phone 81-45-477-1697 Fax 81-45-477-1694 • 1695

http://www.ricoh.co.jp/LSI/english/

RICOH CORPORATION
ELECTRONIC DEVICES DIVISION

SAN JOSE OFFICE
3001 Orchard Parkway, San Jose, CA 95134-2088, U.S.A.
Phone 1-408-432-8800   Fax 1-408-432-8375