N Channel MOSFET

Lead Free Package and Finish

Applications:

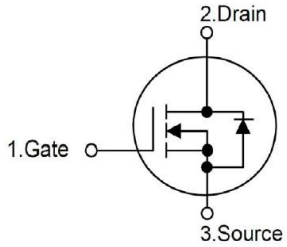
- •PWM applications
- •Load switch
- •Power management

I_D	$R_{DS(ON)}$(Max.)	V_{DSS}
50A	20mΩ	60V

Features:

- •V_{DS}=60V; I_D=50A
  $R_{DS(ON)}$ < 20mΩ @ V_{GS} =10V
  Rds(on) < 25mΩ @ VGS =4.5V
- •Ultra Low On-Resistance
- •High UIS and UIS 100% Test
- •RoHS Compliant

TO-252(DPAK) top view



Ordering Information

Part Number	Package	Marking
RS60N50D	TO-252	RS60N50D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS60N50D	Units
VDSS	Drain-to-Source Voltage	60	V
ID	Continuous Drain Current（Tc=25℃）	50	A
	Continuous Drain Current Tc=100℃	35	
IDM	Pulsed Drain Current (Note*1)	200	
PD	Power Dissipation（Tc=25℃）	89	W
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy (Note*2)	85	mJ
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 175	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS60N50D	Units	Test Conditions
RθJC	Junction-to-Case	1.8	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +175℃.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	60	--	--	V	VGS=0V,ID=250μA
IDSS	Drain-to-Source Leakage Current	--	--	1	μA	VDS=60V,VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+20V VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance (Note*3)	--	14.0	20.0	mΩ	VGS=10V,ID=30A
		--	17.0	25.0	mΩ	VGS=4.5V,ID=30A
VGS(TH)	Gate Threshold Voltage	1.2	1.6	2.5	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	7.4	--	nS	VDS=30V VGS=10V RL=6.7Ω RG=3Ω
trise	Rise Time	--	5.1	--		
td(OFF)	Turn-OFF Delay Time	--	28.2	--		
tfall	Fall Time	--	5.5	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2050	--	pF	VGS=0V VDS=30 Vf=1.0MHz
Coss	Output Capacitance	--	158	--		
Crss	Reverse Transfer Capacitance	--	120	--		
Qg	Total Gate Charge	--	50	--	nC	VDS=30V ID=20A VGS=10V
Qgs	Gate-to-Source Charge	--	6	--		
Qgd	Gate-to-Drain("Miller"）Charge	--	15	--		

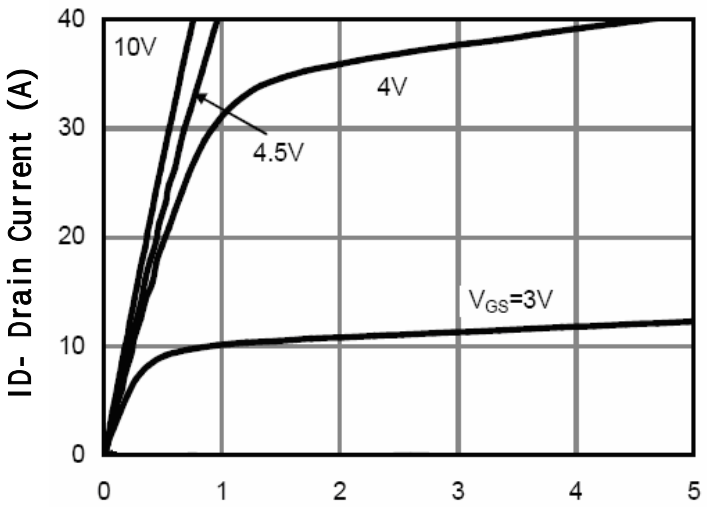
Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{SD}	Source-Drain Current(Body Diode)	--	--	50	A	
I_{SDM}	Pulsed Source-Drain Current(Body Diode)	--	--	200	A	Maximum Pulsed Drain to Source Diode Forward Current
V_{SD}	Diode Forward Voltage	--	--	1.2	V	IS=20A,VGS=0V
trr	Reverse Recovery Time	--	28	--	nS	VGS=0V I_F=120A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	40	--	nC	

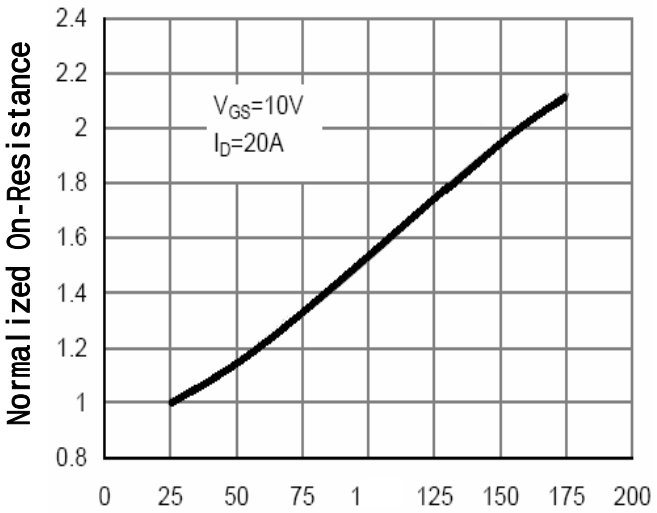
Notes:

*1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
*2. EAS condition: TJ=25℃, VDD=30V, VG=10V, L=0.5mH, RG=25Ω
*3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

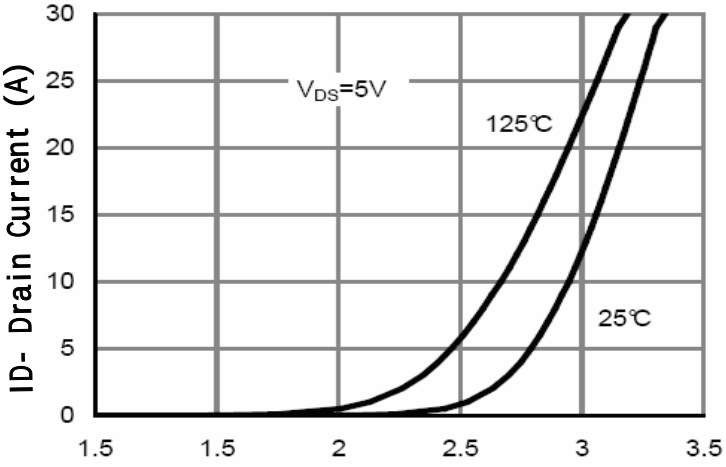
Typical Electrical and Thermal Characteristics (Curves)



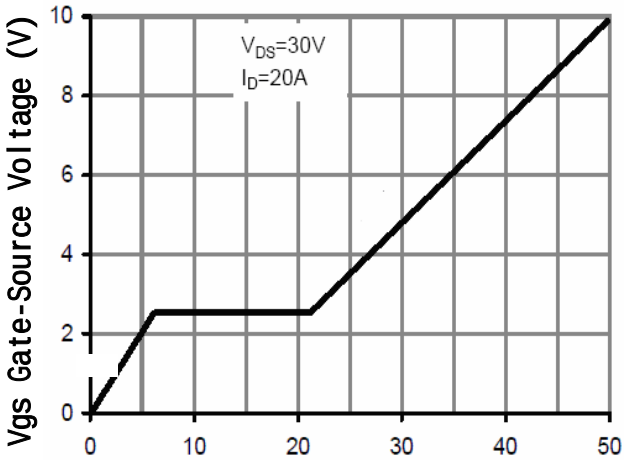
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



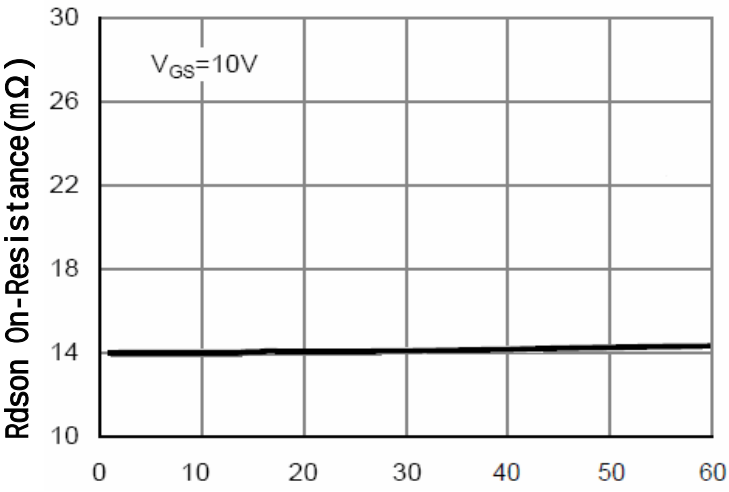
TJ-Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature



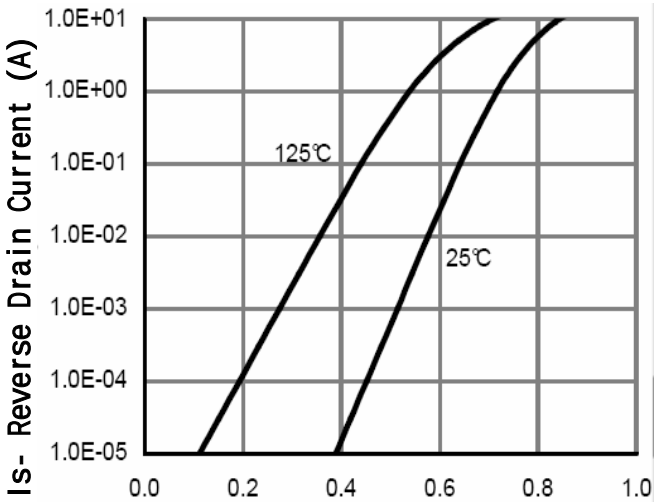
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



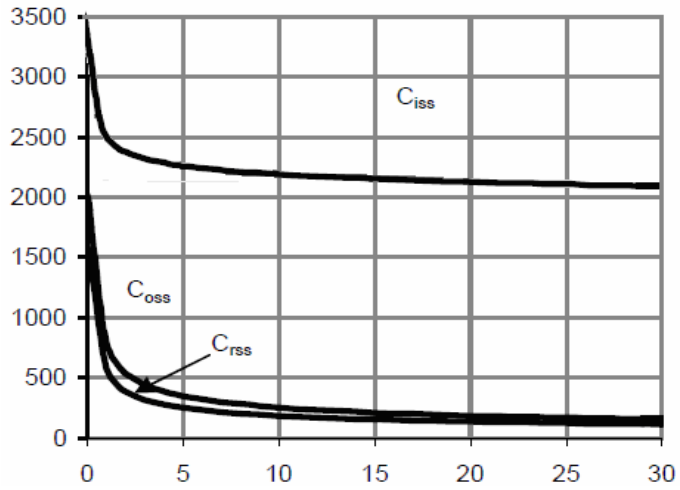
Qg Gate Charge (nC)
Figure 5 Gate Charge



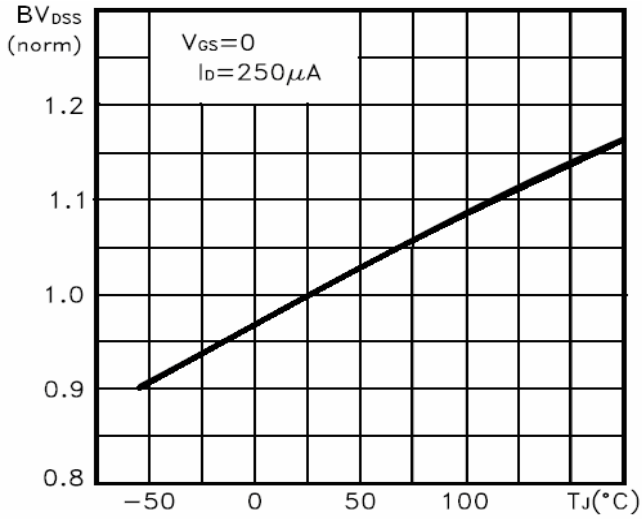
ID- Drain Current (A)
Figure 3 Rdson- Drain Current



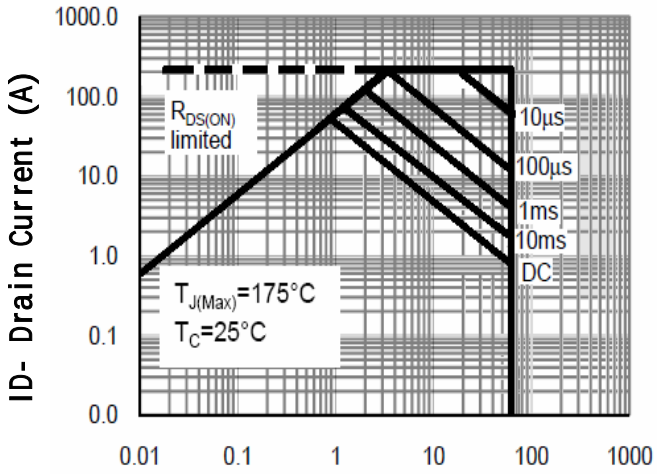
Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



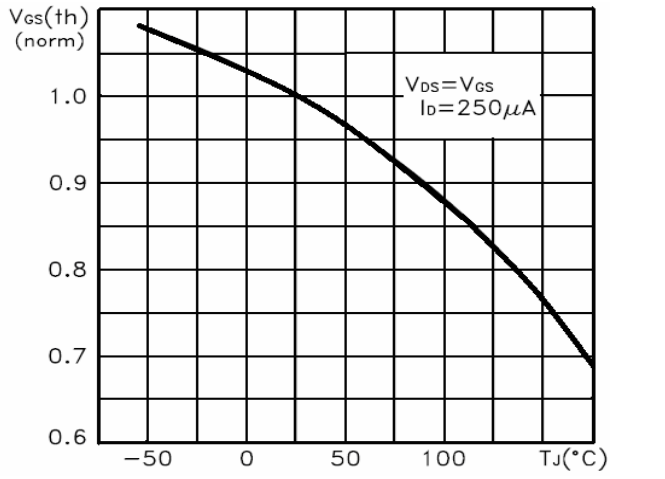
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



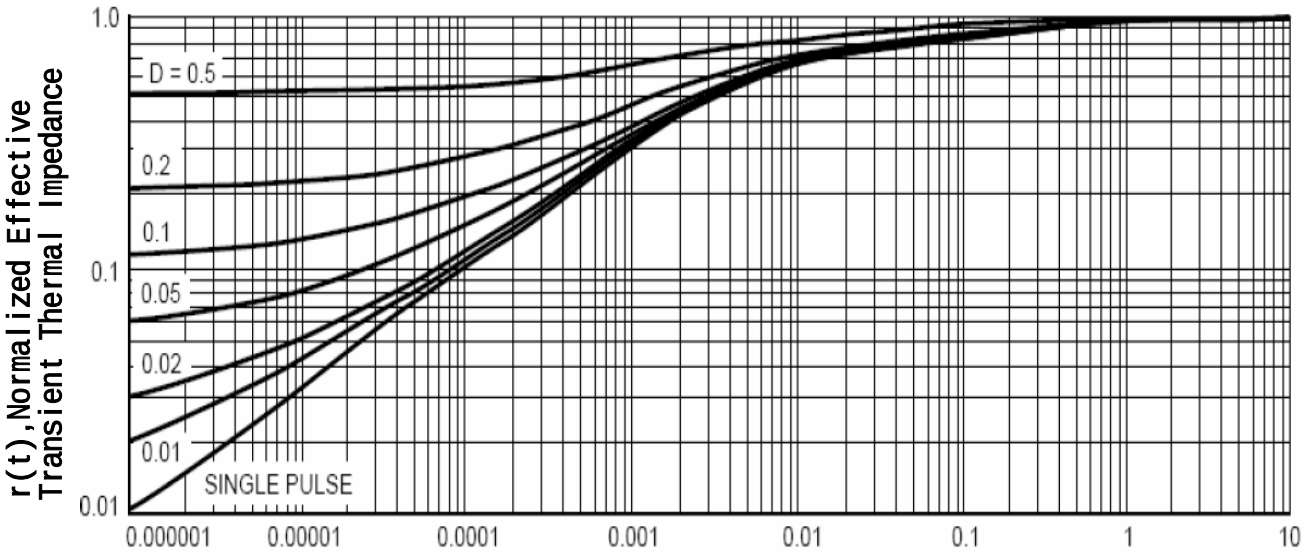
TJ-Junction Temperature(°C)
Figure 10 VGS(th) vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



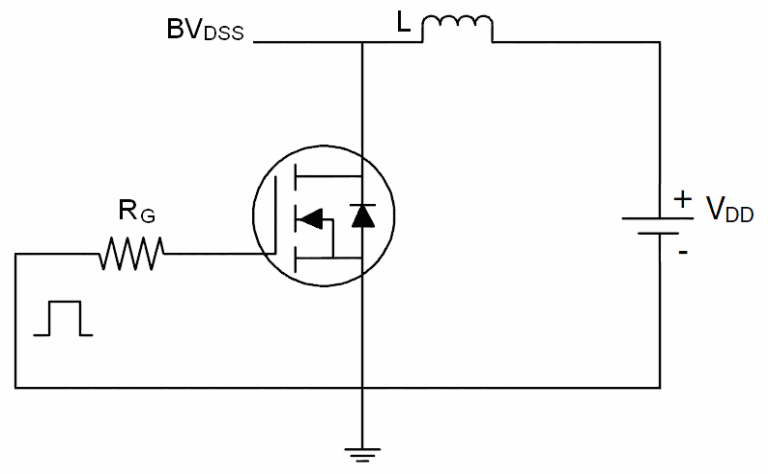
TJ-Junction Temperature(°C)
Figure 10 VGS(th) vs Junction Temperature



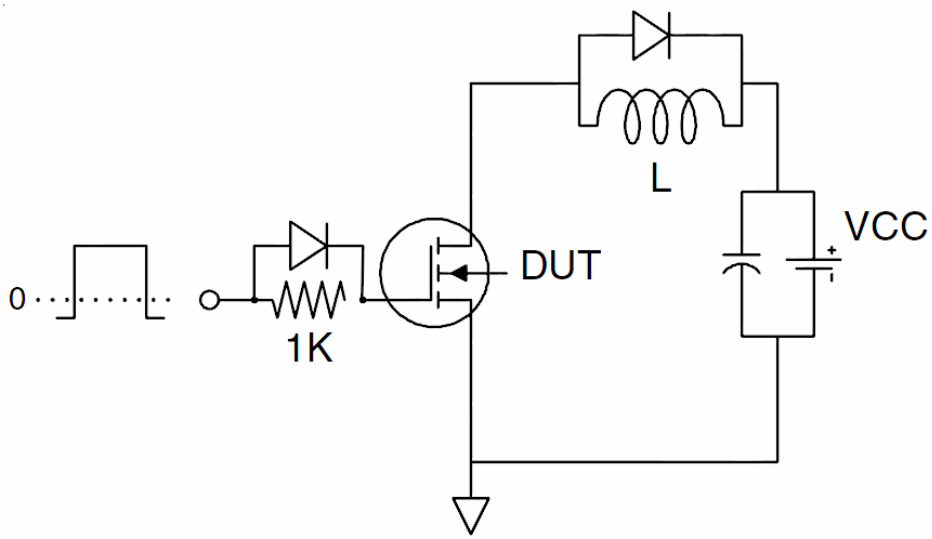
Square Wave Pluse Duration (sec)
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

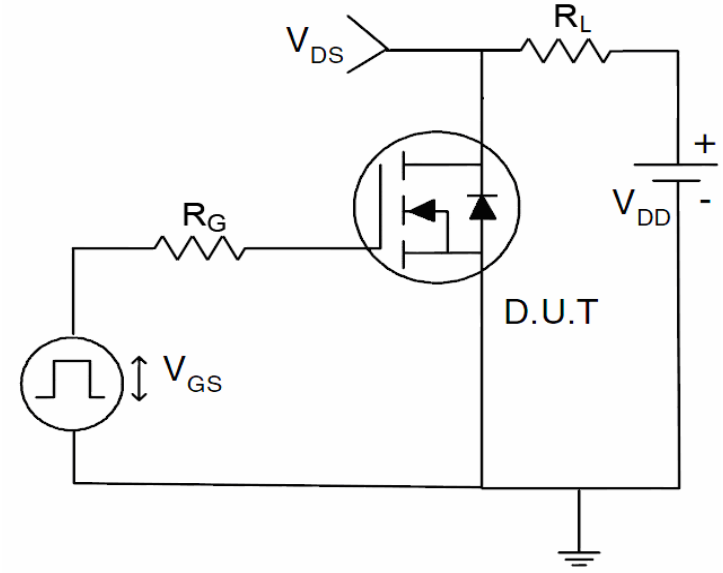
1) EAS test Circuit



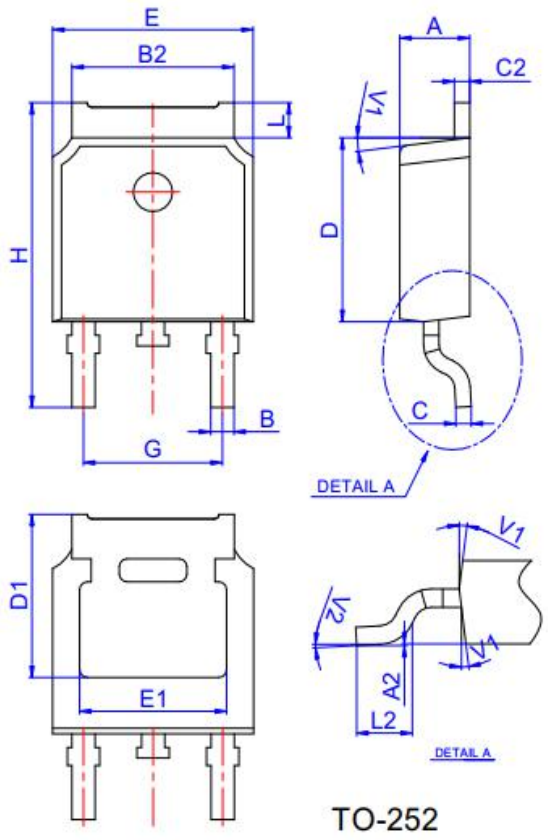
2) Gate charge test Circuit



3) Switch Time Test Circuit



Package outline drawing



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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