Supply Voltage Supervisor with Watchdog and Manual Reset

1 FEATURES

- **Operating Voltage Range:1.0V to 5.5V**
- **Low Power Consumption:40μA (Max)**
- **Precision Supply-Voltage Monitor: 2.63V, 2.93V, 3.08V, 4.00V**
- **Debounced TTL/CMOS Compatible Manual-Reset Input**
- **Guaranteed $\overline{RESET}$ Valid at V_{CC}=1.0V**
- **160ms Reset Pulse Width**
- **Independent Watchdog Timer (1.6sec TYP) Timeout**
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **Operating Temperature Range: -40°C to +125°C**
- **Available in Green Package: SOIC-8(SOP8)**

2 APPLICATIONS

- **Computers**
- **SOC、DSP or Micro Controllers**
- **Embedded Systems**
- **Industrial Equipment**
- **Intelligent Instruments**
- **Critical μP Power Monitoring**
- **Wireless Communications Systems**

3 DESCRIPTIONS

The RS706 microprocessor (μP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery function in μP systems. This device significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The RS706 provide four functions:
1) A reset output during power-up, power-down, and brownout conditions. The reset output remains operational with V_{CC} as low as 1.0V.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds (TYP).
3) A 1.2V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply.
4) An active-low manual-reset input.

The RS706 is available in Green SOIC-8 (SOP8) package. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS706	SOIC-8(SOP8)	4.90mm x 3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 TYPICAL APPLICATION

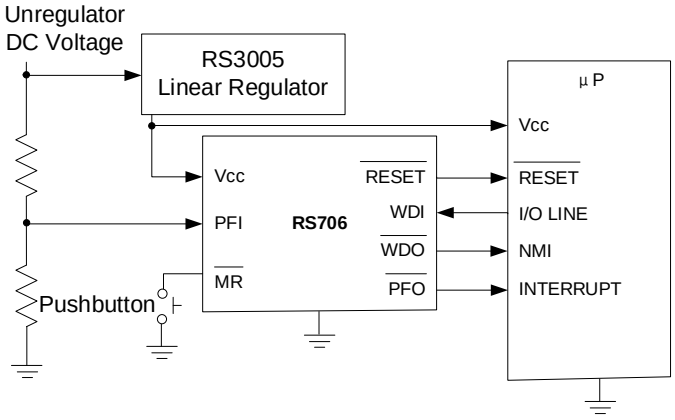


Table of Contents

5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2020/12/13	Initial version completed
A.2	2022/02/22	1.Added the maximum value of t_{MD} on Page 6@RevA.1 2.Modify ELECTRICAL CHARACTERISTICS
A.3	2022/06/27	1. Update Operating Temperature Range: -40°C to +125°C 2. Update Typical Operating Characteristics 3. Update Reset Pulse Width typical value 4. Update V_{CC} to $\overline{RESET}$ delay typical value

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2/3)	PACKAGE OPTION
RS706	RS706-2.63YK	-40°C ~+125°C	SOIC-8(SOP8)	RS706B	Tape and Reel,4000
	RS706-2.93YK	-40°C ~+125°C	SOIC-8(SOP8)	RS706C	Tape and Reel,4000
	RS706-3.08YK	-40°C ~+125°C	SOIC-8(SOP8)	RS706D	Tape and Reel,4000
	RS706-4.00YK	-40°C ~+125°C	SOIC-8(SOP8)	RS706E	Tape and Reel,4000

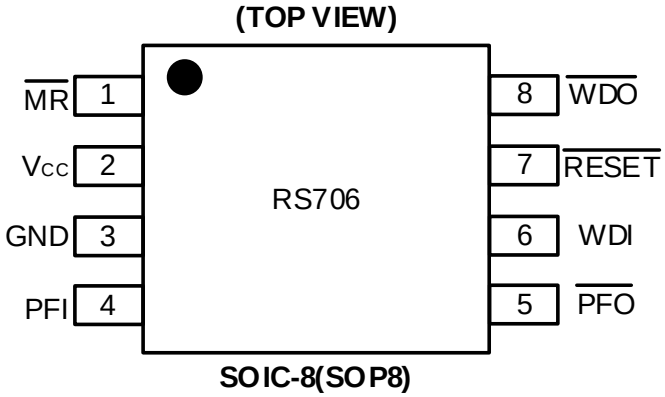
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information(data code and vendor code)，the logo or the environmental category on the device.

(3) B, C, D, E, represents different Reset Thresholds.

7 PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
SOIC-8(SOP8)		
1	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal pull-up resistance. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	V_{CC}	Power Supply Voltage that is monitored.
3	GND	Ground, reference for all signals.
4	PFI	Power-Fail Volta Monitor Input. When PFI is less than 1.2V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} if not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.2V; Otherwise $\overline{PFO}$ stays high.
6	WDI	Watchdog Input. If WDI remains high or low 1.6sec, the internal watchdog timer runs out and WDO goes low. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
7	$\overline{RESET}$	Active-Low Reset Output pulses low for 160ms when triggered, and stays low whenever VCC is below the reset threshold. It remains low for 160ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer finishes, its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay.

8 Specifications

8.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.0	V
V_I	Input voltage range (2)		-0.5	6.0	V
Vo	Voltage range applied to any output in the high-impedance or power-off state(2)		-0.5	6.0	V
Vo	Voltage range applied to any output in the high or low state (2)(3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-20	mA
I_{OK}	Output clamp current	V_O<0		-20	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±20	mA
T_J	Junction temperature (4)		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C
T_A	Operating temperature		-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions table*.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
	Machine model (MM)	±300	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Thermal Information:

THERMAL METRIC (1)		RS706 8PINS SOIC-8(SOP8)	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	124.7	°C/W
$R_{\Theta JC(top)}$	Junction-to-case(top) thermal resistance	66.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	67.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) Thermal resistance varies with operating conditions.

8.4 ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.67V to 5.5V for RS706-1.63; V_{CC} = 2.7V to 5.5V for RS706-2.63; V_{CC} = 3V to 5.5V for RS706-2.93; V_{CC} = 3.16V to 5.5V for RS706-3.08; V_{CC} = 4.1V to 5.5V for RS706-4.00; V_{CC} = 4.51V to 5.5V for RS706-4.40; V_{CC} = 4.77V to 5.5V for RS706-4.65; T_A = -40°C to +125°C, unless otherwise noted, typical at 25°C.) (1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{CC}		1.0		5.5	V
Supply Current	I_{SUPPLY}			20	40	μA
Reset Threshold	V_{RT}	RS706-2.63	2.56	2.63	2.7	V
		RS706-2.93	2.86	2.93	3.0	
		RS706-3.08	3.0	3.08	3.16	
		RS706-4.00	3.9	4.0	4.1	
Reset Threshold Hysteresis		RS706-2.63		12		mV
		RS706-2.93		14		
		RS706-3.08		15		
		RS706-4.00		20		
Reset Pulse Width	t_{RS}		100	160	350	ms
V_{CC} to $\overline{RESET}$ delay	t_{RD}	V_{CC}=3.3V, RS706-2.93		20		μs
Watchdog Timeout Period	t_{WD}		1.0	1.6	2.9	s
WDI Pulse Width	t_{WP}	V_{IL}=0.4V, V_{IH}=V_{CC}	16			ns
$\overline{RESET}$ Output voltage	High	I_{SOURCE} = 500uA	0.7xV_{CC}			V
	Low	I_{SINK} = 1.2mA			0.4	
WDI Input Threshold	High	V_{CC}=5.0V	4.0			V
	Low	V_{CC}=5.0V			0.8	
	High	$V_{RST(MAX)}$ < V_{CC} < 3.6V	0.8xV_{CC}			
	Low	$V_{RST(MAX)}$ < V_{CC} < 3.6V			0.6	
WDI Input Current		WDI = V_{CC}		0.1	1	μA
		WDI = 0V	-1	-0.1		
$\overline{WDO}$ Output Voltage	High	I_{SOURCE} = 800uA	0.7xV_{CC}			V
	Low	I_{SINK} = 1.2mA			0.4	
$\overline{MR}$ Pull-Up Resistor			20	52	120	kΩ
$\overline{MR}$ Pulse Width	t_{MR}		150			ns
$\overline{MR}$ Input Threshold	High	V_{CC}=5.0V	4.0			V
	Low	V_{CC}=5.0V			0.6	
	High	$V_{RST(MAX)}$ < V_{CC} < 3.6V	0.8xV_{CC}			
	Low	$V_{RST(MAX)}$ < V_{CC} < 3.6V			0.15xV_{CC}	
$\overline{MR}$ to Reset Out Delay	t_{MD}			23	200	ns
PFI Input Threshold		V_{CC} = 5.0V	1.14	1.20	1.26	V
PFI Input Current			-10	0.01	10	nA
$\overline{PFO}$ Output Voltage	High	I_{SOURCE} = 800uA	0.7xV_{CC}			V
	Low	I_{SINK} = 1.2mA			0.4	

8.5 Typical Operating Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

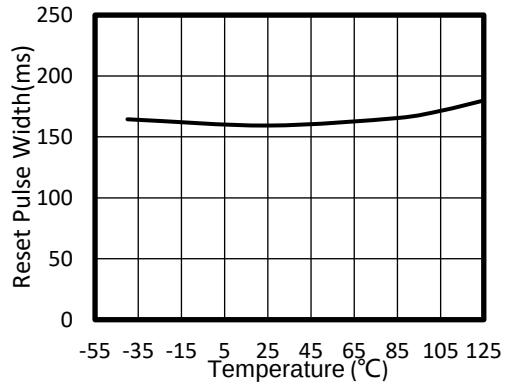


Figure 1. Reset Pulse Width vs Temperature

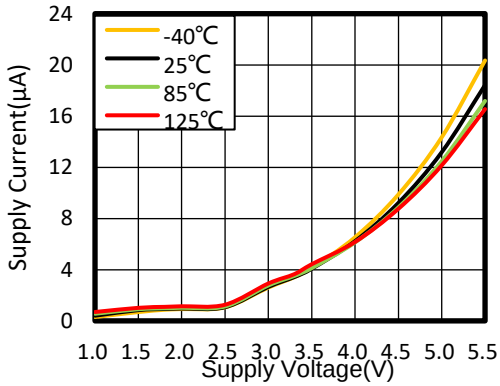


Figure 2. Supply Voltage vs Supply Current

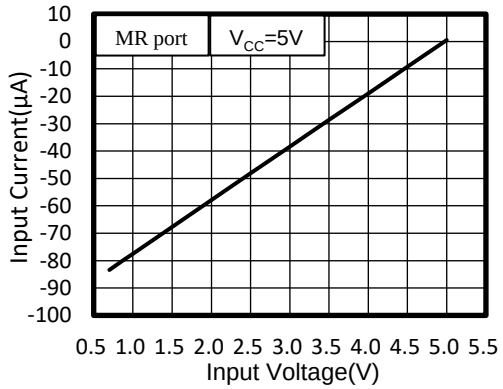


Figure 3. Input Voltage vs Input Current

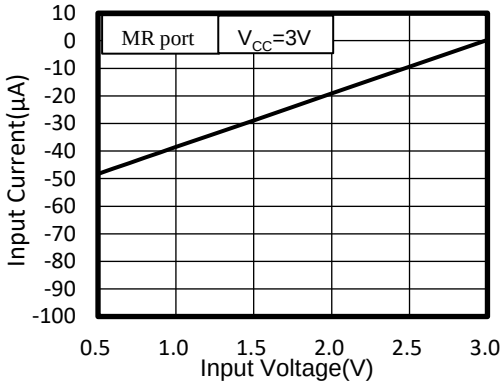


Figure 4. Input Voltage vs Input Current

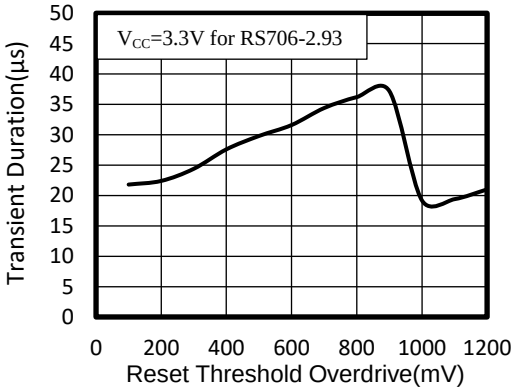


Figure 5. Transient Duration vs Reset Threshold Overdrive

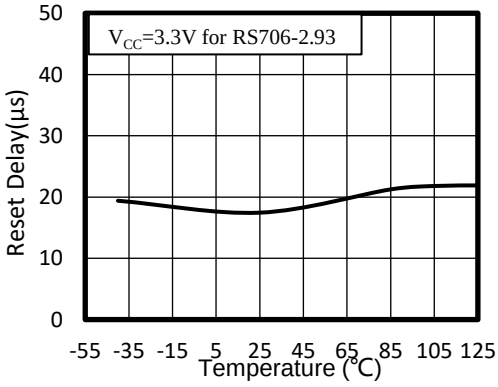


Figure 6. Reset Delay vs Temperature

Typical Operating Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

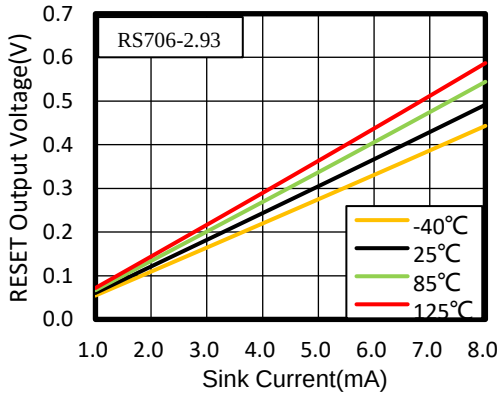


Figure 7. RESET Output Voltage vs Sink Current

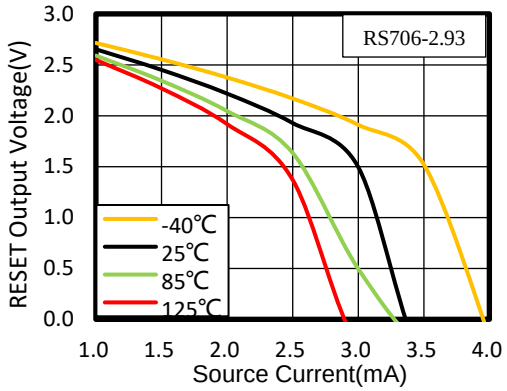


Figure 8. RESET Output Voltage vs Source Current

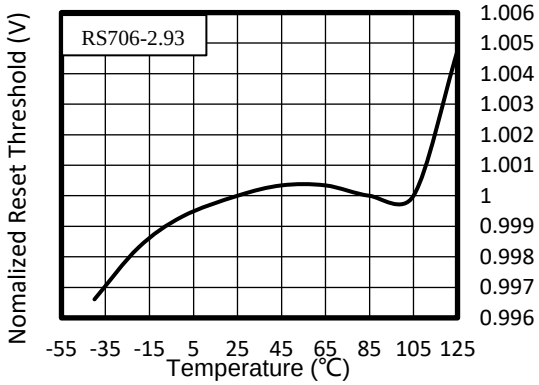


Figure 9. Normalized Reset Threshold vs Temperature

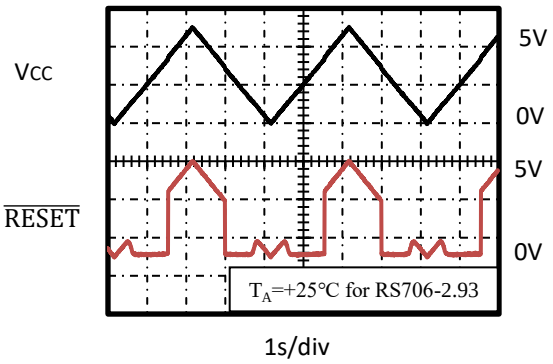


Figure 10. RESET Output Voltage vs Supply Voltage

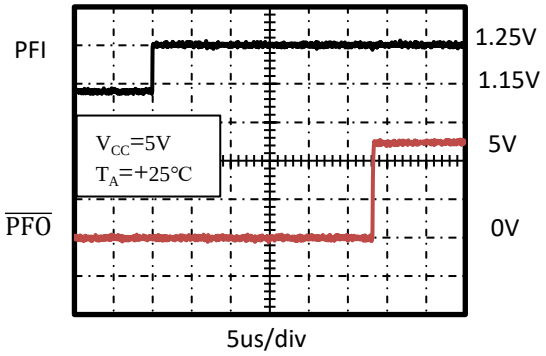


Figure 11. Power-Fail Comparator De-assertion Response Time

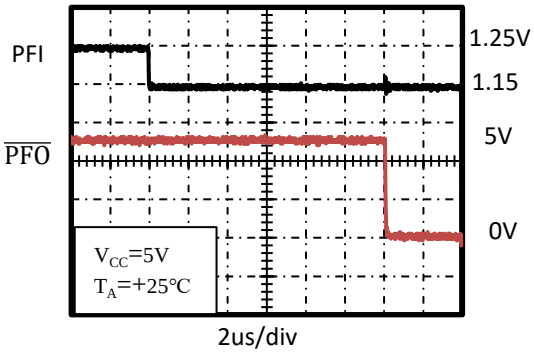


Figure 12. Power-Fail Comparator Assertion Response Time

Typical Operating Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

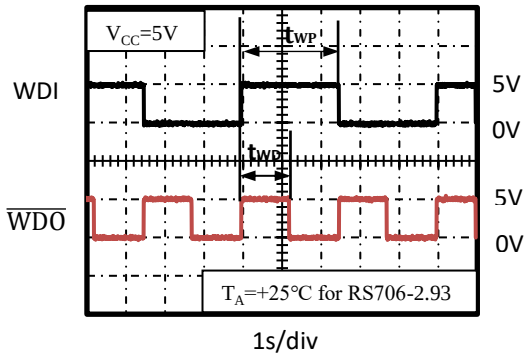


Figure 13. Watchdog Timing

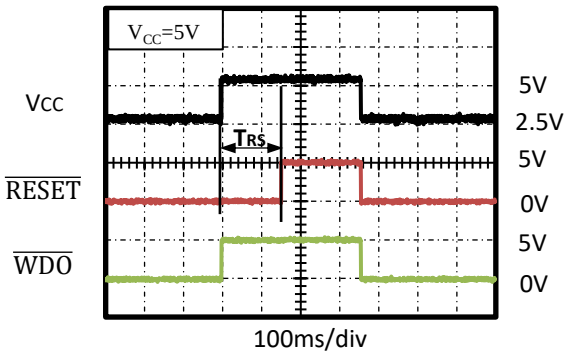


Figure 14. RESET and WDO Timing

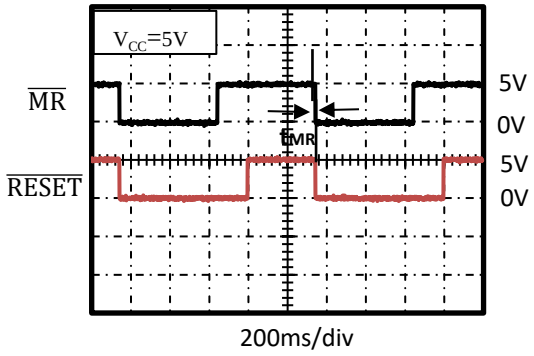


Figure 15. RESET Timing

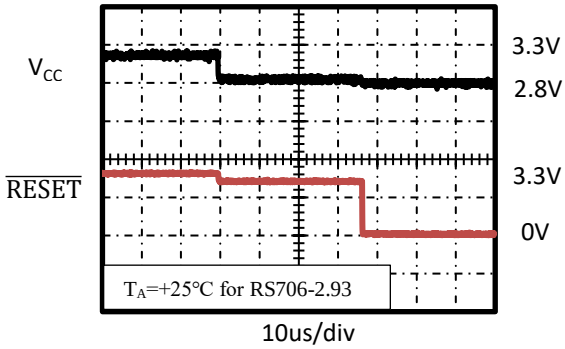
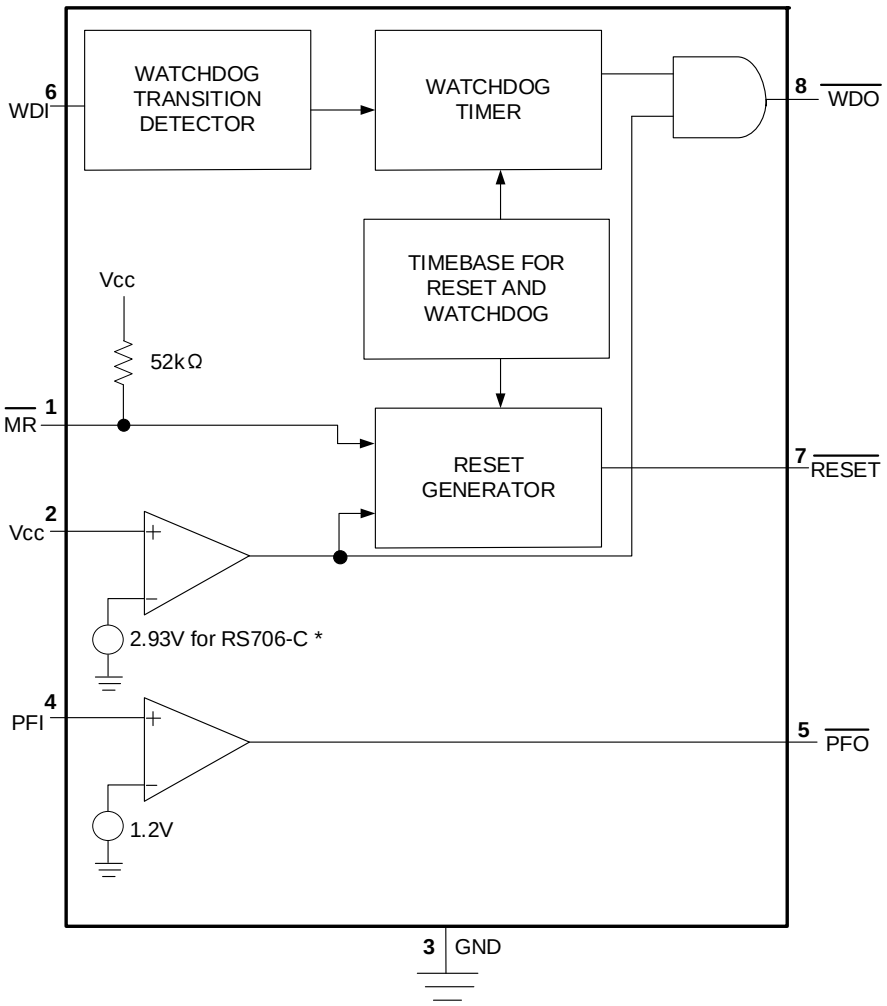


Figure 16. RESET Response Time

9 Function Block Diagram



2.63V for RS706-B
* 2.93V for RS706-C
3.08V for RS706-D
4.00V for RS706-E

10 Detailed Description

10.1 Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The RS706 assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1.0V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. When V_{CC} rises above the reset threshold, an internal timer release $\overline{RESET}$ after about 160ms. $\overline{RESET}$ pulses low whenever V_{CC} dips below the reset threshold. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 100ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less until V_{CC} drops below 1.0V.

10.2 Watchdog Timer

The RS706 watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6 sec (Minimum is 1.0 sec) and WDI is not three stated, $\overline{WDO}$ goes low. As long as $\overline{RESET}$ is asserted or the WDI input is three stated, the watchdog timer stays cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer starts counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ is not connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ goes low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI interrupt.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disable the internal timer, $\overline{WDO}$ goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

10.3 Manual Reset

The manual-reset input ($\overline{MR}$) allows reset to be triggered by a push-button switch. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in the RS706. Simply connect $\overline{WDO}$ to $\overline{MR}$.

10.4 Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and non-inverting input are not internally connected. The inverting input is internally connected to a 1.2V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider. Choose the voltage divider ratio so that the voltage at PFI falls below 1.2V just before the 5V regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down.

11 Applications Information

11.1 Ensuring a Valid RESET Output Down to V_{CC}=0V

When V_{CC} falls down below 1V, the RS706 $\overline{RESET}$ output no longer sinks current, it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left un-driven. If a pull-down resistor is added to the $\overline{RESET}$ pin, as shown in Figure 17, any stray charge or leakage currents will be drained to ground, holding $\overline{RESET}$ low. Resistor value (R1) is not critical. It should be about 100KΩ , large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

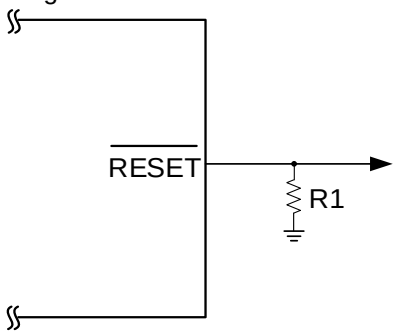


Figure 17. RESET Valid to Ground Circuit

11.2 Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage-divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND reduces the power - fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{RESET}$ can be asserted on other voltages in addition to the 5V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a $\overline{RESET}$ pulse when PFI drops below 1.2V. Figure 18 shows the RS706 configured to assert $\overline{RESET}$ when the 5V supply falls below the reset threshold, or when the 12V supply falls below approximately 11V.

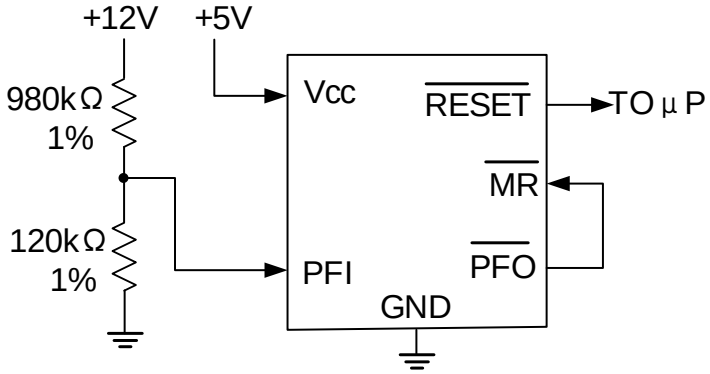


Figure 18. Monitoring Both 5V and 12V

11.3 Interfacing to μPs with Bidirectional Reset Pins

μPs with bidirectional reset pins, can contend with the RS706 $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the μP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor between the $\overline{RESET}$ output and the μP reset I/O, as in Figure 19. Buffer the $\overline{RESET}$ output to other system components.

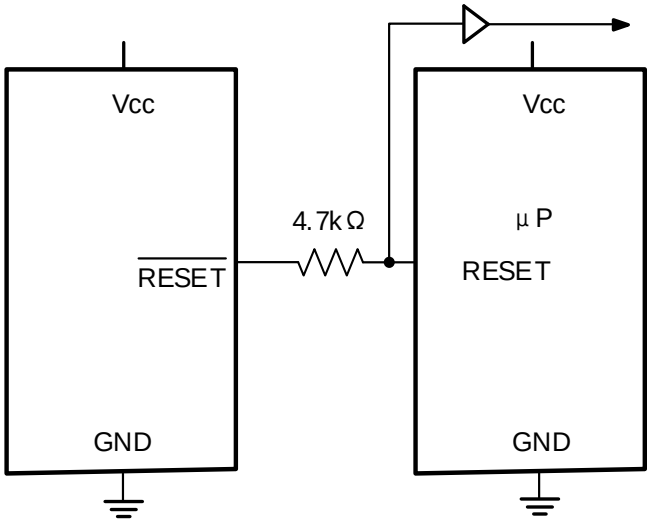
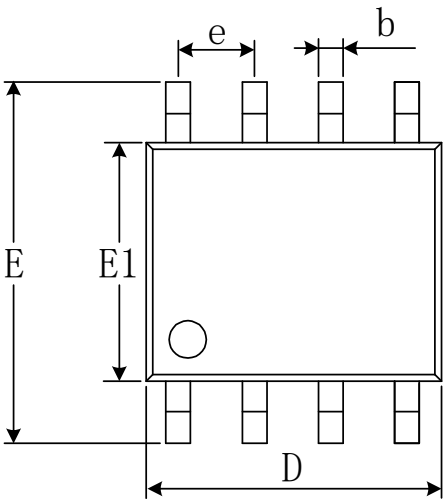
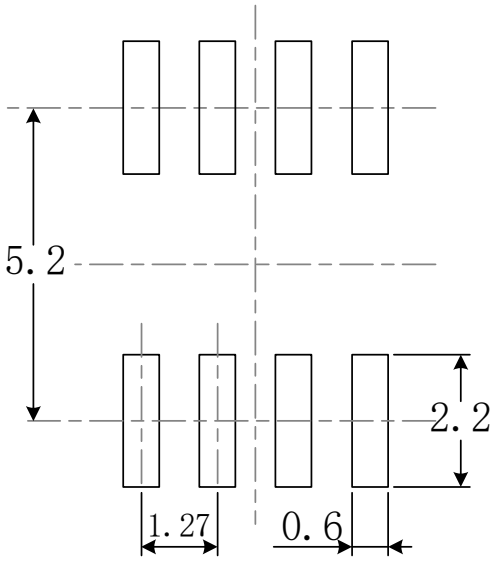


Figure 19. Buffered $\overline{\text{RESET}}$ to other system components

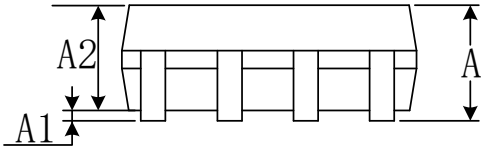
12 PACKAGE OUTLINE DIMENSIONS

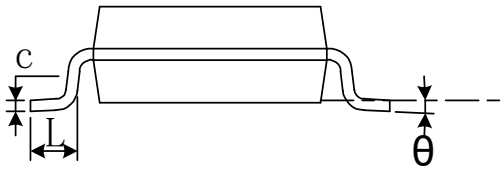
SOIC-8(SOP8)





RECOMMENDED LAND PATTERN (Unit: mm)





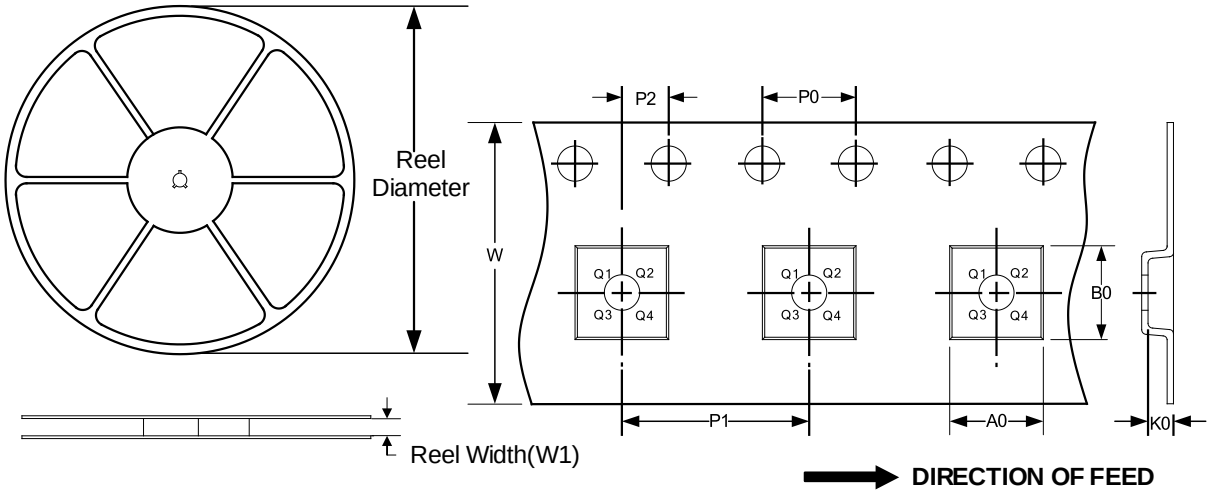
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

A. All linear dimension is in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8(SOP8)	13"	12.4	6.4	5.4	2.1	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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