RSC-300/364
Speech Recognition Microcontroller

DATA SHEET

General Description

The RSC-300/364, from the Interactive Speech ™ family of products, is designed specifically for speech applications in consumer electronic products.

The RSC-300/364 combines an 8-bit processor with neural-net algorithms to provide high-quality speaker-independent speech recognition, speaker-dependent speech recognition, and speaker verification. The chip also supports speech synthesis, voice record/playback, 4-voice music synthesis, and system control. This CMOS device includes on-chip RAM, ROM (RSC-364 only), 16 general-purpose I/O lines, A/D and D/A converters, a microphone pre-amplifier, and a 4-MIPS dedicated processor. The RSC-300 is designed for ROM-less applications that need more ROM space and consequently use off-chip memory.

In addition to providing the horsepower needed to perform speech recognition and speech synthesis, the processor has sufficient cycles available for general-purpose product control. The RSC-300/364 Development Kit allows developers to create custom applications. The Development Kit includes an assembler, linker, simulator, hardware development platform, and library of Sensory technology object code.

The highly integrated nature of this chip reduces external parts count. A complete system may be built with only a few passive components in addition to a battery, speaker, and microphone. Low power requirements and low-voltage operation make the RSC-300/364 an ideal solution for battery-powered and hand-held devices.

The RSC-300/364 uses a pre-trained neural network to perform speaker-independent speech recognition, while high-quality speech synthesis is achieved using a time-domain compression scheme that improves on conventional ADPCM. Four-voice music synthesis allows multiple, simultaneous instruments for harmonizing. Automatic Gain Control can compensate for people not optimally positioned with respect to the microphone or for people who speak too softly or loudly.

Features

High-Performance Processor

- 4-MIPS performance at 14.32 MHz
- 16 general purpose I/O lines
- Interrupts, timers and counters
- Fully static operation; clock rate: DC to 14.32 MHz

Highly-Integrated Single-Chip Solution

- Internal 64 kB of ROM (364 only), 2.5 kB of RAM
- 12 bit A/D (Analog to Digital) converter
- Microphone Pre-amplifier
- Internal 32kHz secondary timer
- 24 x 24 Multiplier
- Can store 6 Speaker Dependent words on-chip

Low Power Requirements

- Requires single 2.85V to 5.25V power supply
- ~10mA operating current at 3V
- Low Power 32kHz oscillator
- Power-down current less than 5 μA

High-Quality Recognition and Synthesis

- Recognition accuracy: better than 97% (Speaker Independent) and 99% (Speaker Dependent).
- Synthesis data rates from 5,000-15,000 bits per second
- 4-voice music synthesis capabilities
- AGC control compensates for variations in input signal

Easily Expanded to Larger-Scale Systems

- Separate 16-bit Address and 8-bit Data buses compatible with common memory components
- Separate Code and Data address spaces and memory strobes

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Introduction

The RSC-300/364 is the newest member in a family of high-performance 8-bit microprocessors featuring a high level of integration, targeted to high-accuracy, low-cost speech recognition applications. The RSC-300/364 is designed to bring accuracy, fast response time and versatility to low-cost, power-sensitive consumer applications.

A design goal of the RSC-300/364 was to reduce total system cost while increasing system performance. By including microphone signal amplification, data conversion, recognition and synthesis functionality, and ROM storage (RSC-364 only) with a CPU core on a single chip, dramatic cost and power reductions are achieved. Thus, the RSC-300/364 is able to provide 4 MIPS of integer performance at 14.32 MHz. This allows customer applications to achieve maximum performance at minimum cost.

The CPU core embedded in the RSC-300/364 is an 8-bit, variable-length-instruction, microprocessor. The instruction set is most similar to the 8051 family of microcontrollers. The RSC-300/364 processor avoids the limitations of dedicated registers by having completely symmetrical source and destinations for all instructions. Of the 2.5 Kbytes of internal SRAM, 2 Kbytes are organized as a Data Space, and 0.5 Kbytes is for register space. All arithmetic operation instructions may be applied to any register. Any pair of adjacent registers (at an even address) may be used as the 16-bit pointer to either the source or destination for a data movement instruction. Instruction classes allow the pointer to access internal or external Code Space, internal Register Space, or external Data Space.

Architecturally, the RSC-300/364's separate data and address buses allow use of standard EPROMs, ROMs, and SRAMs with little or no additional decoding. Provision for separate read and write signals for each external memory space further simplifies interfacing.

Creating applications using the RSC-300/364 requires the development of electronic circuitry, software code, and speech/music data files ("linguistics"). This document provides detailed information on those aspects of the RSC-300/364 architecture that are important to product designers and programmers. It describes the physical interface to the chip, printed circuit board layout and other design considerations, the RSC-300/364's instruction set, and memory organization. Refer to the RSC-300/364 Development Kit Manual for information on using Sensory's technology code for speech recognition, speaker verification, speech synthesis, and voice record and playback. Description of vocabulary development ("linguistics") information is beyond the scope of this document and is covered in a Design Note.

Custom Mask Capabilities of the RSC-364

The RSC-300 provides significant and flexible expansion capabilities through the use of external RAM or ROM Products using the custom-mask version of the chip, the RSC-364, may save considerable per-unit cost by avoiding the need for other active devices. The RSC-300 requires an external Code Space ROM memory to contain the program instructions, synthesis data, and Speaker Independent recognition weights. The custom-masked RSC-364 with no additional external memory devices must rely on the fixed internal memory for all of its ROM and RAM requirements. The internal ROM in the RSC-364 is application specific, with the amount available for user applications decreasing as the number of synthesis words or other technology usage increases.

These finite resources restrict the capabilities of products based on the RSC-364. The product specification for the RSC-364 must be carefully crafted in consultation with Sensory to maximize the use of on-chip memory. Each application will have its own specific limitations, but the table below summarizes some useful guidelines for planning purposes. Not all of the maximums can be achieved in a single custom-masked RSC-364 design. For example, a recognition vocabulary of 40 words may limit the speech synthesis to substantially less than 25 seconds.

Note: The RSC-364 (Custom Mask) column assumes *no external memory*.

Description	RSC-300	RSC-364 (Custom Mask)[1]
Capabilities:		
Speaker independent (SI) recognition	✓	✓
Speaker dependent (SD) recognition	✓	**Limited**
Speech synthesis and special sound effects	✓	✓
Speaker verification	✓	✓
Four-voice music generation	✓	**Limited support**
Voice record and playback	✓	**Not supported**[6]
SI Recognition Capacity :		
Maximum number of words per recognition set[1]	**15**	**15**
Total recognition vocabulary size in words, all sets	**Unlimited**	**40 words**[3]
SD Recognition Capacity :		
Maximum number of words per recognition set[1]	**64**[2]	**6**[3]**/64**[4]
Total recognition vocabulary size in words, all sets	**Unlimited**	**6**[3]**/512**[4]
Speaker Verification Capacity :		
Number of speakers identified per set[1]	**64**[2]	**1**[3]**/64**[4]
Synthesized Speech Capacity:		
Maximum total length of all messages	**Unlimited**	**25 seconds**[3]
Music Synthesis Capacity		
Number of simultaneous independent musical voices	**4**	**4**
Number of musical octaves available	**2-4**[5]	**2**
Number of musical tunes available	**Unlimited**	**6**
Requirement for custom ROM masks:		
Custom-masked parts (RSC-364) are not stocked by Sensory	**No Internal ROM**	**Custom masked ROM required**

1. Software for the RSC-364 (Custom Masked) applications may be completely developed and verified using the RSC-300/364 Development Kit and an external 64K ROM memory before committing to an RSC-364 custom ROM mask.
2. Practical limitations to maintain accuracy above 95%.
3. Assumes the use of on-chip ROM/RAM only
4. Assumes external serial EEPROM memory.
5. Depends on choice of musical instrument.
6. Requires external storage for recordings.

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Rsc-300/364 Hardware Specifications

Architectural Overview of the RSC-300/364

The RSC-300/364 is a highly integrated device that combines:

- An 8-bit RISC microprocessor.
- On-chip ROM (64 Kbytes, RSC-364 only), Register RAM (448 bytes), Data RAM (2 Kbytes) and the ability to address off-chip RAM or ROM.
- Analog-to-digital converter, digital-to-analog converter, and a pulse width modulator.
- A microphone pre-amplifier

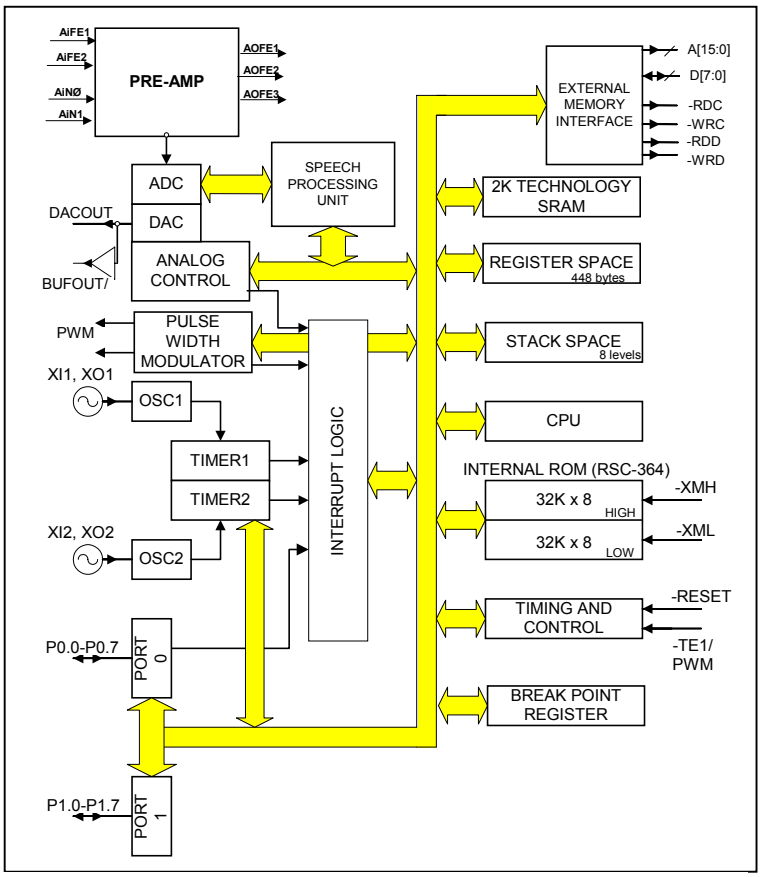

Figure 1 – **RSC-300/364 Block Diagram**

The RSC-300/364 has an external memory interface for accessing external RAMs, ROMs or other parallel memory devices. The RSC-364 also has an internal ROM that can be enabled or disabled (partially or fully) by pin inputs (signals -XMH, -XML; S*ee figure 4*).). When the internal ROM of the RSC-364 is disabled, its performance is identical to the RSC-300. With the RSC-364, the entire program must reside in the internal masked ROM. External memory can only be used to store data.

The 8-bit processor can directly access 448 on-chip general-purpose registers (RAM), and 32 additional Special Functions Registers (SFRs). The instruction set accessing these registers is completely symmetrical, allowing *mov*s, arithmetic, and logical operations with any register as the destination. Two bi-directional ports provide 16 general-purpose I/O pins to communicate with external devices *(See page 9)*. The RSC-300/364 has a high frequency (14.32 MHz) oscillator as well as a low frequency (32,768 Hz) oscillator. The processor clock can be selected from either source, with a selectable divider value. Sensory's technology code requires the use of the 14.32 MHz clock. There are two programmable 8-bit counters / timers, one derived from each oscillator. A variety of wait state configurations allow fast code execution and easy interfacing to slow peripheral memories.

An inexpensive electret microphone connects directly to the microphone input of the RSC-300/364. The internal preamplifier converts the tiny microphone signal to a level suitable for Analog-to-Digital Conversion. (ADC), The RSC-300/364 uses a Sample and Hold (SH) circuit and ADC converter to convert the amplified analog speech signal into digital data. The chip may also be used with line-level inputs. The output audio signal of the RSC-300/364 is derived either from a DAC (Digital-to-Analog Converter) or a PWM (Pulse Width Modulator).

In addition to its on-chip ROM (RSC-364 only) and RAM, the RSC-300/364 has 8 data lines (D[7:0]) and 16 address lines (A[15:0]), along with associated control signals (-RDC, -RDD, -WRC, -WRD, -XML, -XMH) for interfacing to external memory. The memory control signals on the RSC-300/364 and the processor instruction set provide independent Code and Data spaces, allowing configuration of systems up to 192 Kbytes with no additional hardware decoding. The RSC-300/364 features 16 general-purpose I/O pins (Px.y) for product and memory bank control.

Using the RSC-300/364

Creating applications using the RSC-300/364 requires the development of electronic circuitry, software code, and speech/music data files. Software code for the RSC-300/364 can be developed by Sensory or by external programmers using the RSC-300/364 Development Kit. For more information about development tools and services, please contact Sensory, or visit **www.SensoryInc.com**. A typical product will require about $0.30 - $1.00 (in high volume) of additional components, in addition to the RSC-300/364.

The following sample circuit provides an example of how the RSC-300/364 might be used in a low volume consumer electronic product. The external ROM contains the application program, recognition weights, and speech data. A high volume application would likely use an RSC-364 (custom-masked ROM), and would not require the separate ROM.

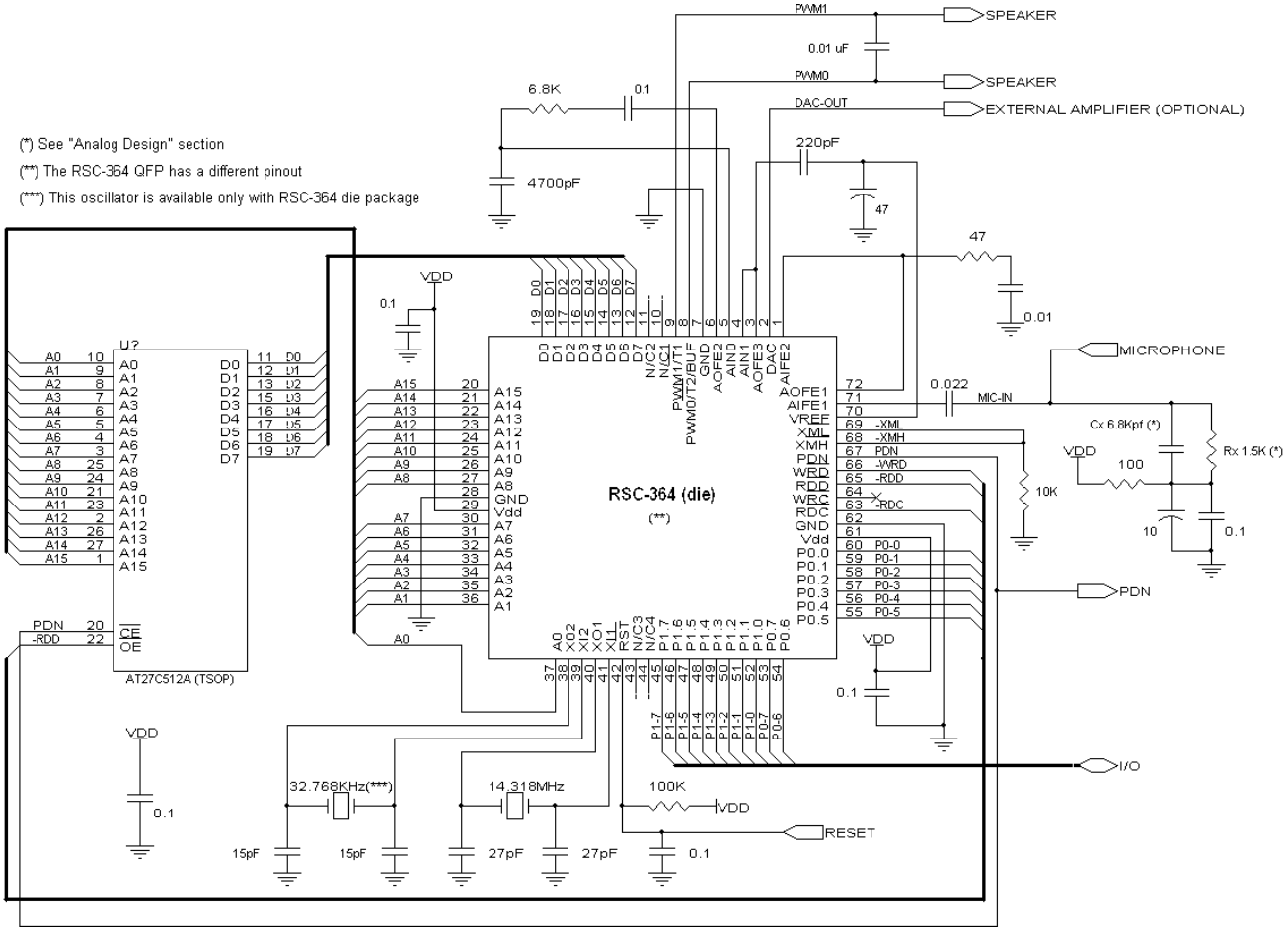

Figure 2 – **Reference Circuit**

Note: Applications using the PWM output may not meet FCC or CE (such as EN55022 Class A or B) standards for radiated emissions. For applications that must meet these standards, Sensory recommends turning off the PWM in the application software, and using an external audio power amplifier connected to the DAC output. Please refer to Sensory's Application Note 80-0105 "DAC Output" for sample circuits and design guidelines.

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Memory Organization

Internal ROM Memory (RSC-364 only)

Internal ROM is organized as two banks of 32 Kbytes each, both mapped into code space. Either of the two internal banks may be independently disabled using external inputs; input pin -XML disables the lower 32K [0000h-7FFFh] bank, while input pin -XMH disables the upper 32K [8000h-FFFFh] bank. When a bank is disabled, read accesses to it are directed to off-chip code space. In most applications the -XML and -XMH signals will both be grounded (for use with external ROM program memory) or both will be left floating (to use internal ROM memory for program memory). Write accesses to the code space are directed to external memory off-chip. Except for specific addresses in the last page of memory (described on page 8), read and write accesses to data space are always directed to external memory.

External Memory

The RSC-300/364 allows for extended message lengths and expanded program functionality by using external memory. There are 30 pins that provide an interface between the RSC-300/364 and external ROM or RAM. The 16 address line outputs, A[15:0], are shared for accesses to external code space or data space. The 8 data lines, D[7:0], are bi-directional, and are normally inputs except when there is a write to external memory. Refer to *MEMORY MAP* (on page 8) for details on accessing external code and data spaces through *movc* and *movx* instructions.

The RSC-300/364 uses the -RDC, -WRC, -RDD and -WRD signals to strobe data to or from memory or I/O devices. The -RDC and -WRC strobes are provided for accessing code space, while the -RDD and -WRD strobes are used to access data space. These four memory strobes are all active low (see page 25 for timing information). Using these strobes, the RSC-300/364 can directly access 64K of external code space (either internal or external) and 64K of external data space. External memory and I/O devices can reside in code space (RSC-300 only) or data space, as determined by the user application. Executable code *must* reside in code space; tables and other data may reside in code space or data space. Using I/O bits, additional external decoding can be used to bank select between multiple RAMs or ROMs. This method allows for external Data Space storage requirements larger than the combined 128K addressed directly by the RSC-300/364. Figure 3 below illustrates a typical large Data Space ROM-only memory configuration. The lowest 64K bank is addressed as Code Space, and the other 7 banks are addressed as Data Space. The ROM is selected by both -RDD and -RDC. Additional logic may be required to use both ROM and RAM/Flash in external Data Space.

Sensory's RSC-300/364 technology code requires code execution at 14.3 MHz with one wait state. External ROM Code memory speeds should be 120 nS or faster. External Data Space access speed may be independently controlled by the insertion of additional wait states for *movx* instructions, simplifying access to slow read/write devices.

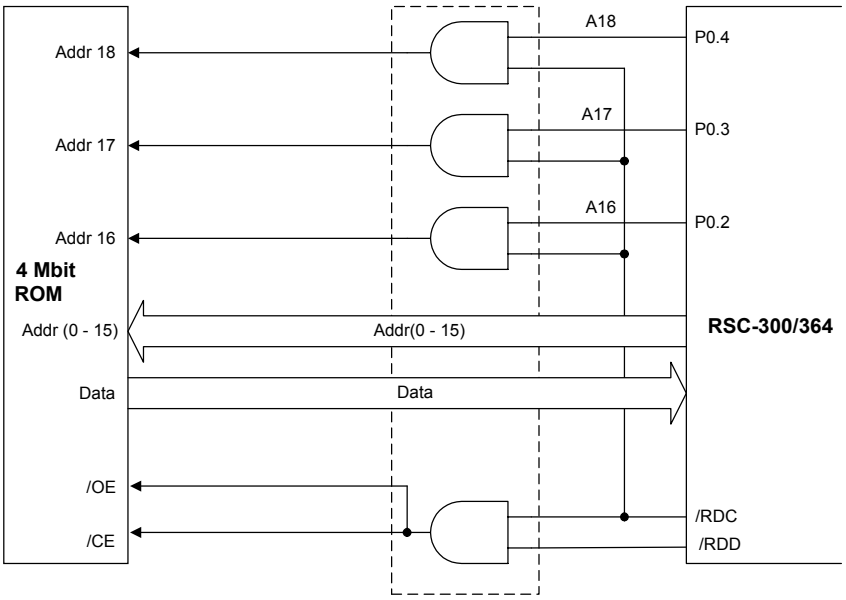

Figure 3 -- **Large ROM Decoding**

Memory Map

The RSC-300/364 has three address spaces: Code Space, Data Space, and Register Space. Code space is typically ROM. Data space may be ROM, RAM, Flash, or other parallel read/write memories. Register space is limited to on-chip SRAM. The instruction set provides separate instructions for accessing each space. Executable code *must* reside in code space; tables and other data may reside in code space or data space. Register space is intended primarily for variables.

The internal ROM (RSC-364 only) and off-chip code space memory (RSC-300 only) may be accessed using *movc* instructions. The off-chip data space is accessed using *movx* instructions, while the on-chip register space is accessed using *mov* instructions. Writes to code space are always directed off-chip.

The internal ROM (RSC-364 only) is organized as two code space banks of 32 Kbytes each. The banks can be independently disabled using external inputs: the low bank (address range 0000h-7FFFh) can be disabled by asserting pin input -XML while the high bank (address range 8000h-FFFFh) can be disabled by asserting pin input -XMH. This feature may be used to expand External addressable code space beyond 64 Kbytes.

The SRAM register space supports 8-bit addresses, so only 256 bytes may be directly addressed. General-purpose registers are located between addresses 000h and 0BFh. A 32-byte bank of SFRs (special function registers) resides at addresses 0E0h-0FFh. The 32-byte bank at addresses 0C0h-0DFh may be mapped to any of the six lower 32-byte banks in page 0 (addresses 000h through 0BFh), or to eight additional 32-byte banks in page 1 (addresses 100h-1FFh. A special function register controls this mapping, providing a total of 448 bytes of SRAM register space. The RSC-300/364 also contains 2 Kbytes of internal data space RAM that is reserved for technology use.

Off-chip memory (and memory-mapped I/O) is accessed using a 16-bit address bus and an 8-bit data bus. Separate read / write strobes are generated for access to external code and data spaces. This allows the RSC-300/364 to directly access 64 Kbytes of external code memory and 64 Kbytes of external data memory. Bank switching is commonly implemented using I/O pins to select additional off-chip memory.
Certain addresses in the range of 0FF00h-0FFFFh of Data Space are mapped internally, so addresses in this last page of data space are not generally accessible.
The RSC-300/364 allows software to adjust the speed of off-chip memory access. This allows using fast memory for performance needs or (if feasible) slower memory for cost savings. The off-chip memory access time can be stretched using wait states defined by the BANK register, and the software can dynamically change the wait state value depending on the particular memory or I/O peripheral. Wait states for external Data Space may be selected independently of Code Space wait states.

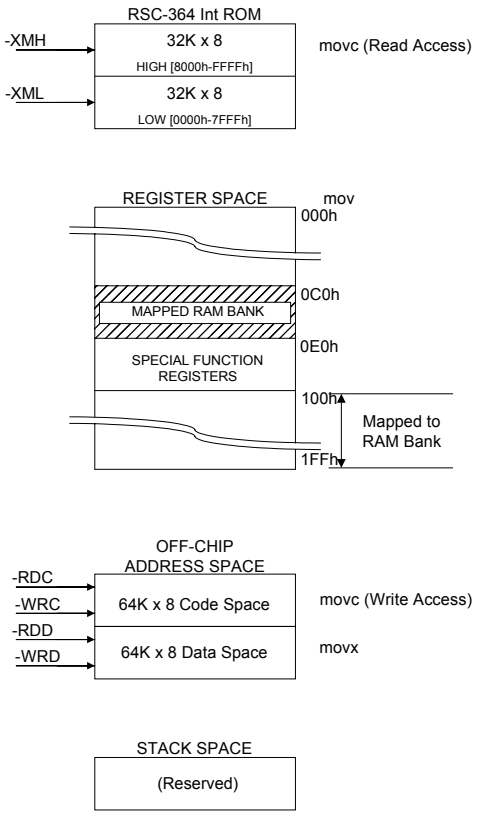

Figure 4 -- **Memory Map**

There is modest stack space on chip. The stack is required for interrupts and allows a limited number of nested calls. Programmers are encouraged to write inline code instead of making deeply-nested subroutine calls. The RSC-300/364 offers limited support for a software stack to allow more deeply nested calls or to store parameters, although this is not usually required. Macros using this software stack are accessible to developers.

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General Purpose I/O

The RSC-300/364 has 16 general-purpose I/O pins (P0.0-P0.7, P1.0-P1.7). Each pin can be programmed as an input with weak pull-up (~200KΩ equivalent device); input with strong pull-up (~10KΩ equivalent device); input without pull-up, or as an output. This is accomplished by having 32 bits of configuration registers for the I/O pins (Port Control Register A and Port Control Register B for ports 0 and 1). *(See page 24)*

After reset, all of the I/O pins are set to be inputs with weak pull-ups. Designers may make use of this start-up feature to assure enabling or disabling of particular functions controlled by I/O pins.

For electrical specifications regarding the general purpose I/O pins, please refer to D.C. Characteristics. All I/O pins are diode clamped to V_{DD} and ground, and are capable of sinking up to 200 mA if V_{DD} is exceeded.

In addition to providing general purpose I/O, port 0 bit P0.0 can serve as an interrupt input (using IMR and IRQ registers). Any I/O pin may be used as a "wakeup" event when the chip is in "sleep" mode.

Typically some of the I/O pins may be used for extended address bits in larger systems having more than 64K of memory. This may be done by connecting port pins directly to Address bit 16 and higher pins of large memory devices.

Interrupts

The RSC-300/364 allows for six interrupt sources, as selected by software. Each has its own mask bit and request bit in the IMR and IRQ registers respectively. The global interrupt enable flag, which enables or disables all interrupts, is located in the FLAGS registers. Bit assignments for the IMR and IRQ registers are listed on page 34. The following events can generate interrupts:

- Positive edge on Port 0, bit 0
- Overflow of Timer 1
- Overflow of Timer 2
- Two Sensory Proprietary functions
- Completion of PWM sample period

Note: If an interrupt occurs while the GIE bit is being cleared, the GIE bit may be restored to an enabled state upon return from the Interrupt Service Routine. Use the CLIx macro (supplied with the Sensory Speech 6 Technology library software) in place of the CLI instruction to assure that interrupts are globally disabled before proceeding.

If an IRQ bit is set high and the corresponding IMR bit is set high and the global interrupt enable bit is set high, an interrupt will occur. Interrupts cannot be nested. The flags register is copied to a holding register and then the global interrupt enable is cleared, preventing subsequent interrupts until the IRET instruction is executed. The IRET instruction will restore the flags register from the holding register.

If the corresponding mask register bit is clear, the IRQ bit will not cause an interrupt. However, it can be polled by reading the IRQ register. IRQ bits can be cleared by writing a 0 to the corresponding bit at address 0FEh (the IRQ register). IRQ bits can *not* be set by writing to 0FEh. Writing a one is a no-op.

The IRQ bits must be cleared within the interrupt handler by an explicit write to the IRQ register rather than by an implicit interrupt acknowledge. Important: clear interrupts this way:

```
mov IRQ, #BITMASK     ; right
```

not this way:

```
and IRQ, #BITMASK     ; wrong
```

The 'and' instruction is not atomic, it is a read-modify-write. If an interrupt occurs during an 'and IRQ' operation the interrupt will be cleared before it is seen, possibly disabling the interrupt until the system is reset.
Because you cannot set bits in the IRQ register, a 'mov IRQ' is a safe, effective, and atomic way to clear bits in the IRQ register. Use it the way you would use an 'and' in other registers.

Note: If Port 0.0 (the external IRQ) is set as an *output*, the external IRQ flag will be set if the output is driven from 0 to 1 under program control.

For each interrupt, execution begins at a different code space address:

Interrupt #0	Address 4
Interrupt #1	Address 8
Interrupt #2	Address 0Ch
Interrupt #3	Address 10h
Interrupt #4	Address 14h
Interrupt #5	Address 18h

Normally the instruction at the interrupt address is a jump to an Interrupt Service Routine (ISR). This jump is called a *vector*. The vectors located at each of these addresses are typically in ROM.

Reset and Clocks

Reset

The reset pin, -RESET, is an active low Schmitt trigger input. The reset pin is provided with hysteresis in order to facilitate power-on reset generation via an RC network. Reset is held internally for 10 msec after the -RESET input signal is de-asserted. This allows the oscillator to stabilize before enabling other processor subsystems. The -RESET signal must be asserted for a minimum of 2 clock periods.

Oscillators

Two independent oscillators in the RSC-300/364 provide a high-frequency clock and a 32 kHz time-keeping clock. The oscillator characteristics are as follows:

Oscillator #1	Pins XI1 and XO1	14.32 MHz
Oscillator #2	Pins XI2 and XO2	32,768 Hz

Oscillator #1 works with an external crystal, a ceramic resonator, or LC. Use of Oscillator #2 requires a crystal for precise timekeeping.

Each oscillator has an enable control. When disabled, the inverter is high-impedance, and a weak pull-up device (~100 KΩ) holds the inverter output high. Both oscillators are controlled by the Clock Control Register (CPU register 0E8h). By default, Oscillator #1 is enabled by reset, while Oscillator #2 is disabled by reset. The effect of reset therefore requires that Oscillator #1 be functional in all designs. The Clock Control Register also determines internal division of the CPU clock source (see below).

Each oscillator has an associated timer that is fully programmable. The RSC-300/364 timers are described in the following section.

Processor Clock

The RSC-300/364 uses a fully static core; the processor can be stopped (by removing the clock source) and restarted without causing a reset or losing contents of internal registers. Static operation is guaranteed from DC to 14.32 MHz. The processor clock is selected from either the Oscillator #1 output (gated by wake-up 10 mS delay) or the Oscillator #2 output, based on bit 2 of the Clock Control Register. This bit is cleared by reset, which selects Oscillator #1. It is the responsibility of the firmware not to select Oscillator #2 until both oscillators have been enabled and stabilized.

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After source selection, the processor clock can be divided-down in order to limit power consumption. Bits 3 and 4 of the Clock Control Register determine the divisor for the processor clock. Between zero and seven wait states must also be selected for the processor clock. Wait states are inserted on reads or writes to all addresses except Register Space RAM and, under certain configurations, internal ROM (RSC-364 only).

Sensory technology code must run with a processor clock of 14.32 MHz, a clock divisor of one, and one wait state. This creates internal RAM cycles of 70 nsec duration and internal ROM (RSC-364 only) or external cycles of 140 nsec duration. Careful design of external decoding logic and close analysis of gate delays may allow operation with Code Space memories having 120 nsec access times. Additional wait states may be selected for external Data Space access.

Timers and Counters

The two independent oscillators of the RSC-300/364 provide counts to two internal timers. Each of the two timers consists of an 8-bit reload value register and an 8-bit up-counter. The reload register is readable and writeable by the processor. The counter is readable with precaution taken against a counter change in the middle of a read. If the processor writes to the counter, the data is ignored. Instead, the counter is preset to the reload register value. That is, *any* write to a counter will cause it to be reloaded. This is the usual way of initializing the counter. When the timer overflows from FF to 00, a pulse is generated that sets IRQ #0 (timer #1) or IRQ #1 (timer #2). If the corresponding IMR bit is set and the Global Interrupt Bit is set, an interrupt will be generated. Instead of overflowing to 00, the counter is automatically reloaded on each overflow.

For example, if the reload value is 0FAh, the counter will count as follows:

0FAh, 0FBh, 0FCh, 0FDh, 0FEh, 0FFh, 0FAh, 0FBh etc.

The overflow pulse is generated during the period *after* the counter value was 0FFh.

Timer #2 may be used as a wakeup when the processor has powered-down.

Refer to the following registers for more information about using timers and counters:

T1R: Timer 1 Reload Register (page 28)
T1V: Timer 1 Counter Register (page 28**)**
T2R: Timer 2 Reload Register (page 29)
T2V: Timer 2 Counter Register (page 29)

Power Down and Wake-Up Operation

The RSC-300/364 can be powered down through software by setting the PD bit (bit7) of the Clock Control Register *(See page 33)*. Setting this bit halts the processor until a “wakeup” event clears the bit. The instruction that causes the power down event may also set or clear other bits in the Clock Control Register to enable or disable any of the clocks, and to select a clock to be used as the processor clock upon wakeup. A wakeup event can be generated from either of two sources:

- bit transition(s) of port 0 or port 1 pins, or
- an overflow pulse from timer 2.

For low power consumption, oscillator #1 (bit 0) and the FC clock (bit 5) should always be disabled during power down. Oscillator #2 (bit 1) must be enabled if the wakeup condition is a timer 2 event. If the wakeup event is an IO pin event, all clocks should be disabled for lowest power consumption.

If oscillator #1 is disabled during power down, *and* the selected processor clock source is oscillator #1, then a wakeup event will require that oscillator #1 be started and stabilized before its output can be used as the processor clock. The oscillator is started when the wakeup event clears bit 0 of the Clock Control Register, but the processor clock is delayed by 10 milliseconds to assure stability.

If the RSC-300/364 is powered down with oscillator #2 selected as the processor clock source, a timer2 wakeup event does not require a delay because it is assumed that oscillator #2 is running and stable. Due to long startup time for oscillator #2, the RSC-300/364 should not be powered down with oscillator #2 disabled *and* selected as the processor clock.

A wakeup event does not cause a reset. The processor, which was “stopped-in-its-tracks” when the PD bit was set, is restarted without loss of context.

Analog Outputs

The RSC-300/364 offers two separate options for analog output. The DAC (Digital to Analog Converter) output provides a general-purpose 10-bit analog output that may be used for speech output (with the inclusion of an audio amplifier), or that may be used for other purposes requiring an analog waveform. Many speech applications may require only driving a small speaker, however, and cost can be saved in these applications by using the Pulse Width Modulator (PWM) outputs of the RSC-300/364 instead of the DAC output.

Special Note:

Applications using the PWM output may not meet FCC or CE (such as EN55022 Class A or B) standards for radiated emissions. For applications that must meet these standards, Sensory recommends turning off the PWM in the application software, and using an external audio power amplifier connected to the DAC output. Please refer to Sensory's Application Note 80-0105 "DAC Output" for sample circuits and design guidelines.

DAC Output

The digital-to-analog converter (DAC) provides its output through DACOUT, with an output impedance of 22KΩ. V_{DACOUT} can swing from 0V to V_{DD}. An external audio amplifier and optional volume control must be used to drive a speaker. Filtering above 5 kHz is recommended to provide the correct frequency response.

PWM Output

The two PWM outputs are designed for driving a 16-Ohm speaker at audio frequencies. These signals produce good quality audio with no additional components. These outputs are actually digital outputs that produce a series of high frequency pulses at varying rates that, when filtered by the mechanical dynamics of a speaker, create the effect of a continuously varying analog signal.

Although it is called a pulse *width* modulator, the RSC-300/364 actually incorporates a pulse *count* modulator: a programmable number of pulses is produced during each sample period. The two PWM outputs connect directly to the two speaker terminals. During operation, the first of the two signals will be at ground and the second will have a pulse train. The pulses will cause the speaker cone to push out (or pull in, depending on the wiring connections). If there are many pulses in a sample period, the speaker will push out a large amount; if there are few pulses, the speaker will push out just a little. Switching the pulse train to the first output and holding the second output at ground effectively reverses the polarity of the signals, so now the speaker will pull in. By controlling the number of pulses in each sample period and the output on which they appear, the speaker can be made to move in and out as required to reproduce an audio waveform.

The PWM0 pin is shared with the BUFOUT signal, and the PWM1 pin is shared with the -TE signal. At power-on, these pins are configured for non-PWM operation. The BUFOUT and -TE signals are both test signals that are typically not used during normal operation. When the Pulse Width Modulator is enabled via software, the pins are switched over to the PWM function. See page 36 for information about programming the PWM. Typically the PWM is controlled by Sensory library code, so there is little need for application programs to alter it.

Hardware Debug Features

Special debugging hardware has been incorporated into the RSC-300/364 to assist developers in producing code quickly. The specialized circuitry provides the following features:

- A 16-bit break register that holds one ROM breakpoint address
- A TRAP bit in the Flags register (Address 0FFh) that enables or disables the breakpoint.

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- A vector at 0FFF8h to which the processor is directed when the Program Counter equals the breakpoint address and the TRAP bit is enabled. The break occurs *before* execution of the instruction at the breakpoint address.
- A special page of Code Space (0FF00h-0FFFFh) for holding the resident debugger software. When this page is entered *via a break*, timers and interrupts are suspended. When execution resumes outside this page, timers and interrupts are restored. Entering this page by means other than a break has no special effect, and timers and interrupts continue to operate as normal.
- A vector at 0FFFCh to which the processor is directed if the -TE pin is held low at power-on. This provides a means for starting up in the debugger.

The debug circuitry, in conjunction with debug monitor software resident in the last page of Code ROM, allows examining the contents of Register, Code, and Data Space addresses. Register space contents may be modified, as may Data or External Code space addresses if implemented in a RSC-writeable device.

Additionally, the RSC-300/364 supports a 4-byte, bi-directional communication interface using external hardware registers. This interface provides one means for another computer to interact with the resident debug monitor.

Design Considerations

Speech recognition accuracy can be degraded by a number of factors. A common problem that causes accuracy degradation is noise: both electrical noise within the system and audio noise picked up by the microphone. A major innovation in the RSC-300/364 is the incorporation of an audio preamp circuit right on the chip. The signal from a typical electret microphone is of the order of a few millivolts, and an overall preamp gain of 200 or more is needed to make this signal useable by the RSC. The RSC-300/364 requires only a few external passive components to provide this amplification. Good grounding practice and elimination of crosstalk into the analog circuitry will further help ensure good recognition accuracy. Product design that encourages the user to speak loudly and close to the microphone helps attain a good signal-to-noise ratio.

Analog Design

The schematic in Figure 5 illustrates a reference input audio preamp design for use with the RSC-300/364. The microphone resistor (Rx) shown as 1.5K has a large influence on the system gain, so the value will depend on the sensitivity of the microphone. The value of 1.5K is typical.

Recommended value for Rx and Cx:

Rx	Cx
1K	0.01uF
1.5K	0.0068uF
2.2K	0.0047uF
2.7K	0.0033uF
3.9K	0.0027uF
4.7K	0.0022uF

Some applications may use the RSC-300/364 with input signals from a device other than an electret microphone. For assistance with such designs, contact Sensory.

PCB Design

A double-sided printed circuit board (PCB) with ground plane is

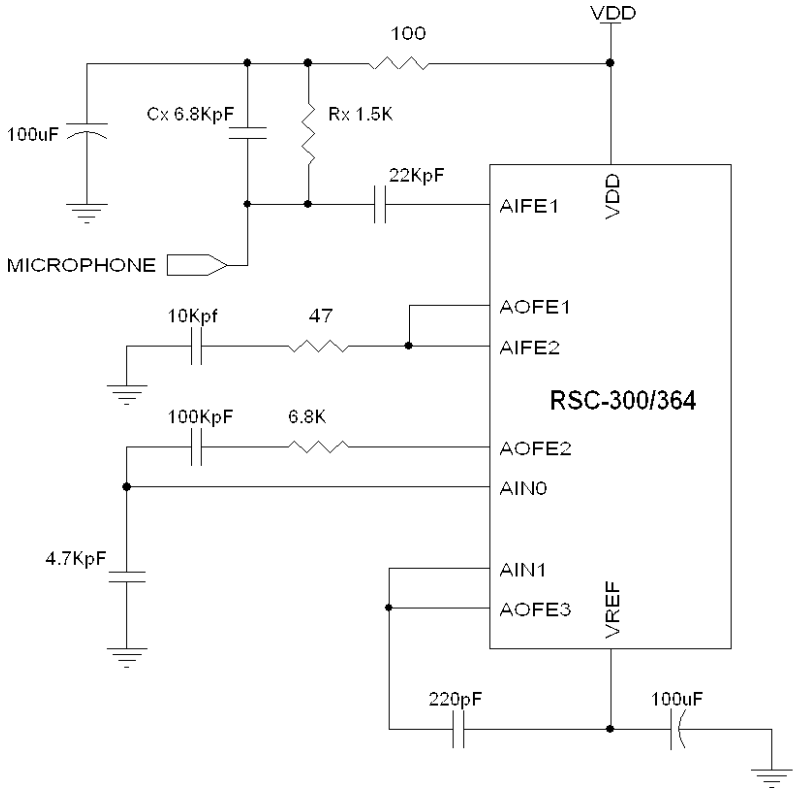

Figure 5 -- **Preamplifier Schematic**

recommended. The ground plane should cover the analog circuitry area and only be tied to ground near the RSC device. In order to reduce crosstalk, the analog and digital circuits should be physically separated as far as is practical. Take special care to keep high-speed clocked lines (e.g., address and data) away from the microphone components and traces.

A 0.1 µF bypass capacitor should be installed immediately next to each digital IC and near the V_{DD} pins of the RSC chip. The bypass capacitors should be stacked or monolithic ceramic type, rated at 50 volts. If a three-terminal voltage regulator (such as a 7805) is used, tantalum bypass capacitors should be connected close to the regulator between the input/output pins and ground.

In a practical application using replaceable AA or AAA batteries, incorporating a protection diode in series with the power supply will avoid damage to the circuit if batteries are inserted with the wrong polarity.
If the RSC is used in a system with other digital clocks (switching power supplies, LCD driver, etc.) take special care to prevent these signal from getting into the audio circuitry of the RSC.

Locating and Mounting the RSC-300/364
The RSC-300/364 is supplied as a bare, tested die or in a 64 lead, 10 x 10 x 1.0 mm TQFP package. The die form may be wire bonded directly to the main PCB or, in some cases, may be bonded to a separate chip-on-board (COB) circuit board. In production this COB assembly may be functionally tested, then attached to the main board as a working module.

There are several methods of attaching the COB to the main board, and a careful choice should be made by the designer. The RSC-300/364 is a 72-pad device requiring good attaching methodology for correct operation. Since cost is always a consideration, COB boards may often be designed as single-sided PCBs.

The simplest way of attaching a single-sided COB to a main board is to lay it, chip side up, on the main board and make solder bridges from the main board up along the thickness of the COB to the electrical contacts on the top of the COB board. In production this is not a reliable technique.

A second technique is to use wires or pins to connect thru-holes between the main board and the COB. This reliable technique may be more time consuming.

A third technique is to put a hole in the main board at the center of the COB location and to mount the COB to the main board UPSIDE DOWN, that is, with the chip facing down into the hole. Then the COB and main boards may be soldered together. In this case, the orientation of the signal leads of the RSC-300/364 is different from that of the other arrangements.

Omni-Directional Microphone

Selecting a Suitable Microphone

For most applications, an inexpensive omni-directional electret capacitor microphone with a minimum sensitivity of -60 dB is adequate. In some applications, a directional microphone might be more suitable if the signal comes from a different direction than the audio noise. Since directional microphones have a frequency response that depends on their distance from the sound source, such microphones should be used with caution. For best performance, speech recognition products should be used in a quiet environment with the speaker's mouth in close proximity to the microphone. If the product is intended for use in a noisy environment, care should be taken to design around the noise. Improving the signal-to-noise ratio will help make the product a success.

Design of Microphone Housing

Proper design and consistent manufacturing of the microphone housing is important, because improper acoustic positioning of the microphone will reduce recognition accuracy. This section describes several important considerations that must be carefully followed in designing the microphone mounting and housing. Many mechanical arrangements are possible for the microphone element, and some will work better than others. We recommend the following guidelines for the microphone housing:

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- **FIRST:** In the product, the microphone element should be positioned as close to the mounting surface as possible and should be fully seated in the plastic housing. There must be NO airspace between the microphone element and the housing. Having such airspace can lead to acoustic resonance, which can reduce recognition accuracy.

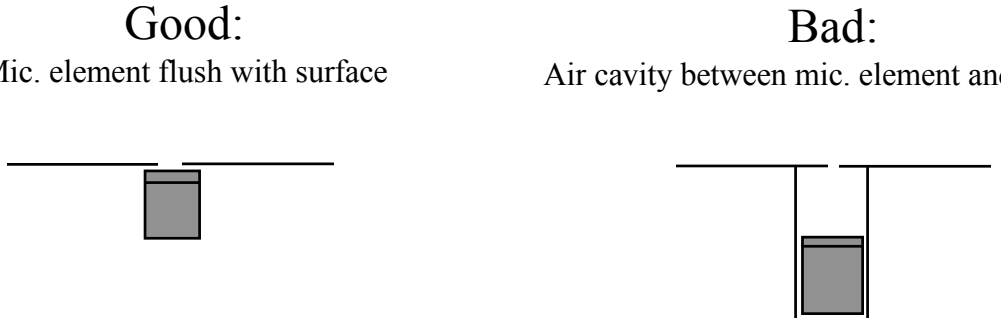

Figure 6 -- **Microphone Mounting (1)**

- **SECOND**: The area in front of the microphone element must be kept clear of obstructions to avoid interference with recognition. The diameter of the hole in the housing in front of the microphone should be at least 5 mm. Any necessary plastic surface in front of the microphone should be as thin as possible, being no more than 0.7 mm if possible.

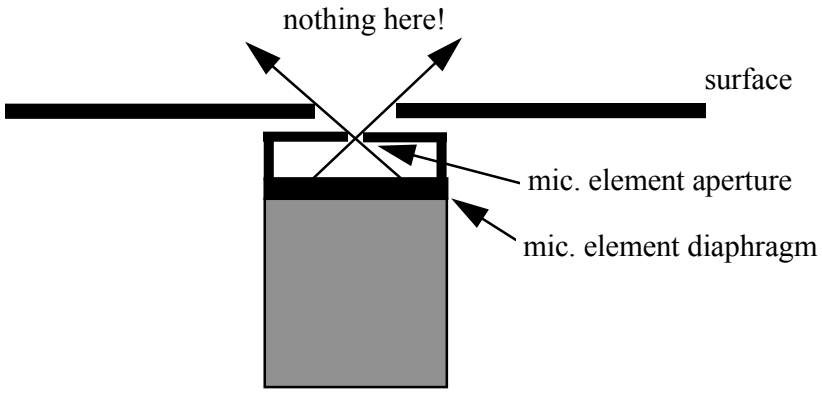

Figure 7 -- **Microphone Mounting (2)**

- **THIRD**: The microphone should be acoustically isolated from the housing if possible. This can be accomplished by surrounding the microphone element with a spongy material such as rubber or foam. Mounting with a non-hardening adhesive such as RTV is another possibility. The purpose is to prevent auditory noises produced by handling or jarring the product from being “picked up” by the microphone. Such extraneous noises can reduce recognition accuracy.

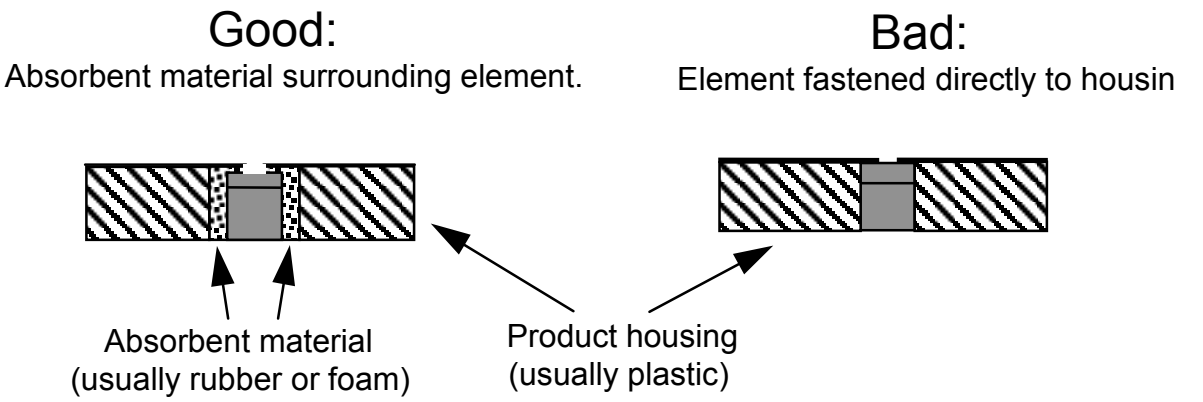

Figure 8 -- **Microphone Mounting (3**)

If the microphone is moved from 6 inches to 12 inches from the speaker's mouth, the signal power decreases by a factor of four. The difference between a loud and a soft voice can also be more than a factor of four. Thus, the recognizer must function over a wide dynamic range of input signal strength and it will have reduced recognition ability if the input signal either saturates the A/D converter or is too weak. The RSC-300/364 provides Automatic Gain Control (AGC) to partially compensate for a too-large or too-small speech signal. This AGC operation is performed inside the microphone preamplifier. If the AGC control range is exceeded, software can provide auditory feedback to the speaker about the voice volume. The product can achieve this by saying "please talk louder" or "please don't talk so loud".

Power Consumption and Power Supply Considerations

In operation, the speech recognition circuit may draw a current of around 10 mA. If the system is powered on continuously to listen for a given word, it will drain a button battery in a few hours, or a large alkaline battery in several days. Thus, if the application requires that the recognizer be on all of the time, the system should operate from mains power. Conversely, if the product is designed to operate from batteries, it must usually remain in the low-power "sleep" mode most of the time, until it is occasionally awakened for a few seconds to recognize a word. The RSC-300/364 can be awakened from a button press or other I/O event, or from the countdown of the Osc2 timer. It cannot be awakened by a speech signal applied to the microphone input.

In order to conserve battery power, the product should be designed to be activated by the user each time it is required to recognize a word. A well-designed program will allow a few seconds after activation before attempting recognition in order to allow reference voltages to stabilize. A speech prompt is a good means of providing this delay. Current drain is higher during speech or music synthesis because power must be delivered to the speaker.

Mains-powered supply ripple should not exceed 5 millivolts measured between the VDD and GND terminals. When using mains power, regulated DC supplies will typically be required. Three-terminal voltage regulators (such as the 7805) are used commonly for this purpose and will provide a minimum of 47 dB of ripple rejection. The power dissipated by these regulators is a function of the voltage differential between the input and output terminals. For instance, powering a 7805 regulator at 9V and delivering 10 mAmp through it will dissipate 40 mWatts of power.

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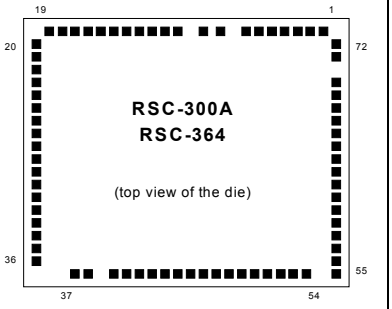
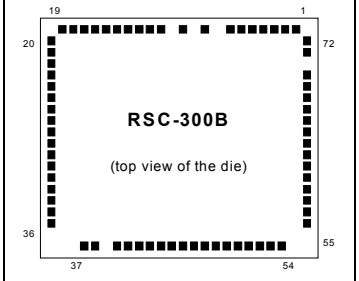
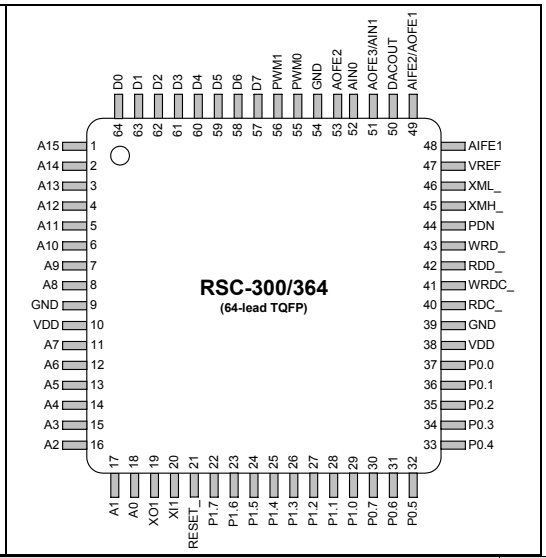
Die Bond Pad and QFP Pin Descriptions





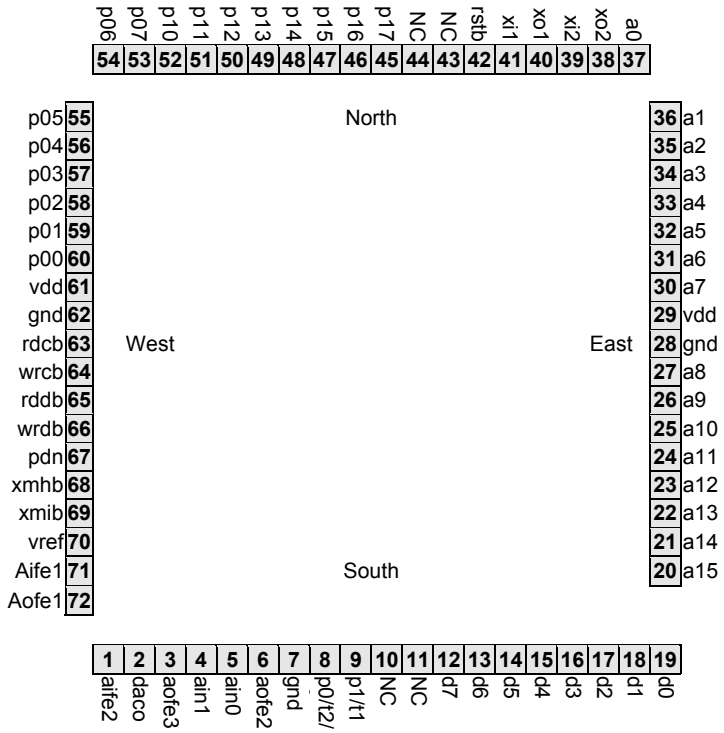


Name	Die Pad	QFP Pin	Description	I/O
A[15:0]	20-27, 30-37	1-8, 11-18	External Memory Address Bus	O
AIN0	5	52	Analog In, low gain. (range AGND to AVDD/2.)	I
AIN1	4	51	Analog In, hi gain (8X input amplitude of AIN0, same range)	I
AOFE1	72	49	Output of 1st stage of preamplifier	O
AOFE2	6	53	Output of 2nd stage of preamplifier	O
AOFE3	3	51	Output of 3rd stage of preamplifier	O
AIFE1	71	48	Output of 1st stage of preamplifier	I
AIFE2	1	49	Output of 2nd stage of preamplifier	I
NC	10,11,43,44		Not Connected	-
PWM0	8	55	Pulse Width Modulator Output0	O
DACOUT	2	50	Analog Output (unbuffered).	O
D[7:0]	12-19	57-64	External Data Bus	I/O
Vss	7,28,62	9, 39,54	Vss	-
PDN	67	44	Power Down. Active high when powered down.	O
P1[7:0], P0[7:0]	43-52,53-60	22-29, 30-37	General Purpose Port I/O. Pin P0.0 can act as an external interrupt input. All I/O pins can act as “wake up” inputs.	I/O
/RDC	63	40	External Code Read Strobe	O
/RDD	65	42	External Data Read Strobe	O
/RESET	42	21	Reset	I
/TE1 or PWM1	9	56	Test Mode *or* Pulse Width Modulator Output1 (multiplexed)	I *or* O
VREF	70	47	Reference Voltage = Vdd/2 or Vdd/4. Depends on software	-
V_{DD}	29,61	10,38	Supply Voltage	-
/WRC	64	41	External Code Write Strobe	O
/WRD	66	43	External Data Write Strobe	O
/XMH	68	45	External Hi-memory enable (low active)	I
/XML	69	46	External Low-memory enable (low active)	I
XO1	40	19	Oscillator 1 output (high frequency)	O
XI1	41	20	Oscillator 1 input	I
XO2	38	NA	Oscillator 2 output (32768 Hz)	O
XI2	39	NA	Oscillator 2 input	I

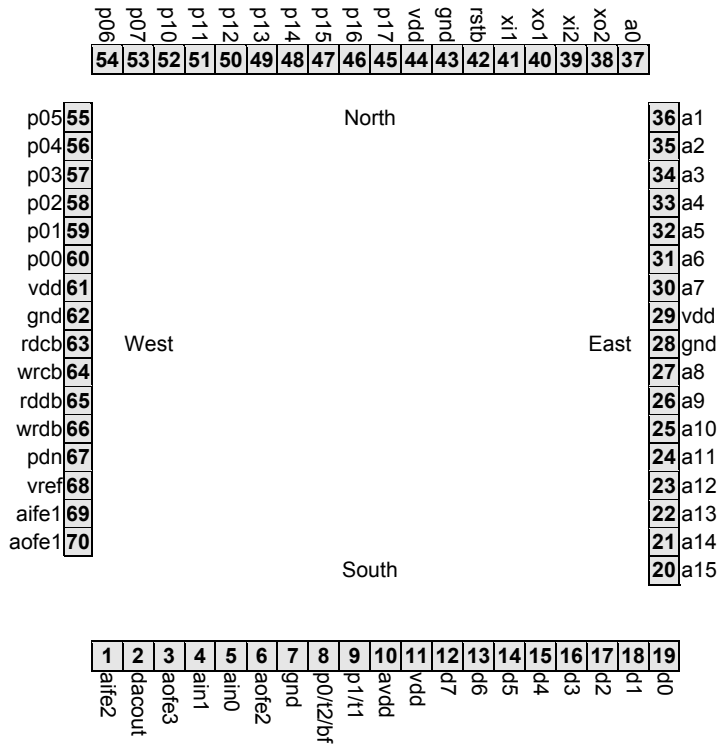
Note*:* Substrate should be connected to VSS

Die Pad Ring

Versions "RSC-364" and "RSC-300A"



Version "RSC-300B"



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RSC-300/364 Die Bonding Pad Locations

Versions "RSC-364" and "RSC-300A"

Note: All locations are the center of the pad. Verify that you are bonding parts marked 65-0087 before using this table!

Pad #	South	X (um)	Y (um)	Pad #	East	X (um)	Y (um)	Pad #	North	X (um)	Y (um)	Pad #	West	X (um)	Y (um)
1	AIFE2	339.05	96.15	20	A15	3268.4	370.7	37	A0	2663.35	3211.6	55	P05	101.1	2513.5
2	DAOUT	462.9	96.15	21	A14	3268.4	494.55	38	XO2	2533.5	3211.6	56	P04	101.1	2389.65
3	AOFE3	586.75	96.15	22	A13	3268.4	618.4	39	XI2	2365.45	3211.6	57	P03	101.1	2265.8
4	AIN1	710.6	96.15	23	A12	3268.4	742.25	40	XO1	2235.65	3211.6	58	P02	101.1	2141.95
5	AIN0	834.45	96.15	24	A11	3268.4	866.1	41	XI1	2105.8	3211.6	59	P01	101.1	2018.1
6	AOFE2	958.3	96.15	25	A10	3268.4	989.95	42	RSTB	1975.9	3211.6	60	P00	101.1	1894.25
7	GND	1090	96.15	26	A9	3268.4	1113.8	43	NC	1830.65	3211.6	61	VDD	101.1	1764.85
8	P0/BF	1312.8	96.15	27	A8	3268.4	1237.65	44	NC	1700.8	3211.6	62	GND	101.1	1635
9	P1/T1	1665	96.15	28	GND	3268.4	1381.95	45	P17	1556.35	3211.6	63	RDCB	101.1	1504.85
10	NC	1870	96.15	29	VDD	3268.4	1511.8	46	P16	1432.5	3211.6	64	WRCB	101.1	1381
11	NC	1999.5	96.15	30	A7	3268.4	1652.1	47	P15	1308.65	3211.6	65	RDDB	101.1	1257.15
12	D7	2131.95	96.15	31	A6	3268.4	1775.95	48	P14	1184.8	3211.6	66	WRDB	101.1	1133.3
13	D6	2255.8	96.15	32	A5	3268.4	1899.8	49	P13	1060.95	3211.6	67	PDN	101.1	1009.45
14	D5	2379.65	96.15	33	A4	3268.4	2023.65	50	P12	937.1	3211.6	68	XMHB	101.1	885.6
15	D4	2503.5	96.15	34	A3	3268.4	2147.5	51	P11	813.25	3211.6	69	XMLB	101.1	761.75
16	D3	2627.35	96.15	35	A2	3268.4	2271.35	52	P10	689.4	3211.6	70	VREF	101.1	637.9
17	D2	2751.2	96.15	36	A1	3268.4	2395.2	53	P07	565.55	3211.6	71	AIFE1	101.1	470.05
18	D1	2875.05	96.15					54	P06	441.7	3211.6	72	AOFE1	101.1	346.2
19	D0	2998.9	96.15												

Notes:

1- Die Size: 3.3695 x 3.3127 mm
2- Chip orgin is at 0.0, 0.0 mm (Lower Left Hand Corner).
3- Pad size is 100um x 100um

Version "RSC-300B"

Note: all locations are the center of the pad. Note: Verify that you are bonding parts marked 65-0098 before using this table!"

Pad #	South	X (um)	Y (um)	Pad #	East	X (um)	Y (um)	Pad #	North	X (um)	Y (um)	Pad #	West	X (um)	Y (um)
1	AIFE2	339.05	96.175	20	A15	3150.925	345.7	37	A0	2449.8	2711.625	55	P05	101.125	2433.05
2	DAOUT	454.05	96.175	21	A14	3150.925	475.7	38	XO2	2334.8	2711.625	56	P04	101.125	2296.05
3	AOFE3	569.05	96.175	22	A13	3150.925	605.7	39	XI2	2166.7	2711.625	57	P03	101.125	2159.05
4	AIN1	684.05	96.175	23	A12	3150.925	735.7	40	XO1	2051.7	2711.625	58	P02	101.125	2022.05
5	AIN0	799.05	96.175	24	A11	3150.925	865.7	41	XI1	1936.7	2711.625	59	P01	101.125	1885.05
6	AOFE2	914.05	96.175	25	A10	3150.925	995.7	42	RSTB	1821.7	2711.625	60	P00	101.125	1748.05
7	GND	1029.8	96.175	26	A9	3150.925	1125.7	43	NC	1706.7	2711.625	61	VDD	101.125	1611.05
8	P0/BF	1244.1	96.175	27	A8	3150.925	1255.7	44	NC	1591.7	2711.625	62	GND	101.125	1474.05
9	P1/T1	1596.7	96.175	28	GND	3150.925	1385.7	45	P17	1476.7	2711.625	63	RDCB	101.125	1337.05
10	NC	1793.2	96.175	29	VDD	3150.925	1515.7	46	P16	1361.7	2711.625	64	WRCB	101.125	1200.05
11	NC	1908.2	96.175	30	A7	3150.925	1645.7	47	P15	1246.7	2711.625	65	RDDB	101.125	1063.05
12	D7	2023.2	96.175	31	A6	3150.925	1775.7	48	P14	1131.7	2711.625	66	WRDB	101.125	926.05
13	D6	2138.2	96.175	32	A5	3150.925	1905.7	49	P13	1016.7	2711.625	67	PDN	101.125	789.05
14	D5	2253.2	96.175	33	A4	3150.925	2035.7	50	P12	901.7	2711.625	68	VREF	101.125	652.05
15	D4	2368.2	96.175	34	A3	3150.925	2165.7	51	P11	786.7	2711.625	69	AIFE1	101.125	483.2
16	D3	2483.2	96.175	35	A2	3150.925	2295.7	52	P10	671.7	2711.625	70	AOFE1	101.125	346.2
17	D2	2598.2	96.175	36	A1	3150.925	2425.7	53	P07	556.7	2711.625				
18	D1	2713.2	96.175					54	P06	441.7	2711.625				
19	D0	2828.2	96.175												

Notes:

1-Die Size: 3.2520 x 2.8127 mm (NOT including Scribe)
2-Chip origin is at 0.0, 0.0 mm (Lower Left Hand Corner).
3-Pad size is 100um x 100um

Absolute Maximum Ratings

Any pin to GND:	-0.1V to +6.5V
Operating temperature(T_O):	0°C to +70°C
Soldering temperature:	260°C for 10 sec
Power dissipation:	1 W
Operating Conditions:	-20°C to +70°C; V_{DD}=2.85 - 5.25V V_{SS}=0V

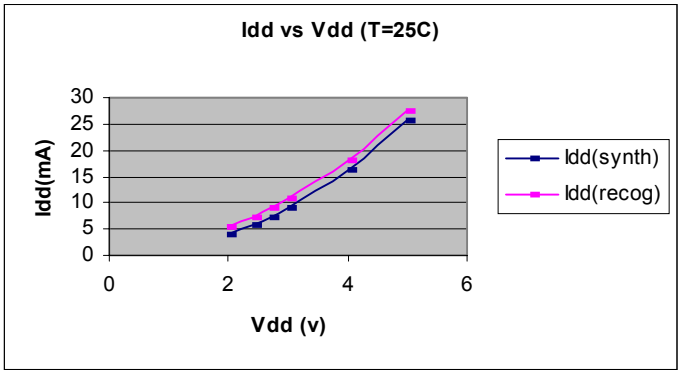
***WARNING**:*
Stressing the RSC-300/364 beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. Characteristics

(T_O = 0°C to +70°C, V_{DD} = 2.85V – 5.25V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.1		0.75	V	
V_{IH}(Vcc<3.6)	Input High Voltage	0.8*Vdd		Vdd+0.3	V	
V_{IH}(Vcc>3.6)	Input High Voltage	3.0		Vdd+0.3	V	
V_{OL}	Output Low Voltage		0.3	0.1*Vdd	V	I_{OL}= 2 mA
V_{OH}	Output High Voltage (I/O Pins)	0.8*Vdd	0.9*Vdd		V	I_{OL}= -2 mA
I_{IL}	Logical 0 Input Current		<1	10	uA	V_{ss}<V_{pin}<V_{dd}
I_{DD1}(Vcc=3.3V)	Supply Current, Active		10	20	mA	Hi-Z Outputs
I_{DD3}(Vcc=3.3V)	Supply Current, Powerdown		1	10	uA	Hi-Z Outputs
Rpu	Pull-up resistance P0.0-P1.7 I/O Pins /XML,/XMH	5, 80, Hi-Z	4.5, 200, Hi-Z 200		kΩ kΩ	Selected with software Fixed

Vdd vs. Idd



Vcc	Idd(synth) *(No Load)*	Idd(recog)
2.4	5.7	7.2
2.7	7.4	8.9
3	9.2	10.7
4	16.3	18
5	25.6	27.3

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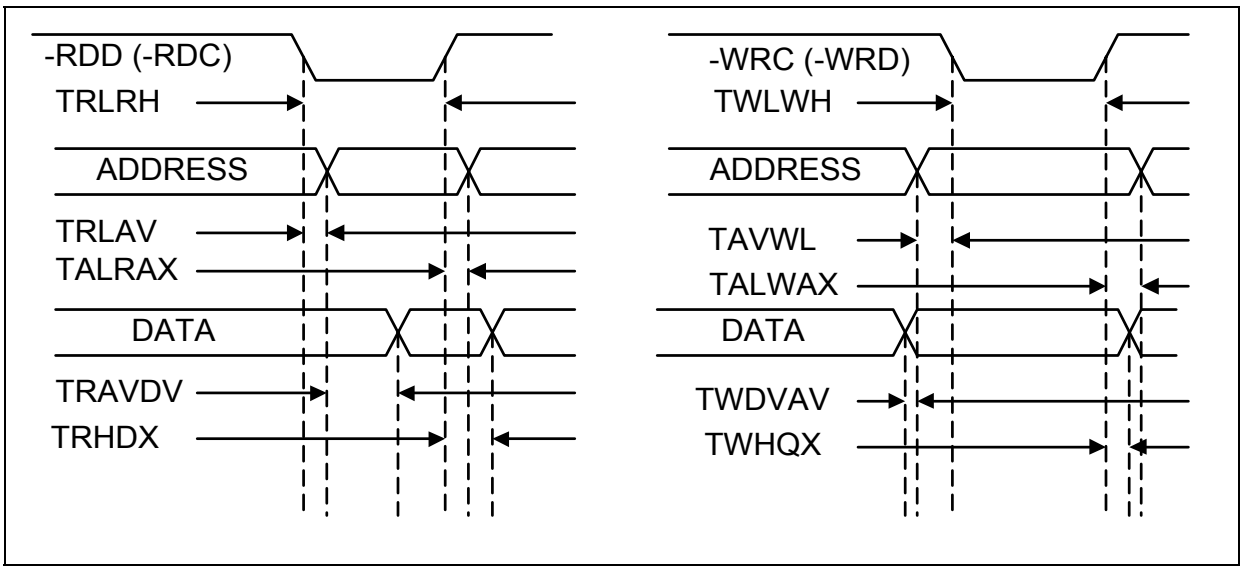
A.C. Characteristics (External Memory Accesses)

(T_O = -20°C to +70°C, V_{DD} = 3.3V; load capacitance for outputs = 80 pF; Osc=14.32 MHz)

SYMBOL	PARAMETER	CPU=osc/1, 1 WS		CPU=osc/2, 0WS		UNITS
		MIN	MAX	MIN	MAX	
1/TCL1	Processor Clock frequency		14.32		7.16	MHz
TRLRH	-RDC (-RDD) Pulse Width		140		140	ns
TRLAV	-RDC (-RDD) Low to Address valid		5		5	ns
TALRAX	Address hold after -RDC (-RDD)		0		0	ns
TRAVDV	Address valid to Valid Data In		135		135	ns
TRHDX	Data Hold after -RDC (-RDD)	0		0		ns
TWLWH	-WRC (-WRD) Pulse Width		140		140	ns
TAVWL	Address Valid to -WRC (-WRD)	35		70		ns
TALWAX	Address Hold after -WRC (-WRD)	35		70		ns
TWDVAV	Write Data Valid to Address Valid		5		5	ns
TWHQX	Data Hold after -WRC (-WRD)	35		70		ns

Timing Diagrams

Note that the -RDC signal does not necessarily pulse for every read from code space, but may stay low for multiple cycles.



External Read Timing External Write Timing

RSC-300/364 Instruction Set

The instruction set for the RSC-300/364 has 54 instructions comprising 10 move, 7 rotate, 11 branch, 11 register arithmetic, 9 immediate arithmetic, and 6 miscellaneous instructions. All instructions are 3 bytes or fewer, and no instruction requires more than 10 clock cycles to execute. The column "Cycles" indicates the number of clock cycles required for each instruction when operating with zero wait states. Wait states may be added to lengthen all accesses to external addresses or to the internal ROM (RSC-364 only), but not internal SRAM. The column "+Cycles/Waitstate" shows the number of additional cycles added for each additional wait state. The wait states used for *movx* instructions may be set independently of those used for *movc* or code fetches. This table assumes movx and fetch wait states are the same. Opcodes are in HEX.

MOVE Group Instructions

Register-indirect instructions accessing code (*movc*) or data (*movx*space locations use an 8-bit operand ("@source" or "@dest") to designate an SRAM register pointer to the 16-bit target address. The "source" or "dest" pointer register must be at an even address. The LOW byte of the target address is contained at the pointer address, and the HIGH byte of the target address is contained at the pointer address+1. Register-indirect instructions accessing register (*mov,push,pop*) space locations use an 8-bit operand ("@source" or "@dest") to designate an SRAM register pointer to the 8-bit target address. The carry, sign, and zero flags are not affected by *mov* instructions.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles Waitstate
MOV	10	dest	source	register to register	3	5	3
MOV	11	@dest	source	register to register-indirect	3	5	3
MOV	12	dest	@source	register-indirect to register	3	6	3
MOV	13	dest	#immed	immediate data to register	3	4	3
MOVC	14	dest	@source	code space to register	3	7	4
MOVC	15	@dest	source	register to code space	3	8	4
MOVX	16	dest	@source	data space to register	3	7	4
MOVX	17	@dest	source	register to data space	3	8	4
POP	18	dest	@++source	register to register data stack pop (source pre-incremented)	3	10	3
PUSH	19	@dest--	source	register to register data stack push (dest post-decremented)	3	9	3

ROTATE Group Instructions

Rotate group instructions apply only directly to register space SRAM locations. The carry flag is affected by these instructions, but the sign and zero flags are unaffected.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles Waitstate
RL	30	dest	-	rotate left, c set from b7	2	5	2
RR	31	dest	-	rotate right, c set from b0	2	5	2
RLC	32	dest	-	rotate left through carry	2	5	2
RRC	33	dest	-	rotate right through carry	2	5	2
SHL	34	dest	-	shift left, c set from b7, b0=0	2	5	2
SHR	35	dest	-	shift right, c set from b0, b7=0	2	5	2
SAR	36	dest	-	shift right arithmetic, c set from b0, b7 duplicated	2	5	2

BRANCH Group Instructions

The branch instructions use direct address values rather than offsets to define the target address of the branch. This implies that binary code containing branches is not relocatable. However, object code produced by Sensory's assembler contains address references that are resolved at link time, so .OBJ modules *are* relocatable. The indirect jump instruction uses an 8-bit operand ("@dest") to designate an SRAM register pointer to the 16-bit target address. The "dest" pointer register must be at an even address. The LOW byte of the target

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address is contained at the pointer address, and the HIGH byte of the target address is contained at the pointer address+1.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles Waitstate
JC	20	dest low	dest high	jump on carry = 1	3	3	3
JNC	21	dest low	dest high	jump on carry = 0	3	3	3
JZ	22	dest low	dest high	jump on zflag = 1	3	3	3
JNZ	23	dest low	dest high	jump on zflag = 0	3	3	3
JS	24	dest low	dest high	jump on sflag = 1	3	3	3
JNS	25	dest low	dest high	jump on sflag = 0	3	3	3
JMP	26	dest low	dest high	jump unconditional	3	3	3
CALL	27	dest low	dest high	direct subroutine call	3	3	3
RET	28	-	-	return from call	1	2	1
IRET	29	-	-	return from interrupt	1	2	1
JMPR	2A	@dest	-	jump indirect	2	4	2

MISCELLANEOUS Group Instructions

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles Waitstate
NOP	00	-	-	no operation	1	2	1
CLC	01	-	-	clear carry	1	2	1
STC	02	-	-	set carry	1	2	1
CMC	03	-	-	complement carry	1	2	1
CLI	04	-	-	disable interrupts	1	2	1
STI	05	-	-	enable interrupts	1	2	1

ARITHMETIC/LOGICAL Group Instructions

Arithmetic and logical group instructions apply only to register space SRAM locations. The results of the instruction are always written directly to the SRAM “dest” register. All but the INCrement and DECrement instructions have both register source and immediate source forms.

In each of the following instructions the sign and zero flags are updated based on the result of the operation. The carry flag is updated by the arithmetic operations (ADD, ADC, SUB, SUBC, CP, INC, DEC) but it is *not* affected by the logical operations (AND, TM, OR, XOR).

Note: the carry is set HIGH by SUB, CP, SUBC, DEC when a borrow is generated.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles Waitstate
AND	40	dest	source	logical and	3	6	3
TM	41	dest	source	like AND, destination unchanged	3	6	3
OR	42	dest	source	logical or	3	6	3
XOR	43	dest	source	exclusive or	3	6	3
SUB	44	dest	source	subtract	3	6	3
CP	45	dest	source	like SUB, destination unchanged	3	6	3
SUBC	46	dest	source	subtract w/carry	3	6	3
ADD	47	dest	source	add	3	6	3
ADC	48	dest	source	add w/carry	3	6	3
INC	49	dest	-	increment	2	5	2
DEC	4A	dest	-	decrement	2	5	2
AND	50	dest	#immed	logical and	3	5	3
TM	51	dest	#immed	like AND, destination unchanged	3	5	3
OR	52	dest	#immed	logical or	3	5	3
XOR	53	dest	#immed	exclusive or	3	5	3
SUB	54	dest	#immed	subtract	3	5	3
CP	55	dest	#immed	like SUB, destination unchanged	3	5	3
SUBC	56	dest	#immed	subtract w/carry	3	5	3
ADD	57	dest	#immed	add	3	5	3
ADC	58	dest	#immed	add w/carry	3	5	3

RSC-300/364 Special Function Register (SFR) Summary

This section describes the registers located in addresses 0E0h through 0FFh of the register space. These special function registers (SFRs) are generally used for configuration control and system level functions. In many cases an applications programmer might need to access these registers only to initialize the ports. Since the SFRs are extensively used by Sensory's library functions, thorough understanding is essential before changing the contents of these registers. Some registers in this address range are for the exclusive use of Sensory Technology functions and are not further described.

The Symbol shown is the name recognized by the assembler for the associated register.

Symbol	Address	Register Name	Type
P0OUT	0E0h	Port 0 Output Register	R/W
P1OUT	0E1h	Port 1 Output Register	R/W
P0IN	0E2h	Port 0 Input Register	Read
P1IN	0E3h	Port 1 Input Register	Read
P0CTLA	0E4h	Port 0 Control Register A	R/W
P1CTLA	0E5h	Port 1 Control Register A	R/W
P0CTLB	0E6h	Port 0 Control Register B	R/W
P1CTLB	0E7h	Port 1 Control Register B	R/W
CKCTL	0E8h	Clock Control Register	R/W
WAKE0	0E9h	Wakeup configuration, Port 0	R/W
WAKE1	0EAh	Wakeup configuration, Port 1	R/W
T1R	0EBh	Timer 1 Reload	R/W
T1V	0ECh	Timer 1 Counter	R/W
T2R	0EDh	Timer 2 Reload	R/W
T2V	0EEh	Timer 2 Counter	R/W
ANCTL	0EFh	Analog Control Register	R/W
STKPTRS	0F6h	Stack Read and Write Pointers	R/W
OSC1EXT	0F7h	Oscillator 1 Extended Functions	R/W
BRKLO	0F8h	Break Address Low Byte	R/W
BRKHI	0F9h	Break Address High Byte	R/W
DAC	0FAh	DAC Hold Register	R/W
BANK	0FCh	RAM Bank Select Register	R/W
IMR	0FDh	Interrupt Mask Register	R/W
IRQ	0FEh	Interrupt Request Register	R/W
FLAGS	0FFh	Flags Register	R/W

Port 0 Output Register (Address 0E0h)

msb			**P0OUT**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used to write values to Port 0. Values written to this register affect bits that have been configured as outputs. Bits that have been configured as inputs are not affected.

Bit Description:

P0OUT: Output bits D0 through D7
Initialization: All bits cleared to 0 upon reset
Read Access: Read output bits from Port 0
Write Access: Write output bits to Port 0
Also refer to: P0CTLA, P0CTLB

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Port 1 Output Register (Address 0E1h)

msb			**P1OUT**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used to write values to Port 1. Values written to this register affect bits that have been configured as outputs. Bits that have been configured as inputs are not affected.

Bit Description:

P1OUT: Output bits D0 through D7
Initialization: All bits cleared to 0 upon reset
Read Access: Read output bits from Port 1
Write Access: Write output bits to Port 1
Also refer to: P1CTLA, P1CTLB

Port 0 Input Register (Address 0E2h)

msb			**P0IN**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used to read values from Port 0.

Bit Description:

P0IN: Input bits D0 through D7
Initialization:
Read Access: Input bits from Port 0
Write Access:
Also refer to: P0CTLA, P0CTLB

Port 1 Input Register (Address 0E3h)

msb			**P1IN**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used to read values from Port 1.

Bit Description:

P1IN: Input bits D0 through D7
Initialization:
Read Access: Input bits from Port 1
Write Access:
Also refer to: P1CTLA, P1CTLB

Port 0 Control Register A (Address 0E4h)

msb			**P0CTLA**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used with P0CTLB to control the function of the general-purpose port 0.

Bit Description:

P0CTLA:
Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access:
Also refer to: P0CTLB

Port 0 Control Register B (Address 0E6h)

msb			**P0CTLB**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used with P0CTLA to control the function of the general-purpose port 0.

Bit Description:

P0CTLB:
Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access:
Also refer to: P0CTLA

The control registers A and B together control the function of the general-purpose port 0:

B	*A*	*Function*
0	0	Input - Weak Pull-up
0	1	Input - Strong Pull-up
1	0	Input - No pull-up
1	1	Output

For example, if register P0CTLB bit 4 is set high, and register P0CTLA bit 4 is low, then pin P0.4 is an input without a pull-up device.

Port 1 Control Register A (Address 0E5h)

msb			**P1CTLA**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used with P1CTLB to control the function of the general-purpose port 1.

Bit Description:

P1CTLA:
Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access:
Also refer to: P1CTLB

Port 1 Control Register B (Address 0E7h)

msb			**P1CTLB**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register is used with P1CTLA to control the function of the general-purpose port 1.

Bit Description:

P1CTLB:
Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access:
Also refer to: P1CTLA

The control registers A and B together control the function of the general-purpose port 1:

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B	*A*	*Function*
0	0	Input - Weak Pull-up
0	1	Input - Strong Pull-up
1	0	Input - No pull-up
1	1	Output

For example, if register P1CTLB bit 3 is cleared, and register P1CTLA bit 3 is set high, then pin P1.3 is an input with a strong pull-up.

Clock Control Register (Address 0E8h)

msb			**CKCTL**				lsb
PD	T2	FC	CD 1	CD 0	PC S	DO 2	EO 1

This register is used to enable the two oscillators, to select the processor clock source and the internal clock divider, and to enable some sleep/wakeup functions. Sensory's library code may initialize specific settings for this register, so it should be changed only with care.

Bit Description:

CKCTL.0: EO1
0: Enable Oscillator #1 inverter
1: Disable Oscillator #1
Cleared by reset or (wakeup & (PCS=0))

CKCTL.1: DO2
0: Disable Oscillator #2 inverter
1: Enable Oscillator #2 inverter
Cleared by reset.

CKCTL.2: PCS
0: Processor clock source = Oscillator 1
1: Processor clock source = Oscillator 2
Cleared by reset.

CKCTL.4-CKCTL.3: CD1-CD0
Select processor clock divisor. The processor clock rate is the fraction of the source clock shown.

	CD0	Division
0	0	1/2
0	1	1/1
1	0	1/8
1	1	1/256

Cleared by reset.

CKCTL.5: FC
0: Disable reserved function clock
1: Enable reserved function clock
Cleared by reset.

CKCTL 6: T2
0: Timer #2 overflow does not cause wakeup
1: Timer #2 overflow causes wakeup
Cleared by reset.

CKCTL.7: PD
0: Processor is in operational state
1: Processor is in PowerDown state ("sleep")
Cleared by reset and wakeup.

Port 0 Wakeup Configuration Register (Address 0E9h)

msb			**WAKE0**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

The Wake0 register controls the enabling of I/O events on port0 that can cause a processor “wakeup”. These wakeup events are recognized independently of whether the processor is running or stopped. The processor may also be waked up by countdown of Timer2.

Bit Description:

WAKE0.7-WAKE0.0 Wake Enable
0: Wakeup is not enabled on corresponding P0 port bit
1: Wakeup is ENABLED on corresponding P0 port bit

Each bit, if set, enables the corresponding general purpose I/O pin of ports P0.0-P0.7 to generate a wake-up event. If enabled, the polarity of the wake-up trigger is determined by the corresponding bit in the output register: if the input matches the output register, a wake-up even is generated. It is assumed that the general-purpose pin is configured to be an input.

Each bit, if clear, prevents the corresponding general-purpose I/O pin of ports P0.0-P0.7 from generating a wake-up event.

Initialization: All bits cleared to 0 upon reset
Also refer to: WAKE1, P0IN, P0CTLA, P0CTLB

Port 1 Wakeup Configuration Register (Address 0EAh)

msb			**WAKE1**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

The Wake1 register controls the enabling of I/O events on port1 that can cause a processor “wakeup”. These wakeup events are recognized independently of whether the processor is running or stopped.
Bit Description:

WAKE1.7-WAKE1.0 Wake Enable
0: Wakeup is not enabled on corresponding P1 port bit
1: Wakeup is ENABLED on corresponding P1 port bit

Each bit, if set, enables the corresponding general-purpose I/O pin of ports P1.0-P1.7 to generate a wake-up event. If enabled, the polarity of the wake-up trigger is determined by the corresponding bit in the output register: if the input matches the output register, a wake-up even is generated. It is assumed that the general-purpose pin is configured to be an input.

Each bit, if clear, prevents the corresponding general purpose I/O pin of ports P1.0-P1.7 from generating a wake-up event.

Initialization: All bits cleared to 0 upon reset
Also refer to: WAKE0, P1IN, P1CTLA, P1CTLB

Timer 1 Reload Register (Address 0EBh)

msb			**T1R**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register contains an 8-bit reload value for timer 1. The reload register is readable and writeable by the processor. When the timer overflows from FF to 00, a pulse is generated that sets IRQ #0 (timer #1).

Bit Description:

T1R:
Initialization: All bits cleared to 0 upon reset
Read Access: Timer #1 Counter Reload (2's complement of period)
Write Access: Timer #1 Counter Reload (2's complement of period)

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Also refer to: T1V

Timer 1 Counter Register (Address 0ECh)

msb			**T1V**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

Timer 1 counter is a read-only register. If the processor writes to the counter, the data is ignored, and the counter is preset to the reload register value from T1R. Instead of overflowing to 00, the counter is automatically reloaded on each overflow.

For example, if the reload value is 0FAh, the counter will count as follows:

0FAh, 0FBh, 0FCh, 0FDh, 0FEh, 0FFh, 0FAh, 0FBh etc.

The overflow pulse is generated during the period *after* the counter value was 0FFh.

The input clock for Timer 1 is always generated from Oscillator #1, gated by the wake-up delay, gated by bit 7 of the Clock Control Register, CKCTL.7 flag = 0, then divided by 16. For normal operation with a 14.3 MHz crystal, Timer 1 counts at a rate of 0.895 MHz. Thus the longest duration that can be directly timed is 255/(0.895 MHz) = 285 microseconds. If the T1P bit of the Oscillator 1 Extension register is set (OSC1EXT.6=1), an additional division by 2 is performed.

Bit Description:

T1V:
Initialization: All bits cleared to 0 upon reset
Read Access: Timer #1 current counter value
Write Access: Force asynchronous load of counter from reload register
Also refer to: T1R, OSC1EXT

Timer 2 Reload Register (Address 0EDh)

msb			**T2R**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

This register contains an 8-bit reload value for timer 2. The reload register is readable and writeable by the processor. When the timer overflows from FF to 00, a pulse is generated that sets IRQ #1 (timer #2).

Bit Description:

T2R:
Initialization: All bits cleared to 0 upon reset
Read Access: Timer #2 Counter Reload (2's complement of period)
Write Access: Timer #2 Counter Reload (2's complement of period)
Also refer to: T2V, CKCTL

Timer 2 Counter Register (Address 0EEh)

msb			**T2V**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

Timer 2 counter is a read-only register. If the processor writes to the counter, the data is ignored, and the counter is preset to the reload register value from T2R. Instead of overflowing to 00, the counter is automatically reloaded on each overflow.

For example, if the reload value is 0FAh, the counter will count as follows:

0FAh, 0FBh, 0FCh, 0FDh, 0FEh, 0FFh, 0FAh, 0FBh etc.

The overflow pulse is generated during the period *after* the counter value was 0FFh.

The input clock for timer #2 is generated from Oscillator #2 divided by 128. With typical operation with a 32,768 Hz crystal for Oscillator #2, the count rate for Timer 2 is 256 Hz. When T2R is set to zero, T2R overflows once per second

The processor can be configured to “wakeup” from the powerdown state on an overflow of the timer2 counter. If Oscillator 1 is turned off during this time, the only current consumption is due to the slow 32 kHz Oscillator2 and counter circuits.

Bit Description:

T2V:
Initialization: All bits cleared to 0 upon reset
Read Access: Timer #2 current counter value
Write Access: Force asynchronous load of counter from reload register
Also refer to: T2R, CKCTL

Analog Control Register (Address 0EFh)

msb			**ANCTL**				lsb
MD		LS1	LS0	DM	BE	DE	M

The analog control register configures the A/D and D/A. Since the RSC analog signals are normally dedicated to functions associated with Sensory’s library code, there is seldom need for applications programs to access this register.

Bit Description:

ANCTL.7: Mode Bit (MD)
If the mode bit is 0, the other bits are as follows:

ANCTL.0: M
1: ADC Mode, comparator powered-up.
0: DAC Mode, comparator powered-down.
Cleared by reset.

ANCTL.1: DE
1: Enable analog output DACOUT
0: Disable analog output DACOUT
Cleared by reset.

ANCTL.2: BE
1: Enable buffered output BUFOUT.
0: Disable buffered output BUFOUT.
Cleared by reset.

ANCTL.3: DM
0: D/A is full-scale.
1: D/A is half-scale.
Cleared by reset.

ANCTL.4: LS0
Provides LSB for full-scale D/A mode.
Cleared by reset.

ANCTL.5: LS1
Provides LSB for half-scale D/A mode, and second to LSB for full-scale D/A mode.
Cleared by reset.

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ANCTL.6: Reserved

Analog Control Register (Address 0EFh) (continued)
If the mode bit is 1, the other bits are as follows:

ANCTL.0-ANCTL.1: Control the inverter strength of the 32,768 Hz oscillator

Bit 1	Bit	Strength
0	0	5 µA
0	1	10 µA
1	0	20 µA
1	1	40 µA

ANCTL.2-ANCTL.3: Control the output resistor of the 32,768 Hz oscillator

Bit 3	Bit 2	Resistance
0	0	50 KΩ
0	1	100 KΩ
1	0	200 KΩ
1	1	400 KΩ

ANCTL.4-ANCTL.6: Reserved

When reading from the Analog Control Register, the side containing the 32,768 Hz oscillator control parameters is **not** read, while the other side is read.
Read Access:
Write Access:
Initialization: On reset, both sides of the Analog Control Register are set to zero.
Also refer to:

Stack Pointers Register (Address 0F6h)

msb			**STKPTRS**				lsb
	WR 2	WR 1	WR 0		RD2	RD1	RD0

The RSC-300/364 has an 8-level hardware stack. This register contains the read and write pointers for the stack. Access to these registers is normally required only by a debugger program.

Bit Description:

STKPTRS.7 Reserved
STKPTRS6-4 Stack Write Pointer. Contains the 3-bit stack address where the next stack write will occur.
STKPTRS.3 Reserved
STKPTRS.2-0 Stack Read Pointer. Contains the 3-bit stack address where the next stack read will occur.

Oscillator1 Extension Register (Address 0F7h)

msb			**OSC1EXT**				lsb
IRW	T1P	MX	WX 4	WX 3	WX 2	WX 1	WX 0

This register controls a variety of extended use options for prescalers and extra wait states derived from Oscillator

Bit Description:

OSC1EXT[4:0] WX4-WX0 Control the number of wait states inserted for *movx* instructions when OSC1EXT.5=1. This allows simplified operation with slow external read/write memories. If no wait states are used, *movx* access duration is one clock. Controlled program delays in the microsecond range can be obtained by setting the desired number of wait states and executing a dummy *movx*.

	0 0 0 0 0	Use zero additional wait states (70 nsec at 14.3 MHz)
	1 1 1 1 1	Use 31 additional wait states (2.24 μsec at 14.3 MHz).
OSC1EXT.5	MX	
	0:	*movx* instructions use wait states in BANK[7:5]
	1:	*movx* instructions use wait states in OSC1EXT[4:0]
		Cleared by reset.
OSC1EXT.6	T1P	
	0:	Timer1 Prescaler uses Osc1
	1:	Timer1 Prescaler uses Osc1/2
		Cleared by reset.
OSC1EXT.7:	IRZ	
	0:	Internal ROM (RSC-364 only) accesses use wait states in Reg BANK[7:5]
	1:	Internal ROM (RSC-364 only) accesses use zero wait states
		Cleared by reset.

Also refer to: CKCTL, BANK

Break Address Low Register (Address 0F8h)

msb			**BRKLO**				lsb
A7	A6	A5	A4	A3	A2	A1	A0

This register contains the low 8-bits of the 16-bit Break Address. The high 8-bits of the Break Address are held in the Break Address High register. These registers may be read or written only when the trap bit is set *(See page 34)*. When the trap bit is set, each pending PC address is compared with the breakpoint address. When a match occurs, then the PC does not fetch the instruction at the breakpoint address, but rather performs a trap. When a trap is performed the flags register is saved, timers are stopped, interrupts are disabled, and execution branches to location 0FFF8h.

Bit Description:

BRKLO.7-0	Break Address Low bits [7:0]
	Set to 0FFh by reset.

Also refer to: BRKHI, FLAGS

Break Address High Register (Address 0F9h)

msb			**BRKHI**				lsb
A15	A14	A13	A12	A11	A10	A9	A8

This register contains the high 8-bits of the 16-bit Break Address. The low 8-bits of the Break Address are held in the Break Address Low register. These registers may be read or written only when the trap bit is set *(See page 34)*. When the trap bit is set, each pending PC address is compared with the breakpoint address. When a match occurs, then the PC does not fetch the instruction at the breakpoint address, but rather performs a trap. When a trap is performed the flags register is saved, timers are stopped, interrupts are disabled, and execution branches to location 0FFF8h.

Bit Description:

BRKHI.7-0	Break Address High bits [15:8]
	Set to 0FFh by reset.

Also refer to: BRKHI, FLAGS

DAC Hold Register (Address 0FAh)

msb			**DAC**				lsb
D7	D6	D5	D4	D3	D2	D1	D0

Holds the eight most significant bits of the value to be converted to an analog signal. Since the analog signal is typically controlled by Sensory library code, there is seldom need for applications programs to access this

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register. This register is not affected during A/D conversions. It contains a signed, 8-bit number and is cleared to 0 by reset.

Bit Description:

DAC:
Initialization: All bits cleared to 0 upon reset
Read Access: DAC Hold Value Write Access: DAC Hold Value
Also refer to:

RAM Bank Select Register (Address 0FCh)

msb			BANK				lsb
W2	W1	W0	B4	B3	B2	B1	B0

The RSC-300/364 architecture supports 1024 bytes of Register Space (RAM). Only 448 of the maximum 1024 bytes are implemented in the RSC-300/364. Since the register space instructions support 8-bit addresses, some registers must be addressed through a banking scheme. The bank register generates address bits 9-5 for accesses associated with register space locations 0C0-0DFH, the "map bank". A 10-bit address is always output to the internal SRAM register space (maximum of 1024 bytes). Bit9 is always 0 in the RSC-300/364, and Bit8 is zero unless the lower bits are in the map bank range.

Bit Description:

BANK.0-BANK.4: These bits select a specific 32-byte block of registers to be addressed as "banked RAM" at locations 0C0H to 0DFH. Any 32-byte block in the internal register space may be mapped to banked RAM except for the SFR block and the map bank itself (the block must be aligned on a 32-byte boundary).

The Special Function Registers (0E0h-0FFh) may only be directly addressed. The first 192 locations (000h-0BFh) may be directly addressed or they may be mapped to the map bank, while the remaining 256 locations (100h-1FFh) may only be accessed via the map bank through bank selection. Sensory's technology code makes extensive use of register space. Bits BANK.0-BANK.4 select the appropriate bank in RAM as follows.

BANK[4:0] value	Address mapped to 0C0h-0DFh	BANK[4:0] value	RAM bank mapped to 0C0h-0DFh
00h	000h-01Fh	08h	100h-11Fh
01h	020h-03Fh	09h	120h-13Fh
02h	040h-05Fh	0Ah	140h-15Fh
03h	060h-07Fh	0Bh	160h-17Fh
04h	080h-09Fh	0Ch	180h-19Fh
05h	0A0h-0BFh	0Dh	1A0h-1BFh
06h	Not Allowed	0Eh	1C0h-1DFh
07h	Not Allowed	0Fh	1E0h-1FFh
010h or greater	The system will wrap around (SRAM bit9 is ignored in RSC-300/364)		

BANK5-BANK7: WAIT STATES.
These bits define the default number of wait states for external/internal memory access (set to 7 on reset). Note that both the internal and external code and data spaces, but not the SRAM, are controlled by these bits. Sensory technology code requires specific wait states, so changes to this register must be restored before invoking any technology code. The Osc1Ext register allows additional flexibility in wait state generation.

BANK:
Initialization: Bits 5-7 set to 1, all other bits cleared to 0 upon reset
Read Access:
Write Access: Wait State Configuration, Bank selection

Also refer to: OSC1EXT

Interrupt Mask Register (Address 0FDh)

msb		**IMR**					lsb
		EI5	E14	EI3	EI2	EI1	EI0

Bit Description:

IMR0-IMR4: EI5: 1= enable interrupt request #5 (Reserved)
EI4: 1= enable interrupt request #4 (PWM complete)
EI3: 1= enable interrupt request #3 (Positive edge of P00)
EI2: 1= enable interrupt request #2 (Reserved)
EI1: 1= enable interrupt request #1 (Overflow of Timer 2)
EI0: 1= enable interrupt request #0 (Overflow of Timer 1)

IMR6-IMR7: Unused

Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access: Interrupt Source Selection
Also refer to: IRQ, FLAGS

Interrupt Request Register (Address 0FEh)

msb		**IRQ**					lsb
		IR5	IR4	IR3	IR2	IR1	IR0

Bit Description:

IRQ0-IRQ4: IR5: 1= interrupt request #5 (Reserved)
IR4: 1= interrupt request #4 (PWM complete)
IR3: 1= interrupt request #3 (Positive edge of P00)
IR2: 1= interrupt request #2 (Reserved)
IR1: 1= interrupt request #1 (Overflow of Timer 2)
IR0: 1= interrupt request #0 (Overflow of Timer 1)

IRQ6-IRQ7: Unused

Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access: The bits in this register *cannot be set* by writing a one to any bit, but they *can be cleared* by writing zeroes. To assure that pending interrupts are not lost, a bit should be cleared by using a *mov* instruction, not an *and* instruction. For example, the Interrupt Service Routine for Timer1 should clear the interrupt by the instruction:
mov irq, #~1
Do **not** use 'and' instructions in the IRQ register.

Also refer to: IMR, FLAGS

Flags Register (Address 0FFh)

msb			**FLAGS**				lsb
C	Z	S	T	K			GIE

The flags register contains three bits related to the result of the last arithmetic/logical/rotate/misc instruction, one bit that controls breakpoint enabling, one bit for warning of stack full condition, two reserved bits, and one bit that controls the generation of interrupts. The flags register is not affected by branch instructions, except that an IRET instruction restores the value preceding the interrupt. The flags register is not affected by mov instructions unless it is the destination register. Other instructions affect the flags register in different ways. Refer to

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RSC-300/364 Instruction Set.
Note*:* If an interrupt occurs while the GIE bit is being cleared, the GIE bit may be restored to an enabled state upon return from the Interrupt Service Routine. Use the CLIx macro (supplied with the Sensory Speech 6 Technology library software) in place of the CLI instruction to assure that interrupts are globally disabled before proceeding.

Bit Description:

FLAGS.0: GIE (Global Interrupt Enable)
0: All interrupts disabled
1: Interrupts Enabled
Cleared by reset
FLAGS.1: Reserved. Do not change values in these bits.
FLAGS.2: Reserved. Do not change values in these bits.
FLAGS.3: K (Stack)
0: Stack not full
1: Stack filled, possibly overflowed
Cleared by reset. The Stack bit is set when there is no more room in the stack. This can occur under normal program operation, but it may indicate program malfunction. Once set, the bit can only be cleared by reset. This bit may be a useful indicator during development.
FLAGS.4: T (Trap)
0: Breakpoint function disabled
1: Breakpoint function enabled
Cleared by reset. When the Trap bit is set, the processor will jump to the debug monitor when the Program Counter equals the value in the breakpoint register. Normally only used by a debugger.
FLAGS.5: S (Sign)
0: Result of last Arithmetic/logical operation was non-negative.
1: Result of last Arithmetic/logical operation was negative
Cleared by reset
FLAGS.6: Z (Zero)
0: Result of last Arithmetic/logical operation was non-zero.
1: Result of last Arithmetic/logical operation was zero.
Cleared by reset
FLAGS.7: C (Carry)
0: No carry from last arithmetic/rotate/misc operation.
1: Last arithmetic/rotate/misc operation produced a carry.
Cleared by reset

Special Data Space Addresses Summary

As described previously, the RSC-300/364 uses *movx* instructions to access all Data Space locations. Typically Data Space locations are external, but a few specific locations are mapped internally in the last page (0FF00h-0FFFFh) of Data Space. For this reason, it is generally best to plan to use *no* external addresses in the last page of Data Space. (The important exception to this is the debugger interface, mapped externally at 0FFFCh-0FFFFh.) The internally-mapped addresses include the Stack registers and the Pulse Width Modulator registers. The RSC-300/364 also has 2 Kbytes of internal data space SRAM. This SRAM is reserved for technology functions and does not conflict with external SRAM.

Stack Registers (8 each of 16 bits)

Occasionally it is useful to manipulate the stack directly (for example, to leave a deeply nested series of calls without unwinding when a fatal error is detected.). Since the RSC-300/364 stack space is limited, the need for such manipulations is unlikely, but the information here allows doing so if desired. The stack pointer registers are described on page 31.

Address	Location Name	Type	Notes
0FFC0h	Stack 0 Low byte	R/W	
0FFC1h	Stack 0 High byte	R/W	
0FFC2h	Stack 1 Low byte	R/W	
0FFC3h	Stack 1 High byte	R/W	
0FFC4h	Stack 2 Low byte	R/W	
0FFC5h	Stack 2 High byte	R/W	
0FFC6h	Stack 3 Low byte	R/W	
0FFC7h	Stack 3 High byte	R/W	
0FFC8h	Stack 4 Low byte	R/W	
0FFC9h	Stack 4 High byte	R/W	
0FFCAh	Stack 5 Low byte	R/W	
0FFCBh	Stack 5 High byte	R/W	
0FFCCh	Stack 6 Low byte	R/W	
0FFCDh	Stack 6 High byte	R/W	
OFFCEh	Stack 7 High	R/W	

Pulse Width Modulator (PWM) Registers

The Pulse Width Modulator registers enable and control the operation of the PWM. When producing speech or music, these registers are controlled by Sensory's technology code and should not be touched by applications.

Address	Location Name	Type	Page
0FFE0h	PWMCTRL	W/O	45
0FFE1h	PWMA	W/O	45
0FFE2h	PWMDATA	R/W	46

PWM Control Register (Data Space Address 0FFE0h)

msb **PWMCTRL** lsb

D7	D6	D5	PWMEN	FADJEN	S2	S1	S0

This register is used to enable the PWM, the PWM frequency adjust, and to select the sample period. The PWM sample rate is derived from Osc#1, divided by various factors controlled by the PWM registers. Sensory's library code may initialize specific settings for this register, so it should be changed only with care.

Bit Description:

PWM_CTRL[2:0]: Sample period

The PWM rate is proportional to 1/(8-S). The fastest rate occurs with S=7. The slowest rate occurs with S=0.

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Cleared by reset

PWMCTRL.3: FADJEN

When the FADJEN bit is set, the PWM rate is further reduced by the value in the PWM_A register as described below.

0: Disable PWM Frequency adjust. PWM sample rate = OSC1/(256*(8-S))

1: Enable PWM Frequency adjust. PWM sample rate = OSC1/((512-A)*(8-S))

Cleared by reset.

PWMCTRL.4: PWMEN

0: Disable Pulse Width Modulator outputs

1: Enable Pulse Width Modulator outputs

Cleared by reset.

PWM Adjust Register (Data Space Address 0FFE1h)

msb				**PWMA**			lsb
D7	D6	D5	D4	D3	D2	D1	D0

The PWM Adjust Register contains an 8-bit unsigned value that may further reduce the sample rate of the PWM. If the FADJEN bit is set, then (256-A) wait states are inserted at the end of each sample period.

- If A=0, 256 wait states are inserted.
- If A=0FFh, one wait state is inserted.

During the wait period, the active output goes to zero. Thus, in addition to lowering the sample rate, smaller values of A also reduce the filtered analog output level.

Bit Description:

PWM_A: Frequency adjust bits D0 through D7
Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access:
Also refer to: PWMCTRL, FLAGS, IMR, IRQ

PWMDATA Register (Data Space Address 0FFE2h)

msb				**PWMDATA**			lsb
D7	D6	D5	D4	D3	D2	D1	D0

The PWMDATA Register contains an 8-bit unsigned value that determines the output pulse pattern (duty cycle) of the active PWM output. When D7=0, the PWM0 output is active and the PWM1 output is zero. The largest output signal for PWM0 is obtained with D=00h. When D7=1, the PWM1 output is active and the PWM0 output is zero. The largest output signal for PWM1 is obtained with D=0FFh. The PWM repeats each data pulse pattern once each sample period. At the end of a sample period, the PWM sets PWMIRQ. The interrupt service routine may provide a new data value. If the IRQ is not serviced, the PWM continues to output the data originally stored in PWMDATA. Output data always lags input by one PWM sample period.

Bit Description:

PWMDATA: Pulse Width Modulator data bits D0 through D7
Initialization: All bits cleared to 0 upon reset
Read Access:
Write Access:
Also refer to: PWMCTRL, PWM_A

Quality and Reliability

Sensory strives to improve customer satisfaction through the on-time delivery of quality products that exceed customer expectations and requirements. To meet these needs, Sensory is committed to the goal of continuous quality improvement. Each organization within the company is empowered to develop and implement programs that improve the quality of products delivered by Sensory. Sensory's quality program extends not only to internal employees, but to its subcontractors and consultants. Sensory works closely with subcontractors to integrate their quality programs within Sensory's own program.

Reliability and Overview

Sensory's reliability program characterizes Sensory products and identifies areas for future improvement. Sensory's overall program is divided into three main categories:

1. Qualification - This program ensures that new product designs, processes, and packages meet their established specifications (e.g., absolute maximum ratings and worst case criteria for use). A variety of tests and statistical analyses are used to create a high confidence level for determining device performance.
2. Monitoring - After qualification of a device, a monitoring program is used to check that ongoing products continue to meet the established operating conditions. A randomly selected sample of devices are used to monitor the predicted reliability of the products.
3. Evaluation and Improvement - This program continuously evaluates the results of the qualification and monitoring programs to identify areas for improvement. Failure analysis is used to understand the test results and insure quality products are being shipped to customers.

Sensory's reliability testing is designed to deliver commercial grade parts. Since Sensory uses top quality manufacturers and designs to stringent requirements, the RSC-300/364 may meet higher reliability standards (e.g., industrial, automotive).

Reliability Tests

Sensory's reliability testing focuses on the RSC-300/364 in a 64-pin TQFP package. Reliability testing is accomplished by subjecting devices to a variety of stress conditions that accelerate failure mechanisms. The tests used by Sensory have been defined by several industrial standards. JEDEC 22 is the source for most of the testing methods used by Sensory in its reliability program.

This document outlines Sensory's reliability testing for the RSC-300/364. This testing outlines the set of tests performed on the RSC-300/364 in order insure that our products meet their listed specifications. Customers interested in higher levels of reliability should contact Sensory. Sensory uses a combination of independent testing houses and vendors to augment Sensory's internal staff.

Reliability Test Descriptions

The following tests were used to determine the reliability of the RSC-300/364. The Table below summarizes each of the tests performed.

Test	Standard	Conditions
Physical Dimensions	JEDEC-STD-22B-B100	
Mark Permanency	JEDEC-STD-22B-B107	
Solderability	JEDEC-STD-22B-B102	
Autoclave	JEDEC-STD-22B-A102-A	96 hours, 30 psi
Preconditioning	JEDEC-STD-22-A113	Level 3
Bias Life	JEDEC-STD-22B-A108	+125C, 1008 hours
HAST	JEDEC-STD-22-A110-A	100 hrs, 120C, 85%RH, 33.3 psi
Lead Integrity	JEDEC-STD-22B-B105-A	
Resistance to Soldering Heat	JEDEC-STD-22B-B106	
Thermal Shock	JEDEC-STD-22B-A106	-65/+150C, 500 cycles
Temperature Cycling	MIL-STD-883-1010.7	-65/+150C, 2000 cycles
ESD	MIL-STD-883-3015.7	HBM, 2000V
Latch Up	EIJ/JESD-STD-78	Class 1

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Package/Process

1. **Autoclave** - reference method JEDEC-STD-22, Method A102-A
   This unbiased test evaluates the moisture resistance of nonhermetic solid-state devices. Devices are subjected to severe conditions of pressure, humidity and temperature to accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors that pass through it. This test is performed under the following conditions: TA=~121C, 100% RH, P=30 psi, 96 hours.
2. **Preconditioning -** reference method JESD-STD-22, Method A113, Level 3.
   This test method simulates a typical industry multiple solder reflow operation. Plastic surface mounted devices are subjected to this test before being submitted to reliability testing. Level 3 refers to the exposed shelf life of the device, which is 168 hours after removal from a vapor barrier bag. This method is also used as an indicator for the package's resistance to typical moisture conditions found in board assembly.

Package/Chip

1. **Bias Life** - reference method JEDEC-STD-22, Method A108
   This test is performed to determine the effects of bias conditions and temperature on solid state devices over an extended period of time. This test accelerates failure mechanisms that are activated by temperature while under bias, and is used to predict long term failure rates based on accepted methods of calculation using acceleration by temperature. It is intended primarily for device qualification and reliability monitoring. This test is performed at a temperature of 125°C for 1008 hours.
2. **Highly Accelerated Temperature And Humidity Stress Test (HAST)**
   Reference method JESD-STD-22, Method A110-A. This test is performed to determine the reliability of non-hermetic packaged solid-state devices in humid environments. It accelerates the penetration of moisture through the device by subjecting the device to severe temperature, humidity, and bias. This test usually activates the same failure modes as JEDEC-STD-22, Method A101 (85/85). The testing conditions are 120C, 85% RH, and 33.3 psia for a duration of 100 hours.
3. **Electrostatic Discharge (ESD)** - reference method MIL-STD-883, Method 3015.7
   This test is performed to determine the susceptibility of the device to a defined electrostatic Human Body Model discharge.
4. **Latch Up** - reference method EIJ/JESD-STD-Method 78
   This test is performed to determine IC latch up characteristics in order to ensure reliability and minimizing failures due to Electrical Overstress.

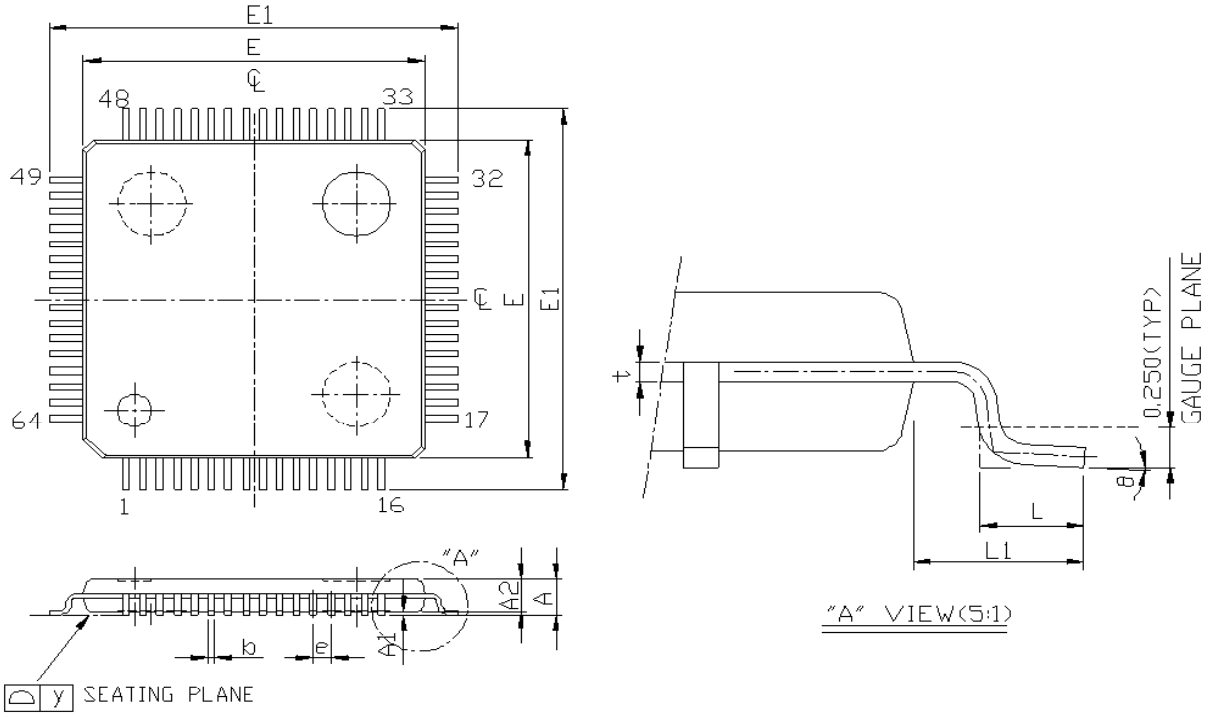
Package Design

1. **Lead Integrity** - reference method JEDEC-STD-22, Method B105-A
   This overall test includes various tests for determining the integrity of device leads, welds, and seals. Devices are subject to various stresses and are then examined for failure criteria.
2. **Resistance to Soldering Heat** - reference method JEDEC-STD-22, Method B106
   This test provides a method for determining whether device leads can withstand the effects of temperature during soldering.
3. **Thermal Shock** - reference method JEDEC-STD-22, Method A106
   This test determines the ability of solid state devices to withstand exposure to extreme changes in temperature. Temperature is cycled to expose damage caused by differing expansion coefficients of the die and package. This test occurs with the chip immersed in liquid. The test consists of 500 cycles between low temperature (-65°C) and high temperature (+150°C) with an immersion time at each temperature of at least five minutes and transitions of ten seconds or less.
4. **Temperature Cycling** - reference method MIL-STD-883-1010.7
   This test determines the resistance of a device to extremes of high (+150°C) and low (-65°C) temperatures, and alternate exposures to these extremes. This test accelerates the effects of temperature changes caused by differing expansion coefficients of the die and package. This test consists of 2000 cycles between low temperature and high temperature with a transition time not to exceed five minutes. Dwell at each extreme is ten minutes.

Packaging

The RSC-300/364 is available as tested, singulated die, tested wafers, or in a 64 lead, 10 x 10 x 1.0 mm TQFP package.

TQFP Mechanical Dimensions



Unit/Symbol	MM (BASE)	INCH (REF)
A	1.200 (MAX)	0.047 (MAX)
A1	0.100±0.05	0.004±0.002
A2	1.00±0.05	0.039±0.002
b	0.170~0.270	0.007~0.011
E1	12.000±0.100	0.472±0.004
E	10.000±0.100	0.394±0.004
e	0.500 (TYP)	0.020 (TYP)
t	0.127 (TYP)	0.005 (TYP)
y	0.076 (MAX)	0.003 (MAX)
θ	0~7°	0~7°
L	0.006±0.150	0.024±0.006
L1	1.000 (REF)	0.039 (REF)

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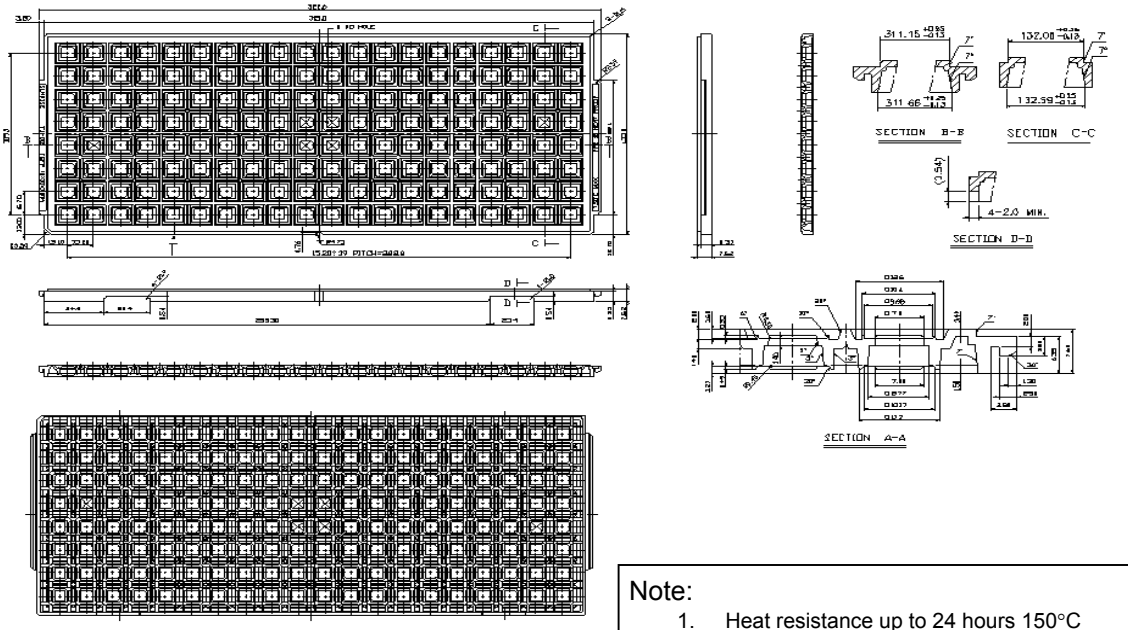
TQFP Tray Mechanical Dimensions



Note:
1. Heat resistance up to 24 hours 150°C
2. Surface electric resistivity less than 10^{12} Ω/sq
3. Warpage is within 0.76mm
4. Tolerance: x=±0.5mm, x.x=±0.25mm, x.xx=±0.13mm

Ordering Information

Part	Shipping P/N	Marketing P/N	Description
RSC-300A Die	65-0087	C300XS1P	Tested, Singulated RSC-300 die in waffle pack
RSC-300B Die	65-0098	C30BXS1P	Tested, Singulated RSC-300B die in waffle pack
RSC-300 QFP	65-0111	C300XV1T	RSC-300 64 pin 10 x 10 x 1.0 mm TQFP
RSC-364 Die	(ROM specific)	C364XS1P	Tested, Singulated RSC-364 die in waffle pack
RSC-364 QFP	(ROM specific)	C364XV1T	RSC-364 64 pin 10 x 10 x 1.0 mm TQFP

The Interactive Speech™ Product Line

The Interactive Speech line of ICs and software was developed to "bring life to products" through advanced speech recognition and audio technology. The Interactive Speech Product Line was designed for consumer telephony products and cost-sensitive consumer electronic applications such as home electronics, personal security, and personal communication. The product line includes award-winning RSC series general-purpose microcontrollers and tools, SC series of speech microcontrollers, plus a line of easy-to-implement chips that can be pin-configured or controlled by an external host microcontroller. Sensory's software technologies run on a variety of microcontrollers and DSPs.

RSC Microcontrollers and Tools

The RSC product line contains low-cost 8-bit speech-optimized microcontrollers designed for use in consumer electronics. All members of the RSC family are fully integrated and include A/D, pre-amplifier, D/A, ROM, and RAM circuitry. The RSC family can perform a full range of speech/audio functions including speech recognition, speaker verification, speech and music synthesis, and voice record/playback. The family is supported by a complete suite of evaluation tools and development kits.

SC Microcontrollers and Tools

The SC-6x product line feature the highest quality speech synthesis ICs at the lowest data rate in the industry. The line includes a 12.32 MIPS processor for high-quality low data-rate speech compression and MIDI music synthesis, with plenty of power left over for other processor and control functions. Members of the SC-6x line can store as much as 37 minutes of speech on chip and include as much as 64 I/O pins for external interfacing. Integrating this broad range of features onto a single chip enables developers to create products with high quality, long duration speech at very competitive price points.

Application Specific Standard Products (ASSPs)

Voice Direct™ 364 provides inexpensive speaker-dependent speech recognition and speech synthesis. This easy-to-use, pin-configurable chip requires no custom programming and can recognize up to 60 trained words in slave mode, and 15 words in stand-alone mode. Ideal for speaker-dependent command and control of household consumer products, Voice Direct™ 364 is part of a complete product line that includes the IC, module, and Voice Direct 364 Speech Recognition Kit.

Voice Extreme™ simplifies the creation of fully custom speech-enabled products by offering developers the capability of programming the chip in a high-level C-like language. Program code, speech data, and even record and playback information can be stored on a single off-chip Flash memory. Based on Sensory's RSC-364 speech processor, Voice Extreme includes a highly efficient on-chip code interpreter, and is supported by a comprehensive suite of low-cost development tools.

Software and Technology

Voice Activation™ micro footprint software provides advanced speech technology on a variety of microcontroller and DSP platforms. A flexible design with a broad range of technologies allows manufacturers to easily integrate speech functionality into consumer electronic products.

Fluent Speech™ small footprint software recognizes up to 50,000 words; offers Animated Speech with the ability to automate enunciation and articulation; performs text-to-speech synthesis in either male or female voices; provides noise and echo cancellation, performs word spotting for natural language usage; offers telephone barge-in; and provides continuous digit recognition.

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