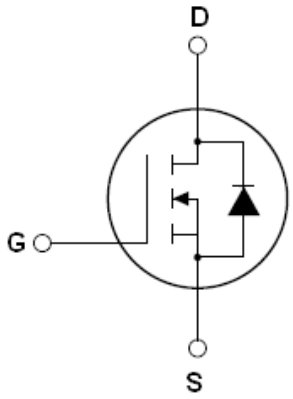
N-Channel Super Junction Power MOSFET Ⅱ

General Description

The series of devices use advanced super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.



Schematic diagram

Features

- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

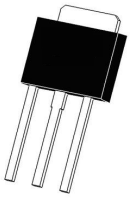
Application

- Power factor correction（PFC）
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）

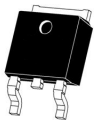
V_{DS}@T_{jmax}	710	V
$R_{DS(ON)\ Max}$	2.4	Ω
I_D	1.8	A

Package Marking And Ordering Information

Device	Device Package	Marking
RSU2N65MD	TO-251	RSU2N65M
RSU2N65D	TO-252	RSU2N65D



TO-251



TO-252

Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS}=0V）	V_{DS}	650	V
Gate-Source Voltage (V_{DS}=0V)	V_{GS}	±30	V
Continuous Drain Current at Tc=25°C	$I_{D\ (DC)}$	1.8	A
Continuous Drain Current at Tc=100°C	$I_{D\ (DC)}$	1.2	A
Pulsed drain current **(Note 1)**	$I_{DM\ (pluse)}$	5.4	A
Maximum Power Dissipation(Tc=25℃) Derate above 25°C	P_D	22 0.176	W W/°C
Single pulse avalanche energy **(Note2)**	E_{AS}	40	mJ
Avalanche current **(Note 1)**	I_{AR}	0.9	A
Repetitive Avalanche energy ， t_{AR} limited by T_{jmax} **(Note 1)**	E_{AR}	0.06	mJ

Parameter	Symbol	Value	Unit
Drain Source voltage slope, V_{DS} ≤480 V,	dv/dt	50	V/ns
Reverse diode dv/dt， V_{DS} ≤480 V,I_{SD}<I_D	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55...+150	°C

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	5.68	°C /W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	75	°C /W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			10	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	3	3.5	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=1A		2200	2400	mΩ
Dynamic Characteristics						
Forward Transconductance	g_{FS}	V_{DS} = 20V, I_D = 0.9A		1.9		S
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz		183		PF
Output Capacitance	C_{oss}			12		PF
Reverse Transfer Capacitance	C_{rss}			1.0		PF
Total Gate Charge	Q_g	V_{DS}=480V,I_D=1.8A, V_{GS}=10V		3.0	10	nC
Gate-Source Charge	Q_{gs}			0.6		nC
Gate-Drain Charge	Q_{gd}			1.1		nC
Intrinsic gate resistance	R_G	f = 1 MHz open drain		10		Ω
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=380V,I_D=0.9A, R_G=50Ω,V_{GS}=10V		6		nS
Turn-on Rise Time	t_r			3		nS
Turn-Off Delay Time	$t_{d(off)}$			64		nS
Turn-Off Fall Time	t_f			11		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	T_C=25°C			1.8	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				5.4	A
Forward On Voltage	V_{SD}	Tj=25°C,I_{SD}=1.8A,V_{GS}=0V		1	1.3	V
Reverse Recovery Time	t_{rr}	Tj=25°C,I_F=1.8A,di/dt=100A/μs		135		nS
Reverse Recovery Charge	Q_{rr}			0.6		uC
Peak reverse recovery current	I_{rrm}			8.2		A

Notes: 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. Tj=25℃,VDD=50V,VG=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

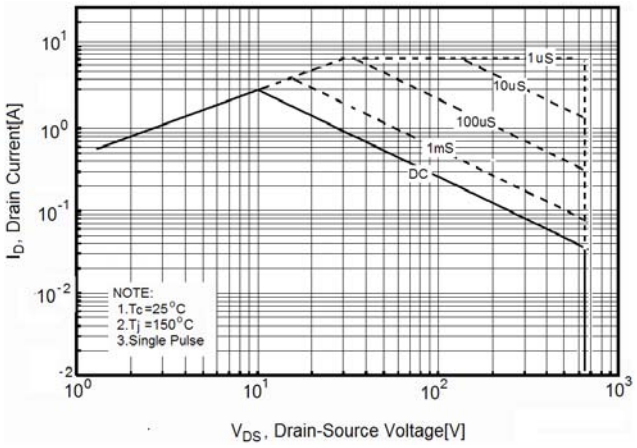


Figure2. Source-Drain Diode Forward Voltage

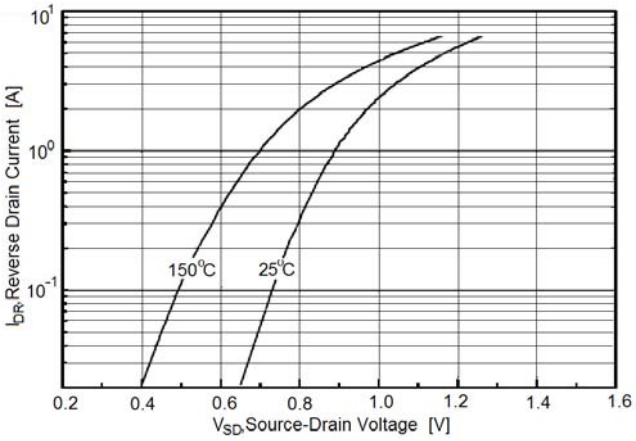


Figure3. Output characteristics

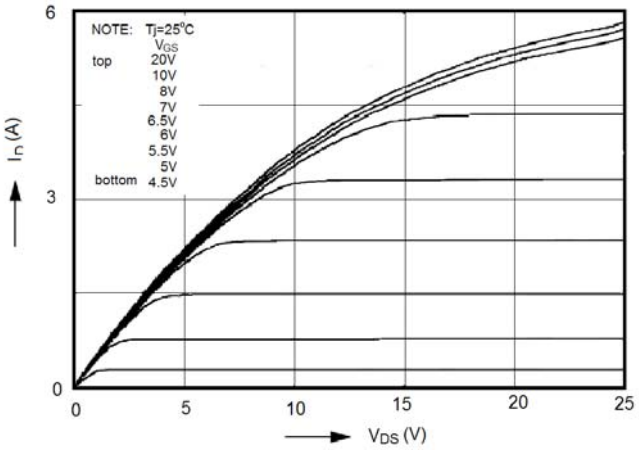


Figure4. Transfer characteristics

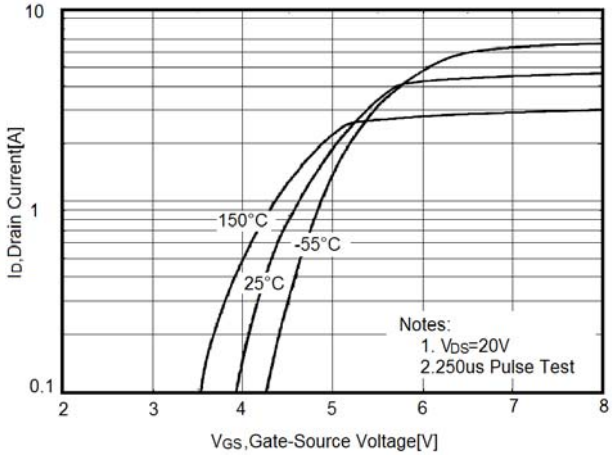


Figure5. Static drain-source on resistance

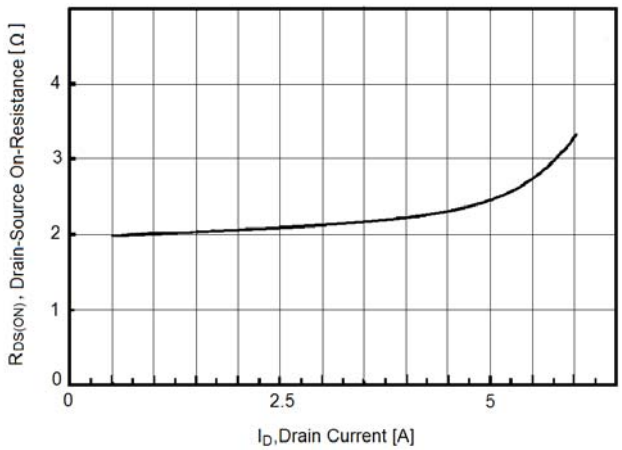


Figure6. $R_{DS(ON)}$ vs Junction Temperature

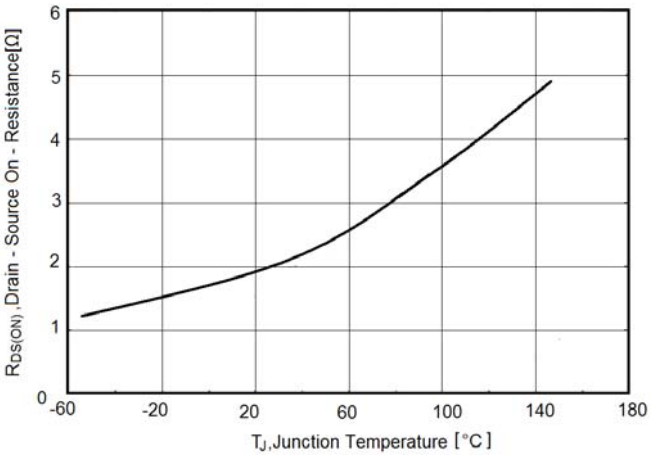


Figure7. BV_{DSS} vs Junction Temperature

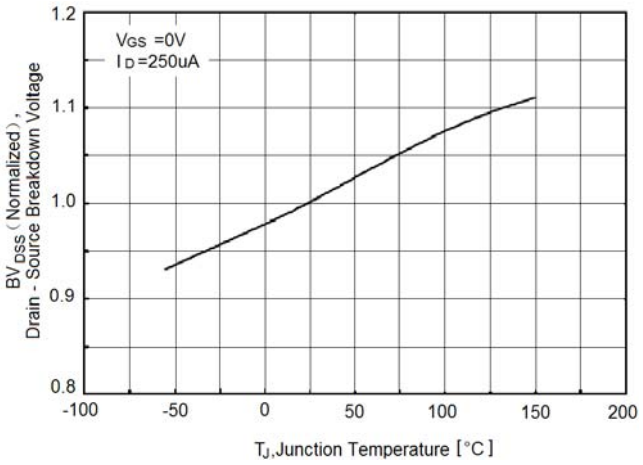


Figure8. Maximum I_D vs Junction Temperature

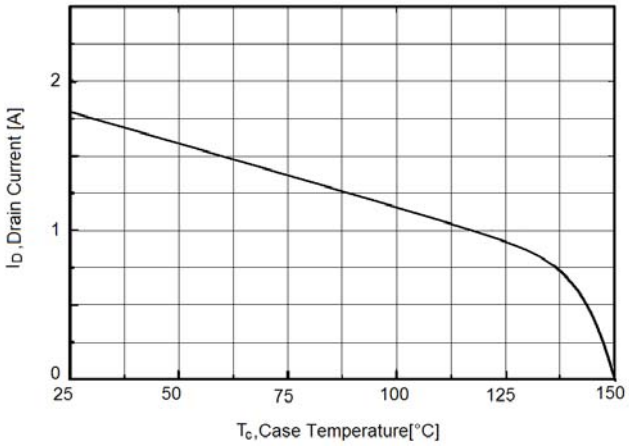


Figure9. Gate charge waveforms

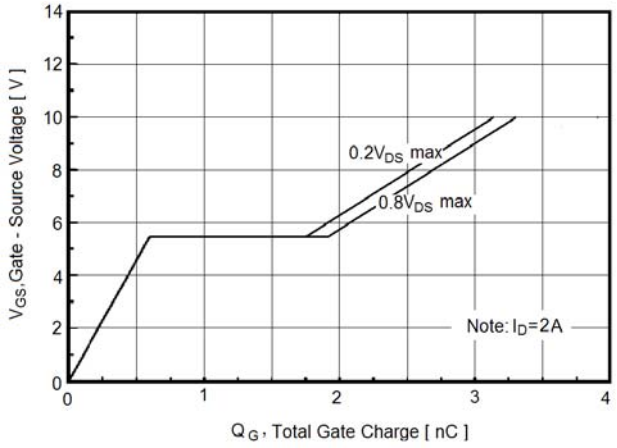


Figure10. Capacitance

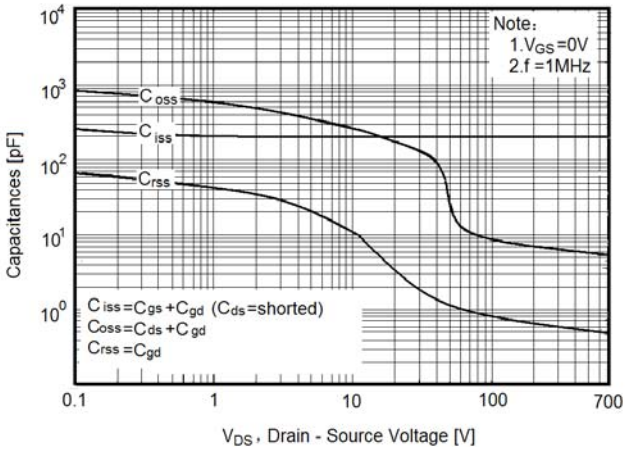
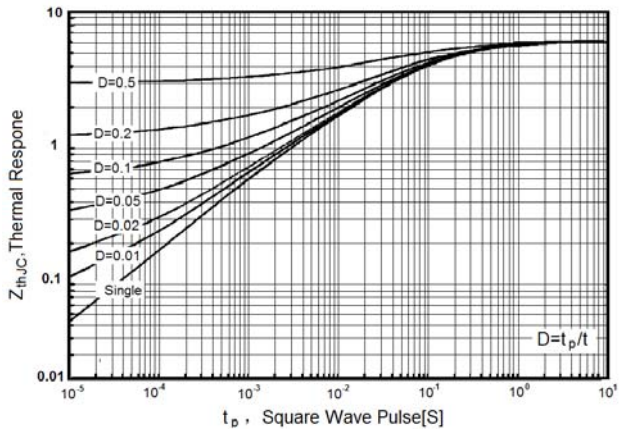
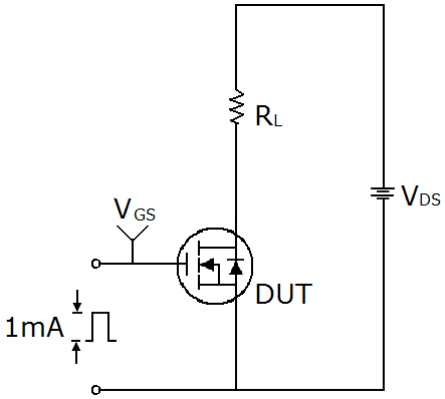


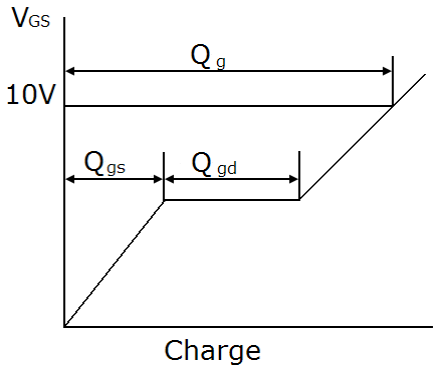
Figure11. Transient Thermal Impedance



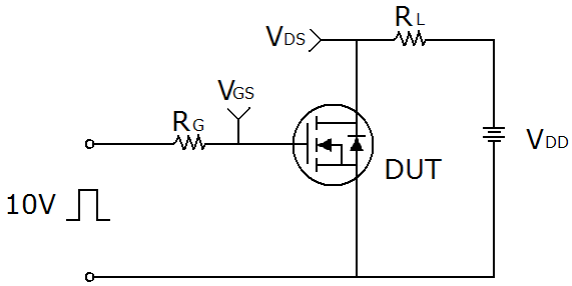
Test circuit

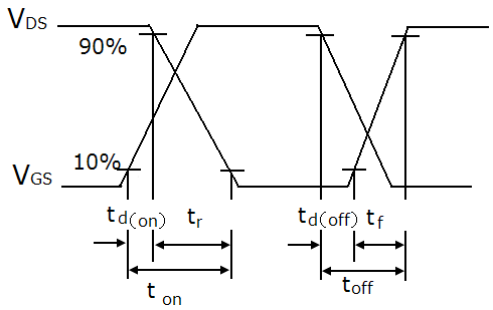
1）Gate charge test circuit & Waveform



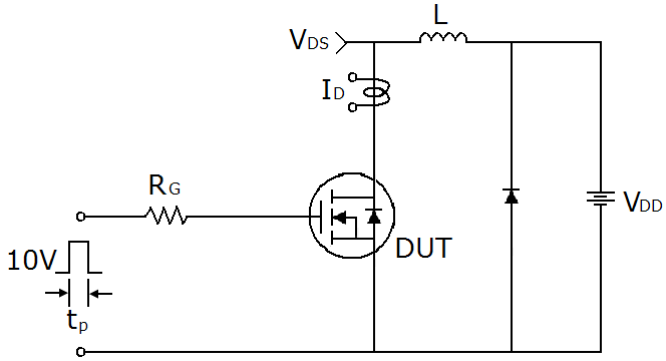


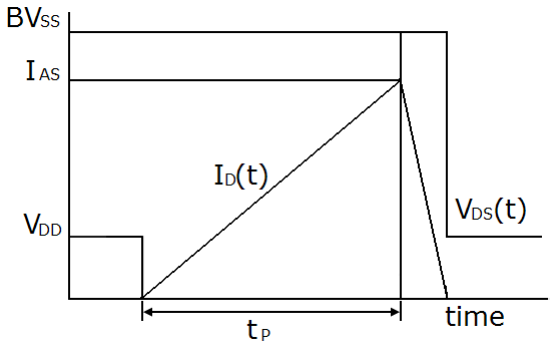
2）Switch Time Test Circuit：



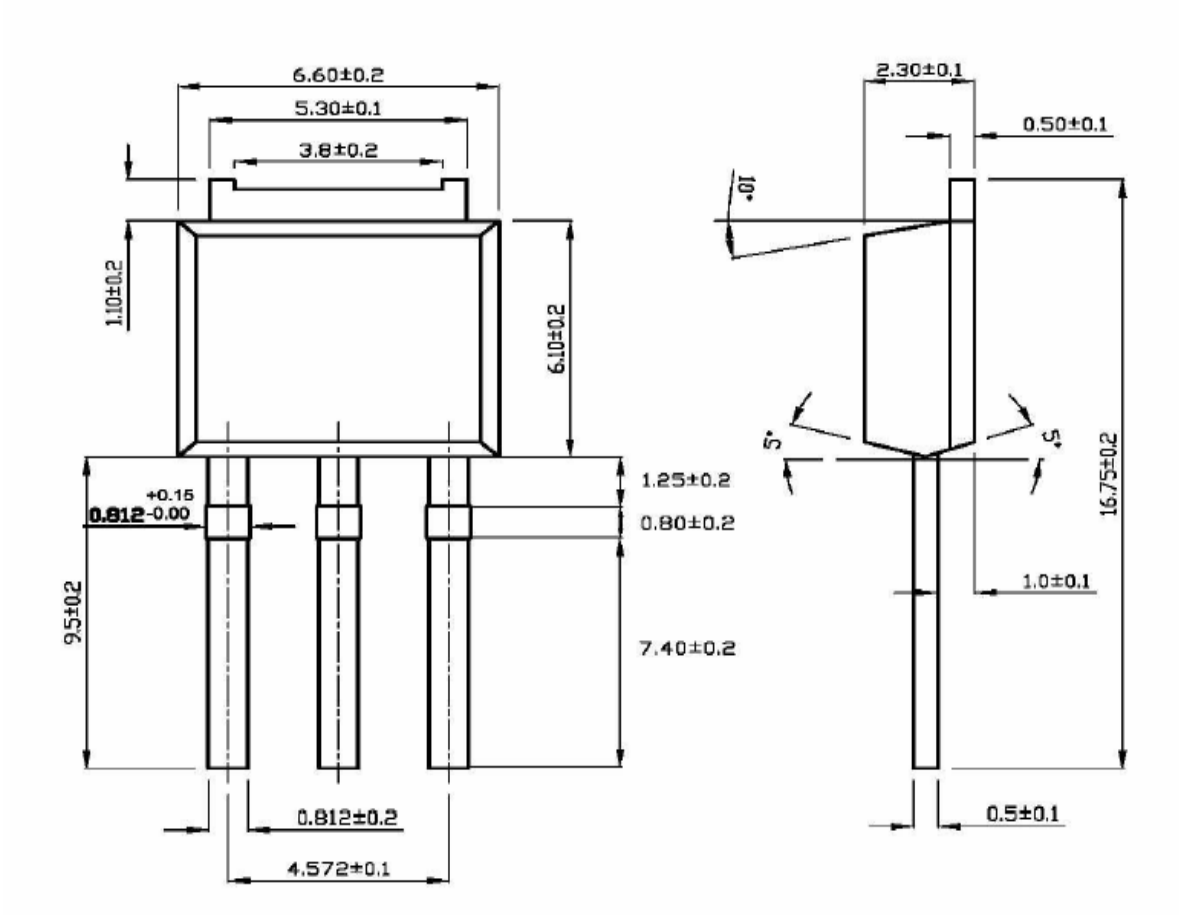


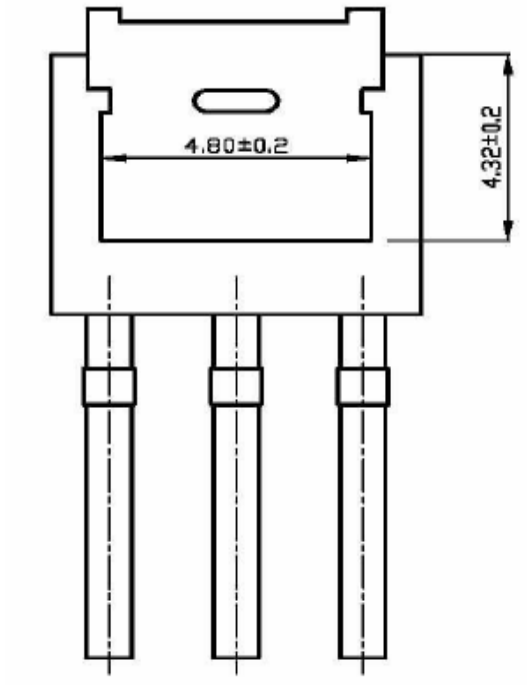
3）Unclamped Inductive Switching Test Circuit & Waveforms



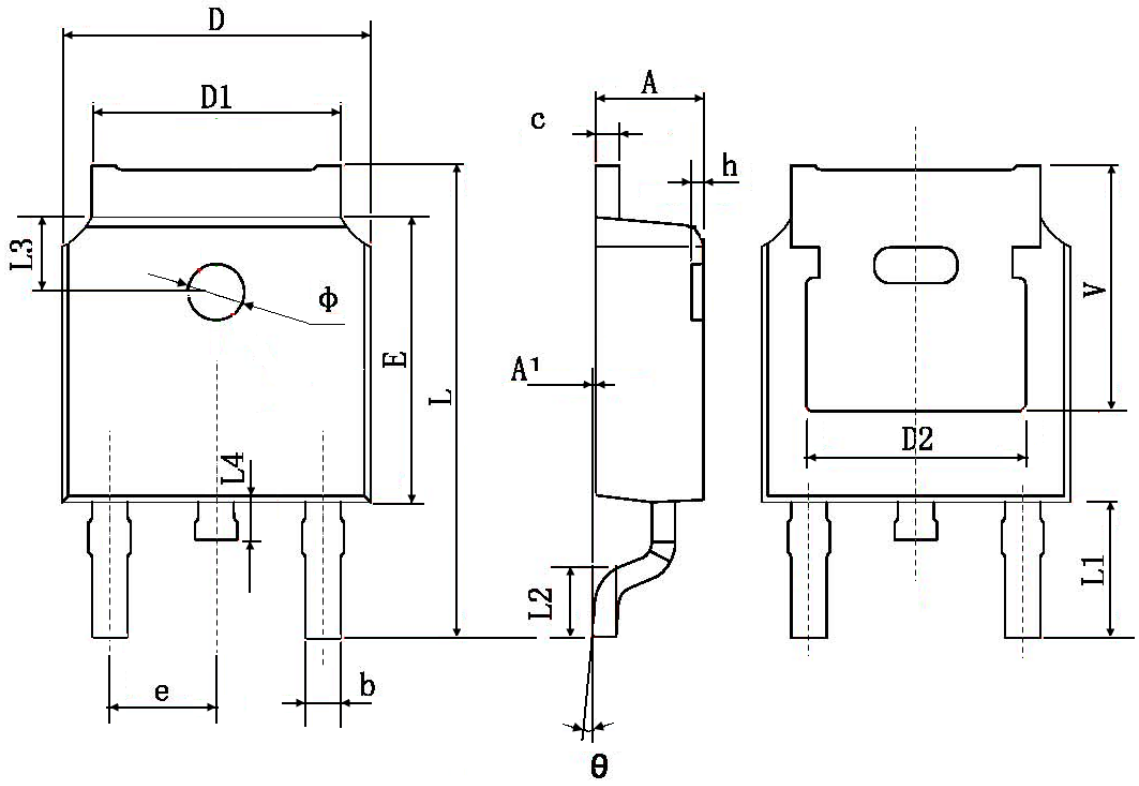


TO-251 Package Information





TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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