DDR Termination Regulator

General Description

The RT2526Q is a 2A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT2526Q possesses a high speed operating amplifier that provides fast load transient response and only requires 20µF of ceramic output capacitance. The RT2526Q supports remote sensing functions and all features required to power the DDRII/DDRIII VTT bus termination according to the JEDEC specification. In addition, the RT2526Q includes integrated sleep-state controls placing VTT in High-Z in S3 (suspend to RAM) The RT2526Q is available in the thermal efficient package SOP-8 (Exposed Pad).

Ordering Information

RT2526Q □□

Package Type
SP : SOP-8 (Exposed Pad-Option 1)

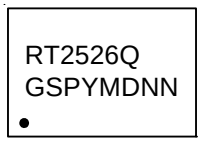
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT2526QGSP : Product Number

YMDNN : Date Code

Features

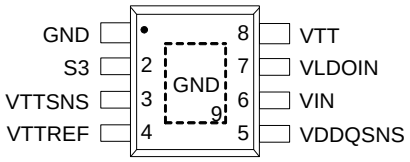
- **Supports DDRII and DDRIII, Low-Power Requirement**
  - **Source/Sink 2A for DDRII and DDRIII**
- **Input Voltage Range : 3.1V to 3.6V**
- **VLDOIN Voltage Range : 1.2V to 1.8V**
- **Requires Only 20µF Ceramic Output Capacitance**
- **Supports High-Z in S3**
- **Integrated Divider Tracks 1/2 VDDQSNS for Both VTT and VTTREF**
- **Remote Sensing (VTTSNS)**
- **±20mV Accuracy for VTT and VTTREF**
- **10mA Buffered Reference (Sourcing/Sinking) (VTTREF)**
- **Built-In Soft-Start**
- **Current Limit**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- DDRII, DDRIII Memory Termination
- SSTL-2, SSTL-18, HSTL Termination

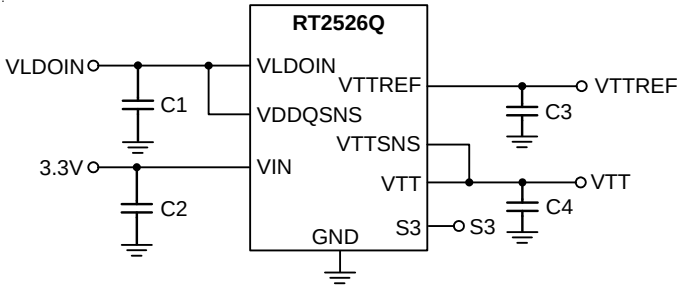
Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
2	S3	Active Low Suspend to RAM Mode Control Input. In S3 state, VTT is turned off and left High-Z, VTTREF is active.
3	VTTSNS	VTT Voltage Sense Input. Connect to plus terminal of the output capacitor.
4	VTTREF	Buffered Output. The reference output voltage equals to VDDQSNS / 2.
5	VDDQSNS	VLDOIN Sense Input.
6	VIN	Supply Voltage Input for Control Circuit.
7	VLDOIN	Power Input for VTT Output Stage.
8	VTT	Power Output of the Regulation. The output voltage equals to VDDQSNS / 2.

Function Block Diagram

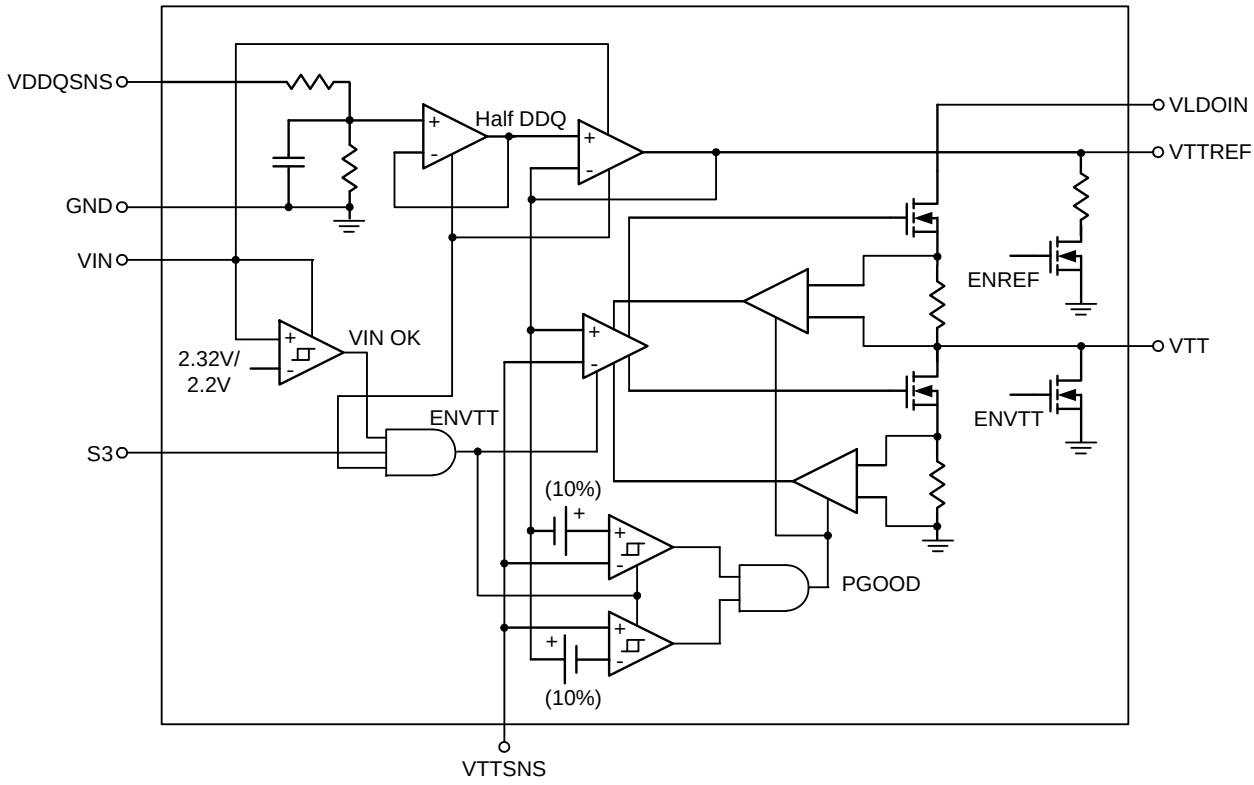


Table 1. S3 Control Table

State	S3	VTT	VTTREF
Normal	High	0.75V	0.75V
Standby	Low	High-Z	0.75V

Operation

Shutdown Mode

The shutdown mode will happen when the S3 input voltage is under the logic threshold. The VTT pin will be high impedance and VTTREF will remain active under shutdown mode.

VIN OK and Thermal Shutdown

The regulator will detect VIN voltage and junction temperature. When VIN is lower than the VIN OK threshold or the junction temperature is over the thermal shutdown threshold, both the VTT and VTTREF will be discharged to GND.

VTTREF Buffer

The buffer senses the input voltage from VDDQSNS and provides an internal reference voltage of VDDQSNS/2 for VTT regulator.

VTT Regulator

The VTT output is capable of sinking and sourcing current while sensing from the VTTSNS pin to regulate the output precisely to VTTREF.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- 6V
- Supply Input Voltage, VLDOIN, VDDQSNS ---------- 3.6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 2.04W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 49°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 3.1V to 3.6V
- Supply Input Voltage, VLDOIN, VDDQSNS ---------- 1.2V to 1.8V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, VLDOIN = VDDQSNS = 1.5V, T_A = –40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Current	I_{VIN}	No Load, S3 = 3.3V	--	--	2	mA
VIN Standby Current	I_{VINSTB}	No Load, S3 = 0V	--	--	300	µA
VLDOIN Supply Current	I_{VLDOIN}	No Load, S3 = 3.3V	--	--	2	mA
VLDOIN Standby Current	$I_{VLDOINSTB}$	No Load, S3 = 0V	--	--	10	µA
VDDQSNS Input Current	$I_{VDDQSNS}$	S3 = 3.3V	--	--	50	µA
VTTSNS Input Current	I_{VTTSNS}	S3 = 3.3V	--	--	1	µA
VTT Output Voltage	VTT	VDDQSNS = VLDOIN = 1.5V	0.735	0.75	0.768	V
VTTREF, VTT Output Tolerance	V_{VTTTOL}	VDDQSNS = VLDOIN = 1.5V, $\lvert I_{VTT} \rvert$ = 0A	–20	--	20	mV
		VDDQSNS = VLDOIN = 1.5V, $\lvert I_{VTT} \rvert$ = 1.5A	–40	--	40	
VTT Source Current Limit	$I_{VTTOCLsr}$	VTT = 0V	2.3	3.3	--	A
VTT Sink Current Limit	$I_{VTTOCLsk}$	VTT = VDDQSNS	2.3	4.3	--	A
VTTREF Output Voltage	V_{VTTREF}	VDDQSNS = 1.5V, I_{VTTREF} = 0mA	0.735	0.75	0.768	V
		VDDQSNS = 1.5V, I_{VTTREF} < 10mA	0.728	0.75	0.772	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
UVLO Threshold Voltage		V_{UVLO}	Rising	--	--	2.7	V
			Falling	1.4	--	2.4	
S3 Input Voltage	Logic-High	V_{IH}		1.6	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
S3 Input Leakage Current		I_{ILK}		--	--	1	μA
Thermal Shutdown Protection		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

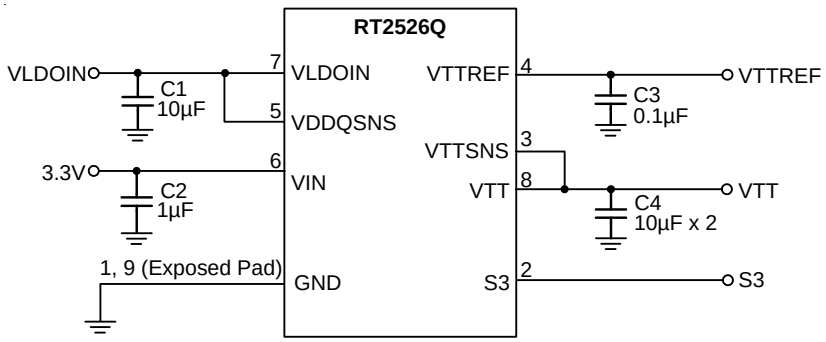
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

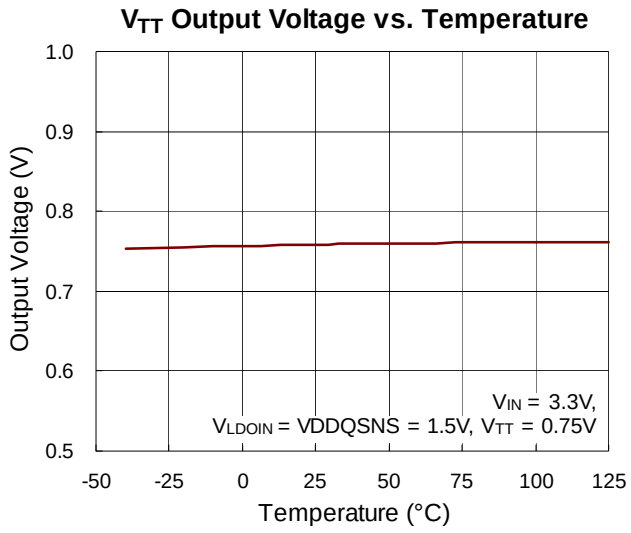
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

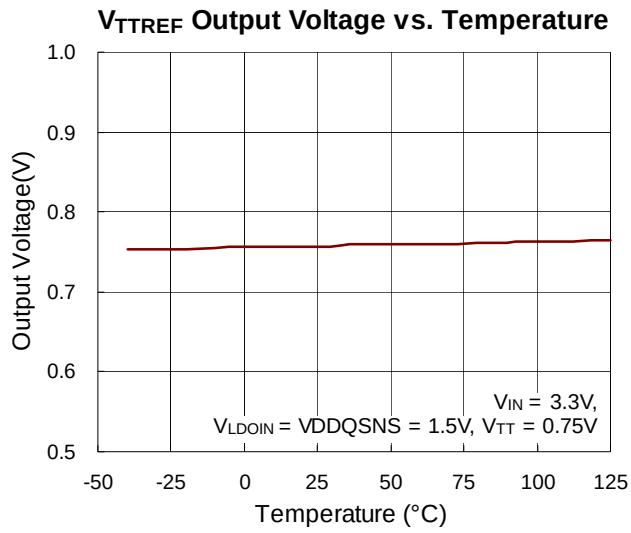
Note 4. The device is not guaranteed to function outside its operating conditions.

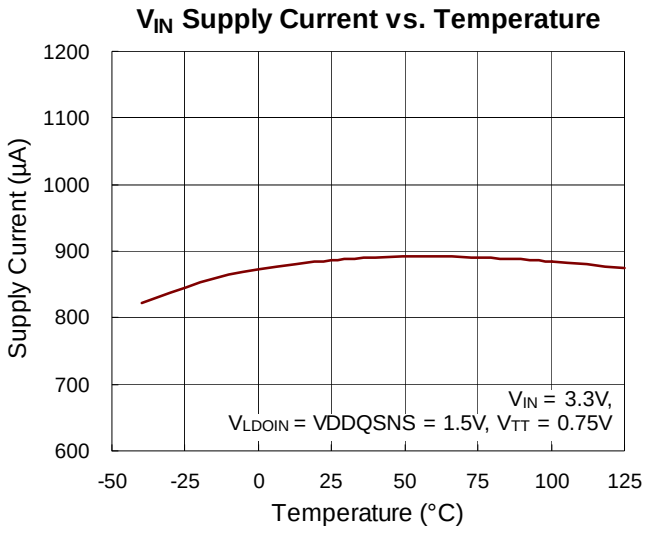
Typical Application Circuit

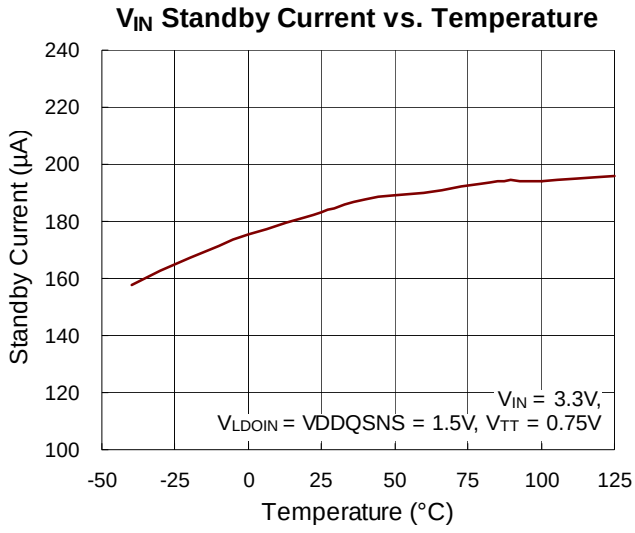


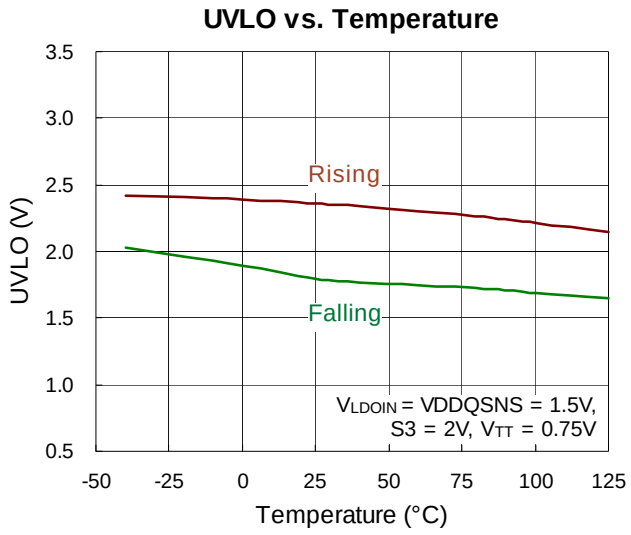
Typical Operating Characteristics

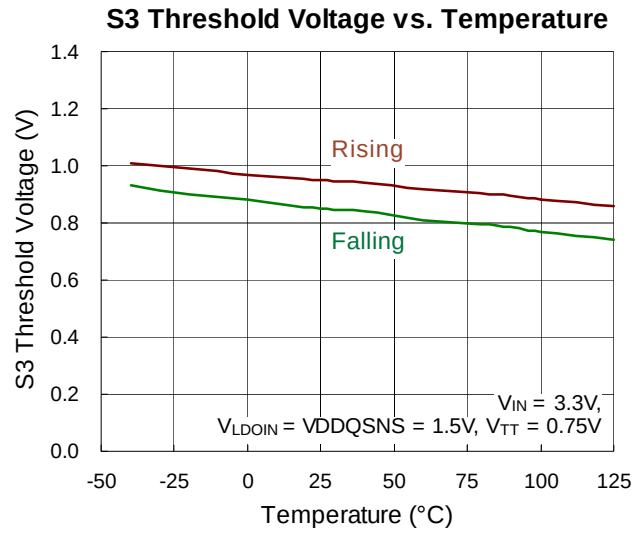




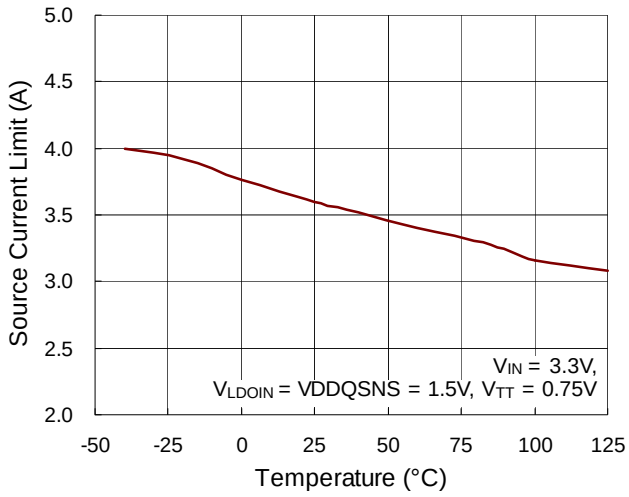




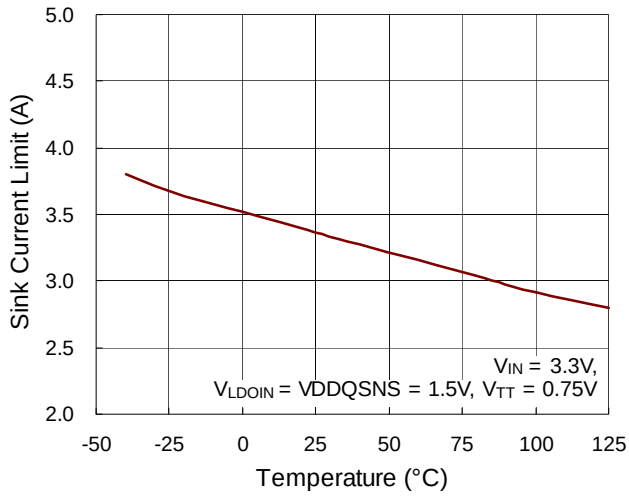




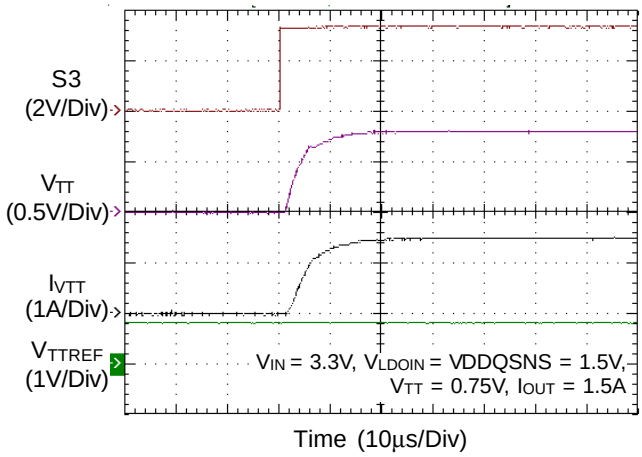
Source Current Limit vs. Temperature



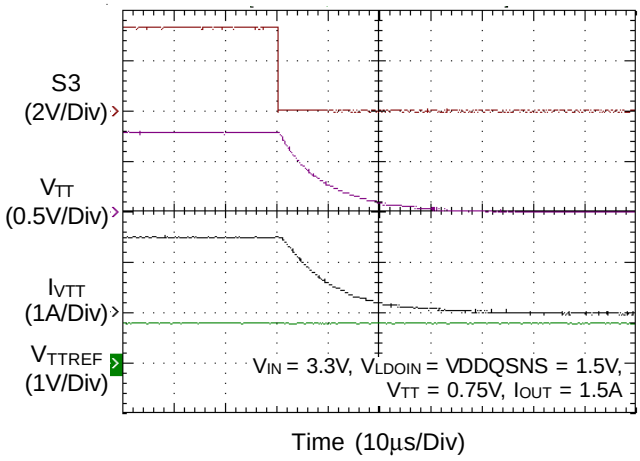
Sink Current Limit vs. Temperature



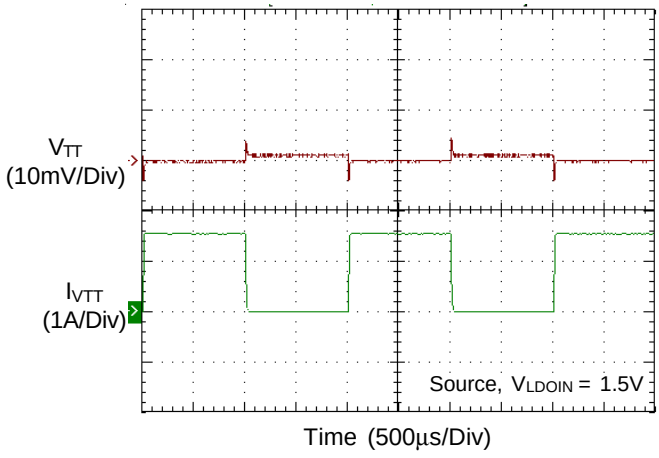
Power On from S3



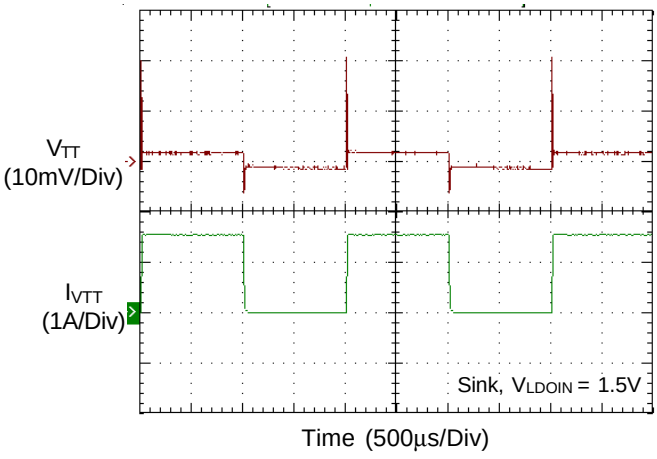
Power Off from S3



0.75VTT @ 1.5A Transient Response



0.75VTT @ 1.5A Transient Response



Application Information

The RT2526Q is a 2A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count system such as notebook PC applications. The RT2526Q possesses a high speed operating amplifier that provides fast load transient response and only requires a 10µF ceramic input capacitor and two 10µF ceramic output capacitors.

VTTREF Regulator

VTTREF is a reference output voltage with source/sink current capability up to 10mA. To ensure stable operation 0.1µF ceramic capacitor between VTTREF and GND is recommended.

S3 Logic Control

The S3 terminal should be connected to SLP_S3 signals respectively. Both VTTREF and VTT are turned on at normal state (S3 = High). In standby state (S3 = Low), VTTREF is kept alive while VTT is turned off and left high impedance.

Table 2. S3 Control Talbe

STATE	S3	VTT	VTTREF
Normal	H	ON	ON
Standby	L	OFF (High-Z)	ON

Capacitor Selection

Good bypassing is recommended from VLDOIN to GND to help improve AC performance. A 10µF or greater input capacitor located as close as possible to the IC is recommended. The input capacitor must be located at a distance of less than 0.5 inches from the VLDOIN pin of the IC.

Adding a 1µF ceramic capacitor close to the VIN pin and it should be kept away from any parasitic impedance from the supply power. For stable operation, the total capacitance of the ceramic capacitor at the VTT output terminal must not be larger than 30µF. The RT2526Q is designed specifically to work with low ESR ceramic output capacitor in space saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. The output capacitor should be located near the VTT output terminal pin as close as possible.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.04W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

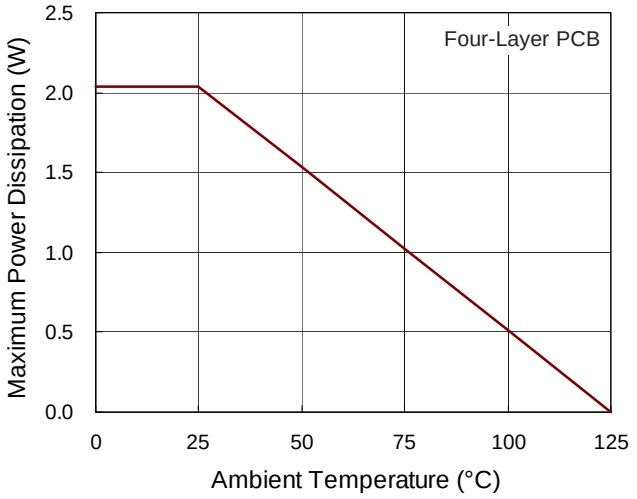
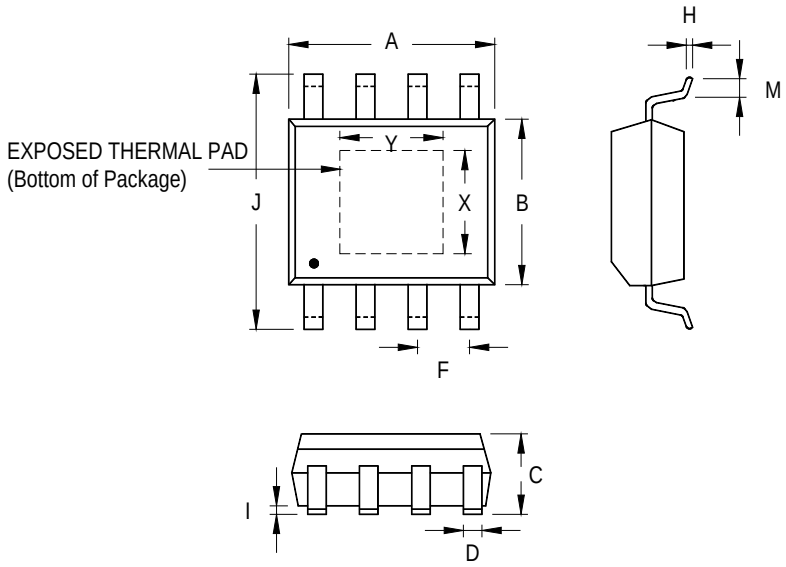


Figure 1. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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