RT2571W

Data sheet

Revision June 22, 2007

Applications

- IEEE802.11a/b/g Wireless Local Area Networks
- Wireless Portable Device/Notebook Computer

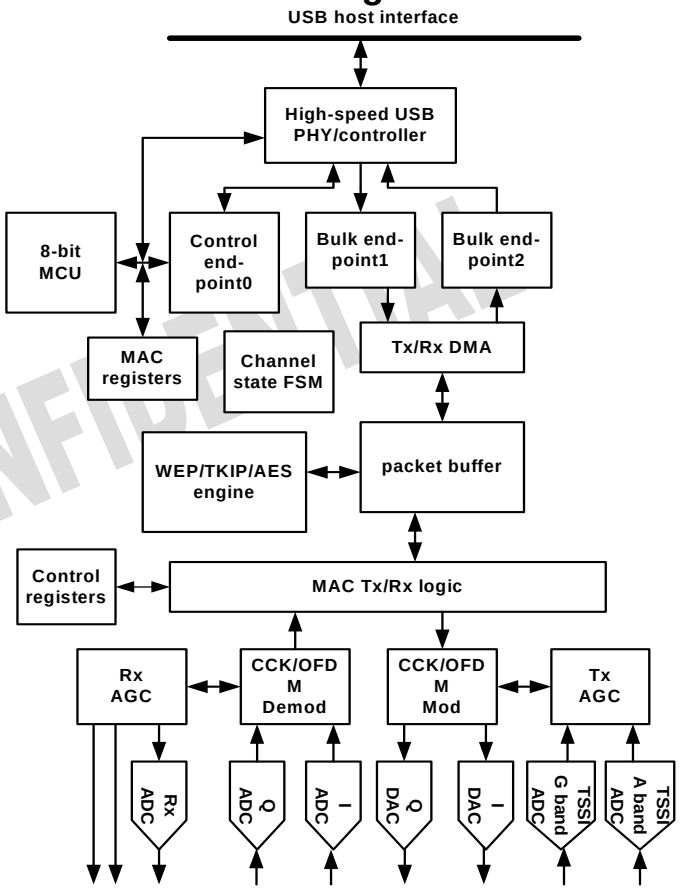
The RT2571W is a highly integrated MAC/baseband processor to support IEEE 802.11a/b/g USB wireless LAN Standards. The processor is part of Ralink chip set RT2501USB for the baseband part, it supports the Direct Sequence Spread Spectrum (DSSS) for 2.4GHz band and Orthogonal Frequency Division Multiplexing (OFDM) for 2.4GHz and 5GHz bands. Using advanced digital signal processing technologies, the optimal reception performance under severe multi-path environments is achieved.

For the MAC part, it provides all the required functions and many optional features in the IEEE standards, such as 802.11e (QOS), 802.11h (TPC/DFS), 802.11i (Security). It has many on-chip acceleration engines to ensure that the highest MAC performance is achieved without overloading host processing power.

Using advanced algorithms and design methodologies, the chip is best-in-class in terms of throughput, power consumption, range and multi-path tolerance.

The RT2571W housed in a 180-pin 12*12mm^2 TFBGA package is well suited for embedded applications. External Interfaces include USB 1.1/ USB 2.0.

Functional Block Diagram



Features

- Host interface: USB1.1 / USB 2.0
- Full Implementation of the MAC Protocol specified in IEEE Standards 802.11-1999 and 802.11g and 802.11g-2003
- Supported Operating System: Windows XP, Windows2000, Windows ME, 98SE, Linux
- Security: 64/128 WEP, WPA, AES
- Advanced Power Saving Algorithm for Dynamic Network Traffic Environment
- On-Chip A/D and D/A Converters for I/Q Data, TSSI and AGCs
- Supports Short Preamble
- Proprietary Robust Demodulator with Patent Protection
- Mitigates Multipath Delay Spread up to 100ns at 54Mbps
- 8 GPIOs interface for WAN extension.
- 2 configurable LEDs to release CPU from LED routine loading
- Support NOR-type flash interface
- Supports 6, 9, 12, 18, 24, 36, 48, 54 Mbps for OFDM; 5.5, 11Mbps for CCK; and 1,2 Mbps for Barker modulation.

Order Information

Part Number	Temp Range	Package
RT2571WF	-10 to 85°C	Lead-free 180B TFBGA

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Cupertino, CA95014 http://www.ralinktech.com

Pin Out

TFBGA180

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DP	DM	ADDR12	ADDR11	ADDR10	ADDR9	ADDR6	ADDR0	DATA4	DATA1	NC	IREQN	PLLCLK	NC
B	NC	RREF	ADDR13	ADDR14	XSCO	SUSPENDM	ADDR7	ADDR3	DATA6	PCMREGN	WAITN	NC	NC	GPIO7
C	NC	GND3_U20	VCC3_U20	XSCI	ADDR8	ADDR15	ADDR5	ADDR2	DATA5	DATA0	NC	BYPASSPLL	NC	GPIO6
D	VCC3IO_U20	RPU	GND18_U20	VCC18_U20	NC	ADDR4	ADDR1	DATA7	DATA2	DATA3	NC	R/B	PLLVDDA	GPIO5
E	TEST_EN	GNDA_U20	NC	GRSTN	GND	VDD_C18	GND	VDDIO	GND	GND	VDD_C18	NC	CEN	GPIO4
F	SCAN_EN	UDCLKSEL	PLL_MODE	VCCA_U20	GND					GND	VDDIO	WPN	NC	GPIO3
G	NC	NC	NC	UDCLK	VDDIO					GND	VDDIO	GPIO1	GPIO2	RF_SD
H	NC	EECS	EECLK	VDD_C18	GND					GND	VDD_C18	RF_LE	GPIO0	RF_SCLK
J	NC	EEDI	LED_ACT	ANSEL_P	GND					VSS33D	VSS33D	GNDSH	NC	NC
K	NC	ANSEL_N	TR_SW_P	VDDIO	GND	GND	VSS18	VSS18	VSS18	VSS33A	VSS33D	VREF	VREF025N	VREF025P
L	NC	TR_SW_N	TR_PE	PA_PE_G	VDD_C18	VDDIO	IREF	VCC18	VCC18	VSS33A	VSS33A	VCC33D	VCC33D	VCC33A
M	NC	EEDO	LED_RDY	NC	AGC_LNA1	VDDIO	AGC	VCC18	GNDSH_DAC	VSS33A	VCC33A	VCC33A	VSS33A	VCC33D
N	RADIO_PE	PA_PE_A	VGA_PULSE	AGC_LNA0	VGA_VALUE1	NC	RFTXI_P	RFTXI_N	NC	TSSI_A	VCC33A	VCC33A	VREFN	RFRXQ_N
P	RF_PE	VGA_VALUE0	VGA_VALUE2	VGA_VALUE3	VGA_VALUE4	NC	RFTXQ_P	RFTXQ_N	NC	TSSI_G	RFRXI_P	RFRXI_N	VREFP	RFRXQ_P

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Pin Description

*Notation: I (Input)., O (Output), I/O (Bi-direction)

Pin No	Pin Name	I/O type	Description
Global signals (9)			
E4	GRSTN	I, pull-up	Global reset, active low.
E1	TEST_EN	I, pull-down	Scan test mode enable. Connect to GND 0: Normal mode. 1: Test mode.
F1	SCAN_EN	I, pull-down	Scan enable. Connect to GND 0: Normal mode. 1: Scan mode.
G4	UDCLK	O	12MHz clock generated by internal PLL.
F3	PLL_MODE	I	Internal PLL mode. 0: PLL can be set to power-down by MAC. 1: PLL is always active. Connect to VCC if use only one crystal.
F2	UDCLKSEL	I, pull-down	Connect to GND.
A13	PLLCLK	I	Base-band 40MHz clock input.
C12	BYPASSPLL	I, pull-down	Bypass internal base-band PLL. Connect to GND.
B6	SUSPENDM	O	Suspend for USB mode. 0: USB device is in power down mode 1: USB device is in normal mode
RF interface (37)			
J4	ANSEL_P	O	Antenna select positive output.
K2	ANSEL_N	O	Antenna select negative output.
M5, N4	AGC_LNA[1:0]	O	AGC LNA control signals.
N3	VGA_PULSE	O	VGA pulse for zero-IF RF.
P5,P4,P3,N5,P2	VGA_VALUE[4:0]	O	VGA value output for zero-IF RF.
N1	RADIO_PE	O	RADIO_PE control to RF system.
H12	RF_LE	O	RF latch enable of serial control interface.
K3	TR_SW_P	O	TR_SW positive output.
L2	TR_SW_N	O	TR_SW negative output.
H14	RF_SCLK	O	RF serial interface clock.
G14	RF_SD	O	RF serial interface data.
P1	RF_PE	O	RF_PE output.
L3	TR_PE	O	TR_PE output to RF system.
L4	PA_PE_G	O	Transmit PA Power enable to PA (Power Amplifier) of 2.4G RF.
N2	PA_PE_A	O	Transmit PA Power enable to PA (Power Amplifier) of 5.2G RF.
M7	AGC	O	Adaptive gain control to TX/RX side of RFIC.
L7	IREF	I	Reference current.
N7	RFTXI_P	O	Differential I+ output, from base-band DAC to RFIC.
N8	RFTXI_N	O	Differential I- output, from base-band DAC to RFIC.
P7	RFTXQ_P	O	Differential Q+ output, from base-band DAC to RFIC.
P8	RFTXQ_N	O	Differential Q- output, from base-band DAC to RFIC.
P10	TSSI_G	I	Transmitted signal strength indicator. From 2.5G RF PA.
N10	TSSI_A	I	Transmitted signal strength indicator. From 5.2G RF PA.
P11	RFRXI_P	I	Differential I+ input, from RFIC to base-band ADC.
P12	RFRXI_N	I	Differential I- input, from RFIC to base-band ADC.
P13	VREFP	Analog	Reference voltage.
N13	VREFN	Analog	Reference voltage.
P14	RFRXQ_P	I	Differential Q+ input, from RFIC to base-band ADC.
N14	RFRXQ_N	I	Differential Q- input, from RFIC to base-band ADC.
K12	VREF	Analog	Reference voltage.
K14	VREF025P	Analog	Reference voltage.
K13	VREF025N	Analog	Reference voltage.
Miscellaneous (15)			

B14,C14,D14,E14, F14,G13,G12,H13	GPIO[7:0]	I/O	GPIO[7:0].
H2	EECS	O	EEPROM chip select.
H3	EECLK	O	EEPROM clock.
J2	EEDI	O	EEPROM data in.
M2	EEDO	I	EEPROM data output.
J3	LED_ACT	O	Activity LED. Active low.
M3	LED_RDY	O	Ready LED. Controlled by software.
D13	PLLVDDA	Analog	Base-band PLL 1.8V analog power.
USB PHY (13)			
A1	DP	I/O	USB data in data positive pin terminal.
A2	DM	I/O	USB data in data negative pin terminal.
B2	RREF	Analog	Connect to external reference resistor (6.195kΩ±5%) to analog ground.
D2	RPU	Analog	Connect to external resistor (1.5kΩ±1%) to analog 3.3V power.
C4	XSCI	I	Crystal oscillator input (12MHz)
B5	XSCO	O	Crystal oscillator output (12MHz)
D1	VCC3IO_U20	Power	Analog power pin. Connect to 3.3V power.
E2	GNDA_U20	Power	Ground pin.
F4	VCCA_U20	Power	Analog power pin. Connect to 3.3V power
D4	VCC18_U20	Power	Digital power pin. Connect to 1.8V power.
D3	GND18_U20	Power	Ground pin.
C3	VCC3_U20	Power	Analog power pin. Connect to 3.3V power.
C2	GND3_U20	Power	Ground pin.
Power/Ground (48)			
M9	GNDSH_DAC	Power	Ground pin.
J12	GNDSH	Power	Ground pin.
M11, M12, N11, N12, L14	VCC33A	Power	Analog power pins. Connect to 3.3V power.
K10, L10, L11, M13, M10	VSS33A	Power	Ground pins.
L12, L13, M14	VCC33D	Power	Digital power pins. Connect to 3.3V power.
J10, J11, K11	VSS33D	Power	Ground pins.
L8, L9, M8	VCC18	Power	Analog power pins. Connect to 1.8V power.
K7, K8, K9	VSS18	Power	Ground pins.
E11, E6, H11, H4, L5	VDD_C18	Power	Digital core power pins. Connect to 1.8V power.
E8, F11, G11, G5, K4, L6, M6	VDDIO	Power	Digital I/O power pins. Connect to 3.3V power.
E10, E7, G10, H5, K6, E5, E9, F10, F5, H10, J5, K5	GND	Power	Ground pins.
Reserved (30)			
C6,B4,B3,A3,A4, A5,A6,C5,B7,A7, C7,D6,B8,C8,D7, A8	ADDR[15:0]	O	NOR flash address. Left NC if no use.
D8,B9,C9,A9, D10,D9,A10,C10	DATA[7:0]	I/O	NOR flash data I/O.
B11	WAITN	O	NOR flash OEN. Left NC if no use.
A12	IREQN	O	NOR flash WEN. Left NC if no use.
B10	PCMREGN	I	NOR flash mode selection. 0: external NOR flash mode. 1: internal ROM mode.
D12	R/B	I	Connect to VDD.
E13	CEN	O	NOR flash CEN. Left NC if no use
F12	WPN	O	Left NC.

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Electrical Specifications

Absolute Maximum Ratings

Core Supply Voltage 1.98V
I/O Supply Voltage 3.6V
Input, Output or I/O Voltage.. . . . . GND –0.3V to Vcc+0.3V

Thermal Information

Thermal Resistance θ_{JA} (^{o}C/W,Note) in free air for TFBGA (12x12mm) package.. . . . .51.4 ^{o}C/W
Maximum Junction Temperature . . . . . .125^{o}C
Maximum Storage Temperature . . . . -40^{o}C to 150^{o}C

Operating Conditions

Ambient Temperature Range . . . . . -10 to 85^{o}C
Maximum Operation Case Temperature . . . 95^{o}C
Core Supply Voltage . . . . 1.8V +/- 10%
I/O Supply Voltage . . . . 3.3V +/- 10%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

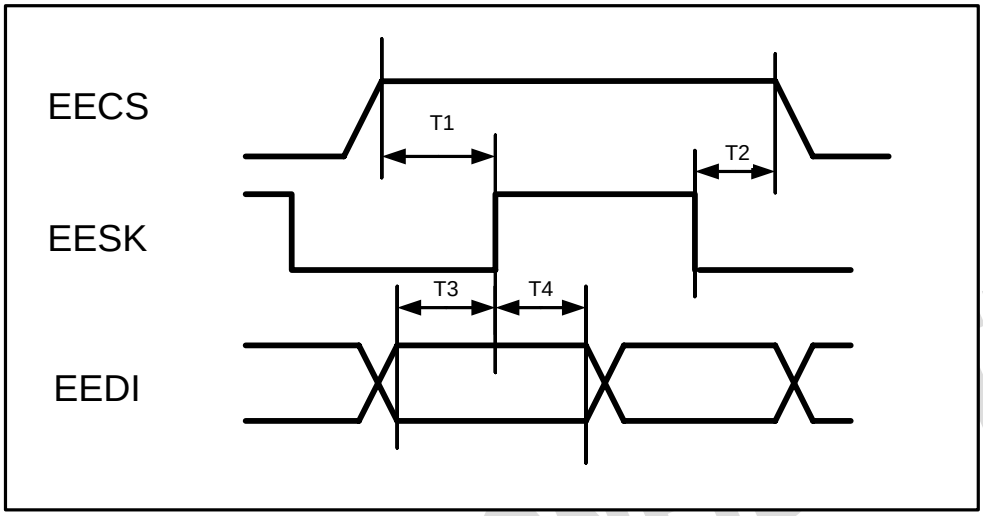
$_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.

DC Electrical Specifications

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
1.8 Power supply current	I_{CC18PT}	V_{DD} = Max, transmit	-	50	-	mA
	I_{CC18PR}	V_{DD} = Max, receive	-	80	-	mA
	I_{CC18SB}	V_{DD} = Max, standby	-	10	-	μA
3.3V Power supply current	I_{CC33PT}	V_{DD} = Max, transmit	-	80	-	mA
	I_{CC33PR}	V_{DD} = Max, receive	-	120	-	mA
	I_{CC33SB}	V_{DD} = Max, standby	-	400	-	μA
Logical one input voltage	V_{IH}		0.7 V_{DD}	-	-	V
Logical zero input voltage	V_{IL}		-	-	0.3	V
Logical one output voltage	V_{OH}	I_{OH} = -1mA, V_{DD} = Min	0.9 V_{DD}	-	-	V
Logical zero output voltage	V_{OL}	I_{OL} = 2mA, V_{DD} = Min	-	0.1	0.1 V_{DD}	V
Input capacitance	C_{IN}	CLKIN frequency 1MHz. All measurements referenced to GND. T_A = 25 ^{o}C	-	5	10	pF
Output capacitance	C_{OUT}		-	5	10	pF

AC Electrical Specifications

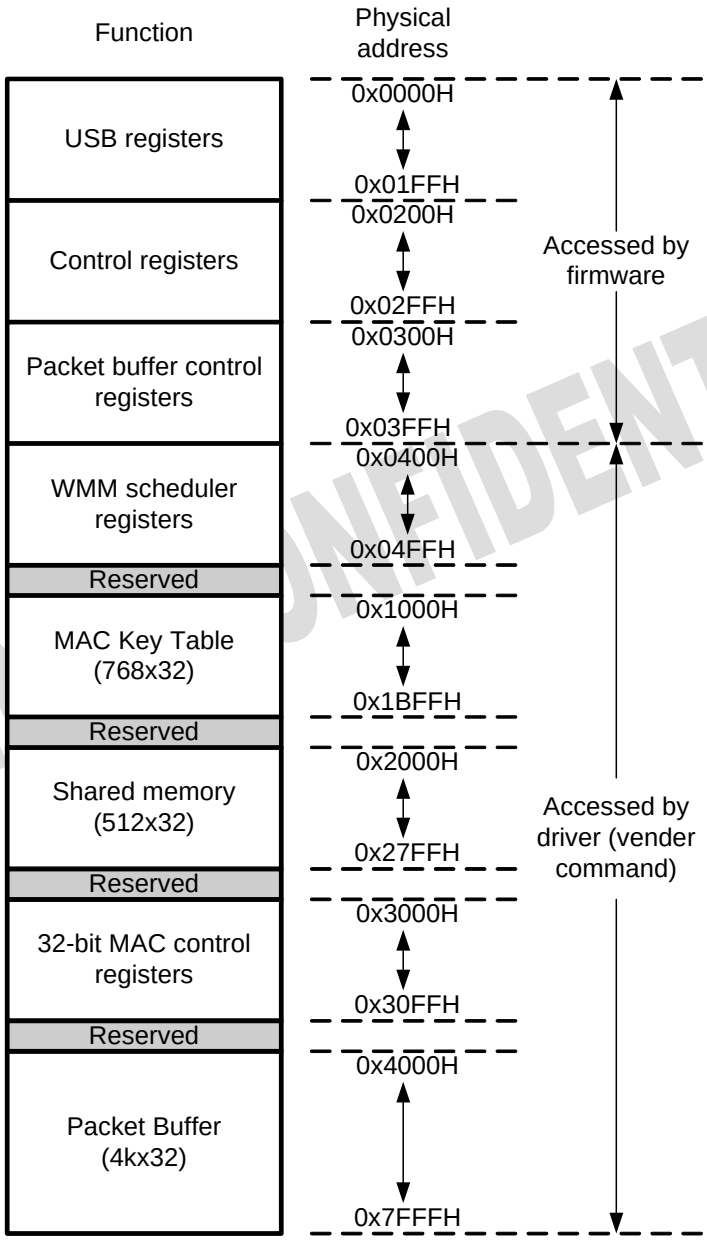
EEPROM Interface Timings



	Symbol	Parameter	Min	Max	Units	Notes
T0	^{t}EESK	Serial Clock Frequency	256	260	KHz	
T1	^{t}EECSS	Delay from EECS High to EESK High	300	-	ns	
T2	^{t}EECSH	Delay from EESK Low to EECS Low	30	-	ns	
T3	^{t}EEDIS	Setup Time of EEDI to EESK	300	-	ns	
T4	^{t}EEDIH	Hold Time of EEDI after EESK	300	-	ns	

Register descriptions

Register map



Security Key Table (Base Address = 0x1000)

Security Key Entry Format (32 bytes per key entry)

Offset	Field	Type	Description
0x00	Bit31:0	R/W	Security Key byte3~0
0x04	Bit31:0	R/W	Security Key byte7~4
0x08	Bit31:0	R/W	Security Key byte11~8
0x0C	Bit31:0	R/W	Security Key byte15~12
0x10	Bit31:0	R/W	TX MIC Key byte3~0
0x14	Bit31:0	R/W	TX MIC Key byte7~4
0x18	Bit31:0	R/W	RX MIC Key byte3~0
0x1C	Bit31:0	R/W	RX MIC Key byte7~4

For WEP40, CKIP40: Security Key is valid at byte4~0.
For WEP104, CKIP104: Security Key is valid at byte12~0
For TKIP, AES: Security Key is valid at byte15~0
TX/RX MIC Key is used only for TKIP MIC calculation.

Pair-wised Transmitter Address Entry Format (8 bytes per key entry)

Offset	Field	Type	Description
0x00	Bit31:0	R/W	TA byte3~0
0x04	Bit31:0	R/W	Bit [15:0] : TA byte5~4 Bit [18:16] : security mode for the pair 0=no security, 1=WEP40, 2=WEP104, 3=TKIP, 4=AES, 5=CKIP40 6=CKIP104, 7=reserved (no security for now) Bit [31:19] : reserved

Security Key Table Layout (total 3072bytes)

The security key table is composed of:
16 shared key entries (32x16 bytes)
32 pair-wise key entries (32x64 bytes, for AP mode)
32 pair-wise transmitter address entries (8x64 bytes)

Offset	length	Type	Description
0x000 0x020 0x040 … 0x1e0	32bytes x16	R/W	16 shared key entries According the multiple BSSID mask setting (MAC_CSR5) CASE1. when BSSID mask = 2'b11 (one BSSID): Key entries from 0x000 to 0x060 are treated as shared keys for key id from 0 to 3. CASE2. when BSSID mask = 2'b01or 2'b10 (two BSSID): Key entries from 0x000 to 0x060 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 0 Key entries from 0x080 to 0x0e0 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 1 CASE3. when BSSID mask = 2'b00 (four BSSID): Key entries from 0x000 to 0x060 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 00 Key entries from 0x080 to 0x0e0 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 01 Key entries from 0x100 to 0x160 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 10 Key entries from 0x180 to 0x1e0 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 11 The key entry format is described above.
0x200 0x220 0x240 …. 0x9e0	32bytes x64	R/W	64 Pair-wised key entries The key entry format is described above.
0xa00 0xa08 0xa10	8bytes x64	R/W	64 Pair-wised transmitter address (TA) entries The mapping of pair-wised TA entries and pair-wised

…. 0xbf8			key entries is one-to-one, where TA entry at offset 0x600 maps to offset 0x200 key entry TA entry at offset 0x608 maps to offset 0x220 key entry and so on. TA entry at offset 0x6f8 maps to offset 0x5e0 key entry

WMM Scheduler Register

AIFSN: Aifsn (offset = 0400h)

Field	Type	Default	Description
Bit 31:16	R/O	0x0	Reserved.
Bit 15:12	R/W	0x0	AIFSN3.
Bit 11:8	R/W	0x0	AIFSN2.
Bit 7:4	R/W	0x0	AIFSN1.
Bit 3:0	R/W	0x0	AIFSN0.

CW_MIN: Cw_min (offset = 0404h)

Field	Type	Default	Description
Bit 31:16	R/O	0x0	Reserved.
Bit 15:12	R/W	0x0	Cw_min3.
Bit 11:8	R/W	0x0	Cw_min2.
Bit 7:4	R/W	0x0	Cw_min1.
Bit 3:0	R/W	0x0	Cw_min0.

CW_MAX: Cw_max (offset = 0408h)

Field	Type	Default	Description
Bit 31:16	R/W	0x0	Reserved.
Bit 15:12	R/W	0x0	Cw_max3.
Bit 11:8	R/W	0x0	Cw_max2.
Bit 7:4	R/W	0x0	Cw_max1.
Bit 3:0	R/W	0x0	Cw_max0.

TXOP01: TXOP0 and TXOP1 (offset = 040Ch)

Field	Type	Default	Description
Bit 31:16	R/W	0x0	AC1 TXOP. Unit: 32uS.
Bit 15:0	R/W	0x0	AC0 TXOP. Unit: 32uS.

TXOP23: TXOP2 and TXOP3 (offset = 0410h)

Field	Type	Default	Description
Bit 31:16	R/W	0x0	AC3 TXOP. Unit: 32uS.
Bit 15:0	R/W	0x0	AC2 TXOP. Unit: 32uS.

MAC Control Register

MAC_CSR0: ASIC version number (offset = 3000h)

Field	Type	Default	Description
Bit 31:0	R	0x2573a	MAC ASIC version number

MAC_CSR1: System control register (offset = 3004h)

Field	Type	Default	Description
Bit 31:3	R	0x0	Reserved
Bit 2	R/W	0x0	Host is ready to work 1 = Ready
Bit 1	R/W	0x1	Hardware Reset BBP: 1: reset BBP 0: release reset
Bit 0	R/W	0x0	Soft-reset MAC 1 = MAC in reset state 0 = MAC in normal state This won't reset MAC register values.

MAC_CSR2: MAC address register 0 (offset = 3008h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	STA MAC address byte3
Bit 23:16	R/W	0x0	STA MAC address byte2
Bit 15:8	R/W	0x0	STA MAC address byte1
Bit 7:0	R/W	0x0	STA MAC address byte0 *Note: **byte0** is the first byte on network; its LSB is the first bit on network. For a MAC address captured on the network 00:01:02:03:04:05, byte0=00, byte1=01 etc.

MAC_CSR3: MAC address register 1 (offset = 300Ch)

Field	Type	Default	Description
Bit 31:24	R	0x0	Reserved
Bit 23:16	R/W	0xFF	"Unicast-to-me" comparison mask for received Address1 and MAC Address on byte5 0: don't care 1: compare
Bit 15:8	R/W	0x0	STA MAC address byte5
Bit 7:0	R/W	0x0	STA MAC address byte4

The multiple BSSID mask for byte5 in MAC_CSR5 also takes effect on unicast-to-me comparison. The "final" unicast-to-me compare mask on byte5 is (uc_to_me_mask[7:0] & bssid_mask[1:0]).

MAC_CSR4: BSSID register 0 (offset = 3010h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	BSSID byte3
Bit 23:16	R/W	0x0	BSSID byte2
Bit 15:8	R/W	0x0	BSSID byte1
Bit 7:0	R/W	0x0	BSSID byte0

MAC_CSR5: BSSID register 1 (offset = 3014h)

Field	Type	Default	Description
Bit 31:18	R	0x0	Reserved
Bit 17:16	R/W	0x3	Multiple BSSID comparison mask, 0: don't care, 1: enable Bit16: comparison mask bit0 of BSSID byte6(MAC_CSR5 bit8) Bit17: comparison mask bit1 of BSSID byte6(MAC_CSR5 bit9) The value will also affect the number of shared keys in the key table. 11: one BSSID; 01, 10: two BSSID; 00: four BSSID
Bit 15:8	R/W	0x0	BSSID byte5
Bit 7:0	R/W	0x0	BSSID byte4

The multiple BSSID mask is used to make bit0, bit1 of BSSID byte5 "don't care" in RX BSSID comparison (which result in "is_my_bssid" flag in RX descriptor).

MAC_CSR6: Maximum frame length register (offset = 3018h)

Field	Type	Default	Description
Bit 31:12	R	0x0	Reserved
Bit 11:0	R/W	0x780	Maximum Frame length in byte unit Default value is1920 bytes, i.e. (128Byte * 16)

ASIC will block incoming frames longer than this maximum size to prevent overwriting RX buffer.

MAC_CSR7: Reserved (offset = 301Ch)

Field	Type	Default	Description
Bit 31: 0	R	0x0	Reserved

MAC_CSR8: SIFS / EIFS register (offset = 3020h)

Field	Type	Default	Description
Bit 31:16	R/W	0x16C	EIFS in unit of 1-us Default 364 us

Bit 15:8	R/W	0x00	SIFS in unit of 1-us, applied after OFDM RX to compensate OFDM RX PHY delay
Bit 7:0	R/W	0x0A	SIFS in unit of 1-us, applied after CCK TX/RX and OFDM TX Default 10 us for 11b/g. Driver will change it to 16 us when operating in 11a

MAC_CSR9: Slot time / contention window register (offset = 3024h)

Field	Type	Default	Description
Bit 31:17	R	0x0	Reserved
Bit 16	R/W	0x0	Use following default value as {cwmin, cwmax} pair. Ignore the {cwmin, cwmax} pair in TX descriptor.
Bit 15:12	R/W	0xa	Defaul value of cwmax
Bit 11:8	R/W	0x3	Default value of cwmin
Bit 7:0	R/W	0x14	Slot time in unit of 1-us. This value is used by Backoff engine to calculate the total backoff time. Default 20us for 11b/g. 11a and 11g-short-slot-mode is 9 us

MAC_CSR10: Power mode configuration register (offset = 3028h)

Field	Type	Default	Description
Bit 31:13	R	0x0	Reserved
Bit 12	R/W	0x0	BBP AD/DA power down in Awake state
Bit 11	R/W	0x0	BBP PLL power down in Awake state
Bit 10	R/W	0x1	RA_PE in Awake state
Bit 9	R/W	0x1	RF_PE in Awake state
Bit 8	R/W	0x1	TR_PE in Awake state (change to 0 automatically when TX)
Bit 7:5	R	0x0	Reserved
Bit 4	R/W	0x1	BBP AD/DA power down in Sleep state
Bit 3	R/W	0x1	BBP PLL power down in Sleep state
Bit 2	R/W	0x0	RA_PE in Sleep state
Bit 1	R/W	0x0	RF_PE in Sleep state
Bit 0	R/W	0x0	TR_PE in Sleep state

MAC_CSR11: Power saving transition time register (offset = 302Ch)

Field	Type	Default	Description
Bit 31:20	R	0x0	Reserved
Bit 19:16	R/W	0xA	Transition time from Sleep to Awake in units of 1-TU (1.024ms) Default: 10 state transition from awake to sleep is 0 by default but will postpone until TX and RX process became idle.
Bit 15	R/W	0x0	Enable Auto Wakeup timer interrupt Once enabled, ASIC will auto wakes up BBP/RF to AWAKE state after the specified time (TbcnExp# * BeaconInterval + DelayAfterLastTbcnExp) has past.
Bit 14:8	R/W	0x0	Number of subsequent Tbcn Expirations before Wakeup Default: 0
Bit 7:0	R/W	0x50	Delay after the last Tbcn expiration in unit of ~~1/16~~ 1-TU Default is 80, which means 20 TU ahead of next TBTT. This lead time should be sufficient for BBP/RF to recover from whatever power state to AWAKE state

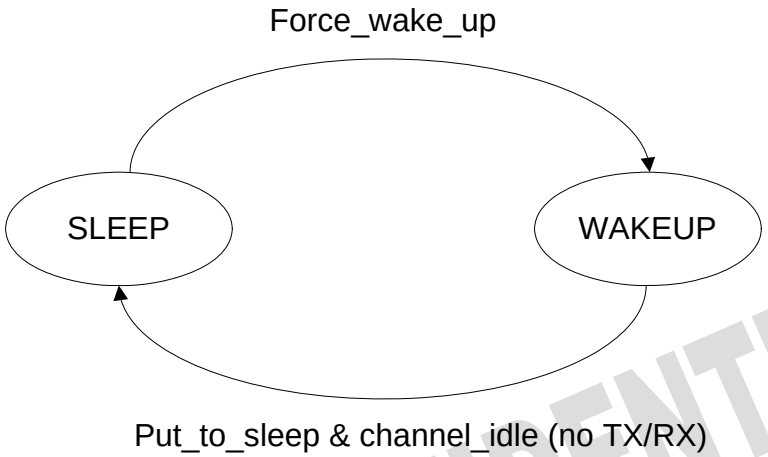
CAUTION!! Please make sure TBTT timer is enabled if auto wakeup interrupt timer is enabled.

MAC_CSR12: Power state control register (offset = 3030h)

Field	Type	Default	Description
Bit 31:3	R	0x0	Reserved
Bit 3	R	0x0	0: BB/RF is not ready 1: BB/RF is stable
Bit 2	WC	0x0	Force wake up, write 1 to put BBP/RF to AWAKE state.
Bit 1	WC	0x0	Put to sleep, write 1 to put BBP/RF to SLEEP state.
Bit 0	R	0x0	Power state, 0:SLEEP mode, 1: AWAKE state

"Put to sleep" command may not be execute right away due to channel busy. The command postpone time is random.
"Force wake up" command will cancel the "Put to sleep" command and wake up MAC immediately anyhow.

CAUTION!! If “Put to sleep” command is issued but power state does not go to sleep state after a long time(due to random postpone time), please issue “Force wake up” command to cancel “Put to sleep” command before treat MAC as in AWAKE state.
“Force wake up” command has higher priority than “Put to sleep” command if they are issued at the same time.



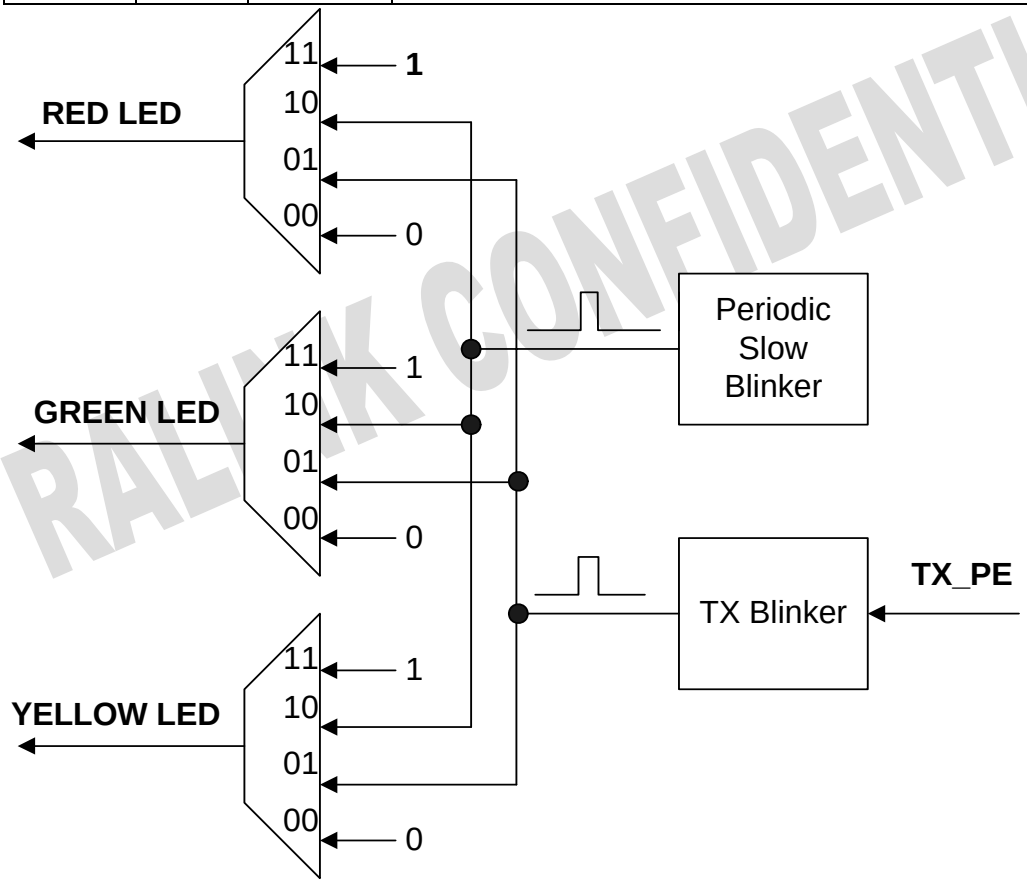
MAC_CSR13: GPIO control register (offset = 3034h)

Field	Type	Default	Description
Bit 31:16	R	0x0	Reserved
Bit 15:8	R/W	0xff	GPIO7-0 direction, 0:input, 1: output
Bit 7:0	R/W	0x00	GPIO7-0 value

MAC_CSR14: LED control register (offset = 3038h)

Field	Type	Default	Description
Bit 31:29	R	0x0	Reserved
Bit 28	R/W	0x0	LED polarity 0: active low 1: active high
Bit 27:26	R/W	0x0	Yellow LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on
Bit 25:24	R/W	0x2	Green LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on

Bit 23:22	R/W	0x1	Red LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on
Bit 21:16	R/W	0x3	Slow blinking period (unit: sec)
Bit 15:8	R/W	0x1E	TX blinking off period in unit of 1-ms Default: 30ms
Bit 7:0	R/W	0x46	Blinking on period in unit of 1-ms Default: 70ms



MAC_CSR15: NAV control register (offset = 303Ch)

Field	Type	Default	Description
Bit 31:16	R	0x0	MAC NAV current counter value (count down, unit: 1us)
Bit 15	WC	0x0	1: Update MAC NAV down-counter value
Bit 14:0	R/W	0x0	New NAV value for update (unit: 1us)

TXRX Control Register

TXRX_CSR0: TX/RX configuration register (offset = 3040h)

Field	Type	Default	Description
Bit 31:26	R	0x0	Reserved
Bit 25	R/W	0x0	Drop ACK/CTS frame
Bit 24	R/W	0x0	Drop broadcast frame
Bit 23	R/W	0x0	Drop multicast frame
Bit 22	R/W	0x1	Drop version error frame
Bit 21	R/W	0x1	Drop ToDs frame 1 = drop all frames with ToDs bit on
Bit 20	R/W	0x1	Drop not to me unicast frame 1 = do not pass unicast-but-not-to-me frames to host
Bit 19	R/W	0x1	Drop control frame
Bit 18	R/W	0x1	Drop physical error frame
Bit 17	R/W	0x1	Drop CRC error frame
Bit 16	R/W	0x1	Disable RX
Bit 15	R/W	0x1	ASIC maintains TX frame's SEQ# 1: enable this feature 0: disable. Let software maintains seq#.
Bit 14:9	R/W	0x18	TSF offset in MAC header Default value is 24. For outgoing frames, if InsertTsf falg in ON in TX descriptor (for BEACON, ProbeResponse only), ASIC will overwrite the TSF field in the outgoing frame with the local TSF. For incoming BEACON frame, ASIC extract remote TSF at this offset and perform TSF synchronization.
Bit 8:0	R/W	0x32	RX ACK Timeout in unit of 1-us Default value is is 50us. If CCA is not asserted within this time limit, ASIC will retry the transmission.

TXRX_CSR1: RX descriptor BBP ID register (offset = 3044h)

Field	Type	Default	Description
Bit 31	R/W	0x1	BBP register 1 Valid
Bit 30:24	R/W	0x33	BBP register 1 ID, default is R51 OFDM RSSI
Bit 23	R/W	0x1	BBP register 0 Valid
Bit 22:16	R/W	0x2A	BBP register 0 ID, default is R42 OFDM RATE
Bit 15	R/W	0x1	BBP register 1 Valid for CCK

Bit 14:8	R/W	0x33	BBP register 1 ID, default is R51 CCK RSSI
Bit 7	R/W	0x1	BBP register 0 Valid for CCK
Bit 6:0	R/W	0x2F	BBP register 0 ID, default is R47 CCK RATE

The specified BBP register values will be automatically attached to the RX descriptor of every received frame

TXRX_CSR2: CCK TX descriptor BBP ID register (offset = 3048h)

Field	Type	Default	Description
Bit 31:24	R/W	0x8A	CCK SIGNAL register ID, default is R10
Bit 23:16	R/W	0x8B	CCK SERVICE register ID, default is R11
Bit 15:8	R/W	0x8C	CCK LENGTH_HIGH register ID, default is R12
Bit 7:0	R/W	0x8D	CCK LENGTH_LOW register ID, default is R13

TXRX_CSR3: OFDM TX descriptor BBP ID register (offset = 304Ch)

Field	Type	Default	Description
Bit 31:24	R/W	0x00	TX Power register ID
Bit 23:16	R/W	0x85	OFDM RATE register ID, default is R5
Bit 15:8	R/W	0x86	OFDM LENGTH_HIGH register ID, default is R6
Bit 7:0	R/W	0x87	OFDM LENGTH_LOW register ID, default is R7

TXRX_CSR4: Auto Responder / TX retransmission register (offset = 3050h)

Field	Type	Default	Description
Bit31:28	R/W	0x7	Short retry limit, applied when TX descriptor -> retry_mode = 0
Bit27:24	R/W	0x4	Long retry limit, applied when TX descriptor -> retry_mode = 1
Bit23	R/W	0x0	1: Auto downgrade initial TX rate (ex:54 ->48) when consecutive retried TX result occurred, downgrade action is cancelled when consecutive no-retried TX result occurred. 0: disable
Bit 22	R/W	0x0	0: OFDM TX rate auto fallback to OFDM 6M only 1: OFDM TX rate auto fallback to CCK 1M, 2M

Bit 21:20	R/W	0x0	OFDM TX rate auto fallback speed 0: fallback one step in rate when TX retry 1: fallback two step in rate when TX retry 2: fallback three step in rate when TX retry 3: fallback four step in rate when TX retry (TX retry rate will not fallback below 6Mbps)
Bit 19	R/W	0x1	OFDM TX rate auto fallback enable
Bit 18	R/W	0x0	Auto responder CCK 2, 5.5, 11Mbps preamble selection 0: long preamble 1: short preamble (ACK/CTS auto responding in CCK 1Mbps always use long preamble.)
Bit 17	R/W	0x1	Enable auto responder 1 = enable ACK/CTS auto responder
Bit 16	R/W	0x0	ACK/CTS power-management bit in MAC header 1: STA in power-saving mode 0: STA in active mode
Bit15:11	R	0x0	Reserved
Bit10:8	R/W	0x7	Auto responder ACK policy upon reception of following CONTROL frame, 0:disable 1:enable Bit8: For Block Acknowledgement Request (BlockAckReq) Bit9: For Block Acknowledgement (BlockAck) Bit10: For Power Save Poll (PS-Poll)
Bit7:0	R/W	0x32	TX ACK/CTS time-out in unit of 1-us. Default is ~~354~~ us. This value specifies how long the “Auto Responder” will wait if an outgoing ACK/CTS is pending due to PHY busy. If an ACK/CTS can’t be sent within this period, it’ll be given up. Time-out timer will be clear once ACT/CTS TX is kicked.

Upon reception unicast-to-me packet:

For management frame, ACK is always replied in SIFS time.

For data frame, ACK is replied in SIFS time according to FC.Qos bit and ACK policy(if Qos control field exist).

For control frame(Block ACK Req, BlockACK, PS-Poll), ACK is replied in SIFS time according to TXRX_CSR4, bit10-8.

For control frame (RTS), CTS is always replied in SIFS time.

For control frame (ACK/CTS/CF-End/CF-End-Ack), no responds.

TXRX_CSR5: Auto responder basic rate, TX power register (offset = 3054h)

Field	Type	Default	Description
Bit 31:28	R/W	0x3	Auto upgrade limit (unit: no-retried packet)
Bit 27:24	R/W	0x3	Auto downgrade limit (unit: retried packet)
Bit 23:16	R/W	0x6	Auto responder TX power
Bit 15:12	R	0x0	Reserved
Bit 11:0	R/W	0x0	Basic rate bit mask, bit0=1: 1 Mbps is basic rate, bit1=1: 2 Mbps is basic rate, bit2=1: 5.5 Mbps is basic rate, bit3=1: 11 Mbps is basic rate, bit4=1: 6 Mbps is basic rate, bit5=1: 9 Mbps is basic rate bit6=1: 12 Mbps is basic rate, bit7=1: 18 Mbps is basic rate, bit8=1: 24 Mbps is basic rate, bit9=1: 36 Mbps is basic rate, bit10=1: 48 Mbps is basic rate, bit11=1: 54 Mbps is basic rate

TXRX_CSR6: ACK/CTS payload consume time (offset = 3058h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0A	ACK/CTS Payload consume time @11M (in unit of 1 us)
Bit 23:16	R/W	0x14	ACK/CTS payload consume time @5.5M (in unit of 1 us)
Bit 15:8	R/W	0x38	ACK/CTS Payload consume time @2M (in unit of 1 us)
Bit 7:0	R/W	0x70	ACK/CTS Payload consume time @1M (in unit of 1 us)

TXRX_CSR7: ACK/CTS payload consume time (offset = 305Ch)

Field	Type	Default	Description
Bit 31:24	R/W	0x06	ACK/CTS payload consume time @18M (in unit of 1-us)
Bit 23:16	R/W	0x09	ACK/CTS payload consume time @12M (in unit of 1-us)
Bit 15:8	R/W	0x0C	ACK/CTS payload consume time @9M (in unit of 1-us)
Bit 7:0	R/W	0x13	ACK/CTS payload consume time @6M (in unit of 1-us)

TXRX_CSR8: ACK/CTS payload consume time (offset = 3060h)

Field	Type	Default	Description
Bit 31:24	R/W	0x02	ACK/CTS payload consume time @54M (in unit of 1-us)
Bit 23:16	R/W	0x03	ACK/CTS payload consume time @48M (in unit of 1-us)
Bit 15:8	R/W	0x03	ACK/CTS payload consume time @36M (in unit of 1-us)
Bit 7:0	R/W	0x05	ACK/CTS payload consume time @24M (in unit of 1-us)

ASIC utilizes these registers (TXRX_CSR6,7,8) together with the received unicast-to-me frame's "duration" field to decide the "duration" value in the outgoing ACK/CTS frame.

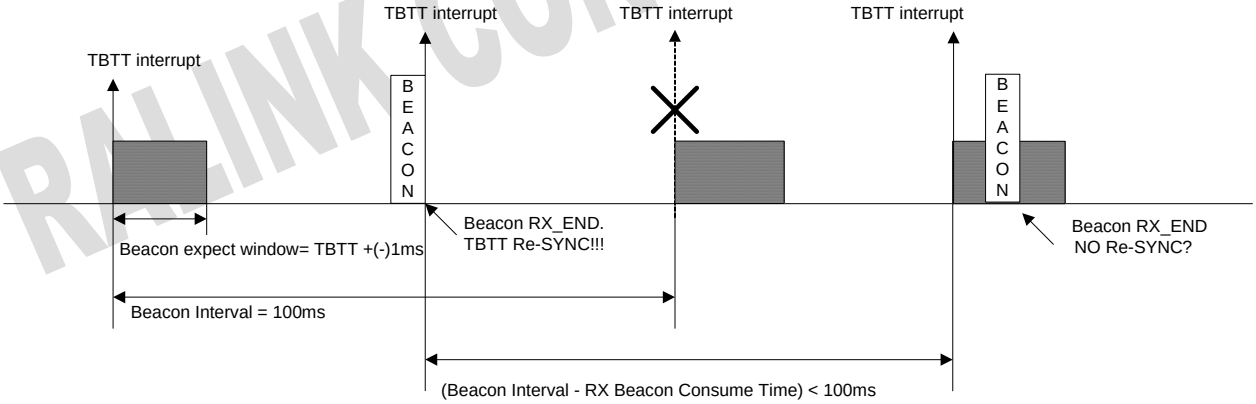
TXRX_CSR9: Beacon Synchronization register (offset = 3064h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	TX timestamp insertion compensation value, default: 0
Bit 23:21	R	0x0	Reserved
Bit 20	R/W	0x0	Enable BEACON TX at TBTT interrupt
Bit 19	R/W	0x0	Enable TBTT timer. A "TBTT interrupt" will happen every "BEACON interval 0 = stop TBTT timer 1 = start TBTT timer
Bit 18:17	R/W	0x0	Synchronize local TSF with remote TSF in the received BEACON frame. 00 = disable 01 = always sync with received "is_mybssid" BEACON (station infra-structure mode) 10 = sync with received "is_mybssid" BEACON only if the remote TSF is greater than local TSF (station ad hoc mode) 11 = sync with no body (AP mode)
Bit 16	R/W	0x0	Enable TSF 1 = start TSF auto counting 0 = stop TSF auto counting A 0-to-1 transition will cause TSF to re-start from 0.
Bit 15:0	R/W	0x0640	BEACON interval in unit of 1/16 TU (64us) Default value is 1600 (=100 TU = 102.4 ms) Maximum beacon interval is about 4000ms

TXRX_CSR10: Beacon time alignment register (offset = 3068h)

Field	Type	Default	Description
Bit 31:16	R	0x0	Reserved
Bit 15:8	R/W	0x10	Beacon Expecting window (unit: 64us), default value is 64*16=1024us(that is, 1% of beacon interval) The window starts right after TBTT interrupt; TBTT timer will not synchronize its phase with remote STA upon receiving “is_my_bssid” beacon in this window.
Bit 7:0	R/W	0x10	IBSS mode TBTT phase adaptive adjustment step (unit: 1us), default value is 16us. In IBSS mode(Ad hoc), if consecutive TX beacon failures (or consecutive success)happened, TBTT timer will adjust it phase to meet will external TBTT time.

Upon receiving a is_my_bssid BEACON from AP or remote peer “AND” RXEnd event is not in beacon expecting window, ASIC would re-align next TBTT to be (local TSF + Beacon interval – RX Beacon Consume Time).
(RX Beacon Consume Time) is the time from CCA assertion to RXEND event of the beacon.



TXRX_CSR11: AES frame control AND/OR mask register (offset = 306Ch)

Field	Type	Default	Description
Bit 31:16	R/W	0x0000	Frame control field OR mask in AES encryption/decryption (applied after AES AND mask below)
Bit 15:0	R/W	0xc78f	Frame control field AND mask in AES encryption/decryption

TXRX_CSR12: MAC TSF Timer Low register (offset = 3070h)

Field	Type	Default	Description
Bit 31:0	R	0x0000	MAC local 64-bit TSF timer value bit31-0

TXRX_CSR13: MAC TSF Timer High register (offset = 3074h)

Field	Type	Default	Description
Bit 31:0	R	0x0000	MAC local 64-bit TSF timer value bit63-32

TXRX_CSR14: MAC TBTT Timer register (offset = 3078h)

Field	Type	Default	Description
Bit 31:17	R	0x0000	Reserved
Bit 16:0	R	0x0000	TBTT Timer, which means time remains before next TBTT time, (unit: 32us) When TXRX_CSR9.bit19 TBTT timer is enabled, the value will down count from beacon interval value specified in TXRX_CSR9.bit15-0 to 0 in unit of 32us. The value of the timer is 0 when TBTT timer is disabled.

TXRX_CSR15: TKIP MIC Priority Byte AND Mask register (offset = 307Ch)

Field	Type	Default	Description
Bit 31:8	R	0x0	Reserved
Bit 7:0	R/W	0x0f	TKIP MIC priority byte AND Mask The Qos control field bit7-0 of the TX/RX Qos data frame is “AND” with this mask to be the priority byte for TKIP MIC calculation.

PHY Control Register

PHY_CSR0: RF/PA configuration register (offset = 3080h)

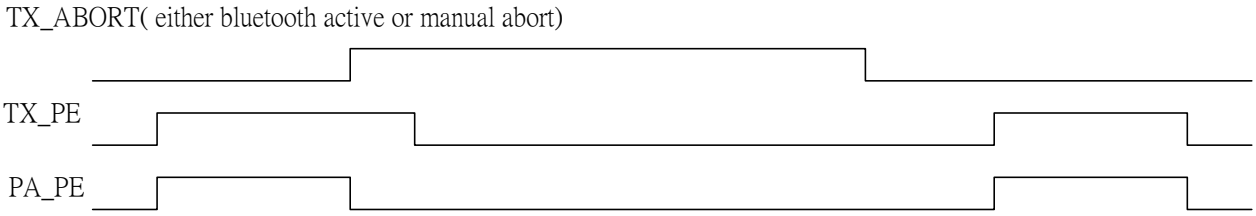
Field	Type	Default	Description
Bit 31:22	R	0x0	Reserved
Bit 21	R/W	0x0	PA_PE_A polarity 0: Active High 1: Active Low
Bit 20	R/W	0x0	PA_PE_G polarity 0: Active High 1: Active Low
Bit 19	R/W	0x0	PA_PE_A (G) always turn on, 0 : Disable, 1: Enable
Bit 18	R/W	0x0	1: PA_PE_A (G) de-assert with TR_PE switching to RX 0: PA_PE_A (G) de-assert with TR_SW switching to RX
Bit 17	R/W	0x1	1: PA_PE_A pin enable, 0: PA_PE_A always low
Bit 16	R/W	0x1	1: PA_PE_G pin enable, 0: PA_PE_G always low
Bit 15:0	R	0x0	Reserved

PHY_CSR1: MISC mode configuration register (offset = 3084h)

Field	Type	Default	Description
Bit 31:17	R	0x0	Reserved
Bit 16	R/W	0x0	0: Disable RF RPI mode 1: Enable RF RPI mode
Bit 15	R/W	0x0	0: normal RX timeout limit (30ns for PLCP RX timeout, 10ns for MPDU RX timeout) 1: double RX timeout limit for 802.11j
Bit 14	R/W	0x0	0: RX defer after last RXD bit comes in 1: RX defer after io_bb_rx_end asserted Note: Please change both SIFS value to the same one in this mode.
Bit 13	R/W	0x1	0: PAPE stays alive until TX complete in TX abortion 1: Disable PAPE Immediately in TX abortion
Bit 12	R/W	0x0	0: Normal TX mode 1: Manual TX halt (Immediately)
Bit 11	R/W	0x0	0: Disable 1: Enable TX abortion when Bluetooth is active
Bit 10	R/W	0x0	Bluetooth active signal polarity 0: high active 1: low active

Bit 9	R/W	0x1	0: Read BBCR at the beginning of per RX 1: Read BBCR at the end of per RX
Bit 8	R/W	0x1	0: Disable TX retry bit replacement 1: Enable
Bit 7	R/W	0x1	Switch Antenna to TX mode (TRSW =1, TRSWB =0) when LNA low gain (LNA1 = 0, LNA0=1) 0:enable 1:disable
Bit 6	R/W	0x0	1: RF_LE is low when standby 0: RF_LE is high when standby
Bit 5	R/W	0x0	BBP Register R/W mode 1: parallel mode 0: serial mode
Bit 4	R/W	0x1	TXD/RXD mode select 1: 1bit mode 0: 2bit mode
Bit 3	R/W	0x0	OFDM RX equivalent time mode, if the bit set, the processing time is the same at every rate
Bit 2	WC	0x0	Kick one-shot RX in one-shot RX mode Write 1 to kick and self-cleared
Bit 1	R/W	0x0	One-shot RX mode for debugging 1:enable, 0:disable (default)
Bit 0	R/W	0x0	Continuous transmit mode, set the bit if BBP is in continuous TX test mode

If PHY_CSR.bit11 is enabled, packet transmission will be aborted immediately as bluetooth activation signal is asserted as “active”.
Manual setting of PHY_CSR1.bit12 to “1” has the same effect to abort TX.
TX abortion does not influence ACK/CTS TX.



PHY_CSR2: BBP pre-TX CCK (offset = 3088h)

Field	Type	Default	Description
Bit 31	R/W	0x1	1: enable this BBP pre-TX command
Bit 30:24	R/W	0x2	BBP pre-TX register ID for OFDM, default R2
Bit 23:16	R/W	0x18	BBP pre-TX register value for OFDM

Bit 15	R/W	0x1	1: enable this BBP pre-TX command
Bit 14:8	R/W	0x2	BBP pre-TX register ID for CCK, default R2
Bit 7:0	R/W	0x00	BBP pre-TX register value for CCK

Need not swap I/Q upon transmission in CCK mode. This register is used to match I/Q interface between BBP and RF.

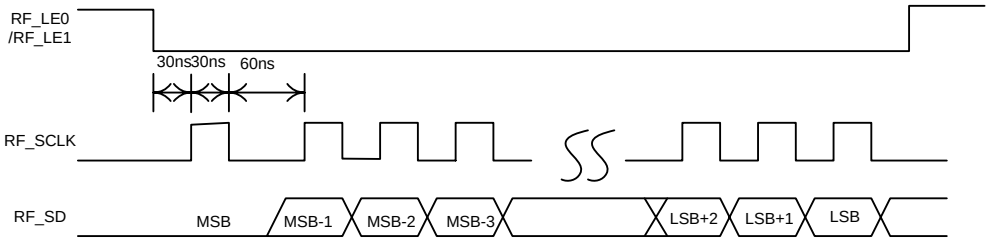
PHY_CSR3: BBP serial control register (offset = 308Ch)

Field	Type	Default	Description
Bit 31:17	R	0x0	Reserved
Bit 16	R/W	0x0	Write one to kick BBP register read/write Read: Busy
Bit 15	R/W	0x0	Read/write direction, 0: Write, 1: Read
Bit 14:8	R/W	0x0	Select BBP register ID
Bit 7:0	R/W	0x0	BBP data written into or read out from BBP

PHY_CSR4: RF serial control register (offset = 3090h)

Field	Type	Default	Description
Bit 31	R/W	0x0	Write: 1: kick RF register write Read: 1:Busy, 0: Idle
Bit 30	R	0x0	PLL_LD The current RF PLL_LD
Bit 29	R/W	0x0	RF selection 0:RF_LE0 activate, 1:RF_LE1 activate
Bit 28:24	R/W	0x16	Numbers of bit Default: 22
Bit 23:16	R/W	0x0	RF register ID and content [23:16]
Bit 15:0	R/W	0x0	RF register ID and content [15:0]

Host should make sure the first bit (MSB in the specified bit number) written to RF is 0 in 1T2R RF chip mode selection.



PHY_CSR5: RX to TX signal switching timing control register (offset = 3094h)

Field	Type	Default	Description
Bit 31:30	R	0x0	Reserved

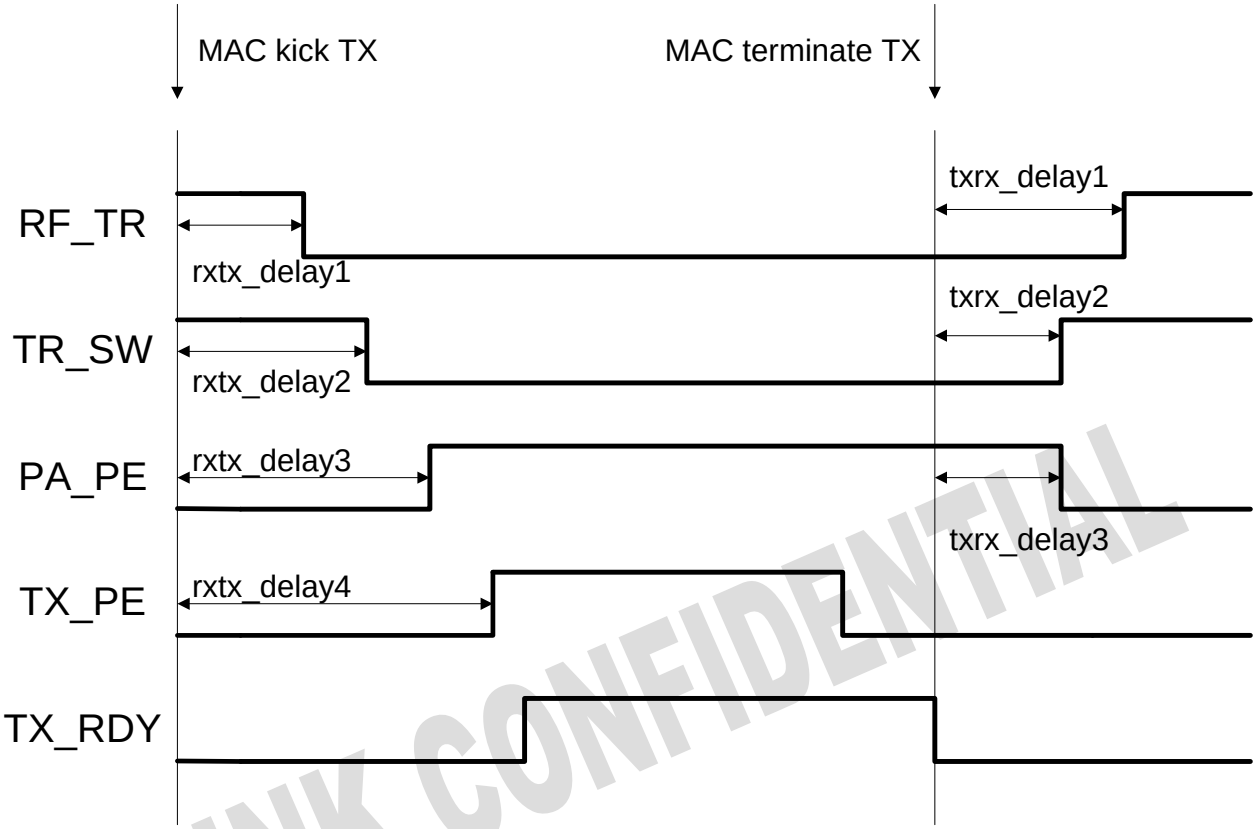
Bit 29:24	R/W	0x0	Delay (in unit of 0.25us) from TX kick-off to (RF chip) RF_TR(RF_PE2) enable
Bit 23:22	R	0x0	Reserved
Bit 21:16	R/W	0x4	Delay (in unit of 0.25us) from TX kick-off to (Antenna) TR_SW enable
Bit 15:14	R	0x0	Reserved
Bit 13:8	R/W	0x8	Delay (in unit of 0.25us) from TX kick-off to (PA) PA_PE enable
Bit 7:6	R	0x0	Reserved
Bit 5:0	R/W	0xC	Delay (in unit of 0.25us) from TX kick-off to (BBP) TX_PE enable

PHY_CSR6: TX to RX signal switching timing control register (offset = 3098h)

Field	Type	Default	Description
Bit 31:22	R	0x0	Reserved
Bit 21:16	R/W	0xC	Delay (in unit of 0.25us) from (BBP) TX_PE disable to (RF chip) RF_TR(RF_PE2) disable
Bit 15:14	R	0x0	Reserved
Bit 13:8	R/W	0x8	Delay (in unit of 0.25us) from (BBP) TX_PE disable to (Antenna) TR_SW disable
Bit 7:6	R	0x0	Reserved
Bit 5:0	R/W	0x8	Delay (in unit of 0.25us) from (BBP) TX_PE disable to (PA) PA_PE disable

PHY_CSR7: TX DAC switching timing control register (offset = 309Ch)

Field	Type	Default	Description
Bit 31:14	R	0x0	Reserved
Bit 13:8	R/W	0x8	Delay (in unit of 0.25us) from TX kick-off to TX DAC enable
Bit 7:6	R	0x0	Reserved
Bit 5:0	R/W	0x8	Delay (in unit of 0.25us) from (BBP) TX_PE disable to TX DAC disable



SEC Control Register

SEC_CSR0: Shared key table control register (offset = 30A0h)

Field	Type	Default	Description
Bit 31:15	R	0x0	Reserved
Bit 15:0	R/W	0x0	Shared key entry valid bit, 1:valid, 0:not valid Bit0 for shared key entry offset 0x000 Bit1 for shared key entry offset 0x020 And so on. Bit15 for shared key entry offset 0x1e0

SEC_CSR1: Shared key table security mode register (key0-7) (offset = 30A4h)

Field	Type	Default	Description
Bit 31	R	0x0	Reserved
Bit 30:28	R/W	0x0	Security mode for shared key offset @ 0x0e0
Bit 27	R	0x0	Reserved
Bit 26:24	R/W	0x0	Security mode for shared key offset @ 0x0c0
Bit 23	R	0x0	Reserved
Bit 22:20	R/W	0x0	Security mode for shared key offset @ 0x0a0
Bit 19	R	0x0	Reserved
Bit 18:16	R/W	0x0	Security mode for shared key offset @ 0x080
Bit 15	R	0x0	Reserved
Bit 14:12	R/W	0x0	Security mode for shared key offset @ 0x060
Bit 11	R	0x0	Reserved
Bit 10:8	R/W	0x0	Security mode for shared key offset @ 0x040
Bit 7	R	0x0	Reserved
Bit 6:4	R/W	0x0	Security mode for shared key offset @ 0x020
Bit 3	R	0x0	Reserved
Bit 2:0	R/W	0x0	Security mode for shared key offset @ 0x000

0=no security, 1=WEP40, 2=WEP104, 3=TKIP, 4=AES, 5=CKIP40 6=CKIP104, 7=reserved (no security for now)

SEC_CSR2: Pair-wise key entry valid register (offset = 30A8h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0000	64 Pair-wise key entry valid bit , 1:valid, 0:not valid Bit0 for pair-wised key entry offset 0x200 Bit1 for pair-wised key entry offset 0x220 And so on. Bit31 for pair-wised key entry offset 0x5e0

SEC_CSR3: Pair-wise key entry valid register (offset = 30ACh)

Field	Type	Default	Description
Bit 31:0	R/W	0x0000	64 Pair-wise key entry valid bit , 1:valid, 0:not valid Bit0 for pair-wised key entry offset 0x600 Bit1 for pair-wised key entry offset 0x620 And so on. Bit31 for pair-wised key entry offset 0x9e0

SEC_CSR4: Pair-wise key lookup control register (offset = 30B0h)

Field	Type	Default	Description
Bit 15:4	R	0x0	Reserved
Bit 3:0	R/W	0x0	Pair-wise key table lookup enable According the multiple BSSID mask setting (MAC_CSR5) Case1: when BSSID mask = 2'b11 (one BSSID) Bit0: 1:keytable lookup enable, 0: disable Bit1-3: no effect. Case2: when BSSID mask = 2'b01 or 2'b10 (two BSSID) Bit0: 1:keytable lookup enable for don't care BSSID bit = 1'b0, 0: disable Bit1: 1:keytable lookup enable for don't care BSSID bit = 1'b1, 0: disable Bit2-3: no effect. Case3: when BSSID mask = 2'b00 (four BSSID) Bit0: 1:keytable lookup enable for don't care BSSID bit = 2'b00, 0: disable Bit1: 1:keytable lookup enable for don't care BSSID bit = 2'b01, 0: disable Bit2: 1:keytable lookup enable for don't care BSSID bit = 2'b10, 0: disable Bit3: 1:keytable lookup enable for don't care BSSID bit = 2'b11, 0: disable

Pair-wise key table lookup shall be performed only when:
(unicast-to-me packet) & (BSSID matched) & (Pair-wise key table lookup for the corresponding BSSID is enabled.)

SEC_CSR5: Shared key table security mode register (key8-15) (offset = 30B4h)

Field	Type	Default	Description
Bit 31	R	0x0	Reserved
Bit 30:28	R/W	0x0	Security mode for shared key offset @ 0x1e0
Bit 27	R	0x0	Reserved
Bit 26:24	R/W	0x0	Security mode for shared key offset @ 0x1c0
Bit 23	R	0x0	Reserved
Bit 22:20	R/W	0x0	Security mode for shared key offset @ 0x1a0
Bit 19	R	0x0	Reserved
Bit 18:16	R/W	0x0	Security mode for shared key offset @ 0x180
Bit 15	R	0x0	Reserved
Bit 14:12	R/W	0x0	Security mode for shared key offset @ 0x160
Bit 11	R	0x0	Reserved
Bit 10:8	R/W	0x0	Security mode for shared key offset @ 0x140
Bit 7	R	0x0	Reserved
Bit 6:4	R/W	0x0	Security mode for shared key offset @ 0x120
Bit 3	R	0x0	Reserved
Bit 2:0	R/W	0x0	Security mode for shared key offset @ 0x100

0=no security, 1=WEP40, 2=WEP104, 3=TKIP, 4=AES, 5=CKIP40 6=CKIP104, 7=reserved (no security for now)

STA Control Register

STA_CSR0: FCS error / RX PLCP error counter (offset = 30C0h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	PLCP error count, cleared by read.
Bit15:0	RC	0x0	FCS error count, cleared by read

STA_CSR1: Long error / CCA false alarm counter (offset = 30C4h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	CCA false alarm count, cleared by read
Bit 15:0	RC	0x0	PHY error count, cleared by read

STA_CSR2: RX FIFO Overflow (offset = 30C8h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	RX Packet buffer overflow error count, cleared by read
Bit 15:0	RC	0x0	MAC RX FIFO overflow count, cleared by read

STA_CSR3: TX beacon counter (offset = 30CCh)

Field	Type	Default	Description
Bit 31:16	R	0x0	Reserved
Bit 15:0	RC	0x0	TX beacon count, cleared by read

STA_CSR4: TX Retry Counters (1) (offset = 30D0h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	One-retry successful TX counter
Bit 15:0	RC	0x0	No-retry successful TX counter

STA_CSR5: TX Retry Counters (2) (offset = 30D4h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	Retry failed TX counter
Bit 15:0	RC	0x0	Multi-retry successful TX counter

QOS Control Register

QOS_CSR0: TXOP holder address 0 register (offset = 30E0h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	TXOP holder address byte3
Bit 23:16	R/W	0x0	TXOP holder address byte2
Bit 15:8	R/W	0x0	TXOP holder address byte1
Bit 7:0	R/W	0x0	TXOP holder address byte0

QOS_CSR1: TXOP holder address 1 register (offset = 30E4h)

Field	Type	Default	Description
Bit 31:16	R	0x0	Reserved
Bit 15:8	R/W	0x0	TXOP holder byte5
Bit 7:0	R/W	0x0	TXOP holder byte4

It is recommend to fill TXOP holder with all 0s' to park early termination interrupt.

QOS_CSR2: TXOP holder early termination control register (offset = 30E8h)

Field	Type	Default	Description
Bit 31:26	R	0x0	Reserved
Bit 25	R/W	0x1	0: disable 1: enable TXOP holder early termination check on queue size(QS) value in the QC field(Qos control field). When RX packet is from TXOP holder specified in QOS_CSR0,1 (mactch with Addr2) and QS value is equal to zero, "TXOP holder early termination" interrupt will be issued after CRC check is ok.
Bit 24	R/W	0x1	0: disable 1: enable TXOP holder early termination check on duration field When RX packet is from TXOP holder specified in QOS_CSR0,1 (mactch with Addr2) and duration value is less than or equal to early termination duration threshold specified below, "TXOP holder early termination" interrupt will be issued after CRC check is ok.
Bit 23:16	R/W	0x0	Early termination duration threshold
Bit 15:9	R	0x0	Reserved

Bit 8	R/W	0x0	0: disable 1: enable TXOP holder early timeout interrupt When this bit is enabled, ASIC will expect CCA while channel listening starts. If ASIC didn't see CCA over the TXOP holder early timeout limit, the "TXOP holder early timeout" interrupt will be issued.
Bit 7:0	R/W	0x0	TXOP holder early timeout limit (unit: 1us)

QOS_CSR3: RX CF-Poll Address1 register0 (offset = 30ECh)

Field	Type	Default	Description
Bit 31:24	R	0x0	Address1 byte3 of RX CF-Poll Packet
Bit 23:16	R	0x0	Address1 byte2 of RX CF-Poll Packet
Bit 15:8	R	0x0	Address1 byte1 of RX CF-Poll Packet
Bit 7:0	R	0x0	Address1 byte0 of RX CF-Poll Packet

QOS_CSR4: RX CF-Poll Address1 register1 (offset = 30F0h)

Field	Type	Default	Description
Bit 31:17	R	0x0	Reserved
Bit 16	R	0x0	1: RX CF-Poll Packet is equal to MAC Address (MAC_CSR2,3)(unicast –to-me) 0: not equal
Bit 15:8	R	0x0	Address1 byte5 of RX CF-Poll Packet
Bit 7:0	R	0x0	Address1 byte4 of RX CF-Poll Packet

QOS_CSR5: RX CF-Poll QOS control field register (offset = 30F4h)

Field	Type	Default	Description
Bit 31:16	R	0x0	Reserved
Bit 15:8	R	0x0	QOS control field byte1 of RX CF-Poll Packet (byte offset =25)
Bit 7:0	R	0x0	QOS control field byte0 of RX CF-Poll Packet (byte offset =24)

QOS_CSR3,4,5 is updated right after RX_CF_POLL interrupt.

USB command

USB Standard Request

All USB devices must respond to a variety of requests called “standard requests”. These requests are used for configuring a device and controlling the state of its interface, along with other miscellaneous features. For more detailed information, please refer to Chapter 9 of the USB Specification Rev. 2.0.

Get Descriptor Request

Format:

RequestType	Request	wValue	wIndex	wLength	Data
80H	06H	Descriptor Type and Index	Zero or Language ID	Descriptor Length	Descriptor

Valid command:

Command	Format	Data stage	Description
Get device descriptor	80 06 00 01 00 00 XX YY	YYXX bytes data	*Max_length*=18 bytes
Get configuration descriptor	80 06 00 02 00 00 XX YY	YYXX bytes data	Return configuration, interface and endpoint descriptors
Get string1 descriptor	80 06 01 03 00 00 XX YY	YYXX bytes data	Get string1 length=YYXX
Get string2 descriptor	80 06 02 03 00 00 XX YY	YYXX bytes data	Get string2 length=YYXX
Get string3 descriptor	80 06 03 03 00 00 XX YY	YYXX bytes data	Get string3 length=YYXX
Get device qualifier	80 06 00 06 00 00 XX YY	YYXX bytes data	*Max_length*=10 bytes
Get other speed configuration	80 06 00 07 00 00 XX YY	YYXX bytes data	Return other configuration, interface and endpoint descriptors

Return *max_length* of descriptors if YYXX > *max_length*

Set Address Request

Format:

RequestType	Request	WValue	wIndex	wLength	Data
00H	05H	Device address	Zero	Zero	N/A

Valid command:

Command	Format	Data stage	Description
Set address	00 05 XX 00 00 00 00 00	N/A	Set device address #XX

Clear feature Request

Format:

RequestType	Request	wValue	wIndex	wLength	Data
00H 01H 02H	01H	Feature selector	Zero Interface Endpoint	Zero	N/A

Feature selector:

Feature selector	Recipient	Value	Action
DEVICE_REMOTE_WAKEUP	Device	1	Not support, stall EP0
ENDPOINT_HALT	Endpoint	0	Stall endpoint
TEST_MODE	Device	2	Set test mode

Valid command:

Command	Format	Data stage	Description
Clear feature EP STALL	02 01 00 00 PP 00 00 00	N/A	Clear endpoint #PP STALL

Set feature Request

Format:

RequestType	Request	wValue	wIndex		wLength	Data
00H 01H 02H	03H	Feature selector	Test mode selector	Zero Interface Endpoint	Zero	N/A

Test mode selector:

Value	Description
01H	Test_J
02H	Test_K
03H	Test_SE0_NAK
04H	Test_Packet
05H	Test_Force_Enable
Others	Reserved

Valid command:

Command	Format	Data stage	Description
Set feature EP STALL	02 03 00 00 PP 00 00 00	N/A	Set endpoint #PP STALL
Set feature Test Mode	00 03 02 00 00 TT 00 00	N/A	Set device test mode #TT (see *Test mode selector*)

Set Configuration Request

Format:

RequestType	Request	wValue	wIndex	wLength	Data
00H	09H	Configuration number	Zero	Zero	N/A

Valid command:

Command	Format	Data stage	Description
Set configuration 0	00 09 00 00 00 00 00 00	N/A	Set configuration #00
Set configuration 1	00 09 01 00 00 00 00 00	N/A	Set configuration #01

Get Configuration Request

Format:

RequestType	Request	wValue	wIndex	wLength	Data
80H	08H	Zero	Zero	One	Configuration number

Valid command:

Command	Format	Data stage	Description
Get configuration	80 08 00 00 00 00 01 00	1 byte	Get configuration number

Set Interface Request

Format:

RequestType	Request	wValue	wIndex	wLength	Data
01H	0BH	Alternate setting	Interface	Zero	N/A

Valid command:

Command	Format	Data stage	Description
Set interface	01 0B 00 00 00 00 00 00	N/A	Set default setting in interface 0

Get Interface Request

Format:

RequestType	Request	wValue	wIndex	wLength	Data
81H	0AH	Zero	Interface	One	Alternate setting

Valid command:

Command	Format	Data stage	Description
Get interface	81 0A 00 00 00 00 01 00	1 byte data	Get interface

Get status

Format:

RequestType	Request	wValue	wIndex	wLength	Data
80H 81H 82H	00H	Zero	Zero Interface Endpoint	Two	Status

Valid command:

Command	Format	Data stage	Description
Get device status	80 01 00 00 00 00 02 00	2 bytes data	Get device status
Get interface status	81 01 00 00 00 00 02 00	2 bytes data	Get interface status
Get endpoint status	82 01 00 00 PP 00 02 00	2 bytes data	Get endpoint # PP status

USB Vendor Request

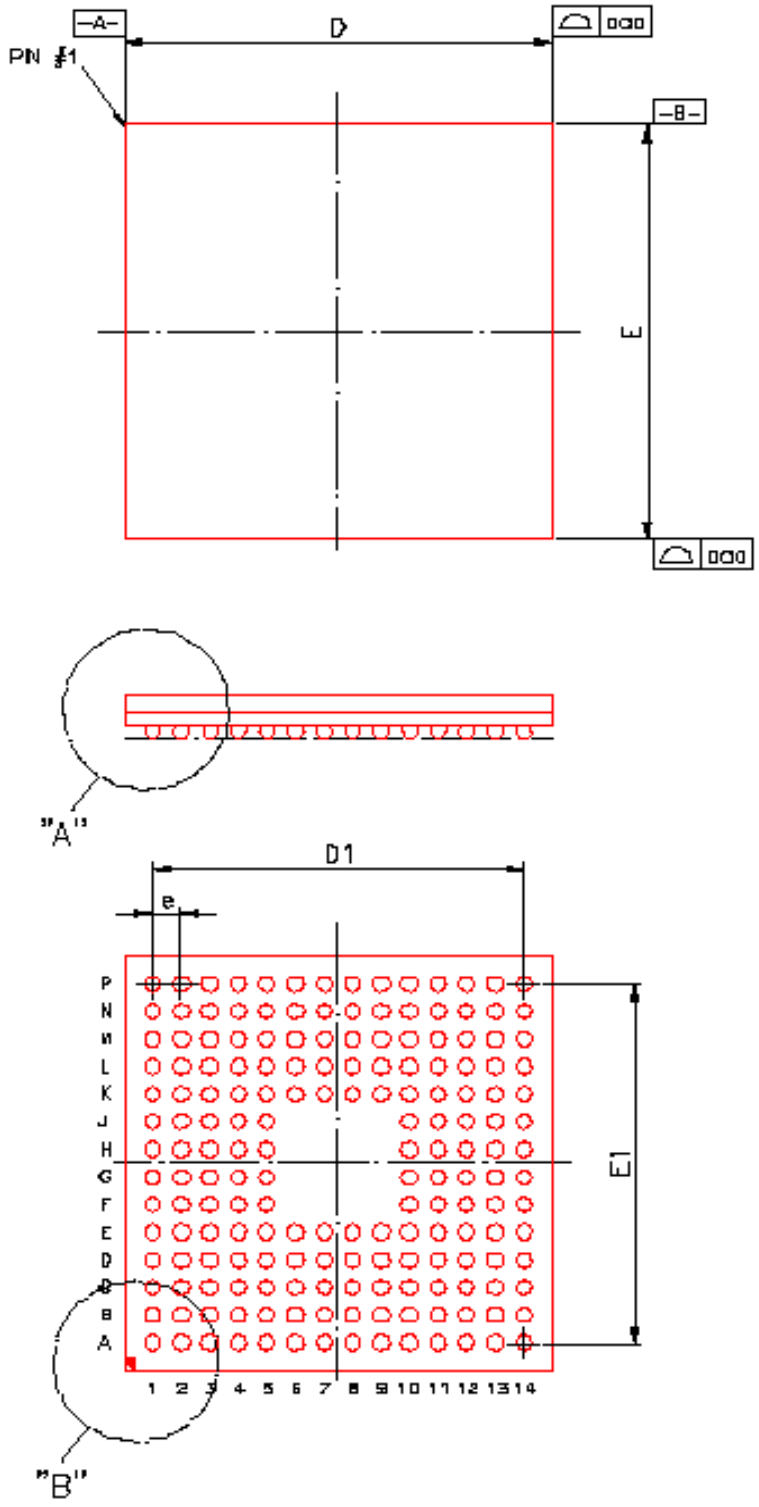
Besides standard requests, RT2571W also offers various vendor requests for internal registers access or special purpose.

Command	Format	Data stage	Description
Vender reset	40 01 01 00 00 00 00 00	N/A	Reset
Disconnect	40 01 02 00 00 00 00 00	N/A	Soft disconnect
Firmware switch	40 01 06 0X 00 00 00 00	N/A	Switch firmware mode (X=0 external, X=1 internal)
Put to sleep	40 01 07 00 00 00 00 00	N/A	Put NIC to sleeping mode
NIC Init OK	40 01 08 00 00 00 00 00	N/A	NIC initialization complete
Wake up	40 01 09 00 00 00 00 00	N/A	Wake up NIC
Single write	40 02 AA BB CC DD 01 00	N/A	XBYTE[DDCC] = AA;
Single write	40 02 AA BB CC DD 02 00	N/A	XBYTE[DDCC] = AA; XBYTE[DDCC+1] = BB
Single read	C0 03 00 00 CC DD 01 00	1 byte data	AA = XBYTE[DDCC]
Single read	C0 03 00 00 CC DD 02 00	2 bytes data	AA = XBYTE[DDCC]; BB=XBYTE[DDCC+1]
Multiple write	40 06 00 00 CC DD EE FF	FFEE bytes data	Write FFEE bytes from address DDCC
Multiple read	C0 07 00 00 CC DD EE FF	FFEE bytes data	Read FFEE bytes from address DDCC
EEPROM write	40 08 00 00 CC DD EE FF	FFEE bytes data	Write FFEE bytes into EEPROM
EEPROM read	C0 09 00 00 CC DD EE FF	FFEE bytes data	Read FFEE bytes from EEPROM
Stop Rx	40 0C 00 00 CC DD 00 00	N/A	Driver attempts to stop Rx
Nor flash erase	40 0D 00 B0 CC 00 00 00	N/A	Erase block, address = CCB000
Nor flash write	40 0E 00 B0 CC 00 00 F0	F000h bytes data	Write F000h Bytes to address CC_B000h (4KB alignment, no crossing 64KB boundary allowed)
Nor flash read	C0 0F 00 B0 CC 00 00 F0	F000h bytes data	Read F000h Bytes from address CC_B000h (4KB alignment, no crossing 64KB boundary allowed)

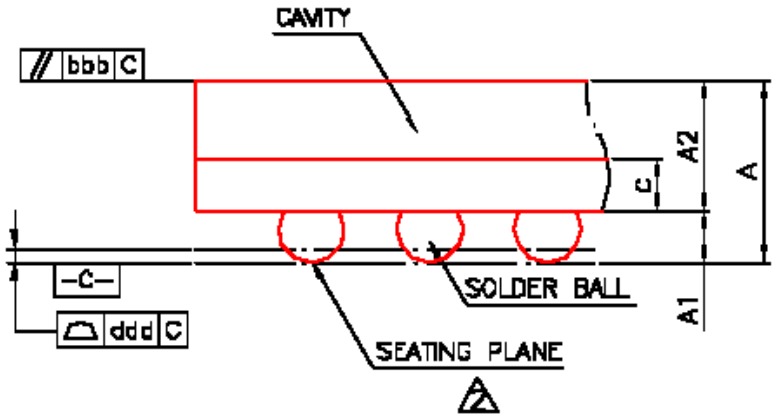
”XBYTE[DDCC]” means write or read one byte data at address “DDCC”.

Package Physical Dimension：

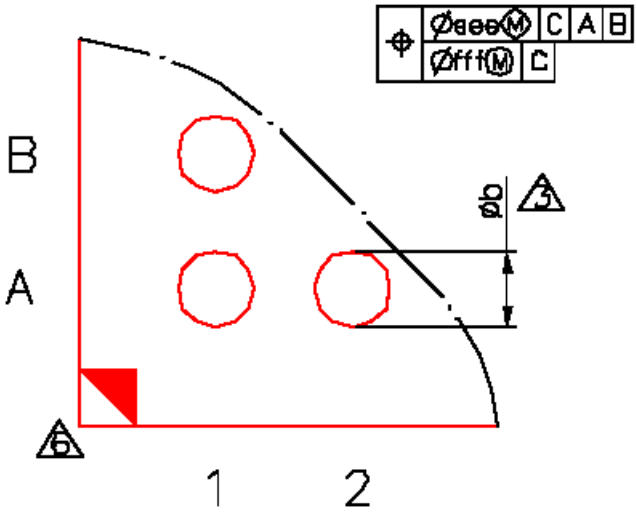
TFBGA 12X12 180B (12x12x1.4mm)



BOTTOM VIEW



DETAIL : "A"



DETAIL : "B"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	10.40	---	---	0.409	---
E1	---	10.40	---	---	0.409	---
e	---	0.80	---	---	0.031	---
b	0.40	0.45	0.50	0.016	0.018	0.020
aaa		0.10			0.004	
bbb		0.10			0.004	
ddd		0.12			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		14/14			14/14	

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-205.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

Revision History

Rev	Date	From	Description
1.0	04/26/05	Max. L	Initiate the data sheet.
2.0	07/01/05	Max. L	Modify the data sheet
2.1	07/20/05	Max. L	Modify MAC_CSR14 LED control register
3.0	06/28/06	Allie	Unify datasheet version
3.1	10/05/06	Max. L	Modify DC Electrical Specifications
3.2	12/22/06	Allie Hsieh	Add the disclaimer in the last page
3.3	6/22/07	Max. L	Modify Pin Description G4