4.5V to 18V, 5A/5A Dual Synchronous Step-Down Converter

General Description

The RT2825 features two synchronous wide input range high efficiency buck converters that cab deliver up to 5A/5A output current from a 4.5V to 18V input supply. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5V, 9V, 12V or 15V systems and have integrated power transistors. The RT2825's current mode architecture allows the transient response to be improved. Cycle-by-cycle current limit provides protection against shorted outputs.

Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The COMP pin allows optimizing transient versus dc accuracy response with a simple RC compensation.

The switching frequency of the converters can either be set with an external resistor connected to ROSC pin or can be synchronized to an external clock if needed. The switching regulators are designed to operate from 200kHz to 1MHz. The converters operate with 180° phase between two channels to minimize the input filter requirements.

The RT2825 also features a low power mode enabled by an external signal, which allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

The RT2825 is available in a VQFN-36L 6x6 package.

Features

- **Wide Input Supply Voltage Range : 4.5V to 18V**
- **Fully Integrated Dual-Buck, Up to 5A/5A**
- **Adjustable Switching Frequency 200kHz to 1MHz Set by External Resistor or SYNC Signal**
- **Dedicated Enable/Soft-Start for Each Buck**
- **Current Mode Control with Simple Compensation Circuit**
- **Adjustable Cycle-by-Cycle Current Limit Set by External Resistor**
- **Over-Temperature Protection**
- **Power Good Indicator**
- **Discontinuous Operating Mode at Light Load when LOWP = L**
- **1% V_{REF} Accuracy**
- **RoHS Compliant and Halogen Free**

Applications

- DTV
- TCON
- BDVD
- Set Top Boxes
- Tablet

Ordering Information

RT2825☐☐☐

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QV : VQFN-36L 6x6 (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

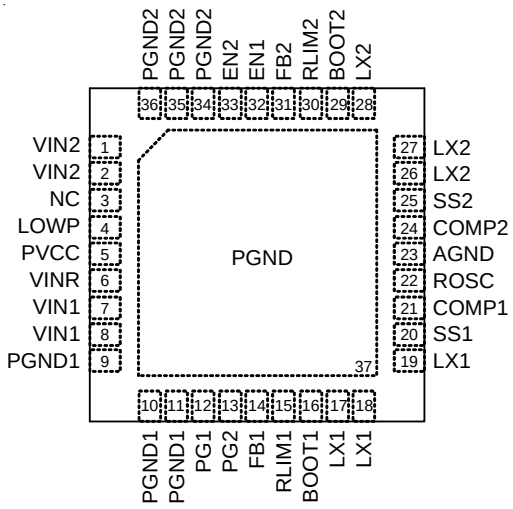
RT2825
GQV
YMDNN
●

RT2825GQV : Product Number

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



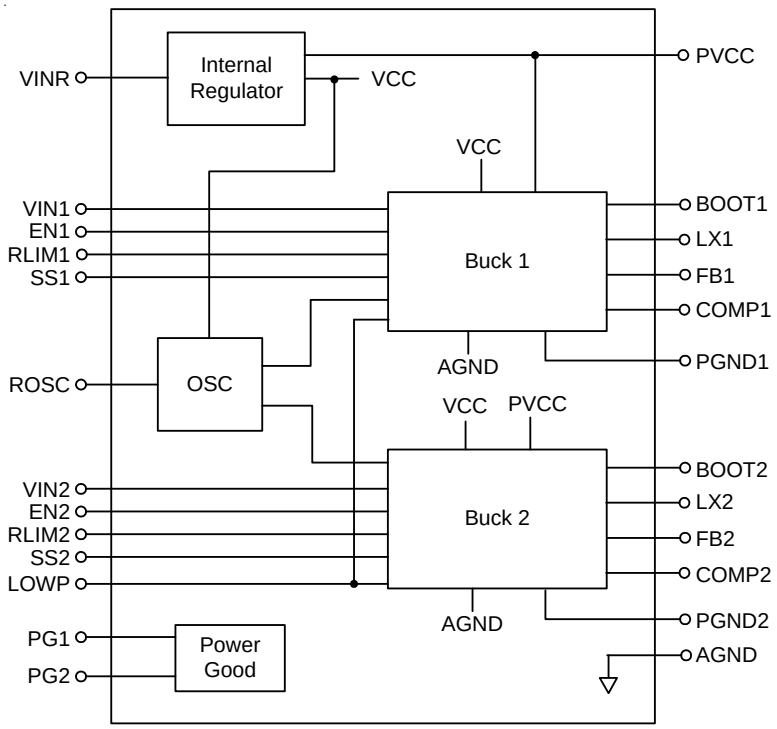
VQFN-36L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VIN2	Power input for CH2. Place a 10μF ceramic capacitor close to this pin.
3	NC	No internal connection.
4	LOWP	Discontinuous operation mode input.
5	PVCC	5V power supply output. Connect a capacitor 1uF between this pin and AGND.
6	VINR	Supply voltage input for internal control circuit.
7,8	VIN1	Power input for CH1. Place a 10μF ceramic capacitor close to this pin.
9, 10, 11	PGND1	Power ground for CH1.
12	PG1	Power good indicator output with open-drain of CH1.
13	PG2	Power good indicator output with open-drain of CH2.
14	FB1	Feedback voltage input for CH1.
15	RLIM1	Current limit setting for CH 1. Connect a resistor from RLIM1 to AGND to set the peak current limit on the output inductor.
16	BOOT1	Bootstrap supply for high-side gate driver of CH1. Connect a 0.1μF ceramic capacitor from this pin to LX1
17, 18, 19	LX1	Switch node of CH1.
20	SS1	Soft-start time setting for CH1. Connect a capacitor to this pin and AGND for soft-start time setting.
21	COMP1	Compensation node for CH1. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to AGND. In some cases, an additional capacitor from COMP to AGND is required.
22	ROSC	Oscillator setting. Connect a resistor from ROSC to GND to set the switching frequency. When this pin connects to an external clock, the internal oscillator will synchronize to the external clock.
23	AGND	Analog ground.

Pin No.	Pin Name	Pin Function
24	COMP2	Compensation node for CH2. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to AGND. In some cases, an additional capacitor from COMP to AGND is required.
25	SS2	Soft-start time setting for CH2. Connect a capacitor to this pin and AGND for soft-start time setting.
26, 27, 28	LX2	Switch node of CH2.
29	BOOT2	Bootstrap supply for high-side gate driver of CH2. Connect a 0.1μF ceramic capacitor from this pin to LX2
30	RLIM2	Current limit setting for CH2. Connect a resistor from RLIM2 to AGND to set the peak current limit on the output inductor.
31	FB2	Feedback voltage input for CH2.
32	EN1	Enable control input for CH1. A low level signal on this pin disables it. If this pin is left open, a weak internal pull-up will allow automatic enables.
33	EN2	Enable control input for CH2. A low level signal on this pin disables it. If this pin is left open, a weak internal pull-up will allow automatic enables.
34, 35, 36	PGND2	Power ground for CH2.
37 (Exposed Pad)	PGND	Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

Functional Block Diagram



Operation

UV Comparator

If the feedback voltage (V_{FB}) is lower than threshold voltage (91% of V_{REF}), the UV Comparator's output goes high and the logic control circuit is allowed to turn on the MOSFET to pull PG1/PG2 pin to low.

OV Comparator

If the feedback voltage (V_{FB}) is higher than threshold voltage (109% of V_{REF}), the OV Comparator's output goes high and the logic control circuit is allowed to turn on the MOSFET to pull PG1/PG2 pin to low.

Voltage Reference

The converter produces a precise ±1% voltage reference over-temperature by scaling the output of a temperature stable bandgap circuit.

Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the FB pin voltage with the SS pin voltage and the internal reference voltage which is 0.6V. The transconductance of the error amplifier is 1300 μA/V during normal operation. The compensation network should be connected between the COMP pin and ground.

Oscillator with RT/SYNC Function

The switching frequency is adjustable by an external resistor connected between the ROSC pin and GND. The available frequency range is from 200kHz to 1MHz. An internal synchronized circuit has been implemented to switch from RT mode to SYNC mode. To implement the synchronization function, connect a square wave clock signal to the ROSC pin with a duty cycle between 10% to 90%. The switching cycle is synchronized to the falling edge of the external clock at ROSC pin.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VINR, VIN1,VIN2 ---------- –0.3V to 20V
- Switch Node Voltage, LX ---------- –0.3V to 20.3V
  LX (t ≤ 10ns) ---------- –7V to 33V
- BOOT Pin Voltage ---------- –0.3V to 26.3V
  BOOT (t ≤ 10ns) ---------- –3.9V to 33V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-36L 6x6 ---------- 3.66W
- Package Thermal Resistance (Note 2)
  VQFN-36L 6x6, θ_{JA} ---------- 27.3°C/W
  VQFN-36L 6x6, θ_{JC} ---------- 4.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 4.5V to 18V, T_A = –45°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Operating Input Voltage	V_{IN}		4.5	--	18	V
Shutdown Supply Current	I_{SHDN}	V_{EN1} = V_{EN2} = 0V	--	5	--	μA
Supply Current (No Switching)	I_{Q_NSW}	V_{EN1} = V_{EN2} = V_{LOWP} = 3.3V, without bucks switching	--	2.6	--	mA
Supply Current (Switching)	I_{Q_SW}	V_{EN1} = V_{EN2} = V_{LOWP} = 3.3V, with bucks switching	--	30	--	mA
VINR Internal UVLO Threshold	UVLO	VINR rising	--	4.25	4.5	V
		VINR falling	3.5	3.75	--	
		Hysteresis	--	0.5	--	
5.1V LDO	V_{PVCC}	VPVCC load current = 0A	--	5.1	--	V
Enable						
EN Threshold	V_{IH}	Rising	--	1.21	1.26	V
EN Threshold	V_{IL}	Falling	1.1	1.17	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Pull High Current		V_{EN} = 1.1V	--	3	--	μA
EN Hysteresis Current		V_{EN} = 1.3V	--	3	--	μA
Oscillator						
Switching Frequency	f_{OSC}	R_{OSC} = 36kΩ	800	1000	1200	kHz
		R_{OSC} = 90.9kΩ	352	440	528	
		R_{OSC} = 210kΩ	160	200	240	
Switching Frequency Range (RT/SYNC Mode)		Include Sync Mode and RT Mode Set Point	200	--	1000	kHz
Minimum Pulse Width			--	20	--	ns
SYNC Threshold Voltage		High-Level	--	--	2	V
		Low-Level	0.8	--	--	
SYNC Falling Edge to LX Rising Edge Delay		Measure at 500kHz with ROSC resistor in series	--	66	--	ns
Buck1, Buck2 Converters						
Reference Voltage	V_{REF}	0A ≤ I_{LOAD} ≤ 6A	0.594	0.6	0.606	V
Line Regulation		I_{OUT} = 2A	--	0.5	--	%/V
Load Regulation		I_{OUT} = (10% - 90%) x $I_{OUT(MAX)}$	--	0.5	--	%/A
Error Amplifier G_M		−2μA < I_{COMP} < 2μA, V_{COMP} = 1V	--	1300	--	μMHOS
COMP to I_{switch} G_N			--	16	--	A/V
SS Charge Current			--	6	--	μA
Upper Switch Current Limit		R_{LIM} = 60.4kΩ	--	8.4	--	A
Lower Sinking Current Limit			--	2.6	--	A
High-Side Switch On-Resistance	$R_{DS(ON)\_U}$		--	31	48	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$		--	23	36	mΩ
Minimum On-Time	t_{ON_MIN}		--	70	100	ns
BOOT-PH UVLO			--	2.1	3	V
Hiccup Wait Time			--	512	--	cycles
Hiccup Time before Re-start			--	16384	--	cycles
Power Good						
Power Good Rising Threshold		V_{FB} rising (Good)	--	94	--	%
		V_{FB} rising (Fault)	--	109	--	
Power Good Falling Threshold		V_{FB} falling (Fault)	--	91	--	%
		V_{FB} falling (Good)	--	106	--	
Over-Temperature Protection						
Thermal Shutdown	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
LOWP Threshold Voltage	High-Level			--	--	2	V
	Low-Level			0.8	--	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

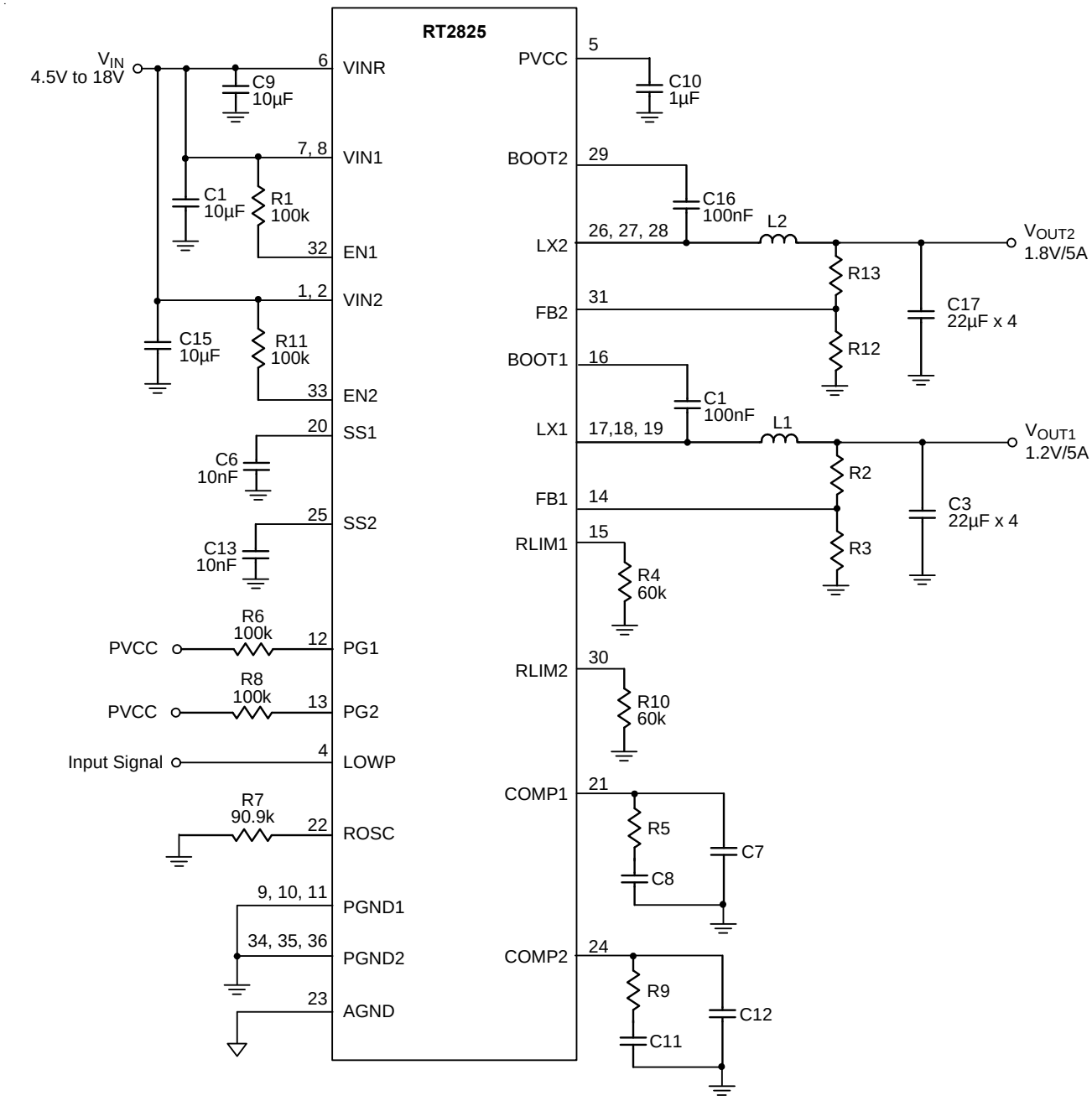
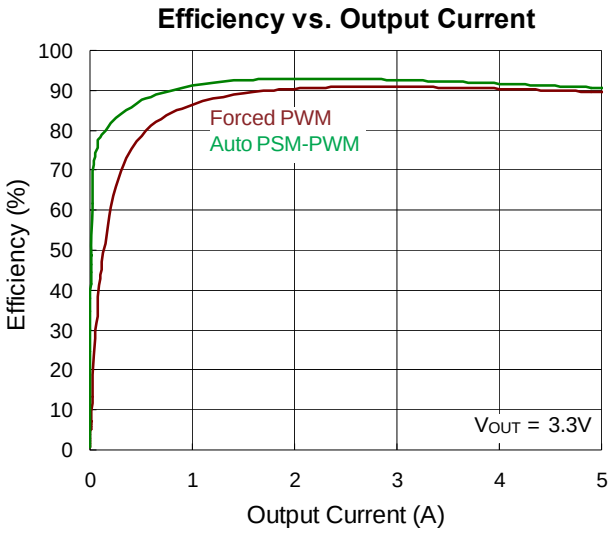


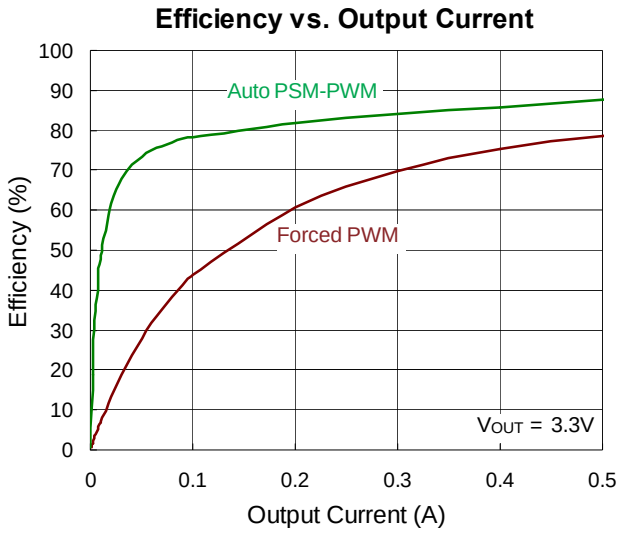
Table 1. Suggested Component Values

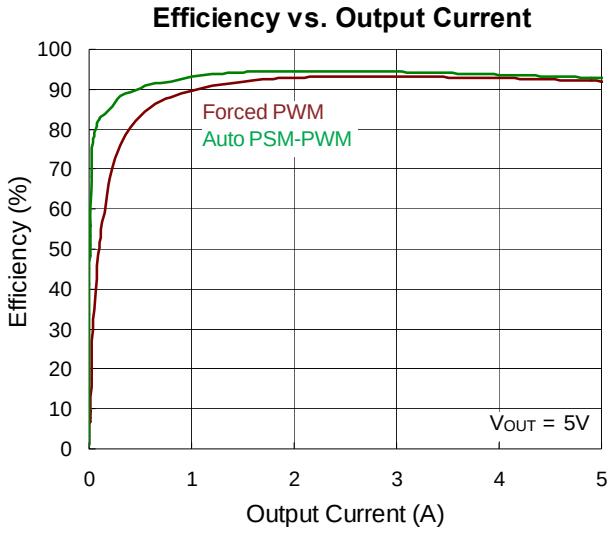
V_{OUT} (V)	R13/R2 (kΩ)	R12/R3 (kΩ)	R5/R9 (kΩ)	C8/C11 (nF)	C7/C12 (pF)	C_{OUT} (μF)	L (μH)
5.0	176	24	6.04	8.2	180	22 x 4	4.7
3.3	108	24	3.3	8.2	180	22 x 4	3.6
2.5	76	24	2.49	8.2	180	22 x 4	3.6
1.8	48	24	2.1	8.2	180	22 x 4	2.2
1.5	36	24	1.4	8.2	180	22 x 4	2.2
1.2	24	24	1.2	8.2	180	22 x 4	2.2
1.0	16	24	1	8.2	180	22 x 4	1.5

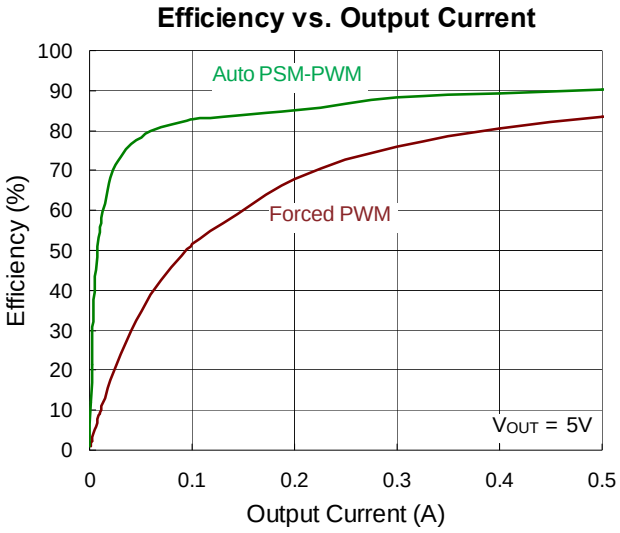
Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

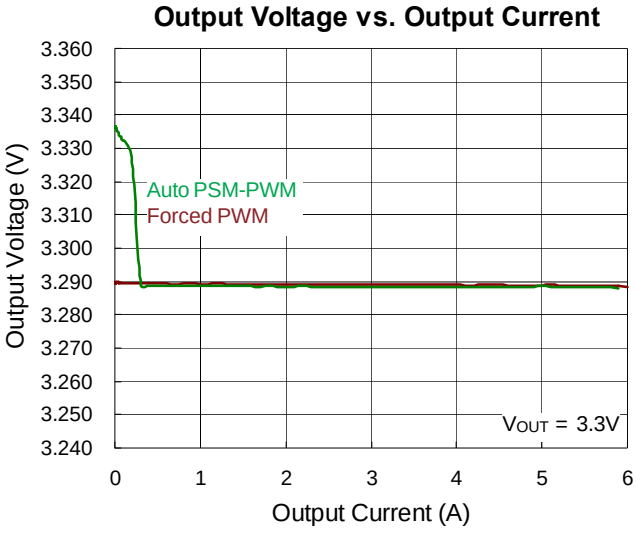
Typical Operating Characteristics

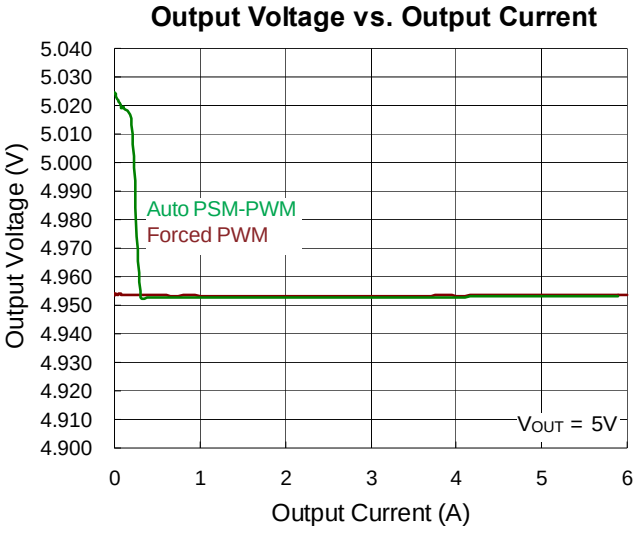




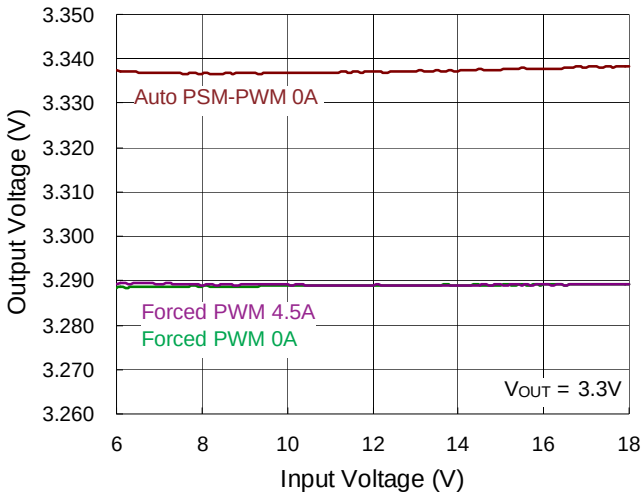




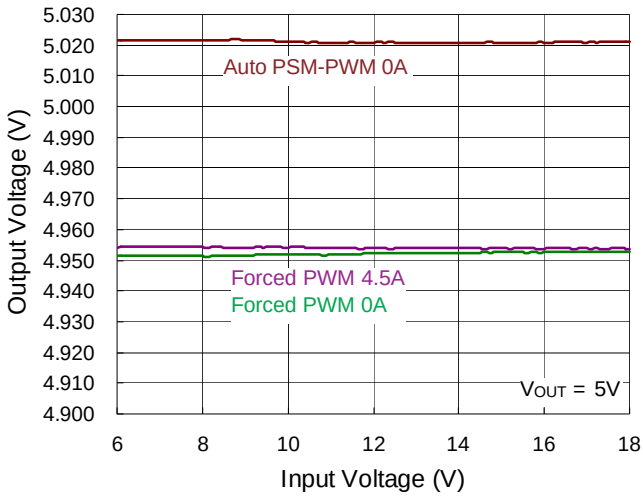




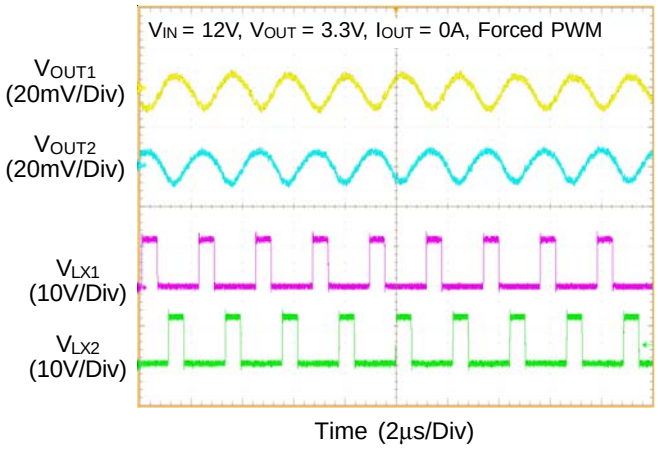
Input Voltage vs. Output Voltage



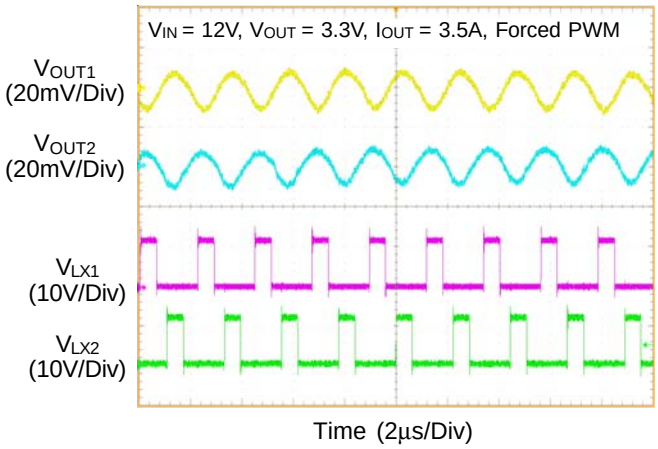
Input Voltage vs. Output Voltage



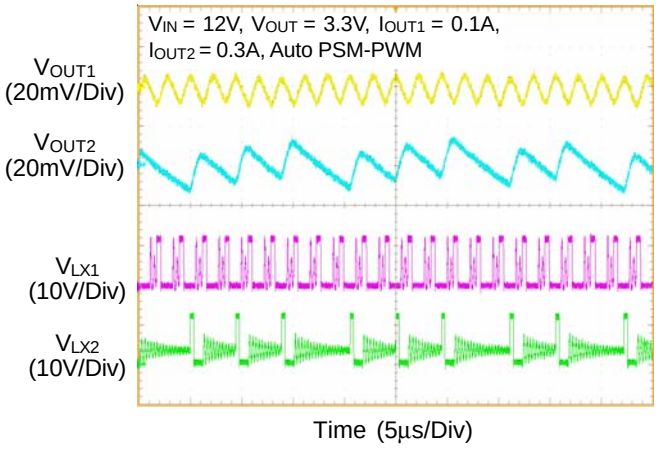
Output Ripple Voltage



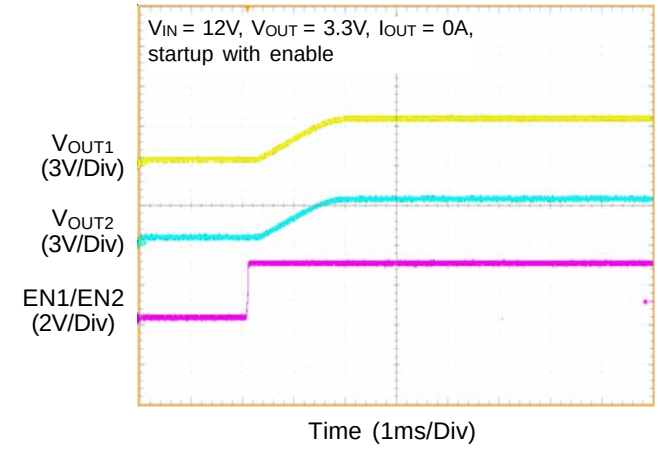
Output Ripple Voltage



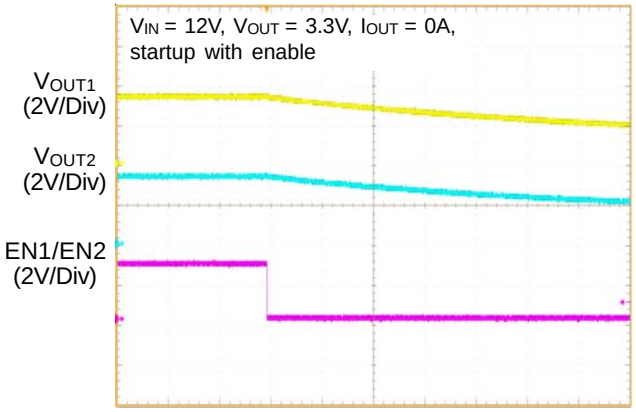
Output Ripple Voltage



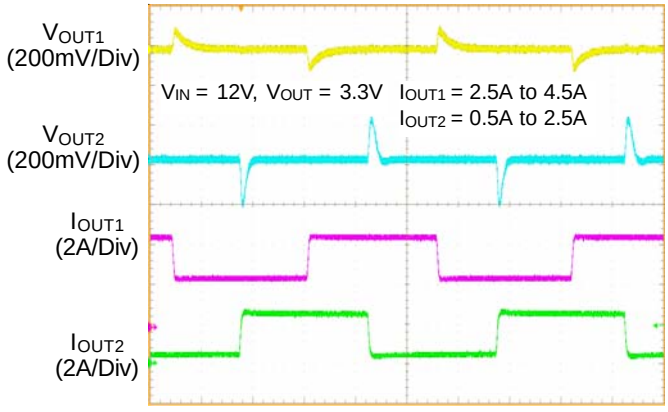
Power On from Enable



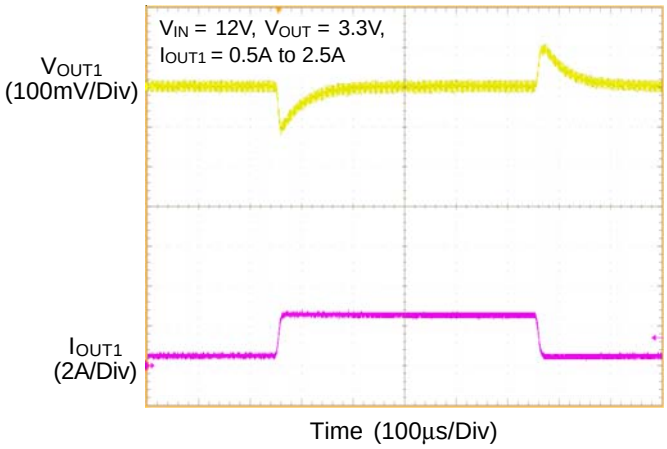
Power Off from Enable



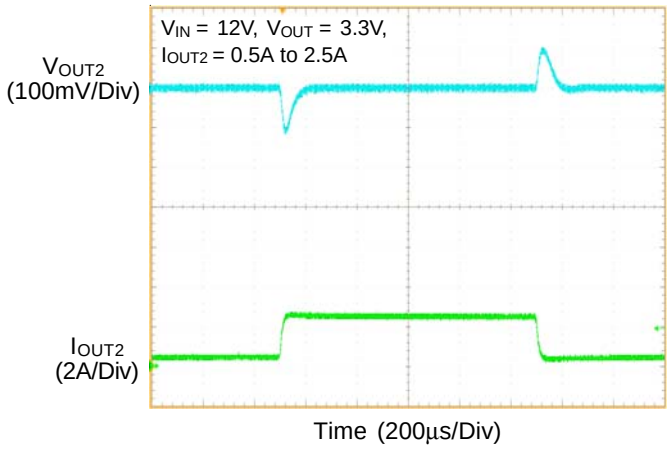
Load Transient Response



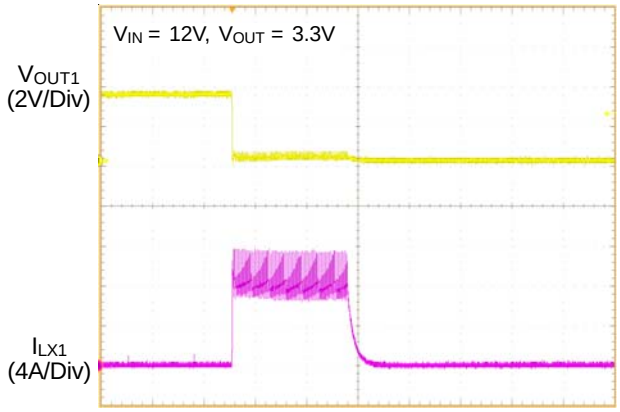
Load Transient Response



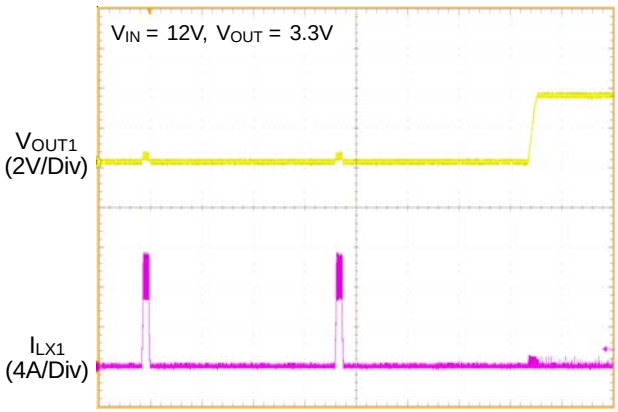
Load Transient Response



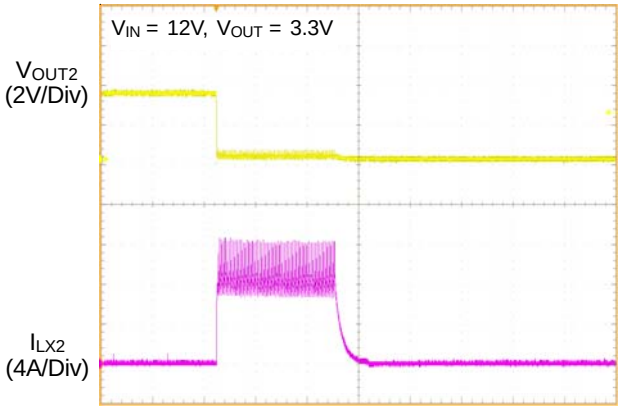
Power On than Short



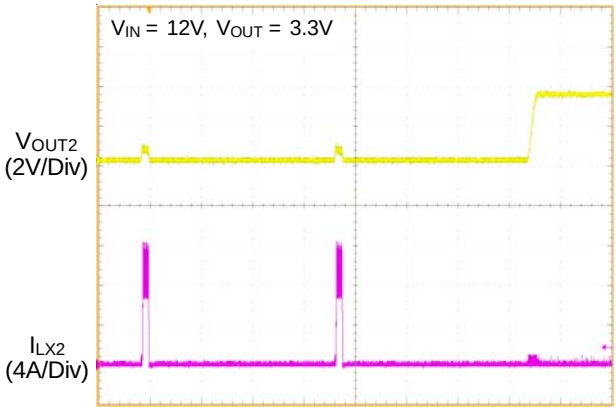
Hiccup Recover



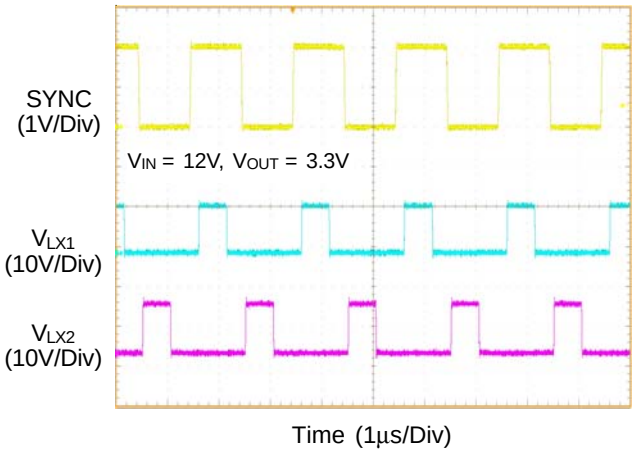
Power On than Short



Hiccup Recover



SYNC at 500kHz



Application Information

The RT2825 features two synchronous wide input range high efficiency buck converters that cab deliver up to 5A/ 5A output current from a 4.5V to 18V input supply. Each Buck PWM converter with two integrated N-MOSFETs. It provides good performance during load and line transients by implementing a single feedback loop, current-mode control, and external compensation. The integrated synchronous power switches can increase efficiency and it is suitable for lower duty cycle applications. The switching frequency can be externally set from 200kHz to 1MHz which allows for high efficiency and optimal size selection of output filter components. In additional, there is a synchronization mode control in this device which can be synchronized to the external clock frequency, and easily switched from internal switching mode to synchronization mode.

The device contains a power good protection and an external soft-start function that is able to monitor the system output voltage for normal regulation and provides a programmable power up sequence for avoiding inrush currents efficiently. Furthermore, the device incorporates a lot of protections such as OVP, OCP, OTP and etc.

Main Control Loop

The device implements an adjustable fixed frequency with peak current-mode control which offers an excellent performance over various line and loading. During normal operation, the internal high-side power switch is turned on by the internal oscillator initiating. Current in the inductor increases until the high-side switch current reaches the current reference converted by the output voltage V_{COMP} of the error amplifier. The error amplifier adjusts its output voltage by comparing the feedback signal from a resistive voltage divider on the FB pin with an internal 0.6V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier increases its current reference until the average inductor current matches the new load current. When the high-side power MOSFET turns off, the low-side synchronous power switch (N-MOSFET) turns on until the beginning of the next clock cycle.

VINR and VIN Pins

The VINR and VIN pins can be used together or separately for a variety of applications. In this device, the VINR pin is an input for supplying internal reference and control circuitry and the VIN pin is an input for providing main power to device system and internal high-side power MOSFET. When the VINR and VIN pins are tied together, both pins can operate from 4.5V to 18V. When the VINR and VIN pins are used separately, VINR pin must be ranged from 4.5V to 18V, and the VIN pin can be applied down to as low as 1.6V to 18V.

The device incorporates an internal Under-Voltage Lockout (UVLO) circuitry on the VIN pin. If the VIN pin voltage exceeds the UVLO rising threshold voltage 4.25V, the converter resets and prepares the PWM for operation. If the VINR pin voltage falls below the falling threshold voltage 3.75V during normal operation, the device is disabled.

Such wide internal UVLO hysteresis of 500mV can efficiently prevent noise caused reset. There is also an external UVLO circuitry which can be achieved by configuring a resistive voltage divider on EN pin for both input VINR and VIN pins and it is able to provide either input pins an adjustable UVLO function to ensure a proper power up behavior. More discussions are located in the section of Enable Operation.

Output Voltage Setting

The resistive voltage divider allows the FB pin to sense the output voltage as shown in Figure 1.

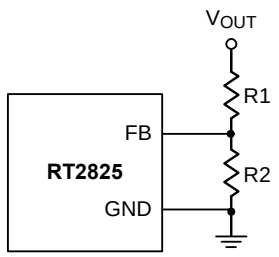


Figure 1. Setting the Output Voltage

For high efficiency, the divider resistance must adopt larger values, but too large values may induce noises and voltage errors by the coupled FB pin input current. It is recommended to use the values between 10kΩ and 100kΩ. The output voltage is set by an external resistive voltage divider according to the following Equation (1) :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right) \quad (1)$$

where V_{REF} is the feedback reference voltage (0.6V typ.).

Soft-Start

The device contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing is programmed by the external capacitor between SS pin and GND. The device provides an internal 6μA charge current for the external capacitor. If a 10nF capacitor is used to set the soft-start, the period can be 1.33ms. The calculations for external charge capacitor C_{SS} and soft-start time t_{SS} are shown in Equation (2) :

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (2)$$

where C_{SS} is the external soft-start capacitor, I_{SS} is the soft-start charge current (6μA), V_{REF} is the feedback reference voltage (0.6V).

Once the input voltage falls below UVLO threshold, the EN pin is pulled low, or the OTP is triggered, the device stops switching and the SS pin starts to discharge. It is held such shutdown condition until the event is cleared and the SS pin has already discharged to ground ensuring proper soft-start behavior.

During the pre-biased start-up sequence, the output of device is not discharged by low-side power switch because the device is designed to prevent low-side MOSFET sinking. It is allowed to sink when the SS pin exceeds 2.1V.

Enable Operation

The EN pin is an device enable input. Pulling the EN pin to logic low that is typically less than the set threshold voltage 1.17V, the device shuts down and enters to low quiescent current state about 2μA. The regulator starts switching again once the EN pin voltage exceeds the threshold voltage 1.21V. In additional, the EN pin is implemented with an internal pull-up current source which allows to enable the device when the EN pin is floating. For general external timing control, the EN pin can be externally pulled high by adding a capacitor and a resistor from the VINR pin as Figure 2.

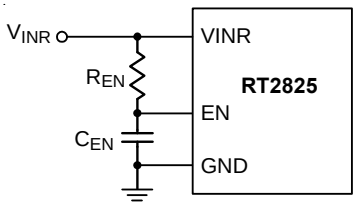


Figure 2. Enable Timing Control

An external MOSFET can be added to implement digital control from the EN pin to ground, as shown in Figure 3. In this case, there is no need to connect a pull-up resistor between the VINR and EN pins since the EN pin is pulled up by the internal current source. The device can simply achieve the digital control only through an external MOSFET on EN pin.

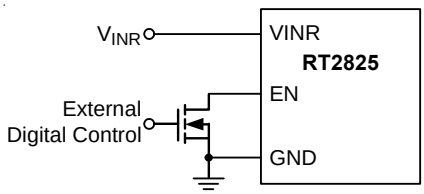


Figure 3. Digital Enable Control

The EN pin can also be applied to adjust its Under-Voltage Lockout (UVLO) threshold with two external resistors divider from the both input VINR and VIN pins used together or separately, and the application structures can refer to Figure 4, Figure 5, and Figure 6.

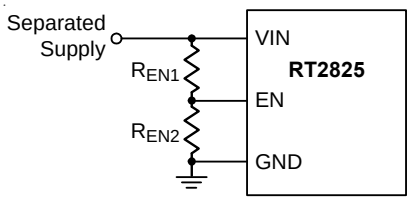


Figure 4. Resistor Divider for VIN UVLO Setting

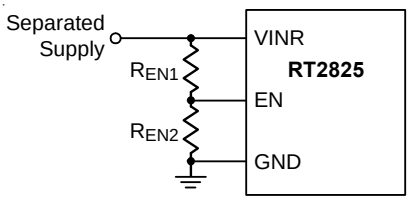


Figure 5. Resistor Divider for VINR UVLO Setting, VINR ≥ 4.5V

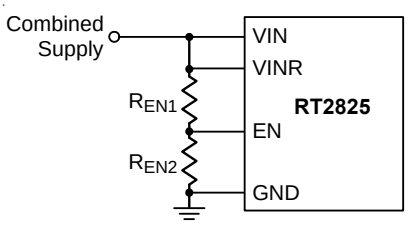


Figure 6. Resistor Divider for VIN and VINR UVLO Setting

Under above application structures, the adjustable UVLO function of EN pin allows to achieve a secondary UVLO on VIN pin, a higher UVLO on VINR pin or even a common UVLO on both VINR and VIN pins. For example, if the EN pin is configured as Figure 5 and the output voltage is set to a higher value 10V. The device may shut down after soft-start sequence is over, and the reason for the result is that the V_{OUT} is still lower than its set target during the V_{INR} rising period even though V_{INR} has already risen to its internal UVLO threshold 4V. To prevent this situation, an adjustable UVLO threshold from EN pin is useful to avoid such high output transfer condition. The exact UVLO thresholds can be calculated by Equation (3). The setting V_{OUT} is 10V and V_{INR} is from 0V to 18V. When V_{INR} is higher than 12V, the device is triggered to enable the converter. Assume R_{EN1} = 56kΩ. Then,

$$R_{EN2} = \frac{R_{EN1} \times V_{IH}}{V_{IN\_S} - V_{IH}} \quad (3)$$

where V_{IH} is the typical threshold of enable rising (1.21V) and V_{IN_S} is the target turn on input voltage (12V in this example). According to the equation, the suggested resistor R_{EN2} is 6.28kΩ.

Adjustable Operating Frequency-RT mode

Selection of the operating frequency is a tradeoff between efficiency and component size. Higher operating frequency allows the use of smaller inductor and capacitor values but it may press the minimum controllable on-time to affect devices stability. Lower operating frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and capacitance to maintain low output ripple voltage.

The operating frequency of the device is determined by an external resistor R_{OSC}, that is connected between the ROSC pin and ground. The value of the resistor sets the ramp current which is used to charge and discharge an internal timing capacitor within the oscillator. The practical switching frequency ranges from 200kHz to 1MHz. Determine the R_{OSC} resistor value by examining the curve in Figure 7.

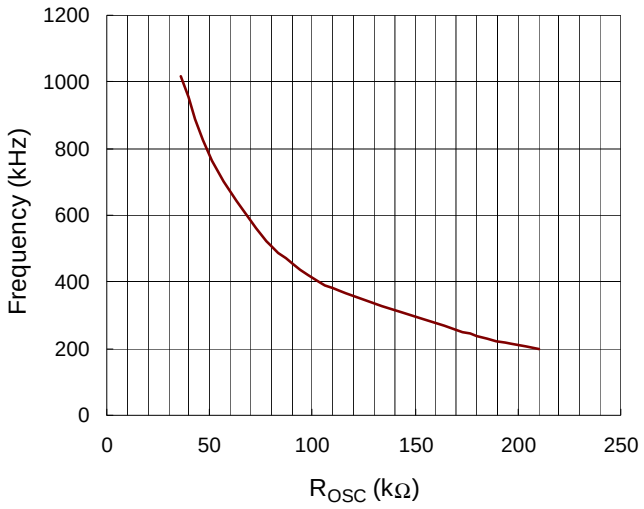


Figure 7. Switching Frequency vs. R_{OSC} Resistor

Synchronization-SYNC mode

The device is allowed to synchronize with an external square wave clock ranging from 200kHz to 1MHz applied to the ROSC pin. The range of sync duty cycle must be from 20% to 80%, and the amplitude of sync signal must be higher than 2V and lower than 0.8V. During the SYNC mode operation, the switching cycle of LX pin is synchronized to the falling edge of the external sync signal.

Before the external sync signal is provided to the ROSC pin, the device operates at the original switching frequency set by resistor R_{OSC}. When the sync signal is provided, the SYNC mode overrides the RT mode to force the device synchronizing to external frequency. This IC can easily switch between RT mode and SYNC mode, and the application structure can be configured as Figure 8.

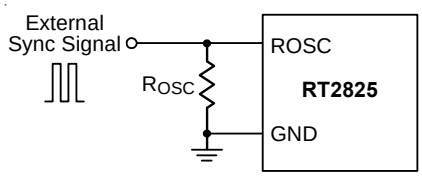


Figure 8. External Sync Signal Control

Power Good Output

The power good output is an open-drain output and needs to connect a voltage source below 5.5V with a pull-up resistor for avoiding the PGOOD floating. When the output voltage is 9% above or 9% below its set voltage, PGOOD is pulled low. It is held low until the output voltage returns within the allowed tolerances ±6% once more. During soft-start, PGOOD is actively held low when V_{IN} is greater than 1V and is only allowed to be high when soft-start period is over that means the SS pin exceeds 2.1V typically and the output voltage reaches 94% of its set voltage. Besides, the PG1/PG2 pin is also pulled low when the input UVLO or OVP are triggered, EN pin is pulled below 1.21V or the OTP is occurred.

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT and LX pins. This capacitor provides the gate driver voltage for the high-side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT2825. Note that the external boot voltage must be lower than 5.5V.

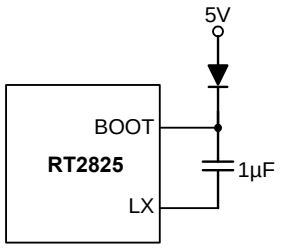


Figure 9. External Bootstrap Diode

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \quad (4)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. Highest efficiency operation is achieved by reducing ripple current at low frequency, but it requires a large inductor to attain this goal.

For the ripple current selection, the value of ΔI_L = 0.24 (I_{MAX}) is a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right] \quad (5)$$

In this device, 3.7µH is recommended for initial design. The current rating of the inductor (caused a 40°C temperature rising from 25°C ambient) must be greater than the maximum load current and ensure that the peak current does not saturate the inductor during short-circuit condition. Referring the Table 1 for the inductor selection reference.

Table 1. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4
WE	744325	10.2 x 10.2 x 4.7
WE	744355	12.8 x 12.8 x 6.2

Input and Output Capacitors Selection

The input capacitance C_{IN} is needed to filter the trapezoidal current at the Source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by Equation (6) :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \quad (6)$$

The formula above has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst condition is commonly used for design because even significant deviations do not offer much relief.

The effective input capacitance is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), rated output current (I_{OUT}), switching frequency (f_{SW}), and input ripple voltage of the regulator (ΔV_{INP}) :

$$C_{IN(MIN)} = \frac{I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW} \times \Delta V_{INP}} \quad (7)$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. It should pay attention that value of capacitors change as temperature, bias voltage, and operating frequency change. For example the capacitance value of a capacitor decreases as the dc bias across the capacitor increases.

Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. Considering the DC bias effects for the input capacitor, the typical operating circuit used one 10µF low ESR ceramic capacitors on the VIN pin and VINR pin respectively and an additional 0.1µF is recommended to place as close as possible to the IC input side for high frequency filtering.

All the recommended input and output capacitors can refer to Table 2 for more detail.

Table 2. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (µF)	Case Size
C_{IN}	**MURATA**	GRM32ER71H106K	10	1210
C_{IN}	**TDK**	C3225X7S1H106K	10	1210
C_{OUT}	**MURATA**	GRM31CR60J476M	47	1206
C_{OUT}	**TDK**	C3225X5R0J476M	47	1210
C_{OUT}	**MURATA**	GRM32ER71C226M	22	1210
C_{OUT}	**TDK**	C3225X5R1C226M	22	1210

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple ΔV_{OUT} is determined by Equation (8) :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right] \quad (8)$$

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Over-Current Protection (Hiccup Mode)

For the RT2825, a hiccup mode of Over-Current Protection (OCP) is incorporated. For example, when the power supply output is shorted to ground and the high-side switch over current condition is kept for more than 512 switching cycles which is named hiccup wait time, the hiccup mode is triggered to force the device to stop switching for a period of time. During the shutdown period, the internal oscillator continuously counts and it is allowed to recover switching after the hiccup time of 16384 cycles. Such periodically re-start condition continues until the OCP condition is removed and then the device returns to normal operation. The hiccup mode of OCP can reduce input average current to avoid the thermal issue in short-circuit conditions efficiently.

Output Over-Voltage Protection

The device provides an output Over-Voltage Protection (OVP) once the output voltage exceeds 109% of V_{OUT}, the OVP function turns off the high-side power MOSFET to stop current flowing to the output which can only be released when the output voltage drops below 106% of V_{OUT}. There is a 5μs delay also built into the over-voltage protection circuit to prevent false transition. Using this OVP feature can easily minimize the output overshoot.

High-Side MOSFET Over-Current Protection

The Over-Current Protection (OCP) of high-side MOSFET is implemented in this device, it adopts monitoring inductor current during the on-state to control the COMP pin voltage for turning off the high-side MOSFET. Each cycle the separated inductor current signal is compared through sensing the external inductor current to the COMP pin voltage from an error amplifier output. If the separated inductor current peak value exceeds the set current limit threshold, the high-side power switch is turned off.

Low-Side MOSFET Over-Current Protection

The device not only implements the high-side over-current protection but also provides the over sourcing current protection and over sinking current protection for low-side MOSFET. With these three current protections, the IC can easily control inductor current at both side power switches and avoid current runaway for short-circuit condition.

For the sourcing current protection, there is a specific comparator in internal circuitry to compare the low-side MOSFET sourcing current to the internal set current limit at the end of every clock cycle. When the low-side sourcing current is higher than the set sourcing limit, the high-side power switch is not turned on and low-side power switch is kept on until the following clock cycle for releasing the above sourcing current to the load. It is allowed to turn on the high-side MOSFET again when the low-side current is lower than the set sourcing current limit at the beginning of a new cycle.

For the sinking current protection, it is implemented by detecting the voltage across the low-side power switch. If the low-side reverse current exceeds the set sinking limit, both power switches are off immediately, and it is held to stop switching until the beginning of next cycle. By incorporating this additional protection, the device is able to prevent an excessive sinking current from the load during the condition of pre-biased output and the SS pin is asserted high that is 2.1V or above.

Over-Temperature Protection

An Over-Temperature Protection (OTP) is contained in the device. The protection is triggered to force the device shutdown for protecting itself when the junction temperature exceeds 160°C typically. Once the junction temperature drops below the hysteresis 20°C typically, the device is re-enable and automatically reinstates the power up sequence.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-36L 6x6 package, the thermal resistance, θ_{JA}, is 27.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.3°C/W) = 3.66W for a VQFN-36L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

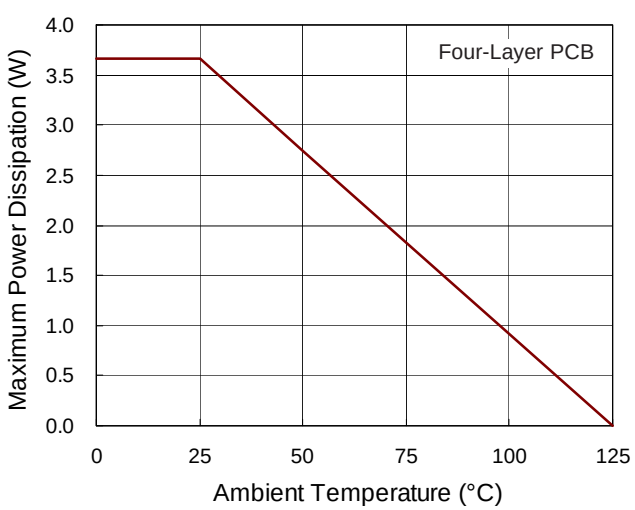
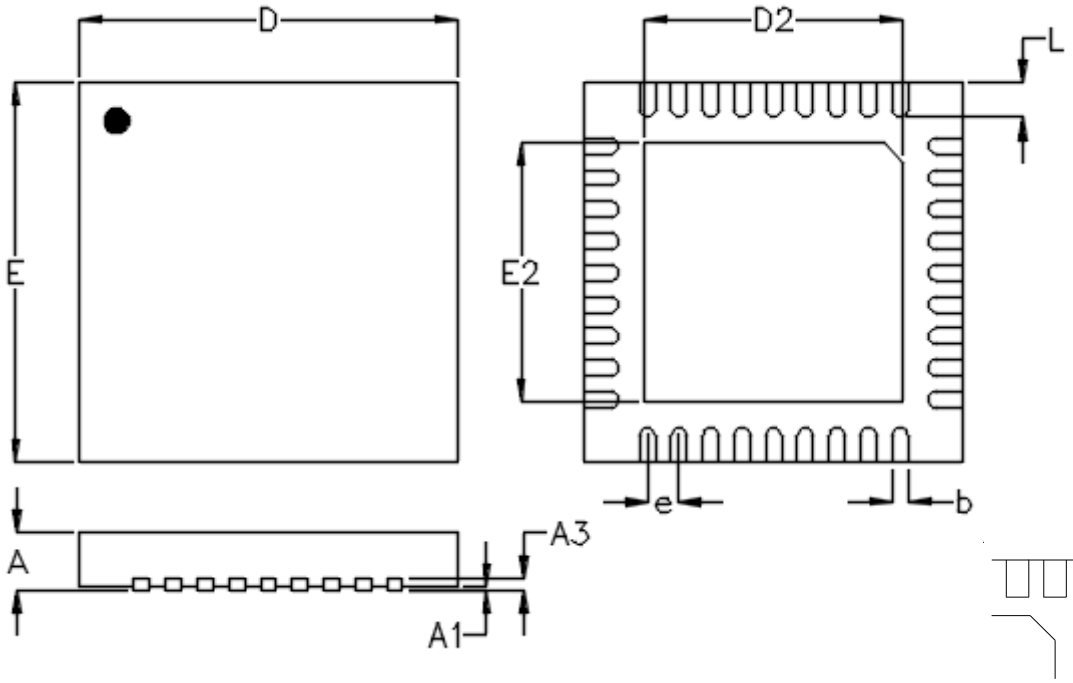
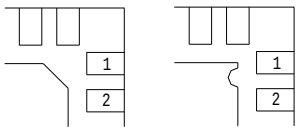


Figure 10. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	5.900	6.100	0.232	0.240
D2	4.050	4.150	0.159	0.163
E	5.900	6.100	0.232	0.240
E2	4.050	4.150	0.159	0.163
e	0.500		0.020	
L	0.500	0.600	0.020	0.024

V-Type 36L QFN 6x6 Package

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