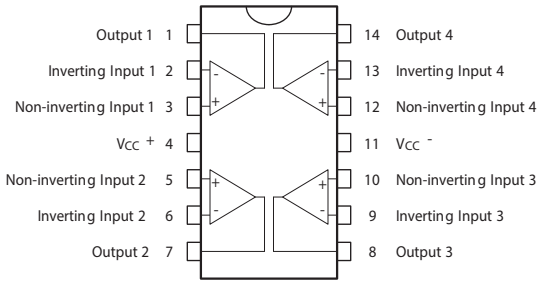
RT2902

RobuST low-power quad operational amplifier

Datasheet - production data

D
SO14
(plastic micropackage)

Pin connections (top view)



Features

- Wide gain bandwidth: 1.3 MHz
- Input common-mode voltage range includes negative rail
- Large voltage gain: 100 dB
- Very low supply current per amplifier: 375 µA
- Low input bias current: 20 nA
- Low input offset current: 2 nA
- Wide power supply range:
  - Single supply: 3 V to 30 V
  - Dual supplies: ±1.5 V to ±15 V
- Intended for use in aerospace and defense applications:
  - Dedicated traceability and part marking
  - Approval documents available for production parts
  - Adapted extended life time and obsolescence management
  - Extended product change notification process
  - Designed and manufactured to meet sub ppm quality goals
  - Advanced mold and frame designs for superior resilience to harsh environments (acceleration, EMI, thermal, humidity)
  - Extended screening capability on request
  - Single fabrication, assembly, and test site
  - Temperature range (-40 °C to 125 °C)

Applications

- Aerospace and defense
- Harsh environments

Description

This circuit consists of four independent, high gain operational amplifiers which employ internal frequency compensation and are specifically designed for aerospace and defense systems.

The device operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low-power supply current drain is independent from the power supply voltage magnitude.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	±16 to 33	V
V_{id}	Differential input voltage(2)	32	
V_{in}	Input voltage	-0.3 to 32	
	Output short-circuit duration(3)	Infinite	s
T_j	Maximum junction temperature	150	°C
I_{in}	Input current(4): V_{in} driven negative	5 in DC or 50 in AC (duty cycle = 10 %, T = 1 s)	mA
	Input current(5): V_{in} driven positive above AMR value	0.4	
T_{stg}	Storage temperature range	-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient(6)	105	°C/W
R_{thjc}	Thermal resistance junction to case(6)	31	
ESD	HBM: human body model(7)	370	V
	MM: machine model(8)	150	
	CDM: charged device model(9)	1500	

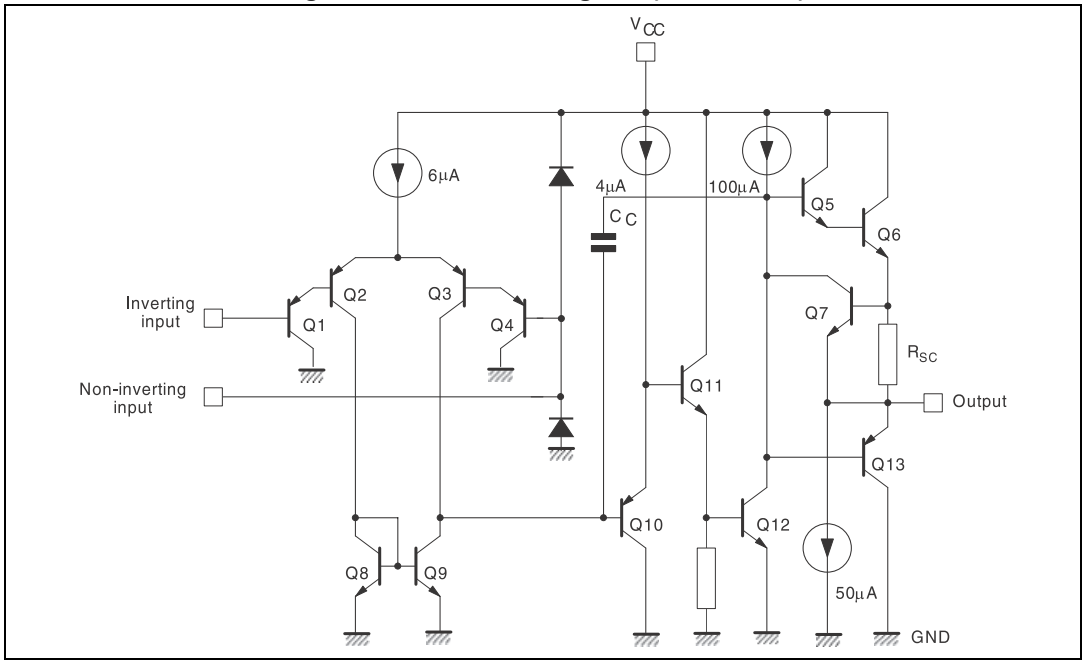
1. All voltage values, except the differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA, independent of the magnitude of V_{CC}^+.
4. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as an input diode clamp. In addition to this diode action, there is an NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amp to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.
5. The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400 µA max (R = (Vin - 36 V)/400 µA).
6. $R_{thja/c}$ are typical values
7. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
8. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
9. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 30	V
V_{icm}	Common mode input voltage range	(V_{CC}^{+}) - 1.5	
	$T_{min} \leq T_{amb} \leq T_{max}$	(V_{CC}^{+}) - 2	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

2 Schematic diagram

Figure 1. Schematic diagram (1/4 RT2902)



3 Electrical characteristics

Table 3. V_{CC}^+ = 5 V, V_{CC}^- = ground, V_o = 1.4 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage(1)		2	7	mV
	Input offset voltage(1), $T_{min} \le T_{amb} \le T_{max}$			9	
$\Delta V_{io}/\Delta T$	Input offset voltage drift		7	30	µV/°C
I_{io}	Input offset current		2	30	nA
	Input offset current, $T_{min} \le T_{amb} \le T_{max}$			40	
DI_{io}	Input offset current drift		10	200	pA/°C
I_{ib}	Input bias current(2)		20	150	nA
	Input bias current(2), $T_{min} \le T_{amb} \le T_{max}$			300	
A_{vd}	Large signal voltage gain (V_{CC}^+ = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V)	50	100		V/mV
	Large signal voltage gain (V_{CC}^+ = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V), $T_{min} \le T_{amb} \le T_{max}$	25			
SVR	Supply voltage rejection ratio (R_S ≤10 kΩ)	65	110		dB
	Supply voltage rejection ratio (R_S ≤10 kΩ), $T_{min} \le T_{amb} \le T_{max}$	65			
I_{cc}	Supply current, all amps, no load V_{CC}^+ = 5 V V_{CC}^+ = 30 V $T_{min} \le T_{amb} \le T_{max}$ V_{CC}^+ = 5 V V_{CC}^+ = 30 V		 0.7 1.5 0.8 1.5	 1.2 3 1.2 3	mA
CMR	Common-mode rejection ratio (R_S ≤ 10 kΩ)	70	80		dB
	Common-mode rejection ratio (R_S ≤ 10 kΩ), $T_{min} \le T_{amb} \le T_{max}$	60			
I_O	Output short-circuit current (V_{id} = 1 V, V_{CC}^+ = 15 V, V_o = 2 V)	20	40	70	mA
I_{sink}	Output sink current (V_{id} = -1 V) V_{CC}^+ = 15 V, V_o = 2 V V_{CC}^+ = 15 V, V_o = 0.2 V	 10 12	 20 50		 mA µA
V_{OH}	High level output voltage (V_{CC}^+ = 30 V) R_L = 2 kΩ $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ $T_{min} \le T_{amb} \le T_{max}$ V_{CC}^+ = 5 V, R_L = 2 kΩ $T_{min} \le T_{amb} \le T_{max}$	 26 26 27 27 3 3.5	 27 28		 V

Table 3. V_{CC}^+ = 5 V, V_{CC}^- = ground, V_o = 1.4 V, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage (R_L = 10 kΩ)		5	20	mV
	Low level output voltage (R_L = 10 kΩ), $T_{min} \le T_{amb} \le T_{max}$			20	
SR	Slew rate (V_{CC}^+ = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain)		0.4		V/µs
GBP	Gain bandwidth product (V_{CC}^+ = 30 V, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)		1.3		MHz
THD	Total harmonic distortion (f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_{CC}^+ = 30 V)		0.015		%
e_n	Equivalent input noise voltage (f = 1 kHz, R_S = 100 Ω, V_{CC}^+ = 30 V)		40		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel separation(3) (1 kHz ≤ f ≤ 20 kHz)		120		dB

1. V_O = 1.4 V, R_S = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 V < V_{ic} < (V_{CC}^+) - 1.5 V.
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so there is no change in the loading charge on the input lines.
3. Due to the proximity of external components ensure stray capacitance does not cause coupling between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Figure 2. Input bias current vs. T_{amb}

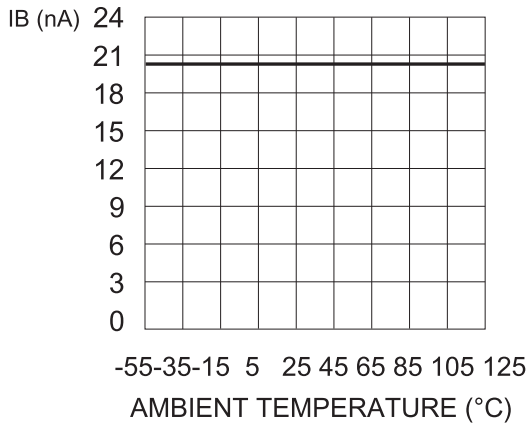


Figure 3. Input voltage range

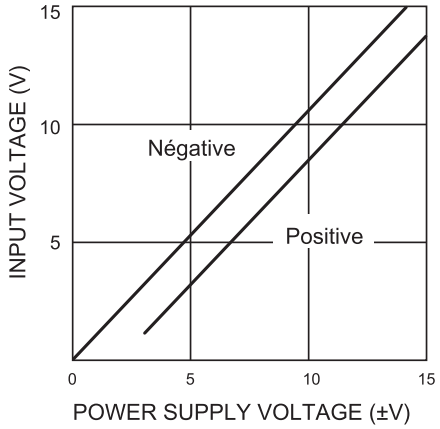


Figure 4. Current limiting

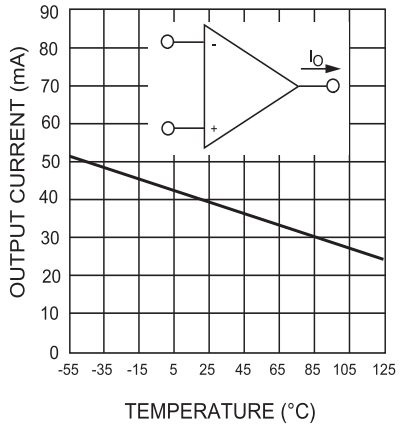


Figure 5. Supply current

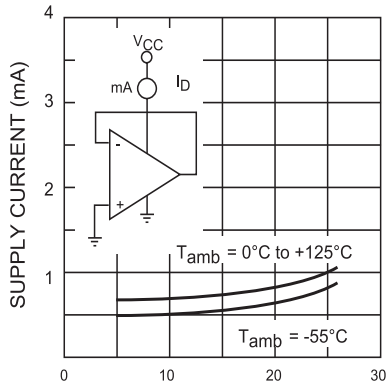


Figure 6. Gain bandwidth product

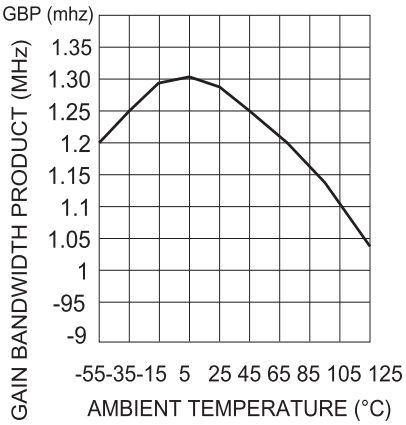


Figure 7. Voltage follower pulse response

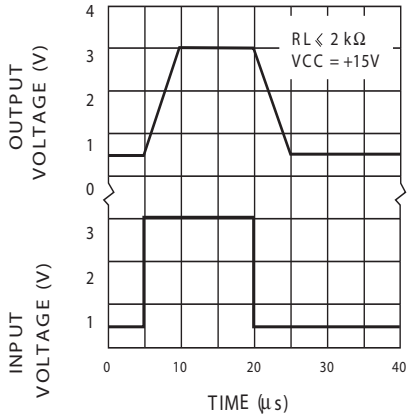


Figure 8. Common mode rejection ratio

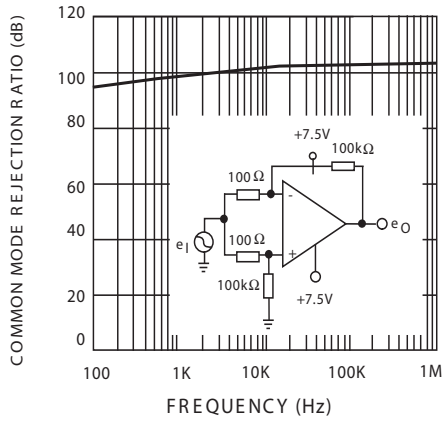


Figure 9. Output characteristics (sink)

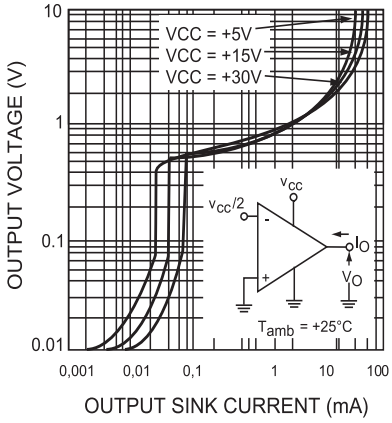


Figure 10. Open-loop frequency response

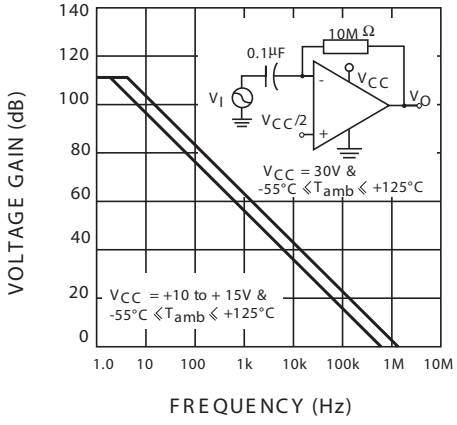


Figure 11. Voltage follower pulse response

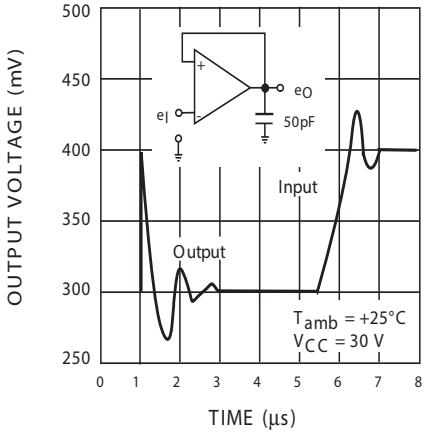


Figure 12. Large signal frequency response

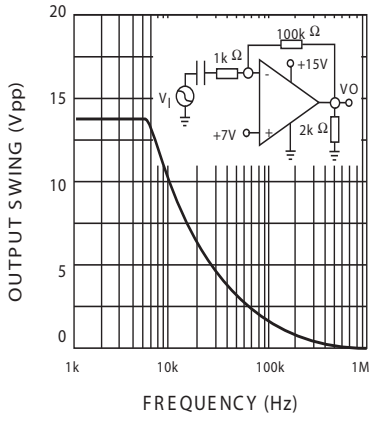


Figure 13. Output characteristics (source)

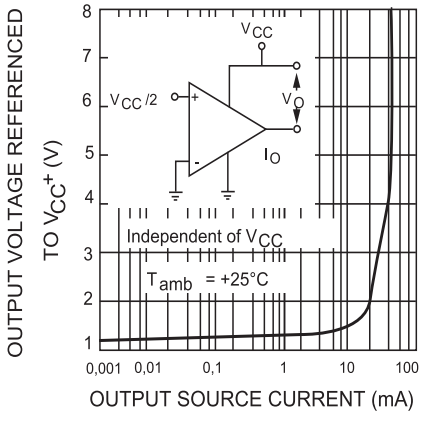


Figure 14. Input current

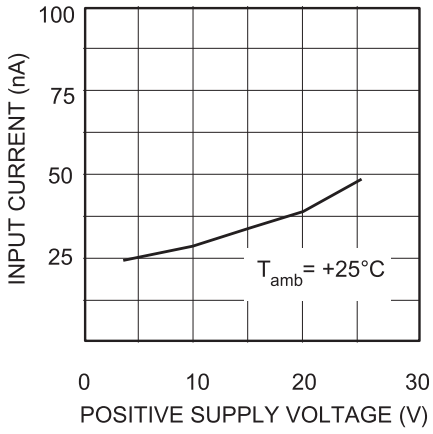


Figure 15. Voltage gain

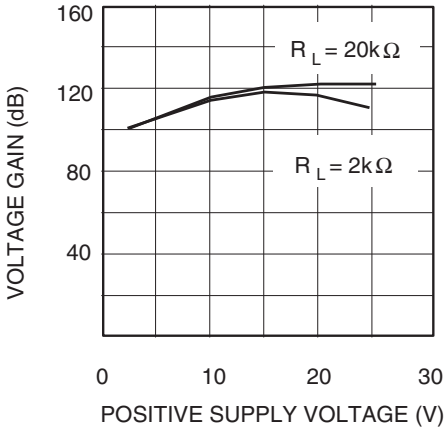


Figure 16. Power supply and common mode rejection ratio

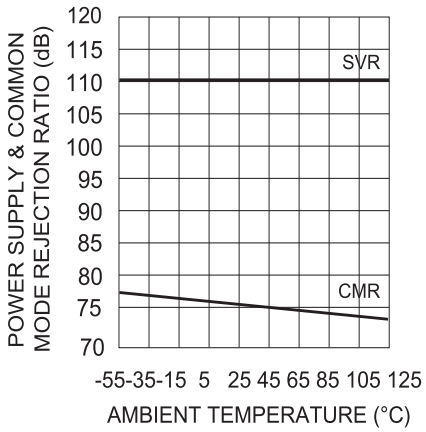
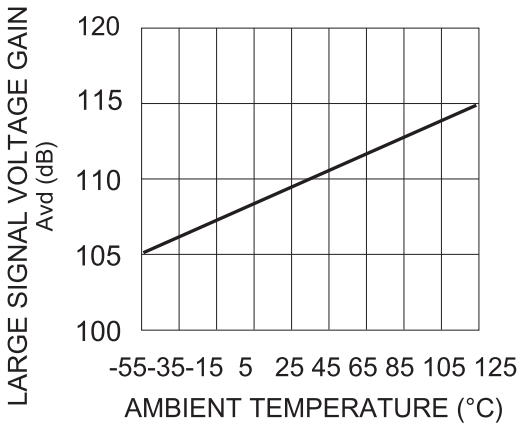


Figure 17. Large signal voltage gain



4 Typical single-supply applications

Figure 18. AC coupled inverting amplifier

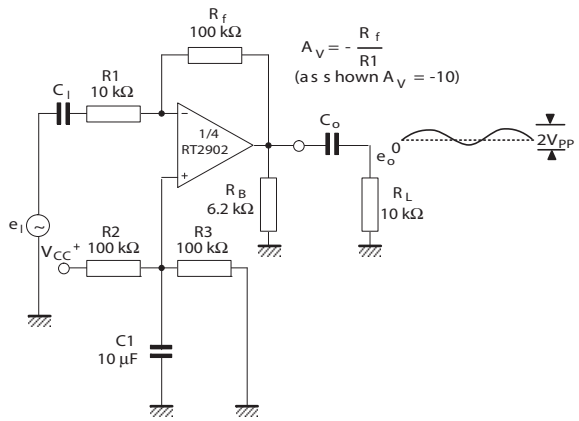


Figure 19. AC coupled non-inverting amplifier

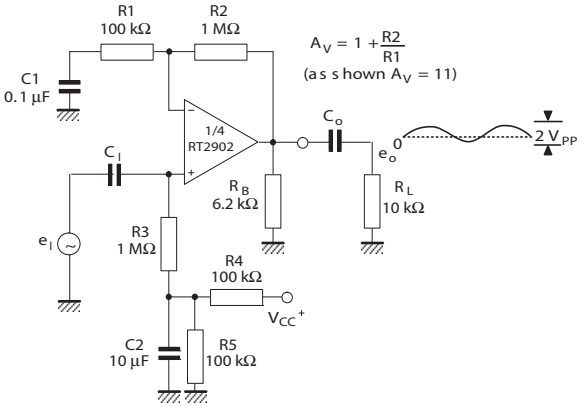


Figure 20. Non-inverting DC gain

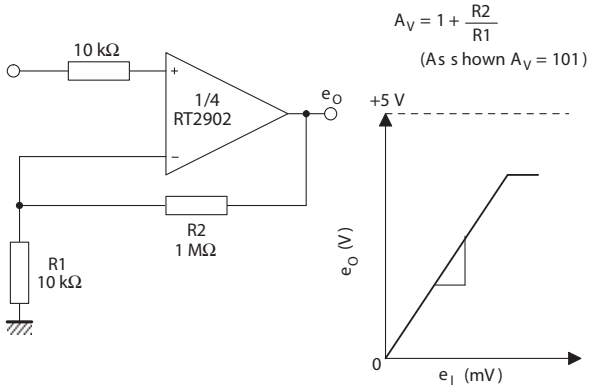


Figure 21. DC summing amplifier

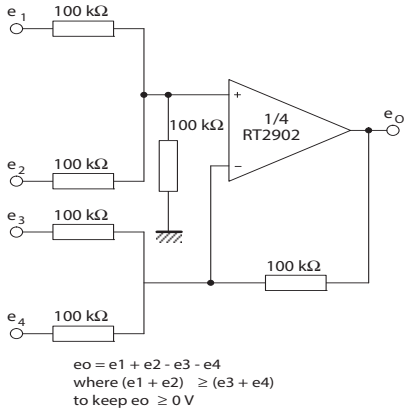


Figure 22. Active bandpass filter

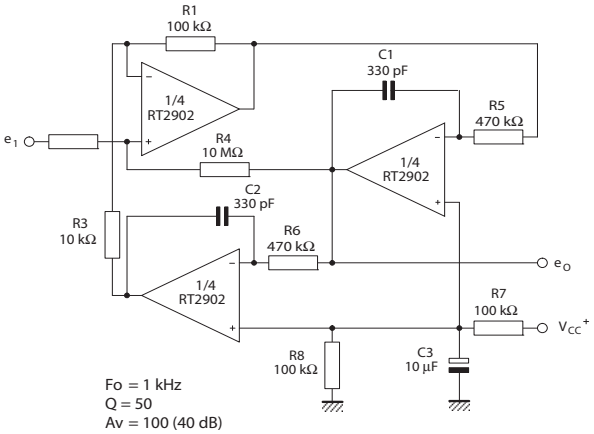


Figure 23. High input Z adjustable gain DC instrumentation amplifier

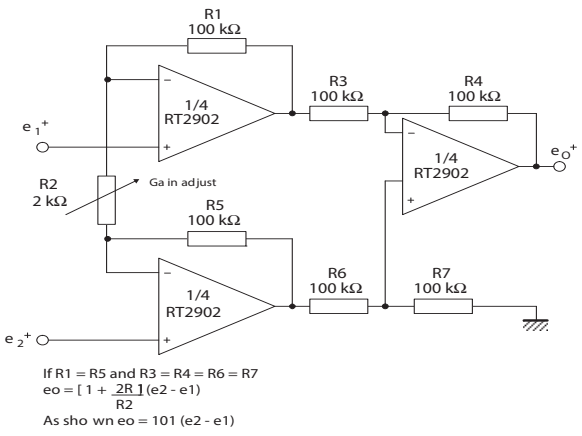


Figure 24. High input Z, DC differential amplifier

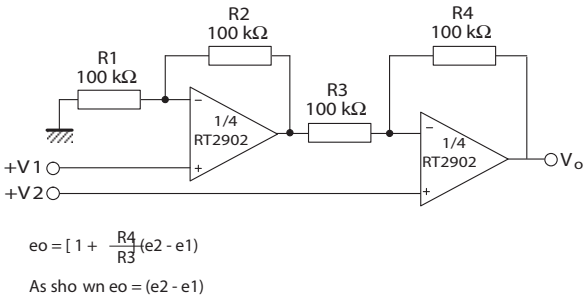


Figure 25. Low drift peak detector

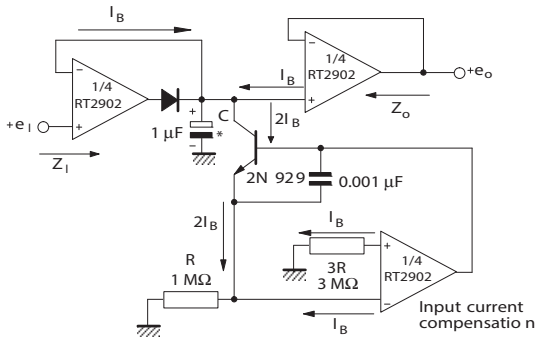
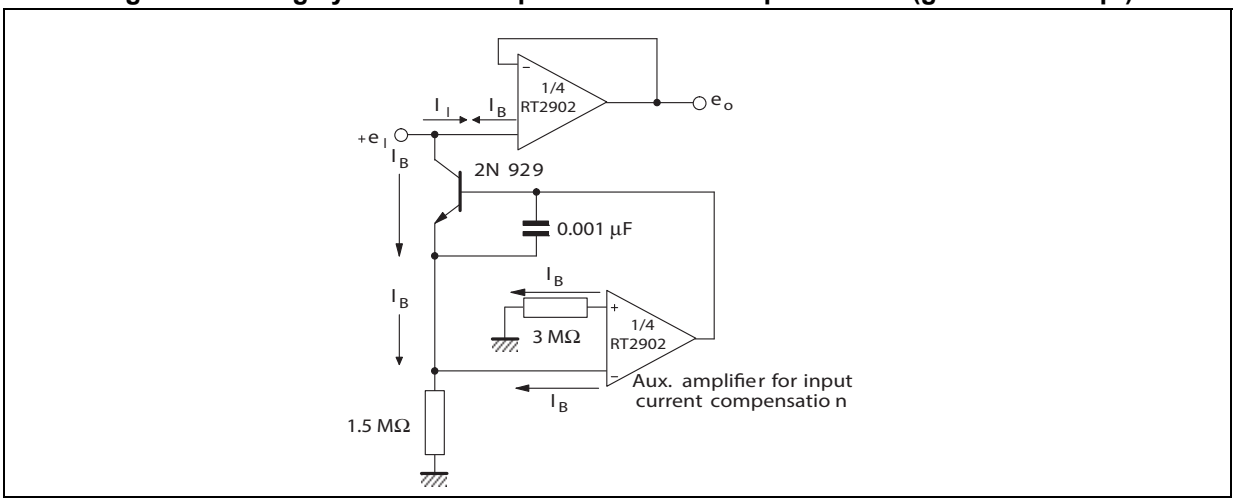


Figure 26. Using symmetrical amplifiers to reduce input current (general concept)



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 SO14 package information

Figure 27. SO14 package mechanical drawing

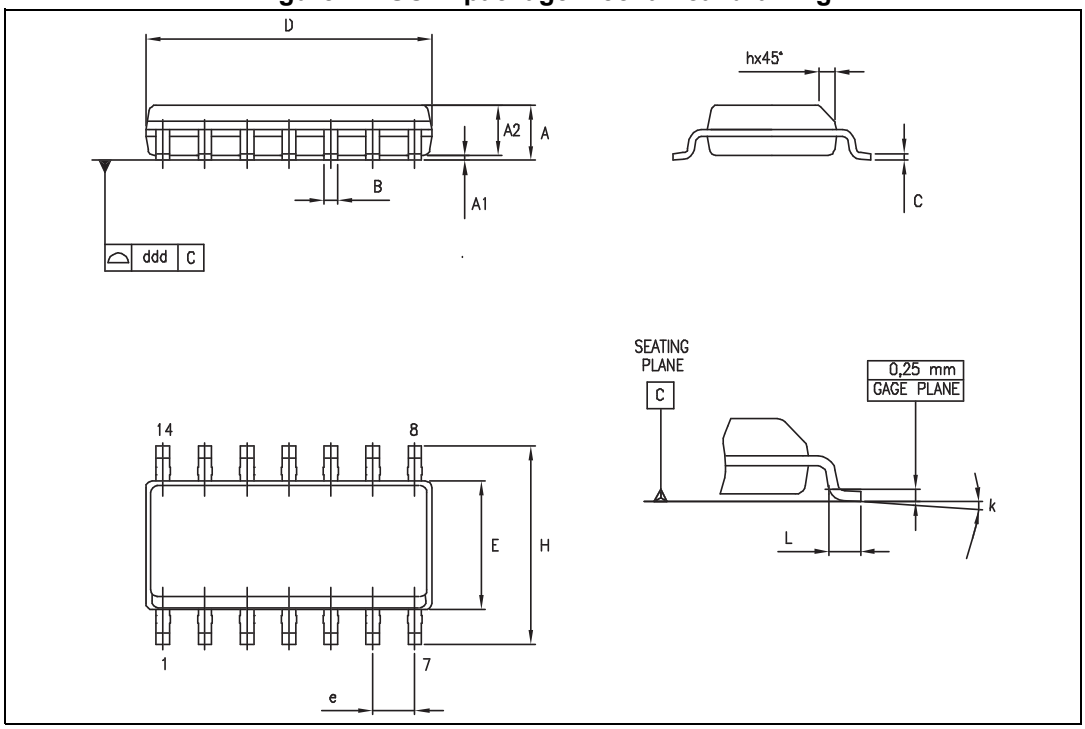


Table 4. SO14 package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

6 Ordering information

Table 5. Order codes

Order code	Temperature range	Package	Packing	Marking
RT2902YDT	-40 °C to 125 °C	SO14	Tape and reel	R2902Y

7 Revision history

Table 6. Document revision history

Date	Revision	Changes
08-Oct-2014	1	Initial release