Triple Channel PWM Controller for IMVP8 Mobile CPU Core Power Supply

General Description

The RT3605BE is an IMVP8 compliant CPU power controller which includes three voltage rails : a 3/2/1 phase synchronous Buck controller, the MAIN VR, a 2/1 phase synchronous Buck controller, the Auxiliary VR, and a single phase synchronous Buck controller, the VCCSA VR. The RT3605BE adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3605BE also features a quick response mechanism for optimized AVP performance during load transient. The RT3605BE supports mode transition function with various operating states. A serial VID (SVID) interface is built in to communicate with Intel IMVP8 compliant CPU. The RT3605BE supports VID on-the-fly function with three different slew rates : Fast, Slow, and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT3605BE varies with VID, load, and input voltage to further enhance the efficiency even in CCM. Moreover, the G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT3605BE integrates a high accuracy ADC for platform setting functions, such as quick response trigger level. The RT3605BE provides VR ready output signals. It also features complete fault protection functions including over-voltage (OV), over-current (OC) and under-voltage lockout (UVLO). The RT3605BE is available in the WQFN-52L 6x6 small foot print package.

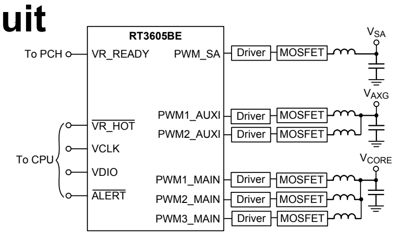
Features

- **Intel IMVP8 Serial VID Interface Compatible Power Management States**
- **3/2/1 Phase (MAIN VR) + 2/1 Phase (Auxiliary VR) + Single Phase (VCCSA VR) PWM Controller**
- **Embedded Audio Noise Suppress Function**
- **Support Multi-Source Dr.MOS and MOSFET**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Accurate Current Balance**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Multiple or Single Phase Operation**
- **Fast Transient Response**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **OVP, OCP, UVLO**
- **Slew Rate Setting**
- **DVID Enhancement**

Applications

- IMVP8 Intel Core Supply
- Notebook/ Desktop Computer/ Servers Multi-Phase CPU Core Supply
- AVP Step-Down Converter

Simplified Application Circuit



Ordering Information

RT3605BE□□

Package Type
QW : WQFN-52L 6x6 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

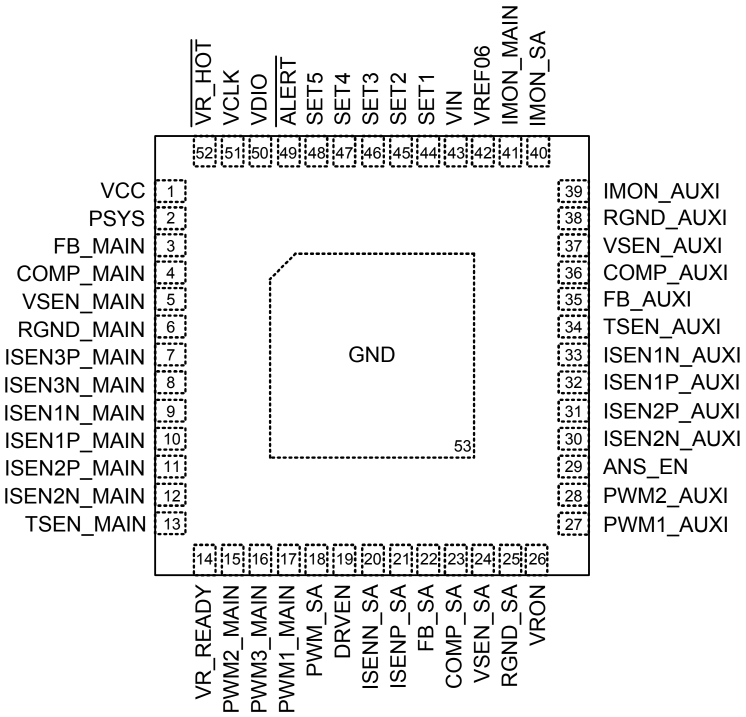
RT3605BE
GQW
YMDNN

RT3605BEGQW : Product Number

YMDNN : Date Code

Pin Configuration

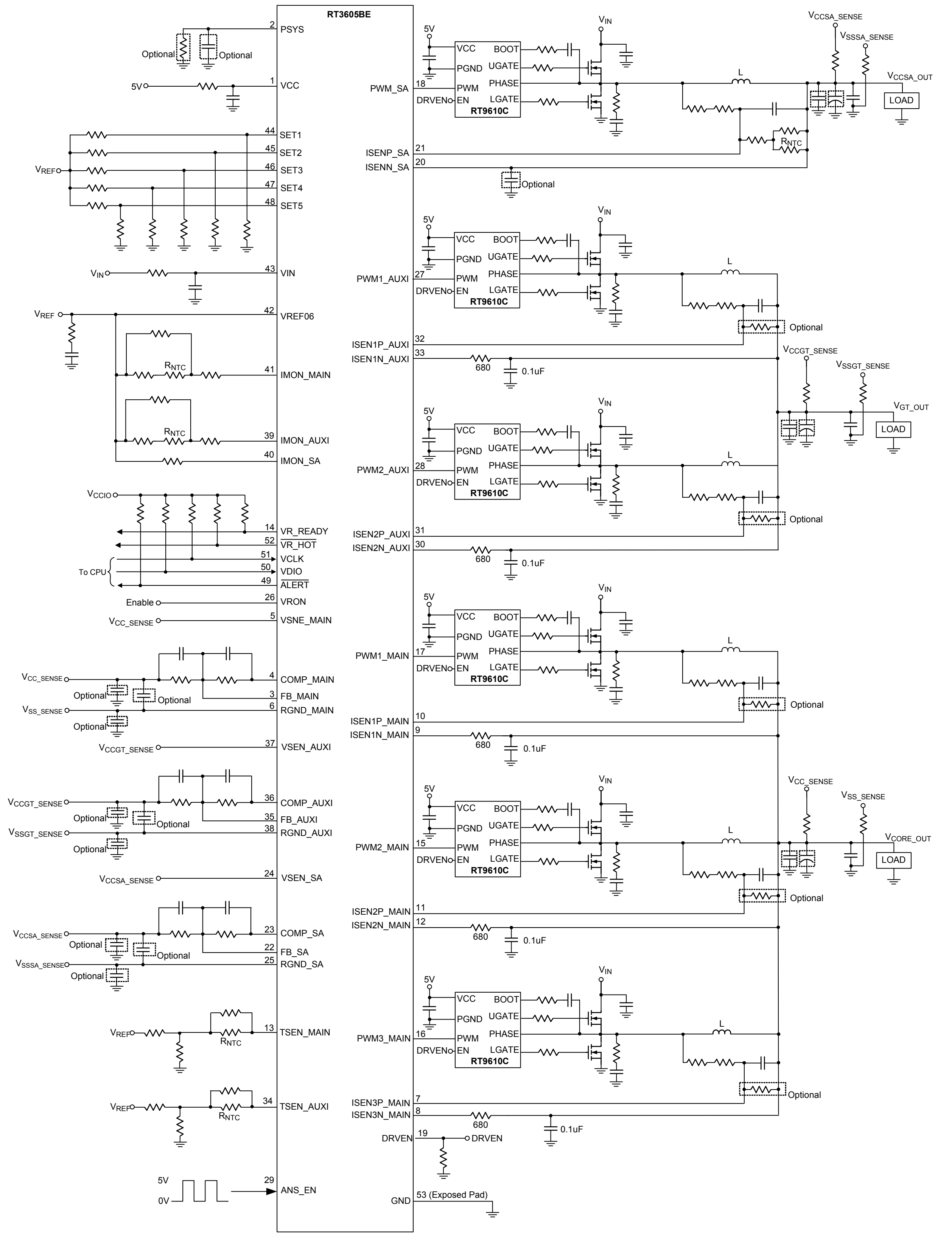
(TOP VIEW)



WQFN-52L 6x6

Typical Application Circuit

For MAIN Two Phase Application

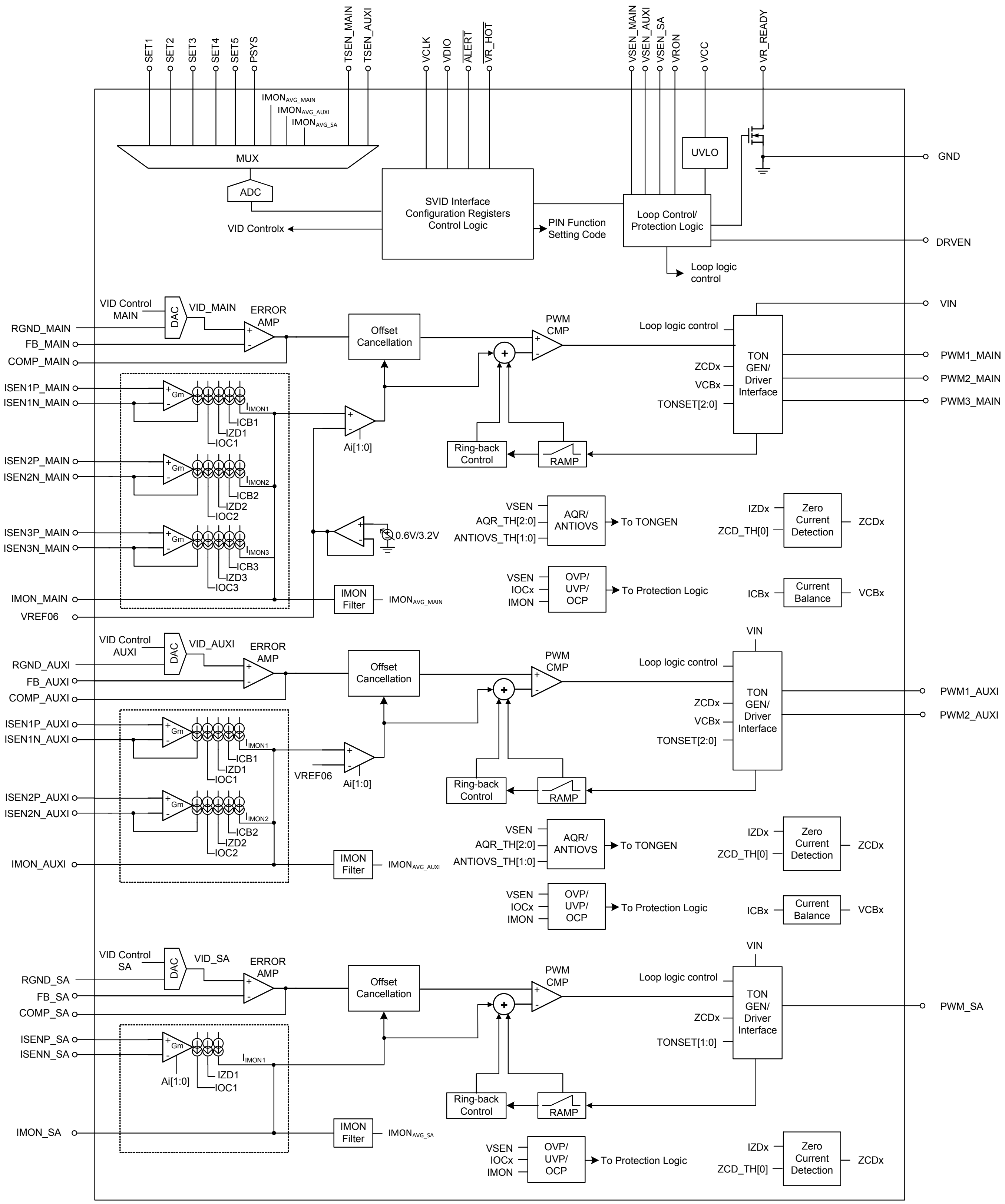


Functional Pin Description

Pin No	Pin Name	Pin Function
1	VCC	Controller power supply. Connect this pin to 5V and place a RC filter, R = 6.2Ω and C = 4.7μF. The decoupling capacitor should be placed as close to the PWM controller as possible.
2	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible.
3	FB_MAIN	Negative input of the error amplifier. This pin is for MAIN rail VR output voltage feedback to controller.
4	COMP_MAIN	MAIN rail VR compensation. This pin is error amplifier output pin.
5	VSEN_MAIN	MAIN rail VR voltage sense input. This pin is connected to the terminal of MAIN rail VR output voltage.
6	RGND_MAIN	Return ground for MAIN rail VR. This pin is the negative node of the differential remote voltage sensing.
10, 11, 7	ISEN[1:3]P_MAIN	Positive current sense inputs of multi-phase MAIN rail VR channel 1, 2 and 3.
9, 12, 8	ISEN[1:3]N_MAIN	Negative current sense inputs of multi-phase MAIN rail VR channel 1, 2 and 3.
13	TSEN_MAIN	Thermal sense input for MAIN rail VR.
14	VR_READY	VR ready indicator.
17, 15, 16	PWM [1:3]_MAIN	PWM outputs for MAIN rail VR of channel 1, 2 and 3.
18	PWM_SA	PWM outputs for SA rail VR.
19	DRVEN	External driver enable control. Connect to driver enable pin.
20	ISENN_SA	Negative current sense input of single-phase SA rail VR.
21	ISENP_SA	Positive current sense input of single-phase SA rail VR.
22	FB_SA	Negative input of the error amplifier. This pin is for SA rail VR output voltage feedback to controller.
23	COMP_SA	SA rail VR compensation. This pin is error amplifier output pin.
24	VSEN_SA	SA rail VR voltage sense input. This pin is connected to the terminal of SA rail VR output voltage.
25	RGND_SA	Return ground for SA rail VR. This pin is the negative node of the differential remote voltage sensing.
26	VRON	VR enable control input.
27, 28	PWM[1:2]_AUXI	PWM outputs for AUXI rail VR.
29	ANS_EN	Acoustic noise suppression function setting. When pulling the pin to VCC, this function is enabled. This pin is not allowed to be floating.
33, 30	ISEN[1:2]N_AUXI	Negative current sense inputs of multi-phase AUXI rail VR channel 1 and 2.
32, 31	ISEN[1:2]P_AUXI	Positive current sense inputs of multi-phase AUXI rail VR channel 1 and 2.
34	TSEN_AUXI	Thermal sense input for AUXI rail VR.
35	FB_AUXI	Negative input of the error amplifier. This pin is for AUXI rail VR output voltage feedback to controller.

Pin No	Pin Name	Pin Function
36	COMP_AUXI	AUXI rail VR compensation. This pin is error amplifier output pin.
37	VSEN_AUXI	AUXI rail VR voltage sense input. This pin is connected to the terminal of AUXI rail VR output voltage.
38	RGND_AUXI	Return ground for AUXI rail VR. This pin is the negative node of the differential remote voltage sensing.
39	IMON_AUXI	AUXI rail VR current monitor output. This pin outputs a voltage which is proportional to the output current.
40	IMON_SA	SA rail VR current monitor output. This pin outputs a voltage which is proportional to the output current.
41	IMON_MAIN	MAIN rail VR current monitor output. This pin outputs a voltage proportional to the output current.
42	VREF06	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of IMON pin. A exact 0.47μF decoupling capacitor and a 3.9Ω resistor must be placed between this pin and GND.
43	VIN	VIN input pin. Connect a low pass filter to this pin to set on-time.
44	SET1	Platform setting. Connect the SET1 pin to 5V and turn-on the EN pin, if the soldering is good, VSEN_MAIN = VSEN_AUXI = 0.9V and VSEN_SA = 1.05V.
45	SET2	Platform setting.
46	SET3	Platform setting.
47	SET4	Platform setting.
48	SET5	Platform setting.
49	$\overline{\text{ALERT}}$	SVID alert. (Active low)
50	VDIO	VR and CPU data transmission interface.
51	VCLK	Synchronous clock from the CPU.
52	$\overline{\text{VR\_HOT}}$	Thermal monitor output. (Active low)
53 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

G-NAVP™ Control Mode

The RT3605BE adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy loadline design and provide high DC accuracy and fast transient response. When sensed current signal reaches sensed voltage signal, the RT3605BE generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage that is inverted and amplified signal of output voltage. While current loading is increasing, referring to Figure 1, COMP rises due to output voltage droop. Then rising COMP forces PWM turn on earlier and closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage and the corresponding output voltage is in the steady state of lower voltage. The loadline, output voltage drooping by an amount which is proportional to loading current, is achieved.

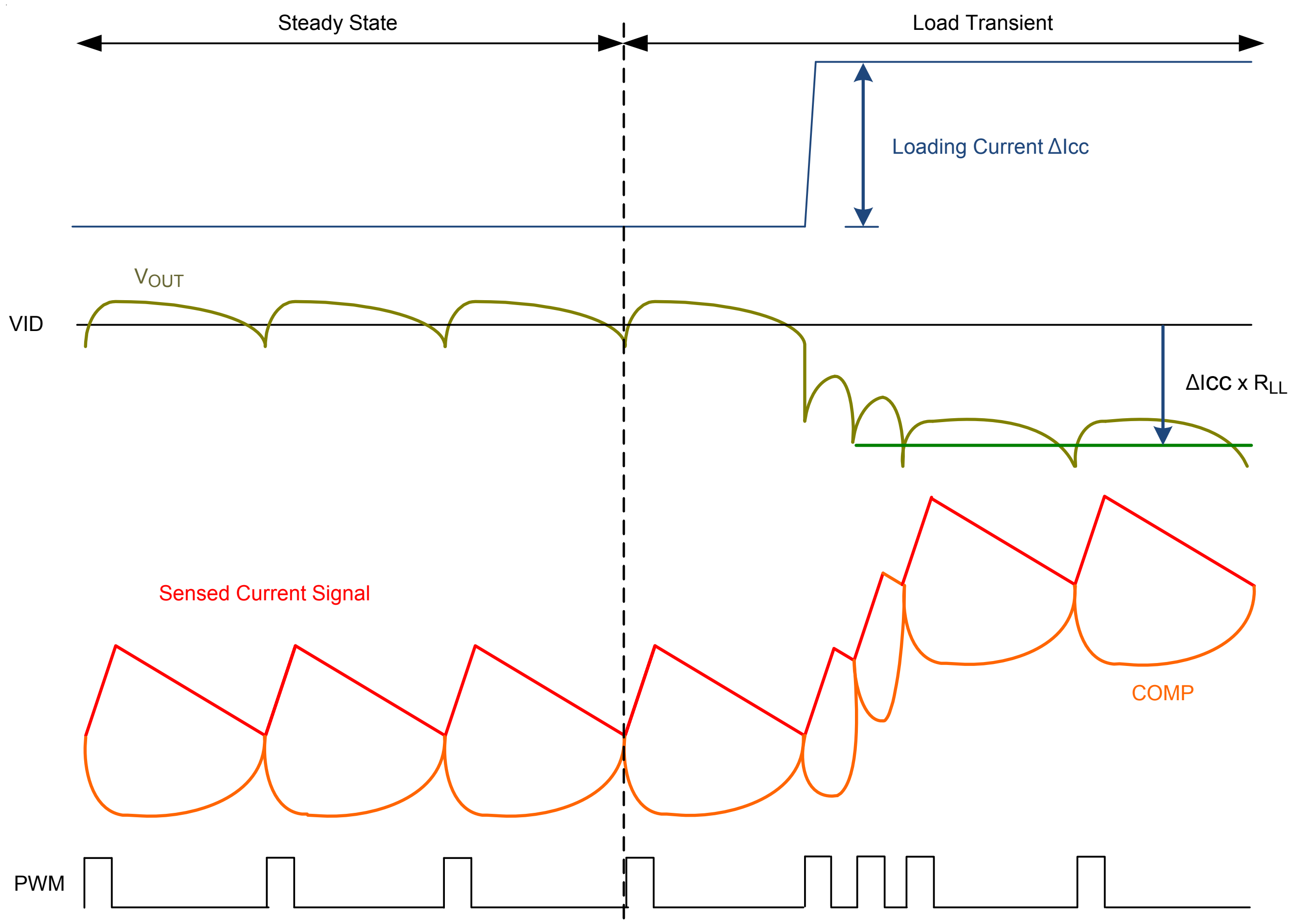


Figure 1. G-NAVP™ Behavior Waveform

SVID Interface/Control Logic/Configuration Registers

SVID Interface receives or transmits SVID signal with CPU. Control Logic executes command (Read/Write registers, setVID, setPS) and sends related signals to control VR. Configuration Registers include function setting registers and CPU required registers.

IMON Filter

IMON Filter is used to average current signal by analog low-pass filter. It outputs $IMON_{AVG}$ to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs of SET1, SET2, SET3, SET4, SET5, TSEN_MAIN, TSEN_AUXI, PSYS, $IMON_{AVG\_MAIN}$, $IMON_{AVG\_AUXI}$, and $IMON_{AVG\_SA}$. The ADC converts these analog signals to digital codes for reporting or function settings.

UVLO

The UVLO detects the VCC voltage. As VCC exceeds threshold, controller issues POR = high and waits VRON. After both POR and VRON are ready, then controller is enabled.

Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition, and PWM sequence.

DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to setVID command, Control Logic dynamically changes VID voltage to target with required slew rate.

ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally setting finite DC gain. The output signal is COMP for PWM trigger.

PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, Current Balance, Zero Current Detection, current reporting and over-current protection.

SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be set by PIN-SETTING(Ai[1:0]). It helps wider application range of DCR and load line. SUM CSGM output is used for PWM trigger.

RAMP

The RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal and sum current signal based on RAMP to trigger PWM.

Offset Cancellation

The offset cancellation is based on VID, COMP voltage and current signal from SUM CSGM to control output voltage accuracy.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result will adjust each phase PWM width to optimize current and thermal balance.

Zero Current Detection

Detect whether each phase current cross zero current. The result is used for DEM power saving and overshoot reduction (Anti-overshoot Function).

AQR/ANTIOVS

The AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWM to turn on. The PWM pulse width triggered by AQR is adaptive to loading level. The AQR trigger level can be set by PIN-SETTING. ANTIOVS can help overshoot reduction which detects loading falling edge and forces all PWM in tri-state until the zero current is detected.

TONGEN/Driver Interface

The PWM comparator output signal will trigger TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by frequency setting, current balance output and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR will allow all PWM to turn on at the same time. Driver Interface provides high/low/tri-state to drive external driver. In power saving mode, Driver Interface forces PWM in tri-state to turn off high-side and low-side power MOSFET according to Zero Current Detection output. In addition, PWM state is controlled by Protection Logic. Different protections force required PWM state.

OCP

The RT3605BE has three over-current protection mechanisms, sum OCP, per phase OCP. and OC limit.

OVP

The over-temperature protection threshold is linked to VID, please refer to classification table and waveform in Table 27 and Figure 27.

UVP

When the output voltage is lower than VID-450mV with 3μs filter time. UVP will be triggered and all PWM will be in tri-state to turn off high-side powe MOSFETs.

Absolute Maximum Ratings (Note 1)

- VIN to GND -- –0.3V to 28V
- VCC to GND -- –0.3V to 6.5V
- RGND to GND -- –0.3V to 0.3V
- Other Pins -- –0.3V to 6.8V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-52L 6x6 -- 3.77W
- Package Thermal Resistance (Note 2)
  WQFN-52L 6x6, θ_{JA} -- 26.5°C/W
  WQFN-52L 6x6, θ_{JC} -- 6.5°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range -- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) -- 2kV

Recommended Operating Conditions (Note 4)

- VIN to GND -- 4.5V to 24V
- Supply Input Voltage, VCC -- 4.5V to 5.5V
- Junction Temperature Range -- –10°C to 105°C

Electrical Characteristics

(V_{CC} = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from –10°C to 105°C, unless other noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input							
Supply Voltage		V_{CC}		4.5	5	5.5	V
Supply Current		I_{VCC}	VRON= H, not switching	--	15	--	mA
Supply Current at PS4		I_{VCC_PS4}	VRON= H, not switching	--	85	--	μA
Shutdown Current		I_{SHDN}	VRON= L	--	--	10	μA
Reference and DAC							
DAC Accuracy		V_{FB}	VID = 0.75V to 1.52V	–0.5	0	0.5	% of VID
			VID = 0.5V to 0.745V	–8	0	8	mV
			VID = 0.25V to 0.495V	–10	0	10	
Slew Rate							
Dynamic VID Slew Rate	Fast Slew Rate	SR	SetVID fast	33.75	--	--	mV/μs
	Slow Slew Rate		SetVID slow Slew rate default = 1/2 Fast	16.625	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EA Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ	70	--	--	dB
Gain-Bandwidth Product	G_{BW}	C_{LOAD} = 5pF	--	5	--	MHz
Slew Rate	SR_{EA}	C_{LOAD} = 10pF (Gain = –4, Rf = 47kΩ, V_{OUT} = 0.5V to 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.3	--	3.6	V
Maximum Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Input Offset Voltage	V_{OSEA}	T_A = 25°C	–3	--	3	mV
Current Sensing Amplifier (MAIN/AUXI)						
Input Offset Voltage	V_{OSCS}		–0.6	--	0.6	mV
Impedance at Positive Input	R_{ISENxP}		1	--	--	MΩ
CS Input Voltage	V_{CSIN}	Differential voltage range of DCR sense. (V_{CSIN}= Inductor current x DCR x DCR divider)	–10	--	100	mV
Current Sense Gain Error	A_{MIRROR}	Internal current mirror gain of per phase current sense I_{IMON} / $I_{CS,PERx}$	0.97	1	1.03	A/A
Current Sensing Amplifier (SA)						
Input Offset Voltage	V_{OSCS_SA}		–0.4	--	0.4	mV
Impedance at Positive Input	R_{ISENxP_SA}		1	--	--	MΩ
CS Input Voltage	V_{CSIN_SA}	Differential voltage range of DCR sense. (V_{CSIN} = Inductor current x DCR x DCR divider)	–40	--	40	mV
Current Sense Gain Error	A_{MIRROR_SA}	Internal current mirror gain of per phase current sense I_{IMON} / $I_{CS,PERx}$	0.97	1	1.03	A/A
TON Setting (Main/Auxi)						
On-Time Setting	t_{ON}	VIN = 19V, VID = 0.9V, k_{TON} = 1.36	--	96	--	ns
Minimum Off-Time	t_{OFF}	VID = 1V under PS1 condition	--	130	300	ns
TON Setting (SA)						
On-Time Setting	t_{ON}	VIN = 19V, VID = 0.9V, k_{TON} = 1	--	100	--	ns
Minimum Off-Time	t_{OFF}	VID = 1V under PS1 condition	--	130	300	ns
Protections						
Under-Voltage Lockout Threshold	VUVLO	Falling edge	3.9	4.1	4.3	V
	ΔVUVLO	Rising edge hysteresis	100	200	300	mV
Over-Voltage Protection Threshold	V_{OV}	Respect to VID voltage, VID>1V	VID + 300	VID + 350	VID + 400	mV
		VID=1V	1.3	1.35	1.4	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Under-Voltage Protection Threshold		V_{UV}	Respect to VID voltage	–510	–450	–390	mV
VRON and VR_READY							
VRON Threshold	Logic-High	V_{IH}		0.7	--	--	V
	Logic-Low	V_{IL}		--	--	0.3	
Leakage Current of VRON				–1	--	1	μA
VR_READY Pull Low Voltage		V_{VR_READY}	I_{VR_READY} = 10mA	--	--	0.13	V
Serial VID and VR_HOT							
VCLK, VDIO Input Voltage	Logic-High	V_{IH}	Respect to INTEL Spec. with 50mV hysteresis	0.65	--	--	V
	Logic-Low	V_{IL}		--	--	0.45	
Leakage Current of VCLK and VDIO		I_{LEAK_IN}		–1	--	1	μA
Pull Low Voltage		V_{VDIO}	I_{VDIO} = 10mA	--	--	0.13	V
		V_{ALERT}	I_{ALERT} =10mA				
		V_{VR_HOT}	I_{VR_HOT} = 10mA				
Leakage Current of ALERT , VR_HOT		I_{LEAK_OUT}		–1	--	1	μA
ANS_EN							
ANS_EN Input Voltage	Logic-High	V_{IH}		VCC –0.7	--	--	V
	Logic-Low	V_{IL}		--	--	1	V
VREF							
VREF06 Voltage		V_{VREF06}	Normal operation	0.59	0.6	0.61	V
ADC							
Digital IMON Set		$dVIMON_{ICC\ MAX}$	V_{IMON}-V_{REF06}=0.8V @ IMAX>=40A V_{IMON}-V_{REF06}=0.4V @ IMAX<40A	--	255	--	Decimal
PSYS Maximum Input Voltage		PSYS	V_{PSYS} = 1.6V	--	255	--	Decimal
Average Period of IMON		t_{IMON}		--	200	--	μs
Average Period of TSEN		t_{TSEN}		--	800	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VR_Hot Assert Threshold	V_{TSEN}	Falling	--	1.092	1.105	V
VR_Hot De-Assert Threshold		Rising	1.119	1.132	1.147	V
Thermal $\overline{ALERT}$ Assert Threshold		Falling, thermal alert status1 register bit 1 assert	1.119	1.132	1.147	V
Thermal $\overline{ALERT}$ Assert Threshold		Falling, thermal alert status1 register bit 1 de-assert	1.161	1.176	1.196	V
ITSEN						
TSEN Source Current	I_{TSEN}	V_{TSEN} = 1.6V, T_A = 25°C	79.2	80	80.8	μA

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

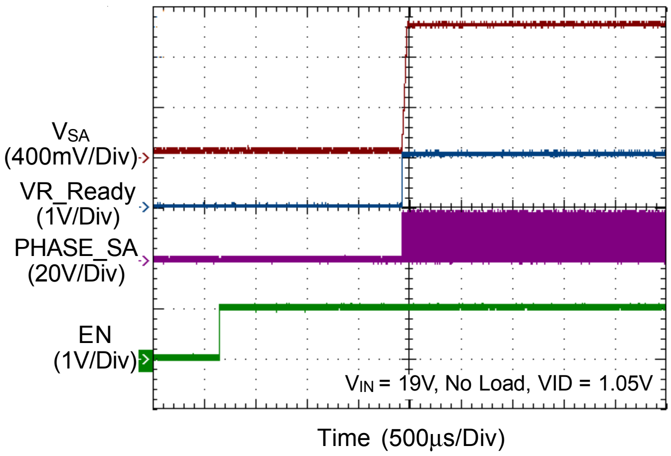
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

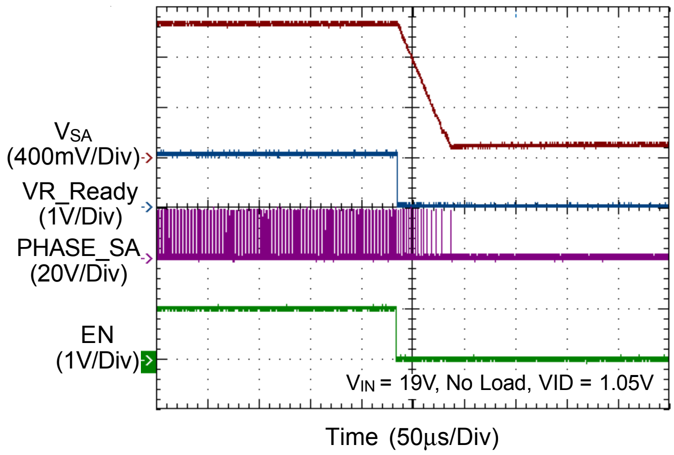
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

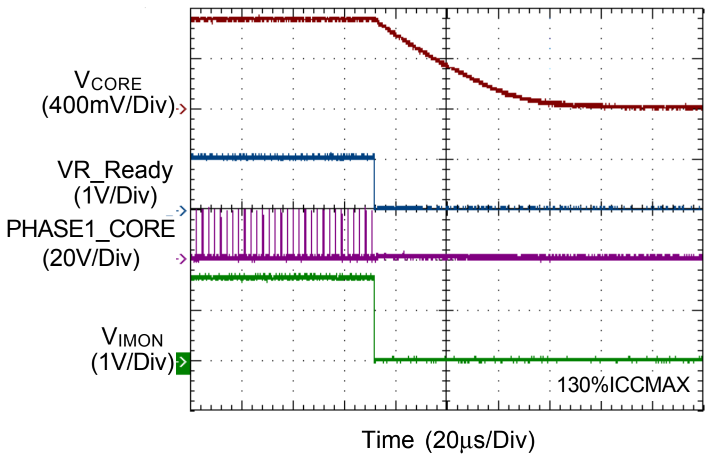
VR Power On from EN



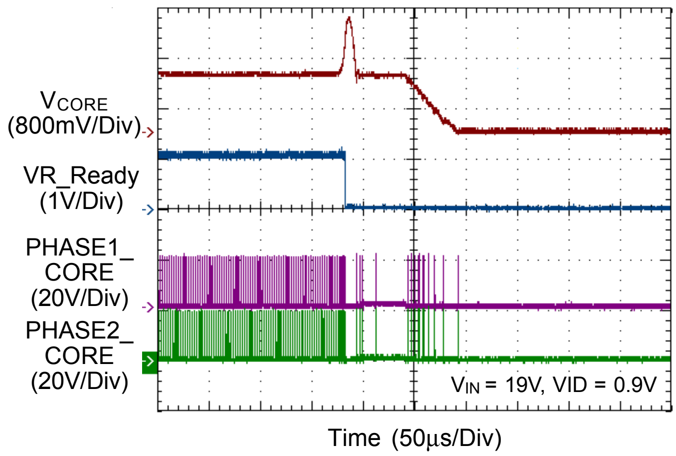
VR Power Off from EN



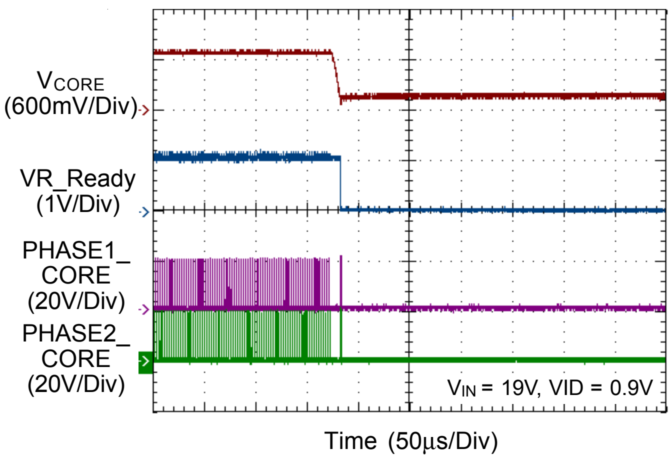
CORE VR OCP



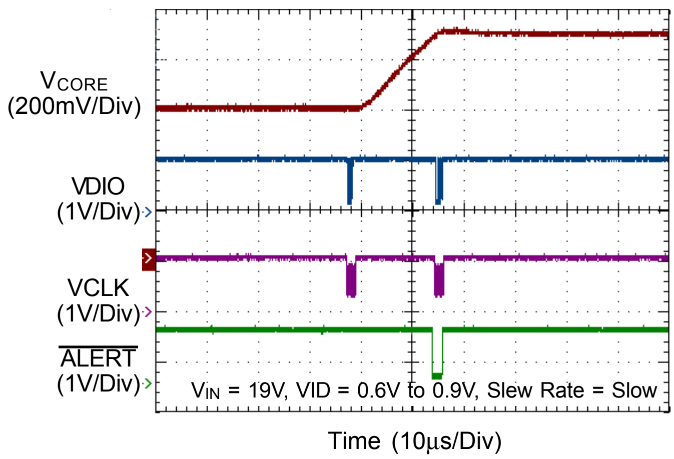
CORE VR OVP



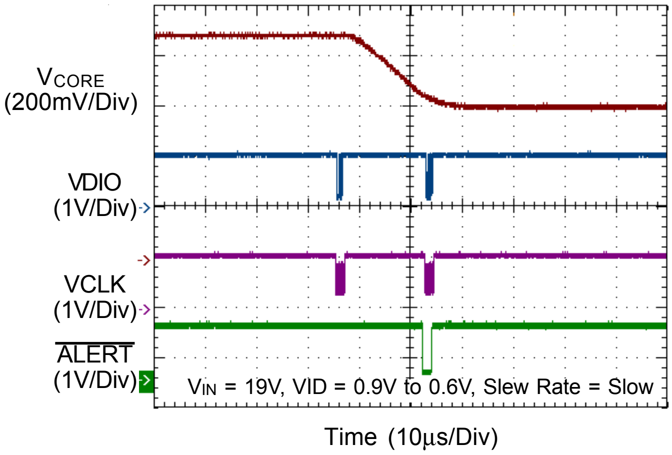
CORE VR UVP



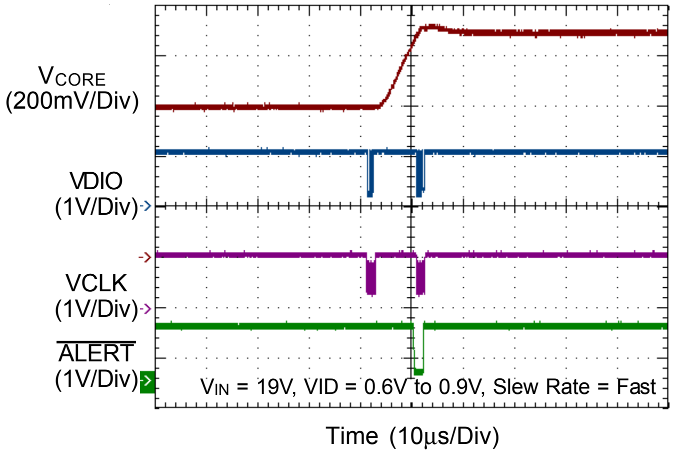
CORE VR Dynamic VID Up



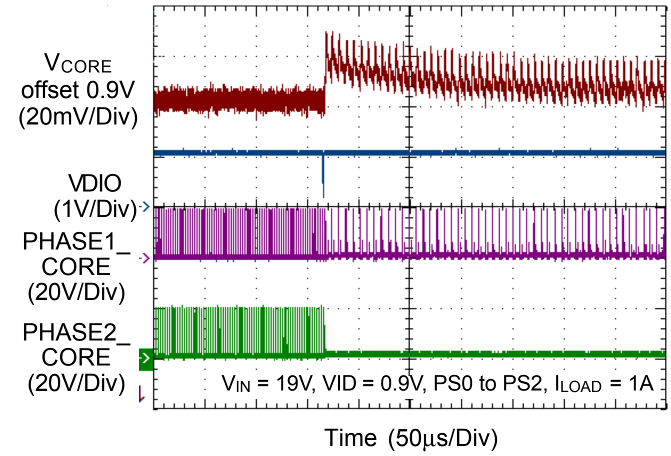
CORE VR Dynamic VID Down



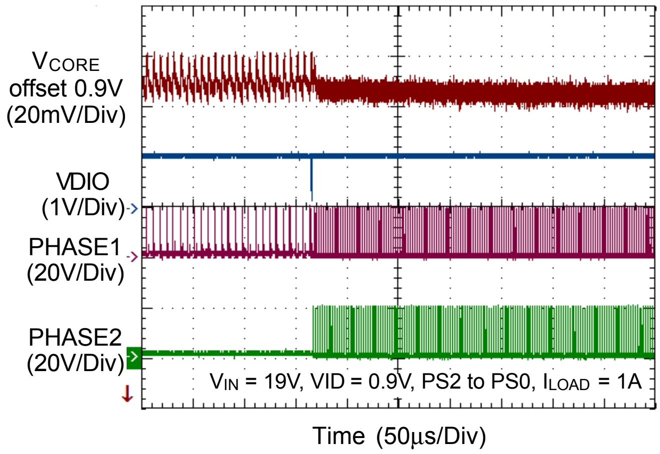
CORE VR Dynamic VID Up



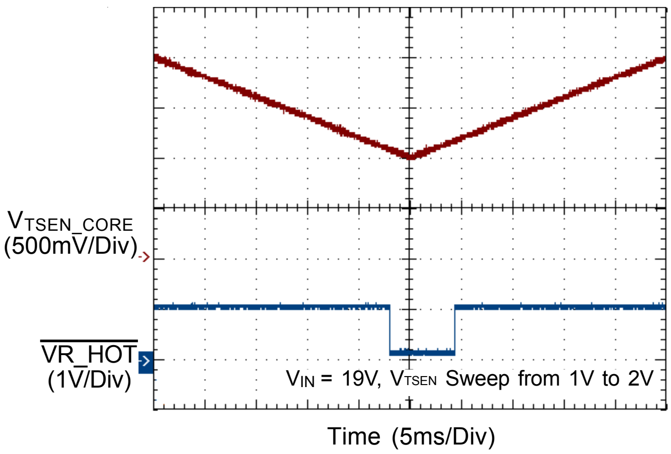
CORE VR Mode Transient



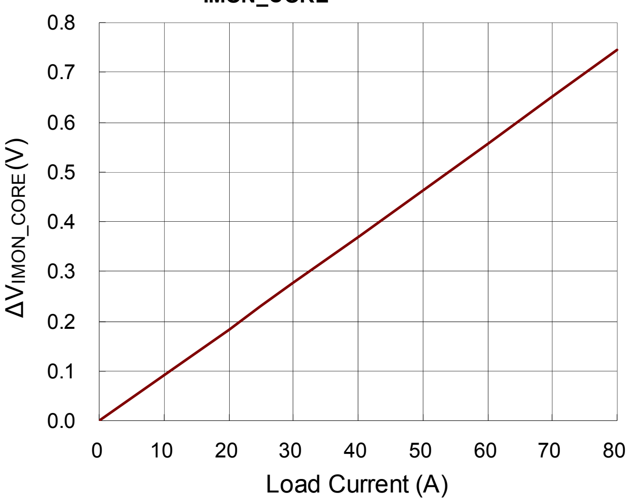
CORE VR Mode Transient



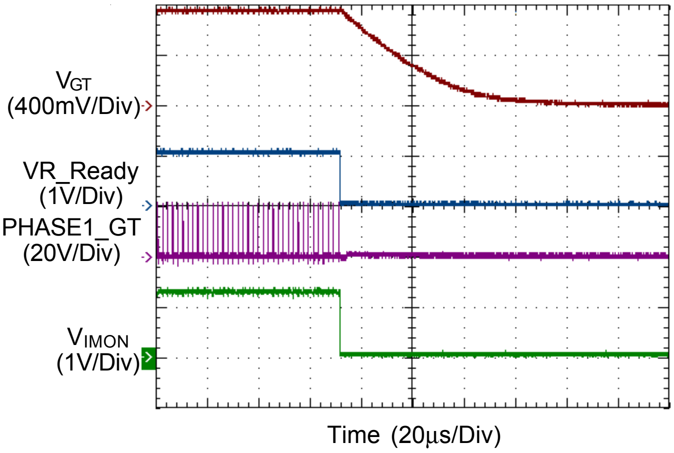
CORE VR Thermal Monitioring



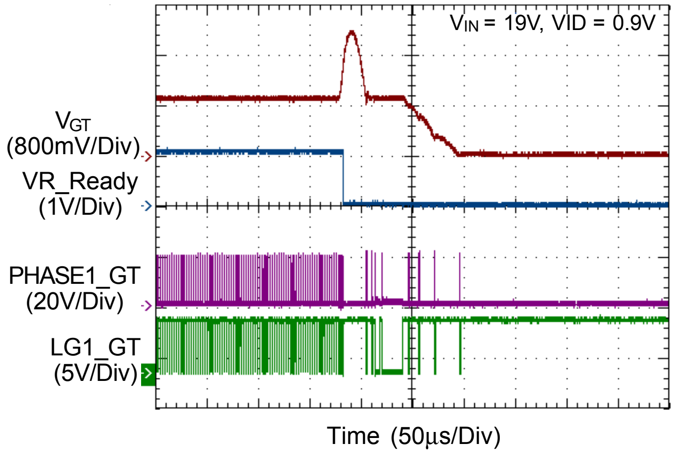
ΔV_{IMON_CORE} vs. Load Current



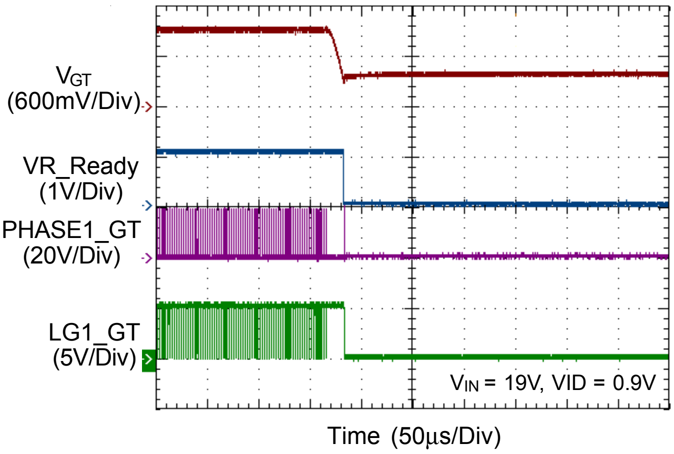
GT VR OCP



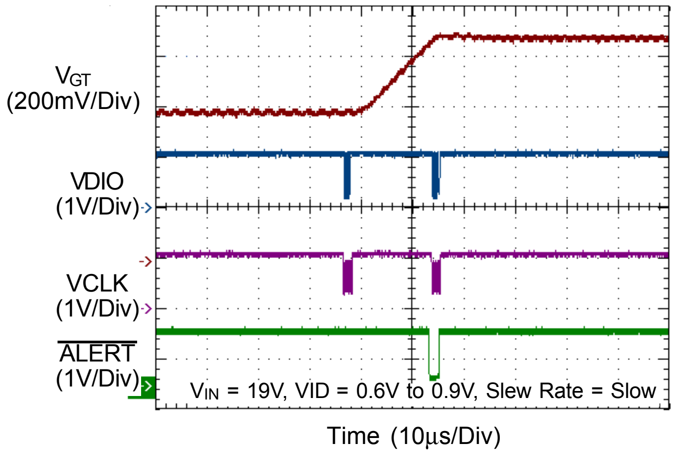
GT VR OVP



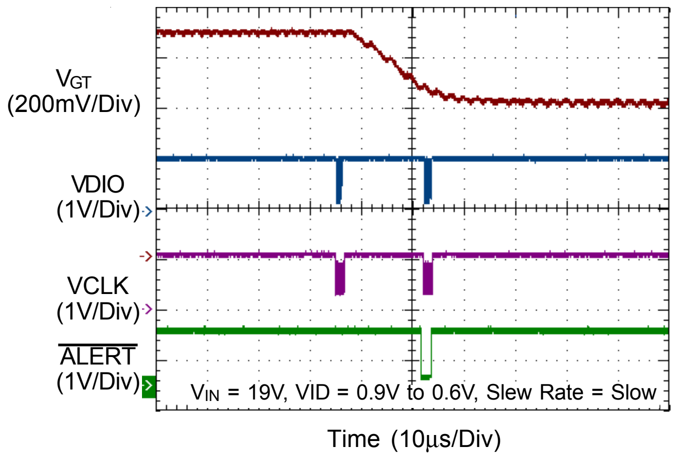
GT VR UVP



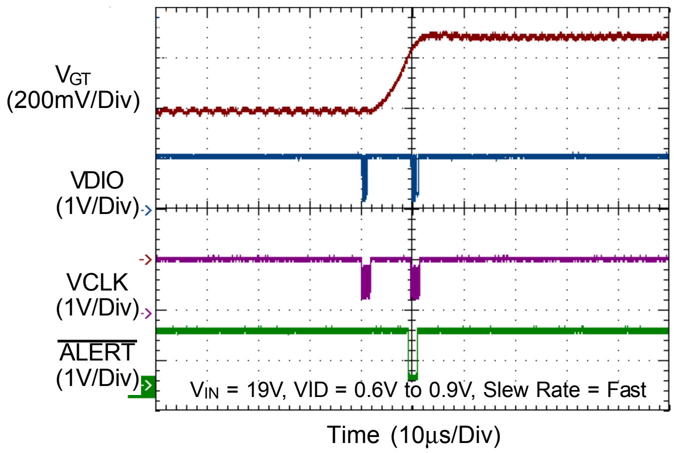
GT VR Dynamic VID Up



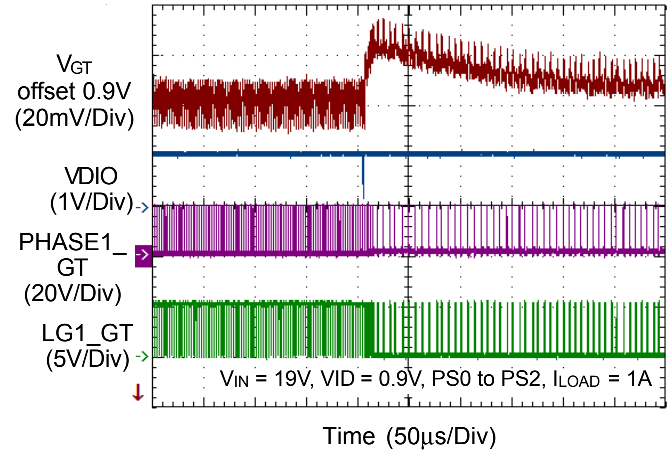
GT VR Dynamic VID Down



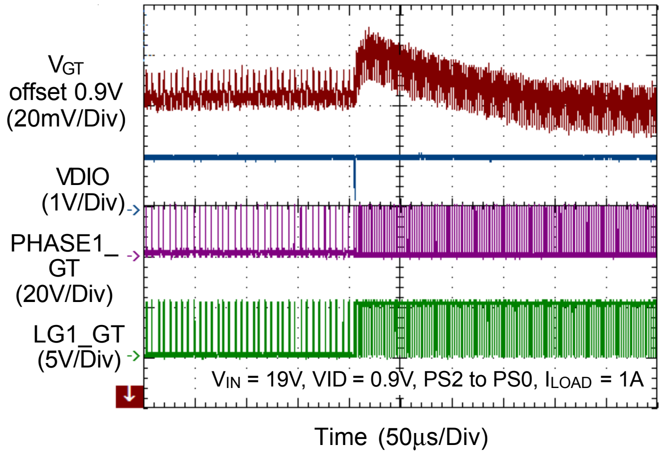
GT VR Dynamic VID Up



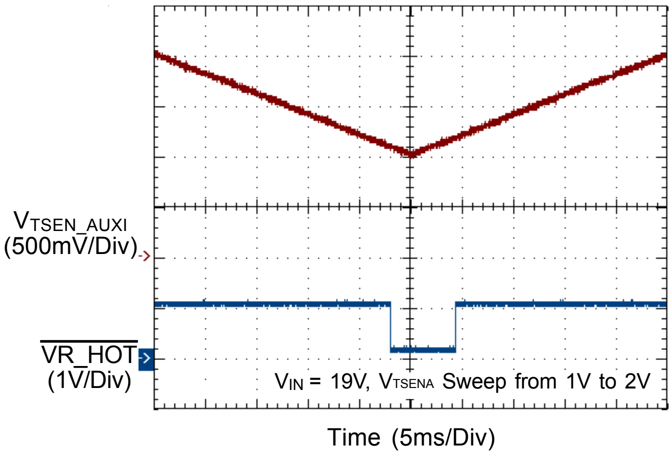
GT VR Mode Transient



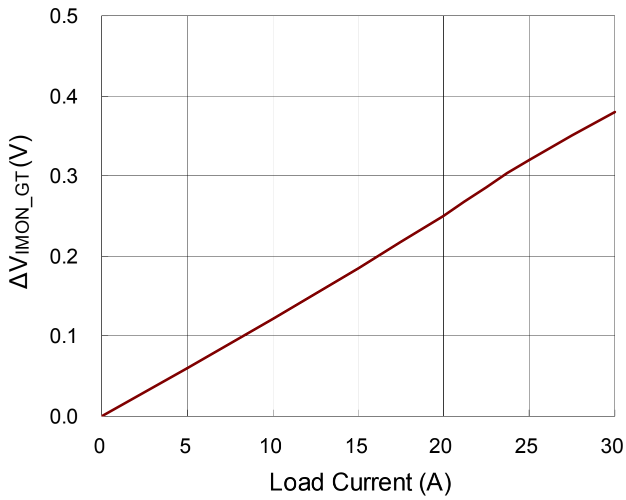
GT VR Mode Transient



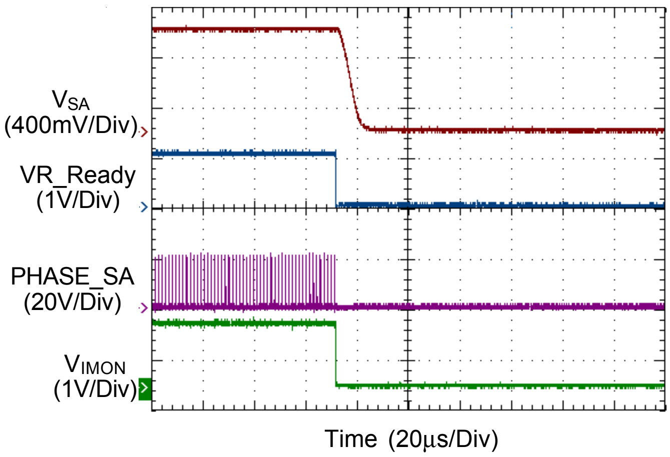
GT VR Thermal Monitoring



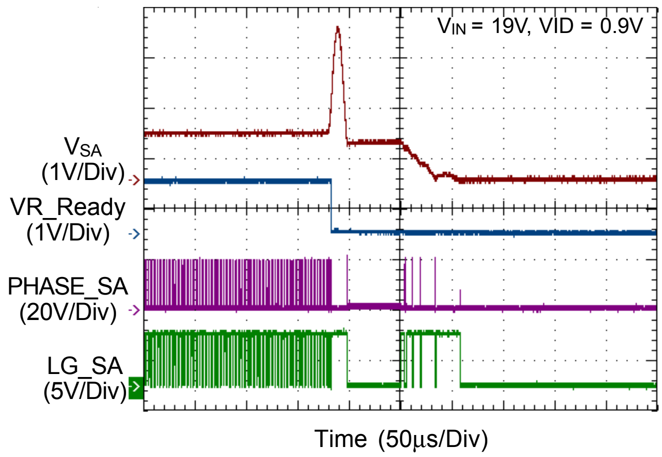
ΔV_{IMON_GT} vs. Load Current



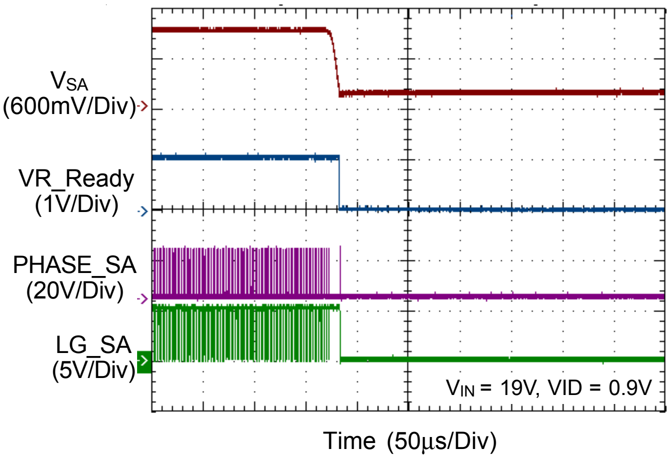
SA VR OCP



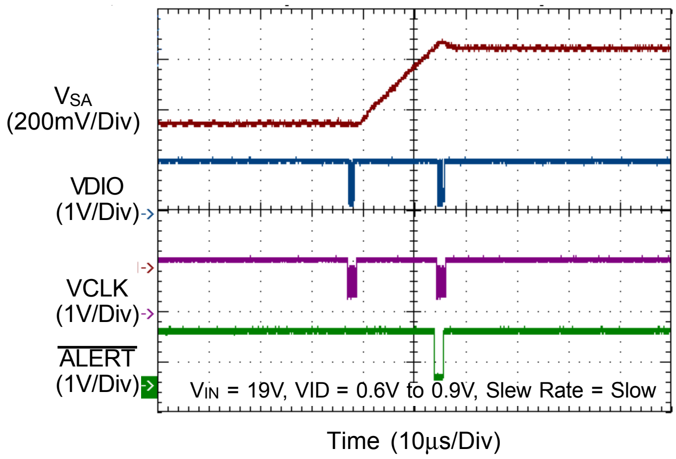
SA VR OVP



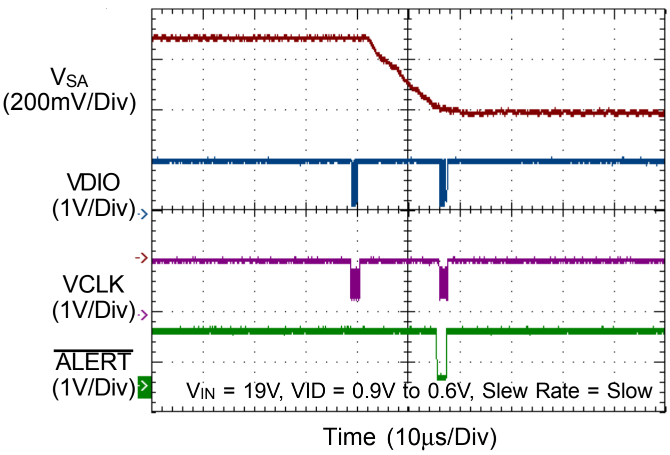
SA VR UVP



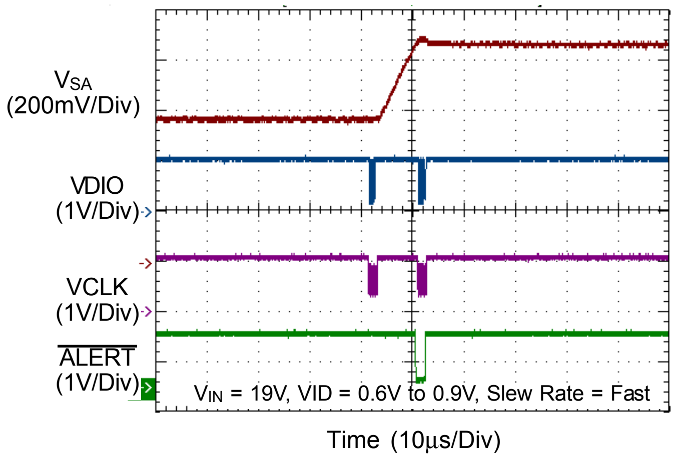
SA VR Dynamic VID Up



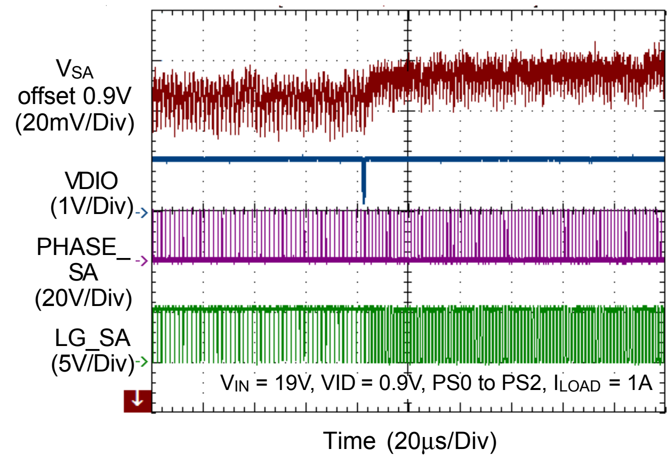
SA VR Dynamic VID Down



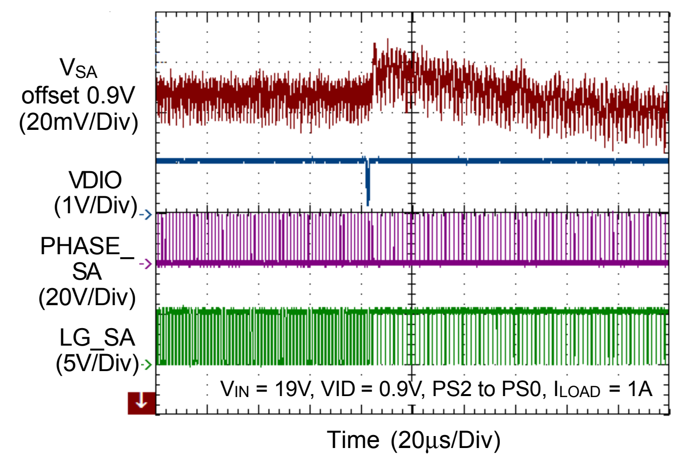
SA VR Dynamic VID Up

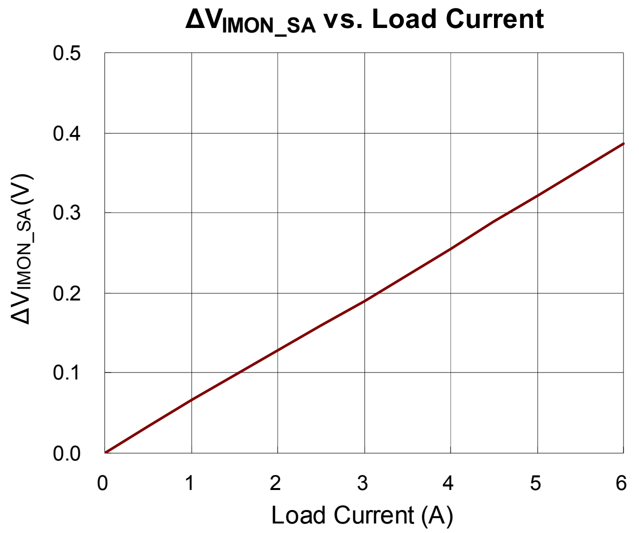


SA VR Mode Transient



SA VR Mode Transient




ΔVIMON_SA vs. Load Current
ΔVIMON_SA (V)
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
6
Load Current (A)

Application Information

Power-ON Sequence

In order to confirm sufficient power supply for proper operation, the VR triggers UVLO if VCC pin drops below 4.3V (max). The UVLO protection shuts down controller and forces high-side MOSFET and low-side MOSFET off. When VCC > 4.45, the RT3605BE issues POR = high and waits for VRON signal. After POR = high and VRON > 0.7V, the controller powers on (Chip Enable = H) and starts VR internal settings, which include internal circuit offset correction and function settings (PIN-SETTING). Users can set multi-functions through SETx and TSEN pins. Figure 2 shows the typical timing of controller power-on. After all internal settings are done and VCCSA rail VBOOT = 1.05V, VR_READY asserts before DVID up to VBOOT. The VR_READY asserts within 2.5ms (max) after Chip Enable = H (VRON = H and VCC > 4.45V). The pull-high power of the VRON pin is recommended as 1.05V, the same power as SVID interface. That can ensure SVID power is ready while VRON = H. For the VR normal operation, VIN should be ready before VCC, and VCC is strongly suggested to be ready before driver power(PVCC) to prevent current flowing back to VCC from PVCC through PWMx pin or DRVEN pin. Moreover, VRON must be the last one to assert after both VCC and PVCC are ready (>UVLO).

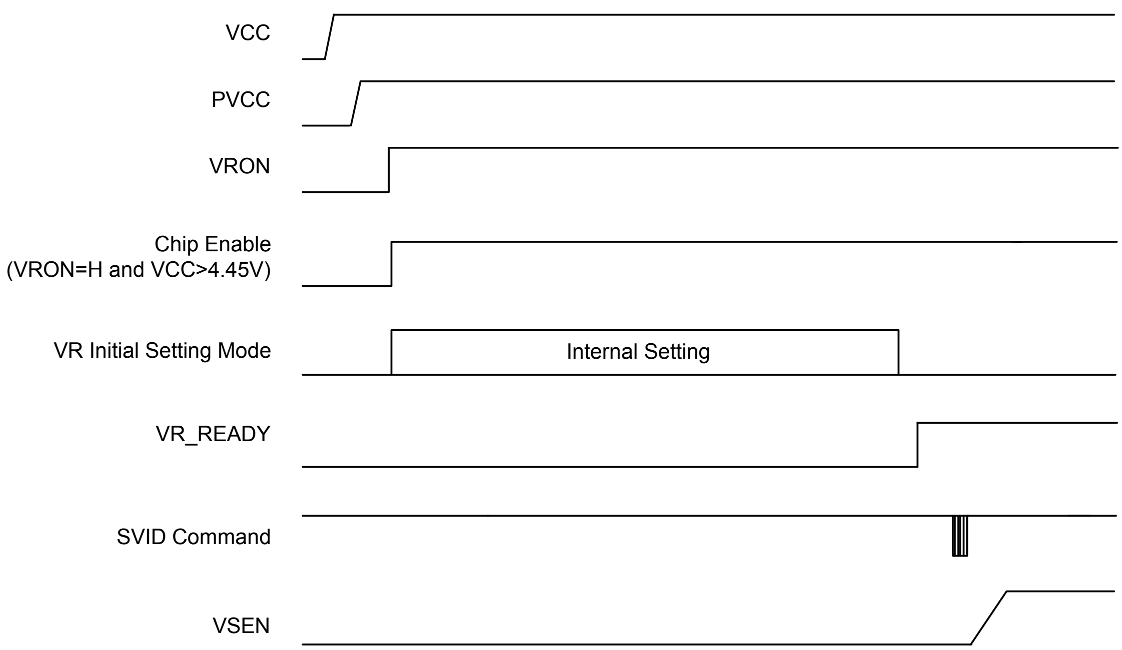


Figure 2. Typical Timing of Controller Power-On

Maximum Active Phase Number Setting

The number of active phase is determined by the ISENxN voltage. The detection is only active and latched at Chip Enable rising edge (VRON=H and VCC>4.45V). While the voltage at ISENxN > (VCC-1V), maximum active phase number is (x-1). For example, pulling MAIN_ISEN3N to VCC programs a 2-phase operation, while pulling MAIN_ISEN2N and MAIN_ISEN3N to VCC programs a 1-phase operation. The unused ISENxP pins are recommended to connect to VCC and the unused PWM pins can be floating. Figure 3 is a MAIN rail 2-phase operation example, the pull-up voltage of ISEN3N should be connected together with VCC of the RT3605BE and the pull-up resistor should be 10kΩ.

PIN-SETTING Mechanism

The RT3605BE provides multiple parameters for platform setting and BOM optimization. These parameters can be set through the SETx and TSEN pins. The RT3605BE adopts two-step PIN-SETTING mechanism to maximize IC pin utilization. Figure 4 illustrates this operating mechanism for SETx.

$V_{divider}$ and $V_{current}$ can be represented as follows :

$$V_{divider} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{current} = \frac{R2}{R1+R2} \times 3.2V + 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

The Divider-Register and the IXR-Register set specified functions. For example, the Divider-Register of SET1 sets the ICCMAX of MAIN and VCCSA; the IXR-Register of SET1 sets the ICCMAX_AUXI and ZCD_TH_MAIN. All setting functions are summarized in Table 1.

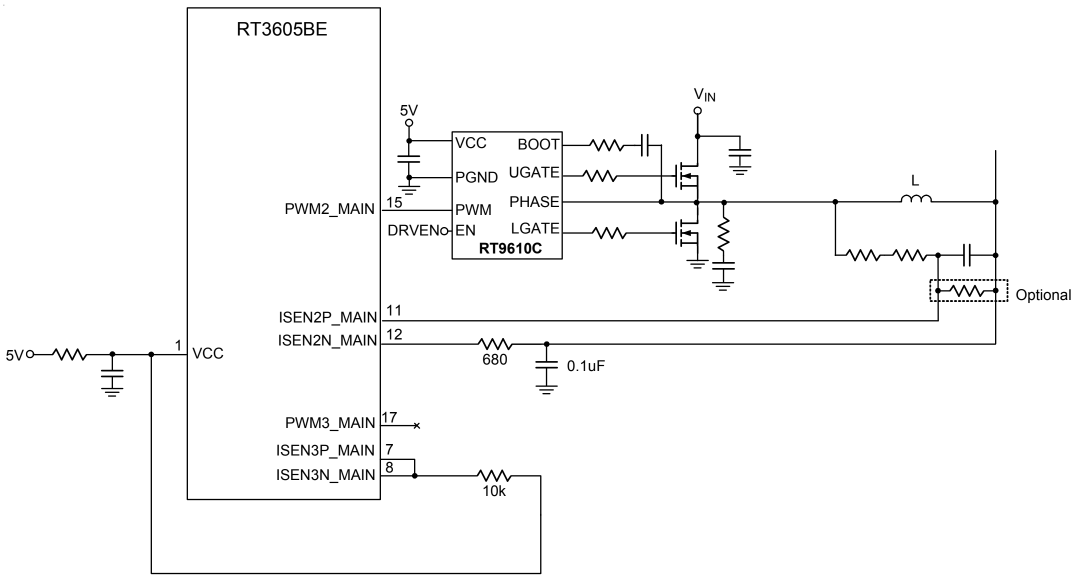


Figure 3. 2-Phases Operation Setting for MAIN rail

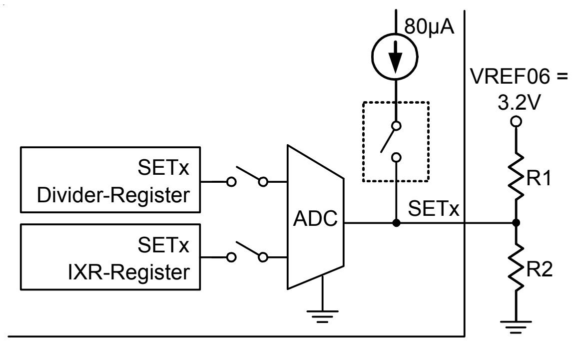


Figure 4. Operating Mechanism for SETx

Table 1. Summary of Pin Setting Functions

		Function Setting	Symbol	Description
SET1	Divider Register[4:2]	ICCMAX_MAIN	ICCMAX_MAIN [2:0]	According to Platform, set corresponding ICCMAX_MAIN.
	Divider Register[1:0]	ICCMAX_SA	ICCMAX_SA [1:0]	According to Platform, set corrsponding ICCMAX_SA.
	IXR Register[4:2]	ICCMAX_AUXI	ICCMAX_AUXI [2:0]	According to Platform, set corrsponding ICCMAX_AUXI.
	IXR Register[1]	MAIN rail Zero Current Detection Threshold	ZCD_TH_MAIN	Detect whether each phase current cross zero current. Set trigger level for MAIN rail.
SET2	Divider Register[4:2]	MAIN rail TON width setting (switching frequency)	TONSET_MAIN[2:0]	According to required frequency, select TON width for MAIN rail.
	Divider Register[1:0]	SA rail TON width setting (switching frequency)	TONSET_SA[1:0]	According to required frequency, select TON width for SA rail.
	IXR Register[4:2]	AUXI rail TON width setting (switching frequency)	TONSET_AUXI[2:0]	According to required frequency, select TON width for AUXI rail.
	IXR Register[1]	AUXI rail Zero Current Detection Threshold	ZCD_TH_AUXI	Detect whether each phase current cross zero current. Set trigger level for AUXI rail.
SET3	Divider Register[4:3]	MAIN rail advanced ramp magnitude in PS0	FLRAMP_PS0 _MAIN[1:0]	Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on in PS0 for MAIN rail.
	Divider Register[2:1]	AUXI rail advanced ramp magnitude in PS0	FLRAMP_PS0 _AUXI[1:0]	Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on in PS0 for AUXI rail.
	Divider Register[0]	MAIN sum OCP ratio	SUM_OC_MAIN	SUM_OC_MAIN = 0 : 160% x ICCMAX SUM_OC_MAIN = 1 : 130% x ICCMAX
	IXR Register[4]	MAIN rail advanced ramp magnitude in PS1	FLRAMP_PS1 _MAIN	Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on in PS1 for MAIN rail.
	IXR Register[3]	AUXI rail advanced ramp magnitude in PS1	FLRAMP_PS1 _AUXI	Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on in PS1 for AUXI rail.
	IXR Register[2:1]	SA rail advanced ramp magnitude in PS0	FLRAMP_PS0 _SA[1:0]	Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on in PS0 for SA rail.

		Function Setting	Symbol	Description
SET4	Divider Register[4:2]	MAIN rail Adaptive Quick Response(AQR) trigger level	AQR_TH_MAIN[2:0]	AQR for loop response speed-up of loading rising edge. Set trigger level MAIN rail.
	Divider Register[1]	MAIN rail high frequency ACLL voltage compensation	HFACLL_LIFT _MAIN	To provide positive offset in high frequency ACLL for MAIN rail.
	Divider Register[0]	AUXI rail high frequency ACLL voltage compensation	HFACLL_LIFT _AUXI	To provide positive offset in high frequency ACLL for AUXI rail.
	IXR Register[4:2]	AUXI rail Adaptive Quick Response(AQR) trigger level	AQR_TH_AUXI[2:0]	AQR for loop response speed-up of loading rising edge. Set trigger level AUXI rail.
	IXR Register[1]	SA rail high frequency ACLL voltage compensation	HFACLL_LIFT_SA	To provide positive offset in high frequency ACLL for SA rail.
SET5	Divider Register[4:3]	MAIN rail undershoot suppression	UDS_MAIN[1:0]	To improve undershoot by applying a positive offset at loading edge. To set trigger level for MAIN rail.
	Divider Register[2:1]	AUXI rail undershoot suppression	UDS_AUXI[1:0]	To improve undershoot by applying a positive offset at loading edge. To set trigger level for AUXI rail.
	Divider Register[0]	SA rail undershoot suppression	UDS_SA	To improve undershoot by applying a positive offset at loading edge. To set trigger level for SA rail.
	IXR Register[4:3]	MAIN rail Anti-overshoot trigger level	ANTIOVS_TH _MAIN[1:0]	ANTIOVS for reduction of overshoot at loading falling edge. To set trigger level for MAIN rail.
	IXR Register[2:1]	AUXI rail Anti-overshoot trigger level	ANTIOVS_TH _AUXI[1:0]	ANTIOVS for reduction of overshoot at loading falling edge. To set trigger level for AUXI rail.
TSEN _MAIN	Divider Register[4:3]	Current Gain_SA	Ai_SA[1:0]	SA rail current gain setting.
	Divider Register[2]	MIAN rail DVID voltage-compensation level	DVID_LIFT_MAIN	DVID_LIFT_MAIN = 0 : Disable DVID_LIFT_MAIN = 1 : 5μA current source sink from FB pin
	Divider Register[1]	AUXI rail DVID voltage-compensation level	DVID_LIFT_AUXI	DVID_LIFT_AUXI = 0 : Disable DVID_LIFT_AUXI = 1 : 5μA current source sink from FB pin
	Divider Register[0]	SA rail DVID voltage-compensation level	DVID_LIFT_SA	DVID_LIFT_SA = 0 : Disable DVID_LIFT_SA = 1 : 5.2μA current source sink from FB pin
TSEN _AUXI	Divider Register[4:3]	Current Gain_MAIN	Ai_MAIN[1:0]	MAIN rail current gain setting.
	Divider Register[2:1]	Current Gain_AUXI	Ai_AUXI[1:0]	AUXI rail current gain setting.
	Divider Register[0]	SA rail Zero Current Detection Threshold	ZCD_TH_SA	Detect whether each phase current cross zero current. Set trigger level for SA rail.

Referring to PIN-SETTING Table 2 to Table 13, users can search corresponding $V_{divider}$ or V_{IXR} according to the desired function setting combinations. Then SETx external resistors can be calculated as follows :

$$R1 = \frac{3.2V \times V_{IXR}}{80\mu A \times V_{divider}}$$

$$R2 = \frac{R1 \times V_{divider}}{3.2V - V_{divider}}$$

Richtek provides a Microsoft Excel-based design tool to calculate the desired PIN-SETTING resistors.

TSEN_x pin also has function settings except for thermal monitoring function. It only utilizes divider part of PIN-SETTING mechanism. The detailed operation is described in Thermal Monitoring and Indicator section.

Table 2. SET1 Pin Setting for ICCMAX_MAIN and ICCMAX_SA

$V_{divider\_SET1}$ (mV)	ICCMAX_MAIN(A)			ICCMAX_SA(A)
	1 Phase	2 Phase	3 Phase	
25	22	35	75	6
75				7
125				8
175				9
225	24	41	81	6
275				7
325				8
375				9
425	36	71	87	6
475				7
525				8
575				9
625	28	53	93	6
675				7
725				8
775				9
825	30	59	99	6
875				7
925				8
975				9
1025	32	65	105	6
1075				7
1125				8
1175				9
1225	34	47	111	6
1275				7
1325				8
1375				9
1425	26	77	117	6
1475				7
1525				8
1575				9

Table 3. SET1 Pin Setting for ICCMAX_AUXI and ZCD_TH_MAIN

V_{IXR_SET1} (mV)	ICCMAX_AUXI(A)		ZCD_TH_MAIN (mV)
	1 Phase	2 Phase	
50	22	35	1.51
150			2.64
250	24	41	1.51
350			2.64
450	26	47	1.51
550			2.64
650	28	53	1.51
750			2.64
850	30	59	1.51
950			2.64
1050	32	65	1.51
1150			2.64
1250	34	71	1.51
1350			2.64
1450	36	77	1.51
1550			2.64

Table 4. SET2 Pin Setting for KTON_MAIN and KTON_SA

$V_{divider\_SET2}$ (mV)	KTON_MAIN	KTON_SA
25	0.64	1.00
75		1.13
125		1.27
175		1.40
225	0.82	1.00
275		1.13
325		1.27
375		1.40
425	1	1.00
475		1.13
525		1.27
575		1.40
625	1.18	1.00
675		1.13
725		1.27
775		1.40
825	1.36	1.00
875		1.13
925		1.27
975		1.40
1025	1.55	1.00
1075		1.13
1125		1.27
1175		1.40
1225	1.73	1.00
1275		1.13
1325		1.27
1375		1.40
1425	1.91	1.00
1475		1.13
1525		1.27
1575		1.40

Table 5. SET2 Pin Setting for KTON_AUXI and ZCD_TH_AUXI

V_{IXR_SET2} (mV)	KTON_AUXI	ZCD_TH_AUXI (mV)
50	0.64	1.51
150		2.64
250	0.82	1.51
350		2.64
450	1	1.51
550		2.64
650	1.18	1.51
750		2.64
850	1.36	1.51
950		2.64
1050	1.55	1.51
1150		2.64
1250	1.73	1.51
1350		2.64
1450	1.91	1.51
1550		2.64

Table 6. SET3 Pin FR_PS0_MAIN, FR_PS0_AUXI and SUM_OCP_MAIN

$V_{divider\_SET3}$ (mV)	FR_PS0_MAIN	FR_PS0_AUXI	SUM_OCP_MAIN
25	25mV	25mV	160%
75			130%
125		75mV	160%
175			130%
225		125mV	160%
275			130%
325		Disable	160%
375			130%
425	75mV	25mV	160%
475			130%
525		75mV	160%
575			130%
625		125mV	160%
675			130%
725		Disable	160%
775			130%
825	125mV	25mV	160%
875			130%
925		75mV	160%
975			130%
1025		125mV	160%
1075			130%
1125		Disable	160%
1175			130%
1225	Disable	25mV	160%
1275			130%
1325		75mV	160%
1375			130%
1425		125mV	160%
1475			130%
1525		Disable	160%
1575			130%

Table 7. SET3 Pin Setting for FR_PS1_MAIN, FR_PS1_AUXI and FR_PS0_SA

V_{IXR_SET3} (mV)	FR_PS1_MAIN	FR_PS1_AUXI	FR_PS0_SA
50	125mV	125mV	60mV
150			80mV
250			100mV
350			Disable
450		175mV	60mV
550			80mV
650			100mV
750			Disable
850	175mV	125mV	60mV
950			80mV
1050			100mV
1150			Disable
1250		175mV	60mV
1350			80mV
1450			100mV
1550			Disable

Table 8. SET4 Pin Setting for AQR_TH_MAIN, HFACLL_LIFT_MAIN and HFACLL_LIFT_AUXI

$V_{divider\_SET4}$ (mV)	AQR_TH_MAIN (mV)	HFACLL_LIFT_MAIN	HFACLL_LIFT_AUXI
25	120mV	Disable	Disable
75			Enable
125		Enable	Disable
175			Enable
225	200mV	Disable	Disable
275			Enable
325		Enable	Disable
375			Enable
425	280mV	Disable	Disable
475			Enable
525		Enable	Disable
575			Enable
625	360mV	Disable	Disable
675			Enable
725		Enable	Disable
775			Enable
825	440mV	Disable	Disable
875			Enable
925		Enable	Disable
975			Enable
1025	520mV	Disable	Disable
1075			Enable
1125		Enable	Disable
1175			Enable
1225	600mV	Disable	Disable
1275			Enable
1325		Enable	Disable
1375			Enable
1425	Disable	Disable	Disable
1475			Enable
1525		Enable	Disable
1575			Enable

Table 9. SET4 Pin Setting for AQR_TH_AUXI and HFACLL_LIFT_SA

V_{IXR_SET4} (mV)	AQR_TH_AUXI (mV)	HFACLL_LIFT_SA
50	120mV	Disable
150		Enable
250	200mV	Disable
350		Enable
450	280mV	Disable
550		Enable
650	360mV	Disable
750		Enable
850	440mV	Disable
950		Enable
1050	520mV	Disable
1150		Enable
1250	600mV	Disable
1350		Enable
1450	Disable	Disable
1550		Enable

Table 10. SET5 Pin Setting for UDS

$V_{divider\_SET5}$ (mV)	UDS_MAIN (mV)		UDS_AUXI (mV)		UDS_SA (mV)
	PS0	PS1	PS0	PS1	
25	Disable	Disable	Disable	Disable	70
75					50
125			200	125	70
175					50
225			200	175	70
275					50
325			250	150	70
375					50
425	200	125	Disable	Disable	70
475					50
525			200	125	70
575					50
625			200	175	70
675					50
725			250	150	70
775					50
825	200	175	Disable	Disable	70
875					50
925			200	125	70
975					50
1025			200	175	70
1075					50
1125			250	150	70
1175					50
1225	250	150	Disable	Disable	70
1275					50
1325			200	125	70
1375					50
1425			200	175	70
1475					50
1525			250	150	70
1575					50

Table 11. SET5 Pin Setting for ANTIOVS_MAIN and ANTIOVS_AUXI

V_{IXR_SET5} (mV)	ANTIOVS_TH_MAIN (mV)	ANTIOVS_TH_AUXI (mV)
50	90mV	90mV
150		150mV
250		210mV
350		Disable
450	150mV	90mV
550		150mV
650		210mV
750		Disable
850	210mV	90mV
950		150mV
1050		210mV
1150		Disable
1250	Disable	90mV
1350		150mV
1450		210mV
1550		Disable

Table 12. TSEN_MAIN Pin Setting for AI_SA and DVID_LIFT

VTSEN_MAIN (mV)	AI_SA	DVID_LIFT_MAIN	DVID_LIFT_AUXI	DVID_LIFT_SA
50			0uA	0uA
150		0uA		5.2uA
250			5uA	0uA
350	0.5			5.2uA
450			0uA	0uA
550		5uA		5.2uA
650			5uA	0uA
750				5.2uA
850			0uA	0uA
950		0uA		5.2uA
1050			5uA	0uA
1150	1			5.2uA
1250			0uA	0uA
1350		5uA		5.2uA
1450			5uA	0uA
1550				5.2uA
1650			0uA	0uA
1750		0uA		5.2uA
1850			5uA	0uA
1950	1.5			5.2uA
2050			0uA	0uA
2150		5uA		5.2uA
2250			5uA	0uA
2350				5.2uA
2450			0uA	0uA
2550		0uA		5.2uA
2650			5uA	0uA
2750	2			5.2uA
2850			0uA	0uA
2950		5uA		5.2uA
3050			5uA	0uA
3150				5.2uA

Table 13. TSEN_AUXI Pin Setting for AI_MIAN, AI_AUXI, and ZCD_TH_SA

V_{TSEN_AUXI} (mV)	AI_MAIN	AI_AUXI	ZCD_TH_SA (mV)
50	0.25	0.25	1.51
150			2.64
250		0.5	1.51
350			2.64
450		0.75	1.51
550			2.64
650		1	1.51
750			2.64
850	0.5	0.25	1.51
950			2.64
1050		0.5	1.51
1150			2.64
1250		0.75	1.51
1350			2.64
1450		1	1.51
1550			2.64
1650	0.75	0.25	1.51
1750			2.64
1850		0.5	1.51
1950			2.64
2050		0.75	1.51
2150			2.64
2250		1	1.51
2350			2.64
2450	1	0.25	1.51
2550			2.64
2650		0.5	1.51
2750			2.64
2850		0.75	1.51
2950			2.64
3050		1	1.51
3150			2.64

Per Phase Current Sense

To achieve higher efficiency, the RT3605BE adopts inductor DCR current sensing to get each phase current signal for multiple and single phase, as illustrated in Figure 5 and Figure 6, respectively. An external low-pass filter R_{X1} and C_X reconstruct the current signal. The low-pass filter time constant $R_{X1} \times C_X$ should match time constant $\frac{L_X}{DCR}$ of inductance and DCR. It's fine to fine tune R_{X1} and C_X for transient performance and current reporting if RC network time constant matches inductor time constant $\frac{L_X}{DCR}$, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant $\frac{L_X}{DCR}$, V_{CORE} waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant $\frac{L_X}{DCR}$, V_{CORE} waveform sags to create an undershooting to fail the specification and mis-trigger over-current protections (sum OCP and per phase OCP). Figure 7 shows the output waveforms according to the RC network time constant. The resistance of R_{CSx} is restricted to 680Ω and the accuracy is within 1%. The R_{X1} is highly recommended as two 0603 size resistors in series to enhance the Iout reporting accuracy for multiple phase application. The X7R type capacitor is suggested for C_X in the application.

$$I_{CS,PERx} = \frac{V_{CSIN}}{680\Omega} = \frac{I_{Lx} \times DCR}{680\Omega}$$

The R_{X2} is optional for prevent VCSIN exceeding current sense amplifier input range. The time constant of (R_{X1}// R_{X2}) x C_X should match $\frac{L_X}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{680\Omega} = \frac{I_{Lx} \times DCR}{680\Omega} \times \frac{R_{X2}}{R_{X1}+R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for loadline control/ current reporting, current balance, zero current detection and over-current protection. The mirrored current to IMON pin is one time of $I_{CS,PER}$. ($I_{IMON} = A_{MIRROR} \times I_{CS,PERx}$, $A_{MIRROR} = 1$)

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

The single phase current sense is demonstrated as Figure 6. It is similar to multiple phase method. In single phase design, the resistance of R_{CS} is equal to 2.15kΩ.

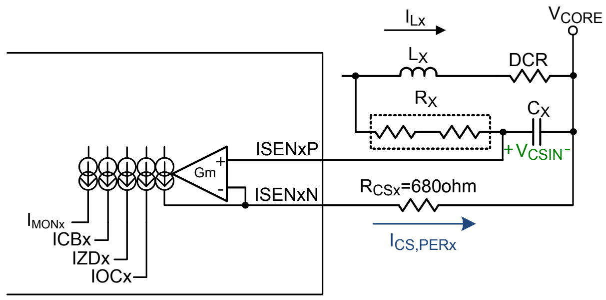


Figure 5. Inductor DCR Current Sensing Method for MAIN and AUXI

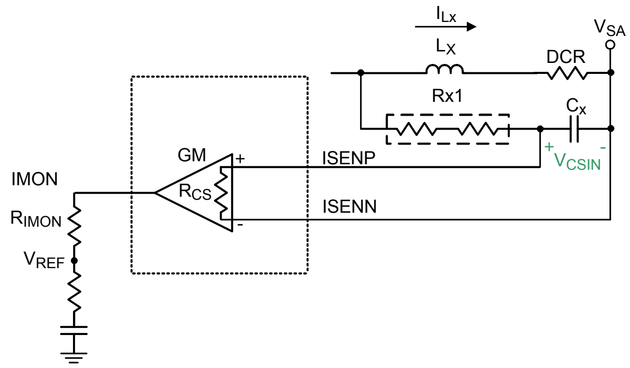


Figure 6. Inductor DCR Current Sensing Method for SA

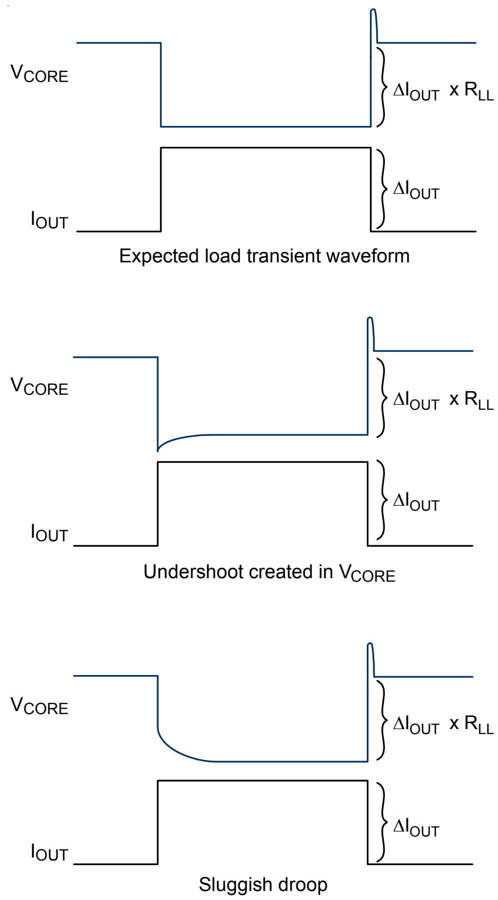


Figure 7. All Kinds of RC Network Time Constant

Single Phase Thermal Compensation for Current Sense

Since the copper wire of inductor has a positive temperature coefficient temperature compensation is necessary for the lossless inductor current sense. For single phase thermal compensation, Figure 8. shows a not only simple but also effective way to compensate temperature variation. An NTC thermistor is put in the current sensing network and it can be used to compensate DCR variation because temperature is changed.

The current sense network equation is as follows :

$$\Delta V_{IMON} = V_{IMON} - V_{REF} = \frac{I_{LX} \times DCR \times \dfrac{R_S + (R_P // R_{NTC})}{R_{X1} + (R_S + R_P // R_{NTC})}}{R_{CS}} \times R_{IMON}$$

Usually the R_P is set equal to R_{NTC} (25°C). R_S is selected to linearize the NTC's temperature characteristic. For a given NTC, the equations below are to get R_{X1} and R_S to compensate the temperature variation of the sense resistor.

Let

$R_{EQU} = R_S + (R_P // R_{NTC})$

According to current sense network, the corresponding equation is represented as follows :

$$\frac{L_X}{DCR} = C_X \times \frac{R_{EQU} \times R_{X1}}{R_{EQU} + R_{X1}}$$

Next, let

$$m = \frac{L_X}{DCR \times C_X}$$

Then

$$m \times \left(R_{X1} + R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right) = R_{X1} \times \left(R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right)$$

Step1 : Given the two system temperature T_R and T_H at which are compensated.

Step2 : Two equations can be listed as

$$m(T_R) \times \left(R_{X1} + R_S + \frac{R_{NTC}(T_R) \times R_P}{R_{NTC}(T_R) + R_P} \right) = R_{X1} \times \left(R_S + \frac{R_{NTC}(T_R) \times R_P}{R_{NTC}(T_R) + R_P} \right)$$

$$m(T_H) \times \left(R_{X1} + R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right) = R_{X1} \times \left(R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right)$$

Step3 : Usually the R_P is set equal to R_{NTC} (T_R). Hence, there are two equations and two unknowns, R_{X1} and R_S, can be found out.

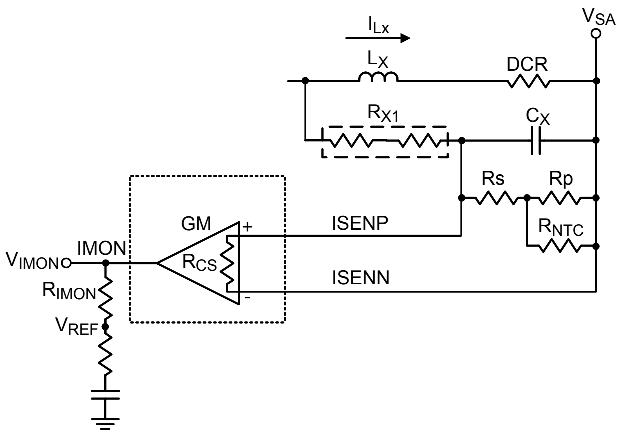


Figure 8. Thermal Compensation method for Single Phase

Total Current Sense (MAIN and AUXI)/ICCMAX Setting/Current Monitoring

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The RT3605BE adopts a patented total current sense method that requires only one NTC resistor for thermal compensation. The NTC resistor is designed within IMON resistor network on IMON pin. It is suggested to be placed near the inductor of the first phase. Figure 9 shows the configuration. All phase current signals are gathered to IMON pin and converted to a voltage signal V_{IMON} by $R_{IMON,EQ}$ based on VREF06 pin. The VREF06 pin provides 0.6V voltage source (as presented as V_{VREF06}) while pin-setting mechanism complete. The relationship between V_{IMON} and inductor current I_{Lx} is :

$$V_{IMON} - V_{VREF06} = (I_{L1} + I_{L2} + ...) \times \frac{DCR}{R_{CSx}} \times R_{IMON,EQ}$$

$V_{IMON} - V_{VREF06}$ is proportional to output current. $V_{IMON} - V_{VREF06}$ is used for output current reporting and loadline loop-control. $V_{IMON} - V_{VREF06}$ is averaged by analog lowpass filter and then transferred to 8-bit ADC. For MAIN rail, the digitized reporting value is scaled such that FFh = ICCMAX_MAIN. The $R_{IMON,EQ}$ should be designed that $V_{IMON} - V_{VREF06} = 0.8V$ while $(I_{L1}+I_{L2}+I_{L3})$ = ICCMAX_MAIN = MAIN ICC_Max register (21h) value, where V_{IMON_MAX} =0.8V when ICCMAX > 40A, else = 0.4V. Additionally, sets the desired ICCMAX_MAIN by the ICCMAX_MAIN[2:0] of the PIN-SETTING Table 2. The PINSETTING value determines Intel MAIN rail ICCMAX register (21h) value. The $\overline{ALERT}$ is asserted while output current exceeds ICCMAX_MAIN ($V_{IMON} - V_{VREF06} > 0.8V$). The behavior is masked during DVID. For loadline loop-control, $V_{IMON} - V_{VREF06}$ is scaled by a percentage of Ai_MAIN, that can be selected by Ai_MAIN[1:0] of PIN-SETTING. The detailed application is described in the loadline setting section.

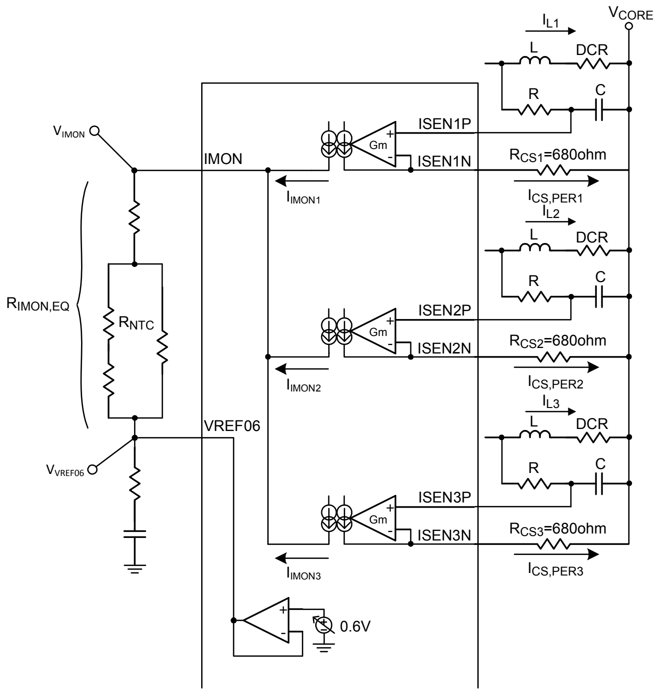


Figure 9. Total Current Sense Method

Loadline Setting (R_{LL})

An output voltage loadline (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of loadline is that the output voltage decreases by an amount which is proportional to the increasing loading current, i.e. the slope between output voltage and loading current (R_{LL}) is shown in Figure 10. Figure 11 shows how the voltage and current loop parameters of RT3605BE achieve loadline. The detailed equation is described for MAIN/AUXI as below :

$$R_{LL}=\frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}}=\frac{DCR}{R_{CSx}}\times R_{IMON,EQ}\times\frac{A_i}{\frac{R_{EA2}}{R_{EA1}}}\times\frac{3}{4}$$

The detailed equation is described for SA as below :

$$R_{LL}=\frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}}=DCR\times\frac{A_i}{\frac{R_{EA2}}{R_{EA1}}}\times 10$$

A_i is current gain. $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and is suggested to be greater than 2 for better transient response. The R_{LL} can be programmed by A_i and A_V. A_i can be selected by PIN-SETTING of Ai[1:0] as listed in Table 14 and 15.

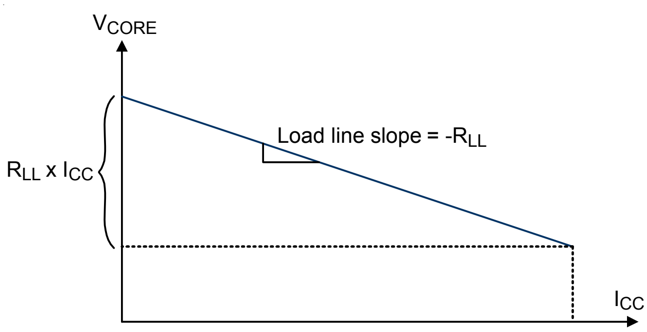


Figure 10. Load-Line (Droop)

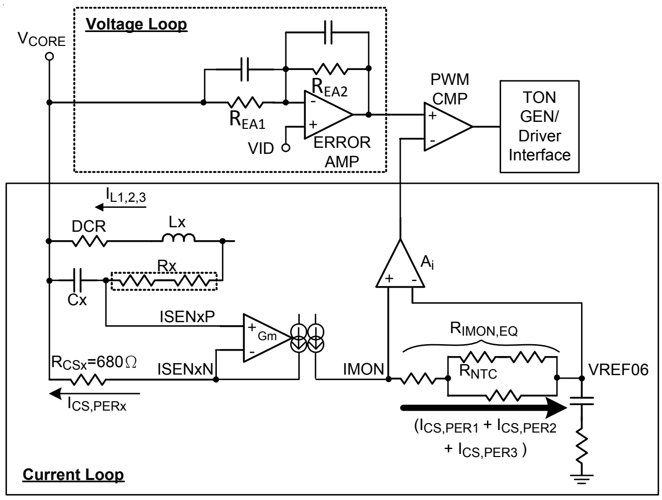


Figure 11. Voltage Loop and Current Loop for Load Line

Table 14 PIN-SETTING of Ai_MIAN/AUXI

Ai[1:0]	Current Gain Setting
00	0.25
01	0.5
10	0.75
11	1

Table 15 PIN-SETTING of Ai_SA

Ai[1:0]	Current Gain Setting
00	0.5
01	1
10	1.5
11	2

Dynamic VID (DVID) Compensation

During DVID transition, an extra current is required to charge output capacitor for increasing voltage. The charging current approximates to the product of the DVID slew rate and output capacitance. For droop system, the extra charging current will induce extra voltage droop so that the output voltage cannot reach target within the specific time. The extra voltage drop approximates to DVID Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the loadline slope, Ω). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 12. The RT3605BE provides one DVID compensation function as shown in Figure 13. An internal current I_{DVID_LIFT} is sinking internally from FB pin to generate DVID compensation I_{DVID_LIFT} x R_{EA1}. The I_{DVID_LIFT} for 30mV/us DVID SR can be set from TSEN_MAIN and SET3 PIN-SETTING of DVID_LIFT. For different scale of DVID SR, I_{DVID_LIFT} is internally adjusted. Compensating magnitude can also be adjusted by R_{EA1}. For IMVP8 spec, output voltage should be within target TOB at 1μs after Alert. While DAC just arrives target (Alert issue timing), inductor current is still high and needs a time to settle down to the DC loading current. In the settling time, the falling down current keeps to charge output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, DVID compensation can be less than DVID Slew Rate x Output Capacitance (Capacitance degeneration should be considered). While output capacitance is such larger that DVID compensation cannot cover, adding resistor and capacitance from FB to GND also can provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects DVID behavior. The final setting should be based on actual measurement.

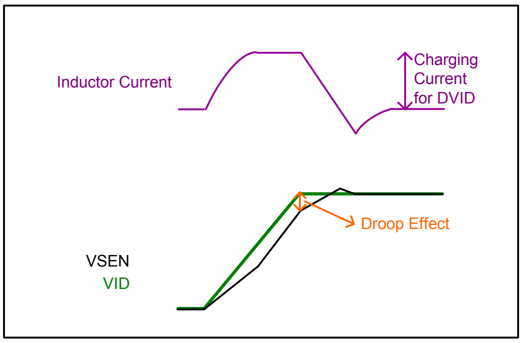


Figure 12. Droop Effect in VID Transition

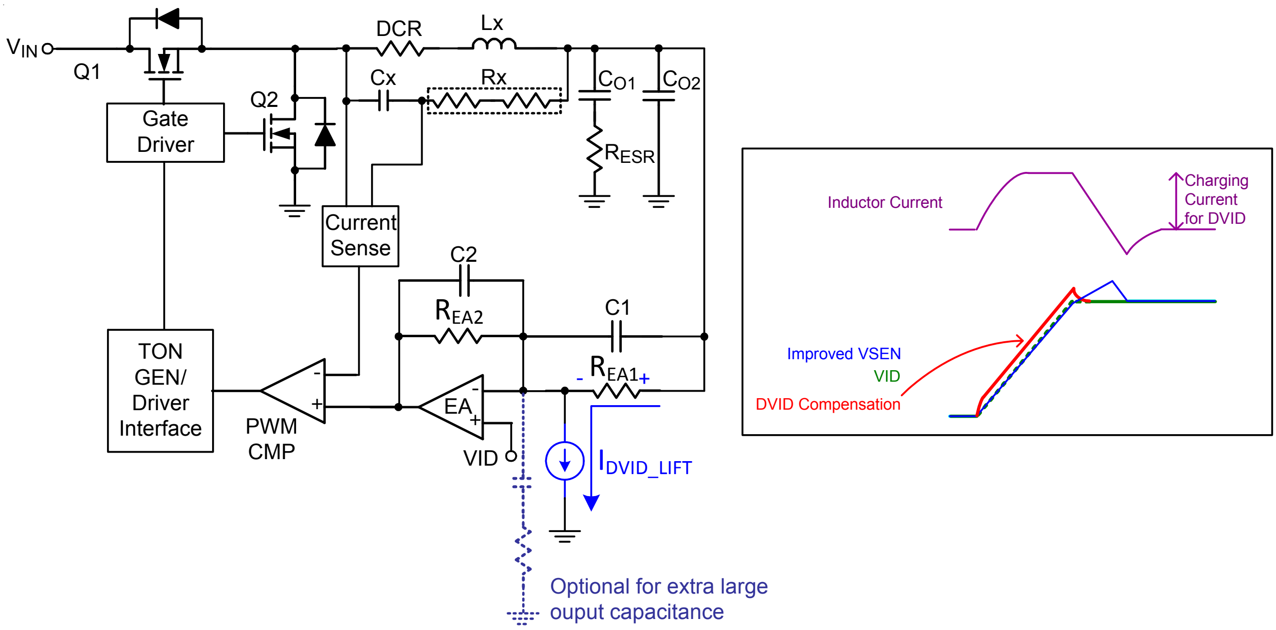


Figure 13. DVID Compensation

Compensator Design

The RT3605BE doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP™ topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 14. For ACLL specification, it is recommended to adjust compensator according to load transient ring back level. Default compensator values are referred to the design tool.

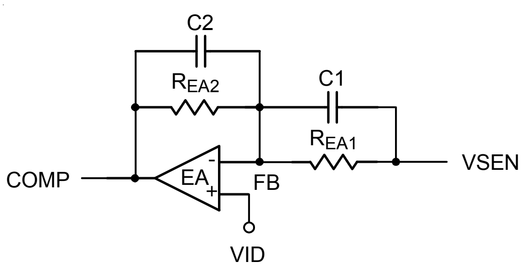


Figure 14. Type I Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. The related connection is shown in Figure 15. The VID voltage (DAC) is referred to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

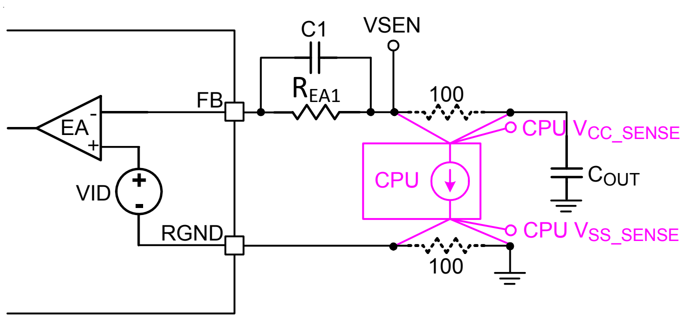


Figure 15. Remote Sensing Circuit

Switching Frequency Setting

The G-NAVP™ (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive T_{ON} (PWM) with input voltage (V_{IN}) for better line regulation. The T_{ON} is also adaptive to VID voltage. For VID < 0.9V, the adaptive T_{ON} is based on constant current ripple concept for better output voltage ripple size control. For VID ≥ 0.9V, the adaptive T_{ON} is based on constant frequency concept for better efficiency performance. Figure 16 is the conceptual chart showing the relationships between switching frequency vs. VID and current ripple vs. VID. The RT3605BE provides a parameter setting of k_{TON} to design T_{ON} width. The k_{TON} is set by PIN-SETTING of TONSET. The related setting table is listed in Table 16 and 17.

The equations of T_{ON} (MAIN / AUXI) are listed as below (k_{TON} should be referred to Table 16) :

VID ≥ 0.9V

$$T_{ON} = 2.206\mu \times \frac{VID}{k_{TON} \times (V_{IN} - 0.9V)} + 15ns$$

VID < 0.9V

$$T_{ON} = 1.985\mu \times \frac{1}{k_{TON} \times (V_{IN} - VID)} + 15ns$$

Table 16. PIN-SETTING of TONSET for MAIN/AUXI

TONSET<2:0>	kTON
000	0.64
001	0.82
010	1.00
011	1.18
100	1.36
101	1.55
110	1.73
111	1.91

The equations of T_{ON} (SA) are listed as below (k_{TON} should be referred to Table 17) :

$VID \geq 0.9V$

$$T_{ON} = 1.78\mu \times \frac{VID}{k_{TON} \times (V_{IN} - 0.9V)} + 11.5ns$$

$VID < 0.9V$

$$T_{ON} = 1.602\mu \times \frac{1}{k_{TON} \times (V_{IN} - VID)} + 11.5ns$$

Table 17. PIN-SETTING of TONSET for SA

TONSET_SA<1:0>	k_{TON}
00	1
01	1.13
10	1.27
11	1.4

The switching frequency can be derived from T_{ON} shown below. The losses in the main power stage and driver characteristics are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times \left(DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL} \right)}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}} \right) \right] \times (T_{ON} - T_D + T_{ONVAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times T_D}$$

VID : VID voltage

V_{IN} : input voltage

I_{CC} : loading current

N : total phase number

$R_{ONLS,max}$: the maximum equivalent of the high-side $R_{DS(ON)}$

n_{HS} : the number of high-side MOSFETs

$R_{ONHS,max}$: the maximum equivalent of the low-side $R_{DS(ON)}$

n_{LS} : number of low-side MOSFETs.

T_D : summation of the high-side MOSFET delay time and rising time

T_{ONVAR} : TON variation value

DCR : the inductor DCR

R_{LL} : loadline setting (Ω)

Although T_{ON} is designed for constant frequency target while $VID \geq 0.9$, the actual frequency is still impacted by main power stage's loss and driver dead time. The switching frequency will be rising as loading current increases. It is recommended to design the switching frequency based on the optimized efficiency and thermal performance at thermal design current (I_{CCTDC}). For example, at $I_{CC} = I_{CCTDC}$, VID = 0.9V and VIN = 19V, the optimized switching frequency is 650kHz. Then, substitute these values into equations to get T_{ON} and relative k_{TON}.

Richtek provides a Microsoft Excel-based design tool to help design k_{TON} setting for the desired switching frequency at TDC.

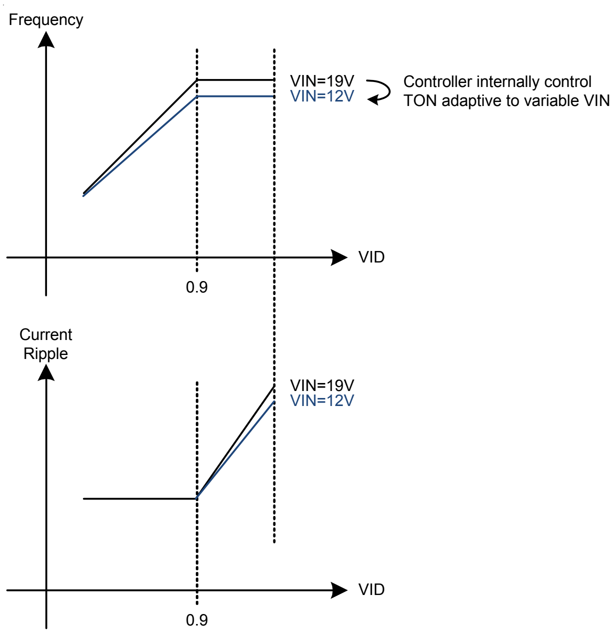


Figure 16. Switching Frequency and Current with Different VID

Adaptive Quick Response (AQR) for MAIN and AUXI

The RT3605BE adopts Adaptive Quick Response (AQR) to optimize transient response. The mechanism concept is illustrated in Figure 17. Controller detects output voltage drop slew rate. While the slew rate exceeds the AQR threshold, all PWM will turn on an 80% constant on time. The RT3605BE provides various AQR threshold through PIN-SETTING of AQR_TH. The following equation can initially decide the AQR starting trigger threshold. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid miss trigger AQR.

$$\text{AQRStartingTriggerThreshold} = -4\mu \times \frac{dVSEN}{dt}$$

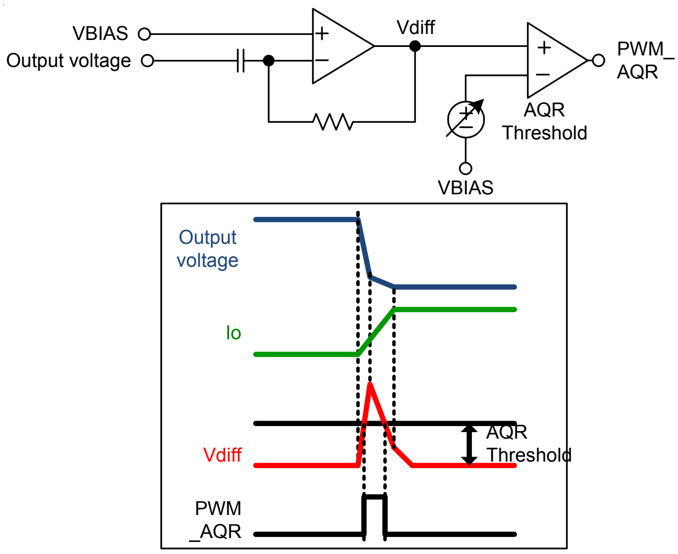


Figure 17. Adaptive Quick Response Mechanism

Table 18. PIN-SETTING of AQR_TH_MAIN/AUXI

AQR_TH[2:0]	AQR Starting Trigger Threshold
000	120mV
001	200mV
010	280mV
011	360mV
100	440mV
101	520mV
110	600mV
111	Disable

Anti-overshoot (ANTI-OVS) for MAIN and AUXI

The RT3605BE provides anti-overshoot function to depress output voltage overshoot. Controller detects overshoot by signals relating to output voltage. The overshoot trigger level can be adjusted by PIN-SETTING listed in Table 19. The main detecting signal comes from COMP. However, COMP varies with compensation. Initial trigger level setting can be based on the following equation :

$$\Delta V_{COMP} \times \frac{4}{3} = \Delta V_{SEN} \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Antiovershoot Threshold of ANTIOVS\_TH}[1:0]$$

The final setting should be according to actual Error AMP compensator design and measurement.

While overshoot exceeds the setting trigger level, all PWMs keep in tri-state until the zero current is detected. Turn-off LGs will force positive current flow through body diode to cause diode forward voltage. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

Table 19. PIN-SETTING of ANTIOVS_TH_MAIN/AUXI

ANTIOVS_TH[1:0]	Anti-overshoot Threshold (mV)
00	90
01	150
10	210
11	Disable

Dual Ramp Mechanism

Normal controllers easily suffer jitter and stability issues under low equivalent series resistance (ESR) of capacitor applications and large loop delay conditions. The large loop delay often comes from PCB parasitic inductance. Figure 18 illustrates how PCB parasitic inductance impacts on the load transient response. The PCB parasitic inductance delays energy delivering and causes VSEN to keep falling. The dropping VSEN induces several successive PWM pulses and then VSEN ring-back occurs. While load current release at the ring back region, it will generate larger overshoot. Thus, more capacitors will be used for the overshoot reduction.

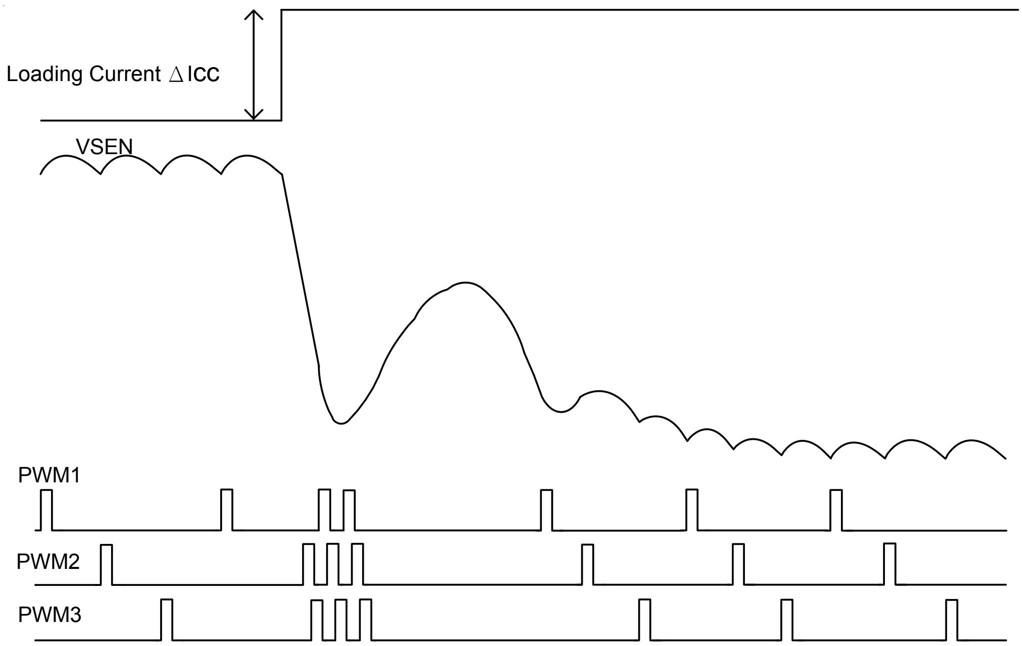


Figure 18. Load Transient Response with PCB Parasitic Inductance

The RT3605BE provides a new generation of dual ramp mechanism to enhance performance. Except original ramp to minimize jitter, additional advanced ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on. The dual ramp mechanism has current signal meaning so the transient ring-back can be effectively suppressed. Figure 19 show the apparent difference of the dual ramp with PCB parasitic inductance condition.

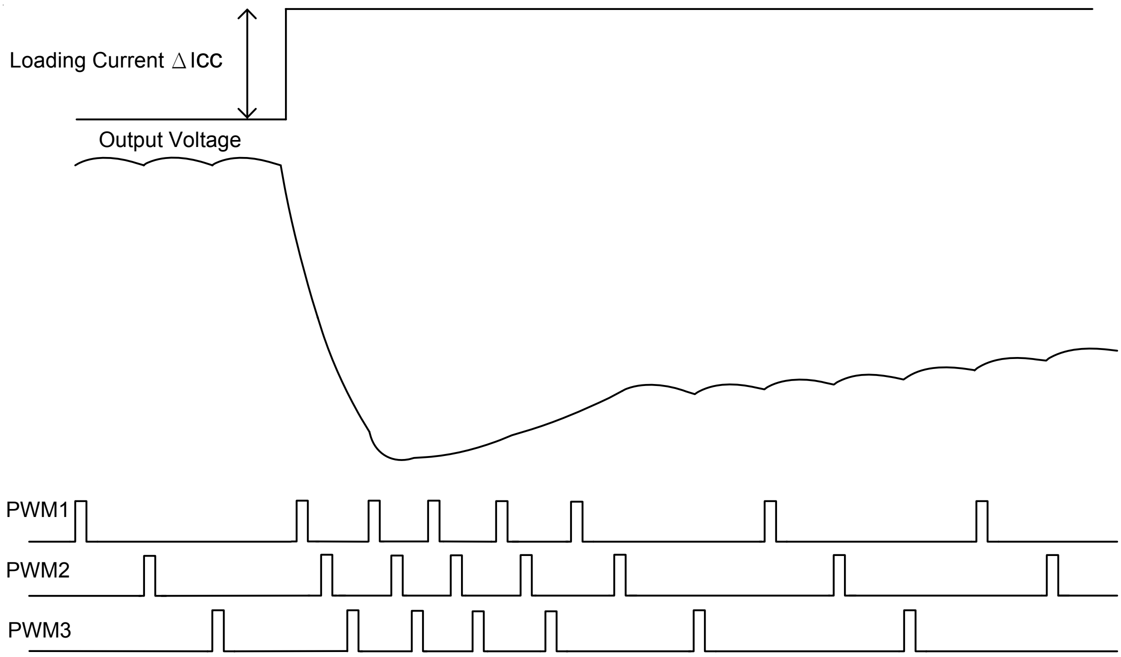


Figure 19. Dual Ramp Behavior with PCB Parasitic Inductance Condition

Through PIN-SETTING, the RT3605BE provides advanced ramp magnitude tuning. The FLRAMP_PS0 and FLRAMP_PS1 are for PS0 and PS1, respectively. According to different application conditions, the setting of parameters is listed in Table 20 to Table 22. The larger magnitude indicates larger parasitic inductance suppression. However, larger magnitude also affects loop response speed and reduces PWM output frequency at loading edge.

Table 20. PIN-SETTING of Advanced Ramp Magnitude in PS0 for MAIN/AUXI

FLRAMP_PS0 [1:0]	Internal Advanced Ramp Magnitude (index)
00	25
01	75
10	125
11	Disable

Table 21. PIN-SETTING of Advanced Ramp Magnitude in PS0 for SA

FLRAMP_PS0_SA [1:0]	Internal Advanced Ramp Magnitude (index)
00	60
01	80
10	100
11	Disable

Table 22. PIN-SETTING of Advanced Ramp Magnitude in PS1 for MAIN/AUXI

FLRAMP_PS1	Internal Advanced Ramp Magnitude (index)
0	125
1	175

ACLL Performance Enhancement

The RT3605BE provides another optional function to improve undershoot by applying a positive offset at loading edge. Controller detects the COMP signal and compares it with steady state. While V_{COMP} variation exceeds a threshold, an additional positive offset will apply to the output voltage. The threshold can be set through PIN-SETTING and separately for PS0 and PS1 as listed in Table 23 and Table 24. The smaller index indicates the easier detection being triggered. The positive offset is related to the compensation.

The ACLL performance enhancement threshold can approximate to 60mV/ $\frac{R_{EA2}}{R_{EA1}}$. In PS0, the slew rate of V_{RAMP} will increase when the V_{COMP} intersects the positive offset. In order to send out another on-time earlier to improve undershoot. In PS1, except for the positive offset, an additional 10mV is applied to the DAC and one pulse of PWM is also forced to turn on while the function is triggered. The positive offset is released gradually with about hundred micro-second. Figure 20 and Figure 21 show undershoot suppression behavior in PS0 and PS1. For different platform, the optimized setting is different. The final setting must be based on actual measurement.

Table 23. PIN-SETTING of Undershoot Suppression for MAIN/AUXI

UDS [1:0]	PS0 (index)	PS1 (index)
00	Disable	Disable
01	200	125
10	200	175
11	250	150

Table 24. PIN-SETTING of Undershoot Suppression for SA

UDS_SA	PS0/PS1 (index)
0	70
1	50

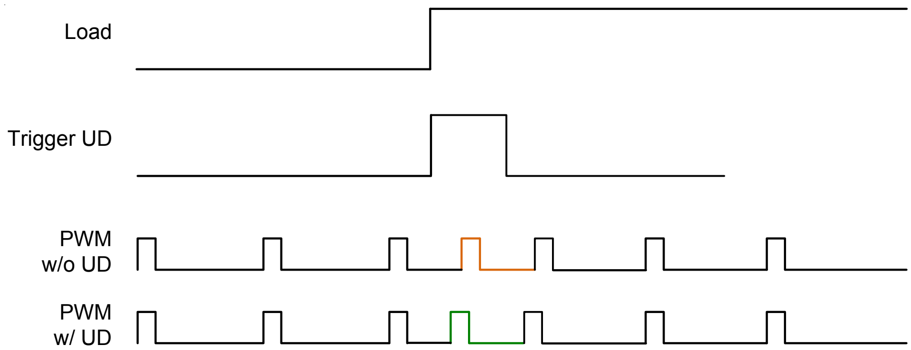


Figure 20. Undershoot Suppression Behavior in Multiple Phase.

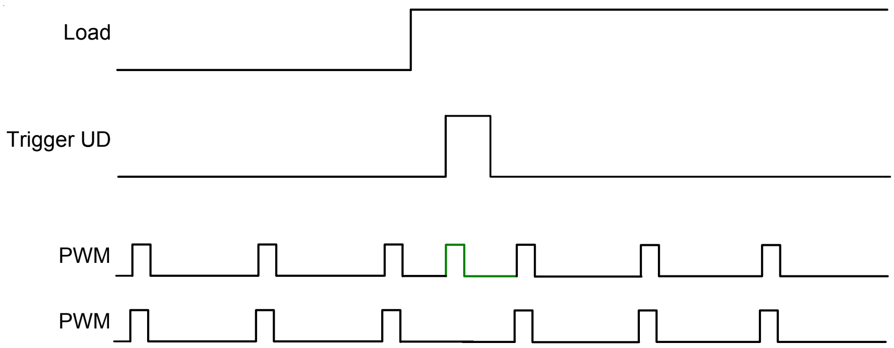


Figure 21. Undershoot Suppression Behavior in Single Phase.

High Frequency ACLL Voltage Compensation

The RT3605BE provides positive offset that only applies to high-frequency ACLL. The positive offset can be enabled through PIN-SETTING. The HFACLL_LIFT is the related setting.

Thermal Monitoring and Indicator

The TSEN pin processes two functions of PIN-SETTING (function setting) and thermal monitoring as shown in Figure 22. After power on, the TSEN has three operation modes: PIN-SETTING, Pre-thermal Sense, and Thermal Sense Mode. The corresponding function blocks of the three modes are shown in Figure 22. In the PIN-SETTING Mode, the TSEN pin voltage = 3.2V x R2/(R1+R2) with VREF06 = 3.2V and is coded by ADC and stored in the PIN-SETTING register. In the Pre-thermal Sense Mode, the TSEN pin voltage = 0.6V x R2/(R1+R2) with VREF06 = 0.6V and is coded and stored in the PRE-Thermal Register. This part helps Thermal Sense Mode calculation. In the Thermal Sense Mode, TSEN pin voltage = 0.6V x R2/(R1+R2) + 80μA x [(R1//R2) + R3] with VREF06 = 0.6V and is coded. The result will subtract the Pre-Thermal Register code and stored in the Thermal Register (The corresponding TSEN voltage = 80μA x [(R1//R2)+R3] which is defined as Thermal Voltage. The R3 is the NTC thermistor network to sense temperature. NTC thermistor is recommended to place near the inductor, the hottest area in the PCB. Higher temperature will cause smaller R3 and lower TSEN. According to NTC thermistor temperature curve, design Thermal Voltage v.s Temperature with proper R3 network to meet Table 25. 100°C Thermal Voltage = 80μA x [(R1//R2)+R3(100°C)] = 1.092V must be required. Controller processes the TSEN pin voltage to report temperature zone register (12h). While the TSEN pin voltage is less than 1.092V, the VR_HOT will be pulled low to indicate thermal alert. The signal is an open-drain signal. Thermal Register data is updated every 100us and the average interval is 800μs. The resistance accuracy of TSEN network is recommended to be less than 1% error.

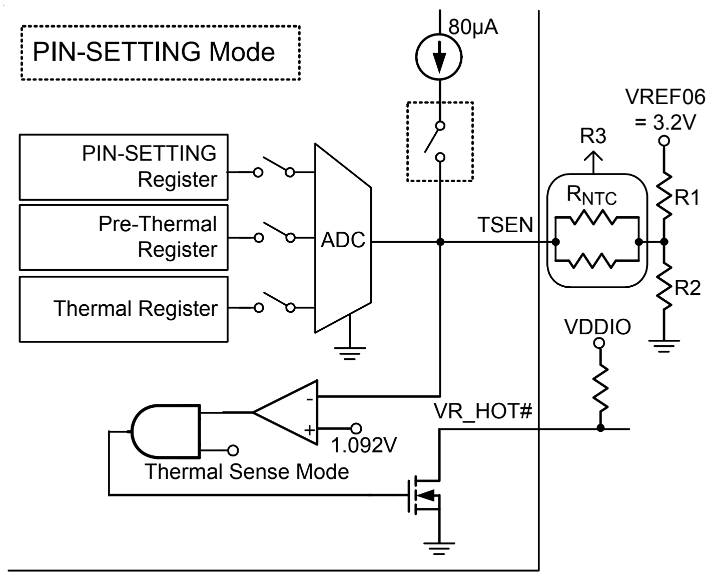


Figure 22. Multi-Function Pin Setting Mechanism for TSEN_MAIN/AUXI

Table 25. Thermal Zone and Detection Encoding

Temperature	Thermal Voltage 80µA x [(R1//R2)+R3]	Temperature Zone Register (12h)
100°C	1.092V	FFh
97°C	1.132V	7Fh
94°C	1.176V	3Fh
91°C	1.226V	1Fh
88°C	1.283V	0Fh
85°C	1.346V	07h
82°C	1.418V	03h
75°C	1.624V	01h

System Input Power Monitoring (PSYS)

The RT3605BE provides PSYS function to monitor total platform system power and report to the CPU via SVID interface. The PSYS function is illustrated as in Figure 23. The PSYS meter measures system input current and outputs a proportional current signal I_{PSYS}. The R_{PSYS} is designed for the PSYS voltage = 1.6V with maximum I_{PSYS} for 100% system input power. 1.6V is a full-scale analog signal for FFh digitized code.

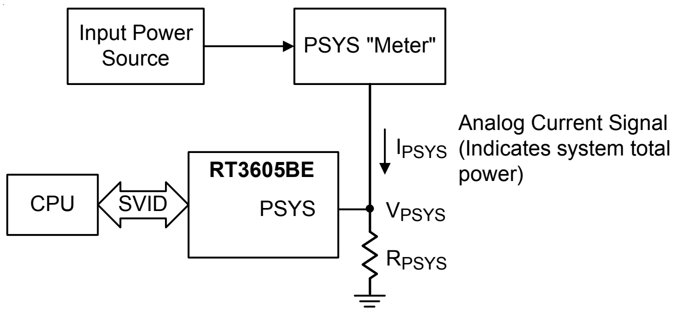


Figure 23. PSYS Function Block Diagram

Acoustic Noise Suppression

The RT3605BE supports acoustic noise suppression function for reducing acoustic noise induced by Piezoelectric Effect from MLCC. As output voltage transition, especially in Dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band and the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3605BE adopts acoustic noise suppression function which is enabled by pulling Pin 29 pull to VCC to reduce ΔV when SetVID Decay down in DEM mode.

Over-Current Protection (OCP)

The RT3605BE has three OCP mechanisms, sum OCP, per phase OCP, and OC limit.

Sum OCP

The threshold of sum OCP for PS0 is defined as

$$I_{SUM\_OC,PS0} = K_{SOCP} \times VIMON_{ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$$

PS1/2/3 sum OCP is defined as

$$I_{SUM\_OC,PS1} = \frac{1}{\text{phase number}} \times K_{SOCP} \times VIMON_{ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}} \text{ when ICCMAX} \geq 40A$$

$$I_{SUM\_OC,PS1} = K_{SOCP} \times VIMON_{ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}} \text{ when ICCMAX} < 40A$$

While $R_{IMON,EQ}$ is designed exactly for

$$VIMON_{ICCMAX} = I_{CC}\_\text{Max register}(21h) \text{ value} \times \frac{DCR}{R_{CSx}} \times R_{IMON,EQ}$$

$I_{CC}\_\text{Max register}(21h)$ value = ICCMAX, and

$$VIMON_{ICCMAX} = 0.8V \text{ when ICCMAX} \geq 40A$$

$$VIMON_{ICCMAX} = 0.4V \text{ when ICCMAX} < 40A$$

And K_{SOCP} is sum OCP ratio which value is 1.6. For MAIN rail, K_{SOCP} can be set to 1.3 by Pin Setting Function of the TSEN_AUXI pin. When ICCMAX<40A, K_{SOCP} always keeps 1.6.

SUM OCP threshold can be simplified as $I_{SUM\_OC,PS0}$ = K_{SOCP} x ICCMAX and $\frac{1}{\text{phase number}} \times K_{SOCP} \times ICCMAX$. Note that the modification of ICCMax register (21h) value cannot change sum OCP threshold. While inductor current above sum OCP threshold lasts 40μs, controller will de-assert VR_READY and latch PWM in tri-state to turn off high-side and low-side power MOSFETs.

OCP_SUM is masked during DVID period and 80μs after VID settles. They are also masked while VID = 0V.

Over-Voltage Protection (OVP)

The OVP threshold is linked to VID. The classification table and waveform are illustrated in Table 26 and Figure 24. While VID = 0V, in case of VR internal setting mode or DACOFF or PS4, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, OVP threshold is 1.85V to allow not-fully-discharged VSEN. Otherwise, the OVP threshold is relative to VID and equals to VID+350mV with minimum limit = 1.35V. While VID<1V, the OVP threshold is limited at 1.35V.

The OV protection mechanism is illustrated in Figure 25. When OVP is triggered with 1μs filter time, controller de-asserts VR_READY and forces all PWMs low to turn on low-side power MOSFETs. PWMx remains low until the output voltage is pulled down below VID. After 60μs from OVP trigger, the VID starts to ramp down to 0V with slow slew rate. During the period, the PWMx is not allowed to turn on. Controller controls PWM to be low or tri-state to pull down the output voltage along with VID.

Table 26. Summary of Over-Voltage Protection

VID Condition	OVP Threshold	Example	Protection Action	Protection Reset
VID=0 (VRON=L or VR internal setting mode or DACOFF or PS4)	OVP is masked		PGOOD latched low. Actively pulls the output voltage to below VID value, then ramp down to 0V	VCC or VRON Toggle
DVID up period from 0V to 1st PWM pulse after VID settles	1.85V			
DVID period from non-zero VID	VID+350mV minimum threshold=1.35V	VID=1.2V, OVP threshold=1.55V VID=0.9V, OVP threshold=1.35V		
VID ≠ 0	VID+350mV minimum threshold=1.35V			

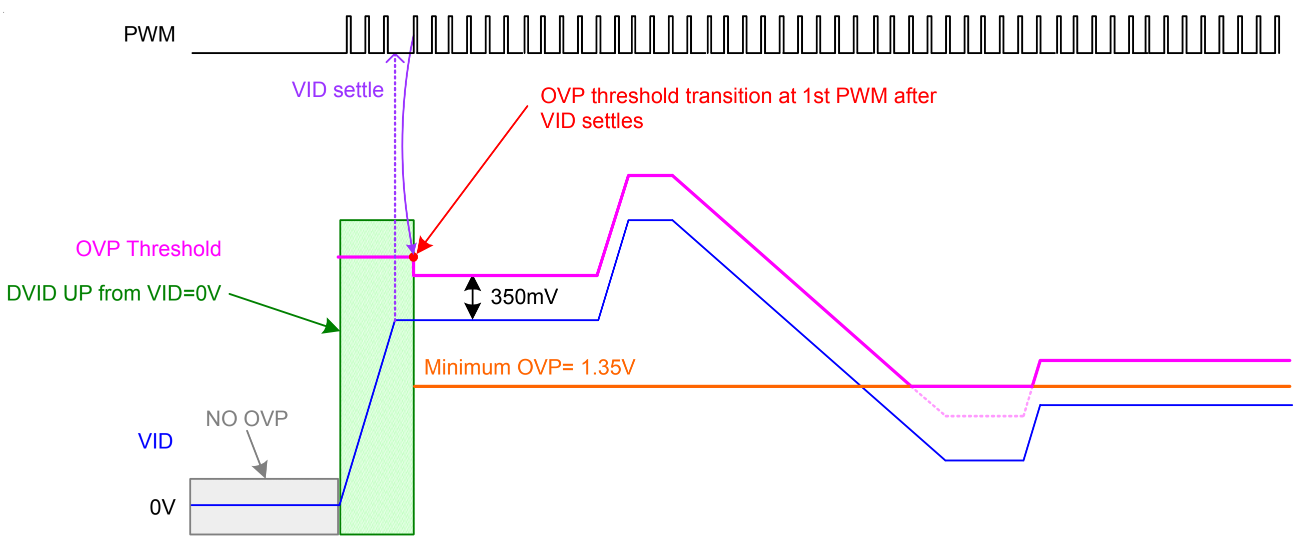


Figure 24. Timing Chart for Over-Voltage Threshold

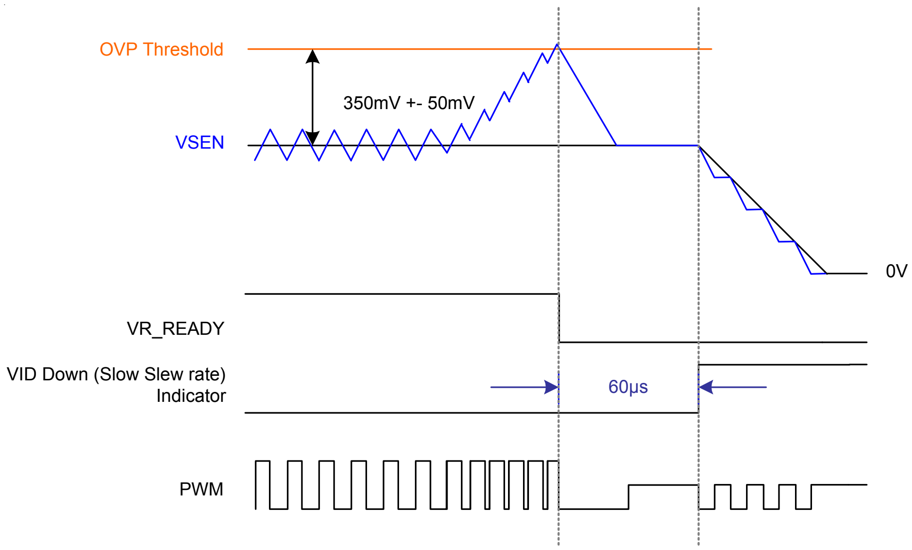


Figure 25. Over-Voltage Protection Mechanism

Under-Voltage Protection

When the output voltage is lower than VID-450mV with 3µs filter time, the UVP will be triggered and all PWM will be in tri-state to turn off high-side and low-side power MOSFETs. The UVP is masked during DVID period and 80µs after VID settles. The mechanism is illustrated in Figure 26.

All protections are reset by VCC or VRON toggle. The UVP and OCP protections are listed in Table 27.

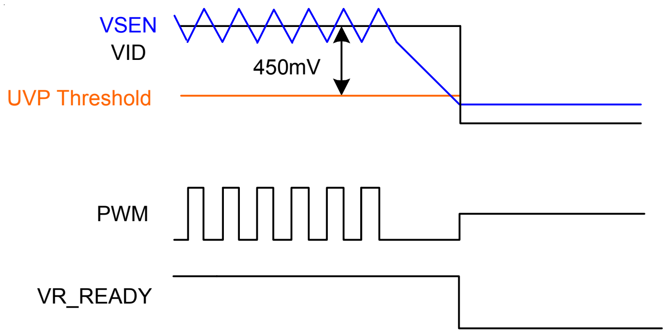


Figure 26. Under-Voltage Mechanism

Table 27. Summary of UVP and OCP Protection

Protection Type	Protection Threshold	Protection Action	DVID Mask Time	Protection Reset
Sum OC for PS0	$I_{SUM\_OC,PS0} = K_{SOCP} \times VIMON_{ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$	PWM tri-state, PGOOD latched low	DVID+80µs	VCC or VRON Toggle
Sum OC for PS1/PS2/PS3	$I_{SUM\_OC,PS1} = \frac{1}{\text{phase number}} \times K_{SOCP} \times VIMON_{ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$			
UV	VID-450mV			

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-52L 6x6, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (26.5°C/W) = 3.77W for a WQFN-52L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 27 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

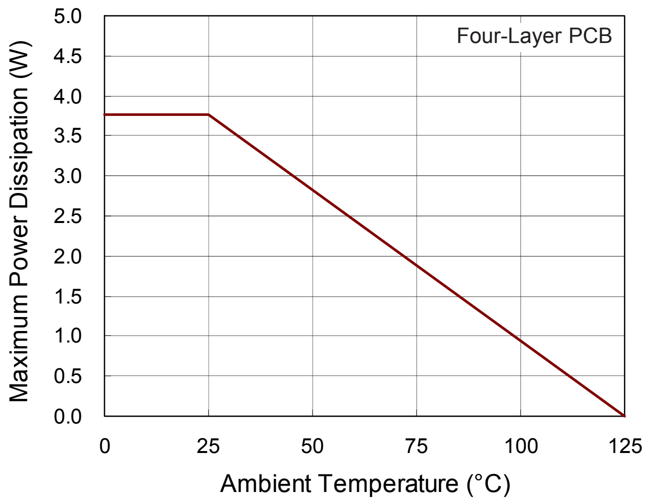
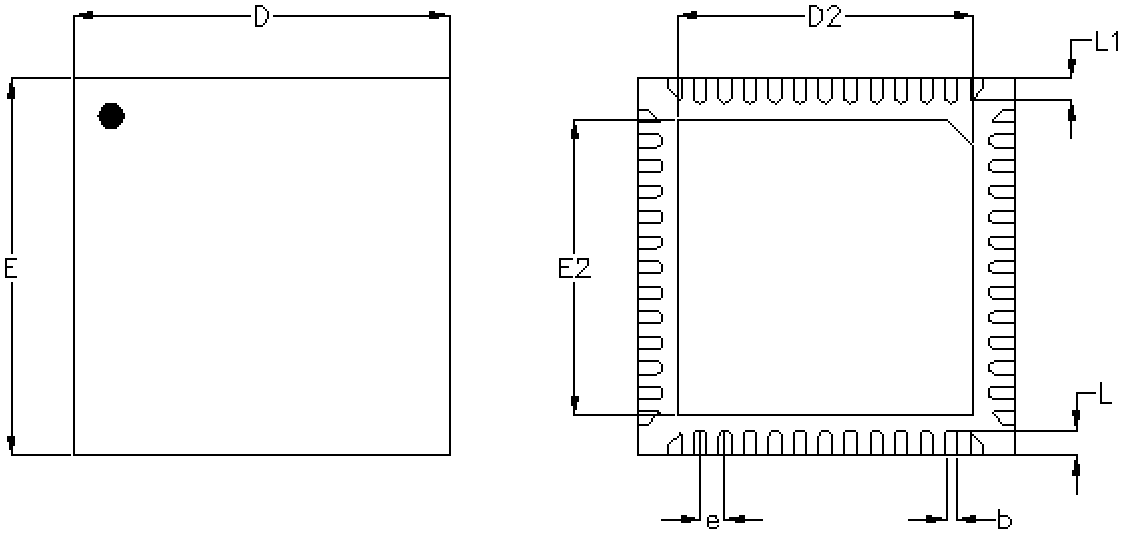
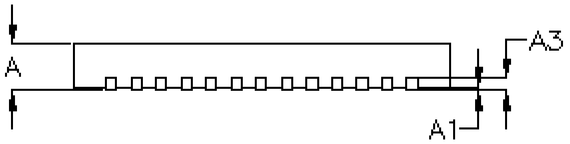
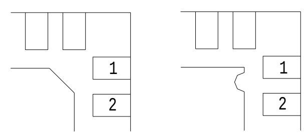


Figure 27. Derating Curve of Maximum Power Dissipation

Outline Dimension







DETAIL A

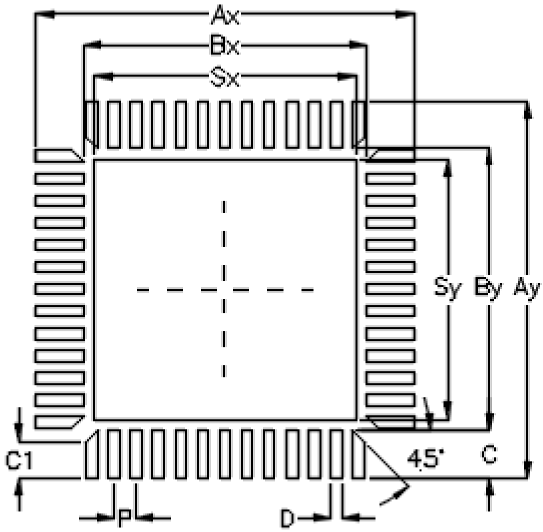
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*52	C1*8	D	Sx	Sy	
V/W/U/XQFN6*6-52	52	0.40	6.80	6.80	5.10	5.10	0.85	0.65	0.20	4.70	4.70	±0.05

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Datasheet Revision History

Version	Date	Item	Description
P00	2018/8/8		First Edition
P01	2018/10/29	General Description Marking Information Pin Configuration Typical Application Circuit	Modify
P02	2018/11/14	Pin Configuration Typical Application Circuit Absolute Maximum Ratings Recommended Operating Conditions Electrical Characteristics	Modify
P03	2018/11/29	Recommended Operating Conditions Electrical Characteristics	Modify
P04	2019/2/15	Functional Pin Description Functional Block Diagram Absolute Maximum Ratings Operation Electrical Characteristics Application Information	Modify
P05	2019/6/26	Functional Block Diagram Absolute Maximum Ratings Electrical Characteristics Application Information	Modify
P06	2019/10/3	General Description Features Functional Pin Description Operation Electrical Characteristics Typical Operating Characteristics Application Information	Modify
P07	2019/11/8	Operation Application Information	Modify