

2-Phase PWM Controller with Dual Integrated Drivers for IMVP9 CPU Core Power Supply

General Description

The RT3612EB is a 2/1 phase synchronous buck controller designed to meet Intel IMVP9 compatible CPU specification with a serial VID control interface. The RT3612EB adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3612EB features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and reduce output capacitors. The RT3612EB supports mode transition function with various operating states. A serial VID (SVID) interface is built in the RT3612EB to communicate with Intel IMVP9 compliant CPU. The RT3612EB supports VID on-the-fly function with three different slew rates: Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT3612EB varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0V to 2.74V with 10mV per step. The RT3612EB integrates a high accuracy ADC for platform and function settings, such as ICCMAX, switching frequency, over-current threshold and AQR trigger level. The RT3612EB provides VR Ready and thermal indicators. It also features complete fault protection functions including over-voltage (OV), under-voltage (UV), over-current (OC) and under-voltage lockout (UVLO).

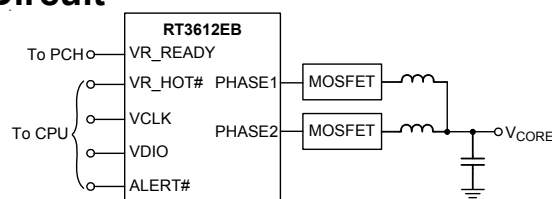
Features

- Intel IMVP9 Serial VID Interface Compatible Power Management States
- 2/1 Phase PWM Controller and 2 Embedded MOSFET Drivers
- G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology
- 0.5% DAC Accuracy
- Differential Remote Voltage Sensing
- Built-in ADC for Platform Programming and Reporting
- Accurate Current Balance
- System Thermal Compensated AVP
- Diode Emulation Mode at Light Load Condition
- Fast Transient Response-Adaptive Quick Response (AQR)
- VR Ready Indicator
- Thermal Monitoring and Indicator
- Current Monitoring
- IMVP9 System Input Power Monitoring
- OVP, OCP, UVLO, UVP
- Switching Frequency Range Setting
- Slew Rate Setting
- DVID Enhancement
- Acoustic Noise Suppression
- Small 32-Lead WQFN Package

Applications

- IMVP9 Intel Core Supply
- Notebook Computer Multi-Phase CPU Core Supply
- AVP Step-Down Converter

Simplified Application Circuit



Ordering Information

RT3612EB □ □

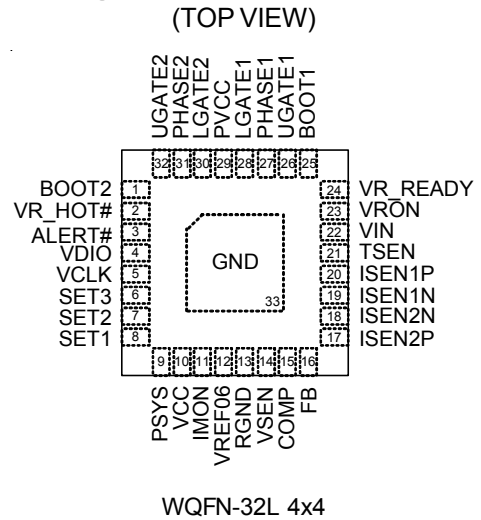
- Package Type
QW : WQFN-32L 4x4 (W-Type)
- Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

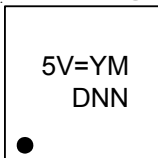
Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



Marking Information



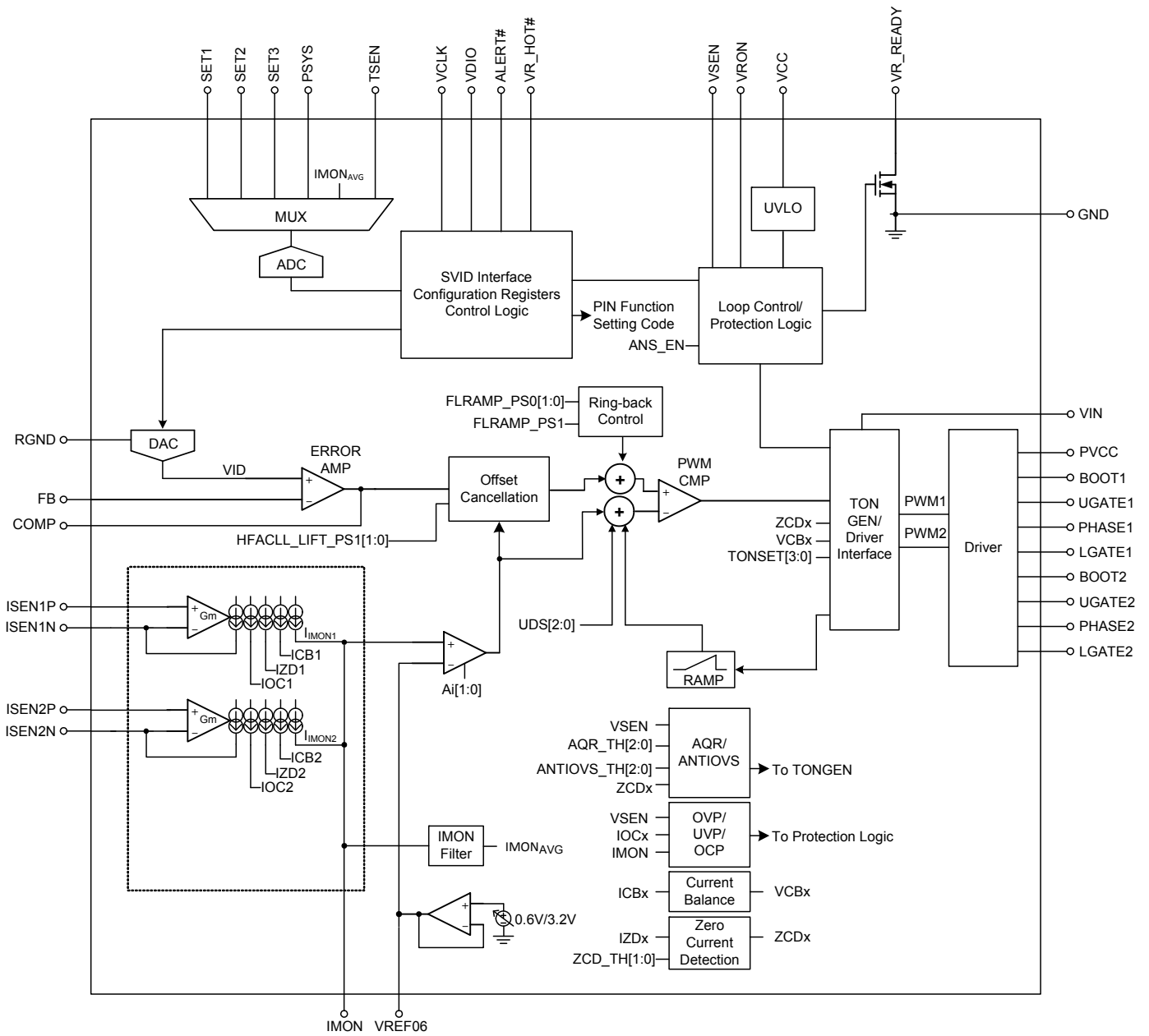
5V= : Product Code
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
25, 1	BOOT[1:2]	Bootstrap supply for high-side gate MOSFET driver.
2	VR_HOT#	Thermal monitor output. (Active low).
3	ALERT#	SVID alert. (Active low).
4	VDIO	VR and CPU data transmission interface.
5	VCLK	Synchronous clock from the CPU.
6	SET3	Function settings for loop response speed-up adaptive quick response (AQR) trigger level, zero current detection, sum OCP ratio and undershoot suppression.
7	SET2	Function settings for anti-overshoot trigger level, current gain (Ai), DVID fast slew rate, acoustic noise suppression and high frequency ACLL voltage compensation in PS1.
8	SET1	Function settings for ICCMAX, TON width setting (switching frequency) and VBOOT. Connect the SET1 pin to 5V and turn on the VRON pin, if the soldering is good, the output voltage is 1.8V.
9	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible.
10	VCC	Controller power supply. Connect this pin to 5V and place an RC filter, R = 6.2Ω and C = 4.7μF. The decoupling capacitor should be as close as physically possible to the VCC pin.
11	IMON	Current monitor output for controller. This pin outputs a voltage proportional to the output current.

Pin No.	Pin Name	Pin Function
12	VREF06	Voltage source output. During controller internal setting period, it outputs 3.2V. In normal operation, it outputs 0.6V to offset IMON signal. While controller shuts down or in PS4, voltage source shuts down. An exact 0.47 μ F capacitor and 3.9 Ω resistor from this pin to GND are required for stability.
13	RGND	Return ground. This pin is the negative input of output voltage differential remote sense.
14	VSEN	Voltage sense input. This pin is connected to the terminal of controller output voltage.
15	COMP	Error amplifier output pin.
16	FB	Negative input of the error amplifier. This pin is for output voltage feedback to controller.
20, 17	ISEN[1:2]P	Positive current sense inputs of channel 1 and 2.
19, 18	ISEN[1:2]N	Negative current sense inputs of channel 1 and 2.
21	TSEN	Thermal sense input and function settings for advanced ramp magnitude in PS1, advanced ramp magnitude in PS0, zero loadline enable and DVID voltage compensation.
22	VIN	Input voltage pin. Connect an RC filter whose time constant need less than switch period for sensing input voltage.
23	VRON	Controller enable pin. A logic high signal enables the controller.
24	VR_READY	VR ready indicator.
26, 32	UGATE[1:2]	High-side driver output. Connect the pin to the gate of high-side MOSFET.
27, 31	PHASE[1:2]	Switch node of high-side driver. Connect the pin to high-side MOSFET source together with the low-side MOSFET drain and inductor.
28, 30	LGATE[1:2]	Low-side driver output. This pin drives the gate of low-side MOSFET.
29	PVCC	Driver power supply input. Connect this pin to 5V and place a minimum 2.2 μ F ceramic capacitor.
33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

G-NAVP™ Control Mode

The RT3612EB adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy loadline design and provide high DC accuracy and fast transient response. When sensed current signal reaches sensed voltage signal, the RT3612EB generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage, that is inverted and amplified signal of output voltage. While current loading is increasing, referring to Figure 1, COMP rises due to output voltage droop. Then rising COMP forces PWM turn on earlier and closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage and corresponding output voltage is in the steady state of lower voltage. The loadline, output voltage drooping by an amount proportional to loading current, is achieved.

SVID Interface/Control Logic/Configuration

Registers

SVID Interface receives or transmits SVID signal with CPU. Control Logic executes command (Read/Write registers, setVID, setPS) and sends related signals to control VR. Configuration Registers include function setting registers and CPU required registers.

IMON Filter

IMON Filter is used to average current signal by analog low-pass filter. It outputs IMON_{AVG} to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs of SET1, SET2, SET3, TSEN, PSYS and IMON_{AVG}. The ADC converts these analog signals to digital codes for reporting or function settings.

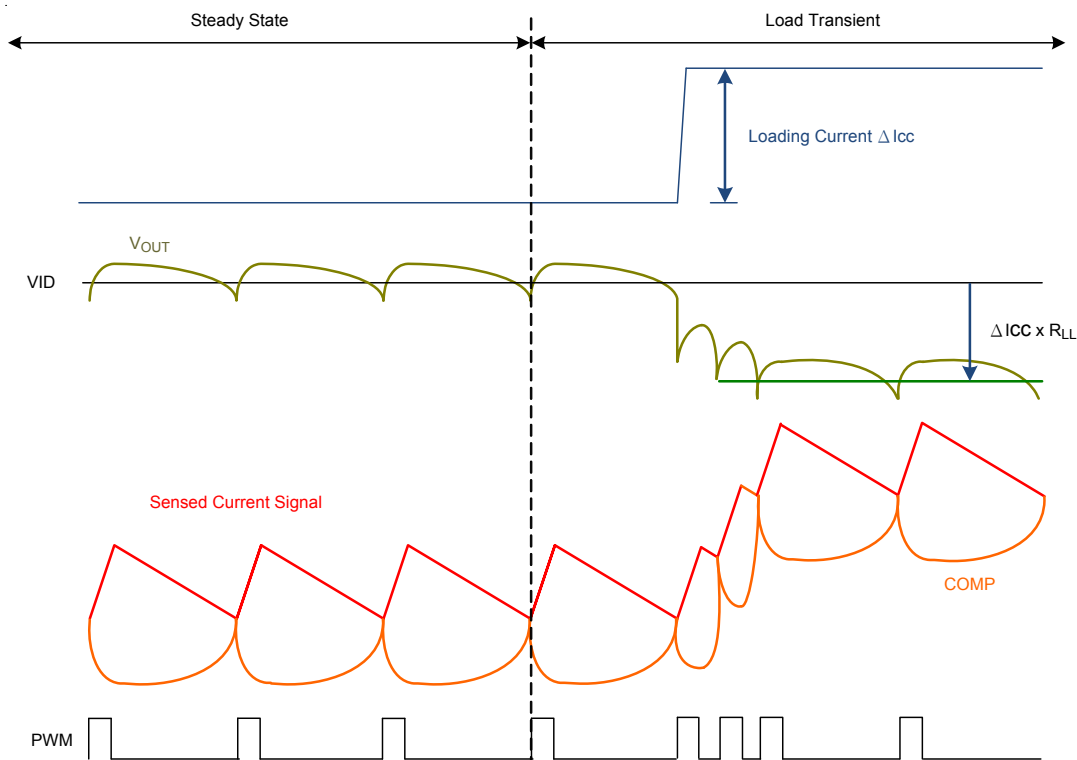


Figure 1. G-NAVP™ Behavior Waveform

UVLO

Detects the VCC voltage. As VCC overs threshold, controller issues POR = high and waits VRON. After both POR and VRON are ready, then controller is enabled.

Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition, and PWM sequence.

DAC

Generates a reference VID voltage according to the VID code sent by Control Logic. According to setVID command, Control Logic dynamically changes VID voltage to the target with required slew rate.

ERROR AMP

Inverts and amplifies the difference between output voltage and VID with externally set finite DC gain. The output signal is COMP for PWM trigger.

PER CSGM

Senses per-phase inductor current. The outputs are used for loop response, current balance, zero current detection, current reporting and over-current protection.

SUM CSGM

Senses total inductor current with R_{MON} gain adjustment. SUM CSGM output current ratio can also be set by PIN-SETTING (Ai[1:0]). It helps wider application range of DCR and load line. SUM CSGM output is used for PWM trigger.

RAMP

RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal and sum current signal based on RAMP to trigger PWM.

Offset Cancellation

Cancel the current signal/comp voltage ripple issue to control output voltage accuracy.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

Zero Current Detection

Detects whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (Anti-overshoot function).

AQR/ANTIOVS

AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWM to turn on. PWM pulse width triggered by AQR is adaptive to loading level. AQR trigger level can be set by PIN-SETTING. ANTIOVS can help overshoot reduction which detects loading falling edge and forces all PWM in tri-state until the zero current is detected.

TONGEN/Driver Interface

PWM comparator output signal triggers TONGEN to generate PWM pulse. The PWM sequence is controlled by loop control. PWM pulse width is determined by frequency setting, current balance output and adaptive quick response (AQR) settings. Once AQR is triggered, VR allows all PWM to turn on at the same time. Driver Interface provides high/low/tri-state to drive external driver. In power saving mode, driver interface force PWM in tri-state to turn off high side and low side power MOSFET according to zero current detection output. In addition, PWM state is controlled by protection logic. Different protections force required PWM state.

OVP/UVP/OC

Over-voltage protection/Under-voltage protection/Over-current protection.

Absolute Maximum Ratings (Note 1)

• VIN to GND	-----	-0.3V to 28V
• VCC to GND	-----	-0.3V to 6.5V
• RGND to GND	-----	-0.3V to 0.3V
• PVCC to GND	-----	-0.3V to 6.5V
• BOOTx to PHASEx		
DC	-----	-0.3V to 6.8V
< 100ns	-----	-5V to 7.5V
• PHASEx to GND		
DC	-----	-0.3V to 32V
< 100ns	-----	-10V to 38V
• UGATEx to PHASEx		
DC	-----	-0.3V to 6.8V
< 100ns	-----	-5V to 7.5V
• LGATEx to GND		
DC	-----	-0.3V to 6.8V
< 100ns	-----	-2.5V to 7.5V
• Other Pins	-----	-0.3V to 6.8V
• Power Dissipation, P _D @ T _A = 25°C		
WQFN-32L 4x4	-----	3.59W
• Package Thermal Resistance (Note 2)		
WQFN-32L 4x4, θ _{JA}	-----	27.8°C/W
WQFN-32L 4x4, θ _{JC}	-----	7°C/W
• Junction Temperature	-----	150°C
• Lead Temperature (Soldering, 10 sec.)	-----	260°C
• Storage Temperature Range	-----	-65°C to 150°C
• ESD Susceptibility (Note 3)		
HBM (Human Body Model)	-----	2kV

Recommended Operating Conditions (Note 4)

• VIN to GND	-----	4.5V to 24V
• Supply Input Voltage, VCC	-----	4.5V to 5.5V
• Junction Temperature Range	-----	-10°C to 105°C

Electrical Characteristics

(V_{CC} = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from -10°C to 105°C, unless other noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input							
Supply Voltage		V _{CC}		4.5	5	5.5	V
Supply Current		I _{VCC}	VRON = H, not switching	--	6.5	--	mA
Supply Current at PS4		I _{VCC_PS4}	VRON = H, not switching	--	0.08	0.097	mA
Shutdown Current		I _{SHDN}	VRON = L	--	--	10	μA
Slew Rate							
Dynamic VID Slew Rate	Fast Slew Rate	SR (Y/U/H-line)	SetVID fast	48	--	--	mV/μs
	Slow Slew Rate		SetVID slow, slew rate default = 1/4 fast	12	--	--	
EA Amplifier							
DC Gain		A _{DC}	R _L = 47kΩ	70	--	--	dB
Gain-Bandwidth Product		GBW	C _{LOAD} = 5pF	--	5	--	MHz
Slew Rate		S _{REA}	C _{LOAD} = 10pF (Gain = -4, R _f = 47kΩ, V _{OUT} = 0.5V to 3V)	5	--	--	V/μs
Output Voltage Range		V _{COMP}	R _L = 47kΩ	0.3	--	3.6	V
Maximum Source/Sink Current		I _{OUTEA}	V _{COMP} = 2V	--	5	--	mA
Input Offset Voltage		V _{OSEA}	T _A = 25°C	-3		3	mV
Current Sensing Amplifier							
Input Offset Voltage		V _{OCS}		-0.6	--	0.6	mV
Impedance at Positive Input		R _{ISENXP}		1	--	--	MΩ
CS Input Voltage		V _{CSIN}	Differential voltage range of DCR sense. (V _{CSIN} = Inductor current x DCR x DCR divider)	-10	--	100	mV
Current Sense Gain Error		A _{MIRROR}	Internal current mirror gain of per phase current sense I _{MON} / I _{CS,PERx}	0.97	1	1.03	A/A
TON Setting							
On-Time Setting		t _{ON}	V _{IN} = 19V, V _{VID} = 1.8V, K _{TON} = 1.36	--	165	--	ns
Minimum Off-Time		t _{OFF}	V _{DAC} = 1.8V under PS1 condition	--	150	--	ns
Protections							
Under-Voltage Lockout Threshold	V _{UVLO}	Falling edge		3.9	4.1	4.3	V
	ΔV _{UVLO}	Rising edge hysteresis		100	170	250	mV
Over-Voltage Protection Threshold	V _{Ov}	Respect to VID voltage, VID > 1.88V		VID + 300	VID + 350	VID + 400	mV
		VID ≤ 1.88V		--	2.23	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Under-Voltage Protection Threshold	V _{UV}	Respect to VID voltage	-760	-660	-550	mV	
VRON and VR_READY							
VRON Threshold	Logic-High	V _{IH}	0.7	--	--	V	
	Logic-Low	V _{IL}	--	--	0.3		
Leakage Current of VRON			-1	--	1	μA	
VR_READY Pull Low Voltage	V _{V_R_READY}	I _{V_R_READY} = 10mA	--	--	0.13	V	
Serial VID and VR_HOT#							
VCLK, VDIO Input Voltage	Logic-High	V _{IH}	Respect to INTEL spec. with 50mV hysteresis	0.65	--	--	V
	Logic-Low	V _{IL}		--	--	0.45	
Leakage Current of VCLK and VDIO		I _{LEAK_IN}		-1	--	1	μA
Pull Low Voltage		V _{VDIO}	I _{VDIO} = 10mA	--	--	0.13	V
		V _{ALERT#}	I _{ALERT#} = 10mA				
		V _{V_R_HOT#}	I _{V_R_HOT#} = 10mA				
Leakage Current of ALERT#, VR_HOT#		I _{LEAK_OUT}		-1	--	1	μA
VREF							
VREF06 Voltage	V _{VREF06}	Normal operation	0.59	0.6	0.61	V	
ADC							
Digital IMON Set	dV _{IMONICCMAX}	V _{IMON} - V _{VREF06} = 1.6V	--	255	--	Decimal	
PSYS Maximum Input Voltage	PSYS	V _{PSYS} = 1.6V	--	255	--	Decimal	
Average Period of IMON	t _{IMON}		--	200	--	μs	
ADC							
VR_Hot# Assert Threshold	V _{TSEN}	Falling	--	1.092	1.118	V	
VR_Hot# De-Assert Threshold		Rising	1.106	1.132	1.16		
Thermal ALERT# Assert Threshold		Falling, thermal alert status1 register bit 1 assert	1.106	1.132	1.16		
Thermal ALERT# Assert Threshold		Falling, thermal alert status1 register bit 1 de-assert	1.148	1.176	1.207		
Average Period of TSEN	t _{TSEN}		--	800	--	μs	
I_{TSEN}							
TSEN Source Current	I _{TSEN}	V _{TSEN} = 1.6V, T _A = 25°C	79.2	80	80.8	μA	
Internal BOOT Switch							
Internal Boot Switch On Resistance	R _{BOOT}	V _{CC} to BOOT, 10mA	--	--	80	Ω	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Time						
UGATEx Rise Time	tUGATEr	3nF load	--	8	--	ns
UGATEx Fall Time	tUGATEf	3nF load	--	8	--	ns
LGATEx Rise Time	tLGATEr	3nF load	--	8	--	ns
LGATEx Fall Time	tLGATEf	3nF load	--	4	--	ns
UGATEx Turn-On Propagation Delay	tPDHU	Outputs unloaded	--	20	--	ns
LGATEx Turn-On Propagation Delay	tPDHL	Outputs unloaded	--	20	--	ns
Output						
UGATEx Driver Source Resistance	RUGATEsr	100mA source current	--	1	--	Ω
UGATEx Driver Source Current	IUGATEsr	VUGATE – VPHASE = 2.5V	--	2	--	A
UGATEx Driver Sink Resistance	RUGATEsk	100mA sink current	--	1	--	Ω
UGATEx Driver Sink Current	IUGATEsk	VUGATE – VPHASE = 2.5V	--	2	--	A
LGATEx Driver Source Resistance	RLGATEsr	100mA source current	--	1	--	Ω
LGATEx Driver Source Current	ILGATEsr	VLGATE = 2.5V	--	2	--	A
LGATEx Driver Sink Resistance	RLGATEsk	100mA sink current	--	0.5	--	Ω
LGATEx Driver Sink Current	ILGATEsk	VLGATE = 2.5V	--	4	--	A

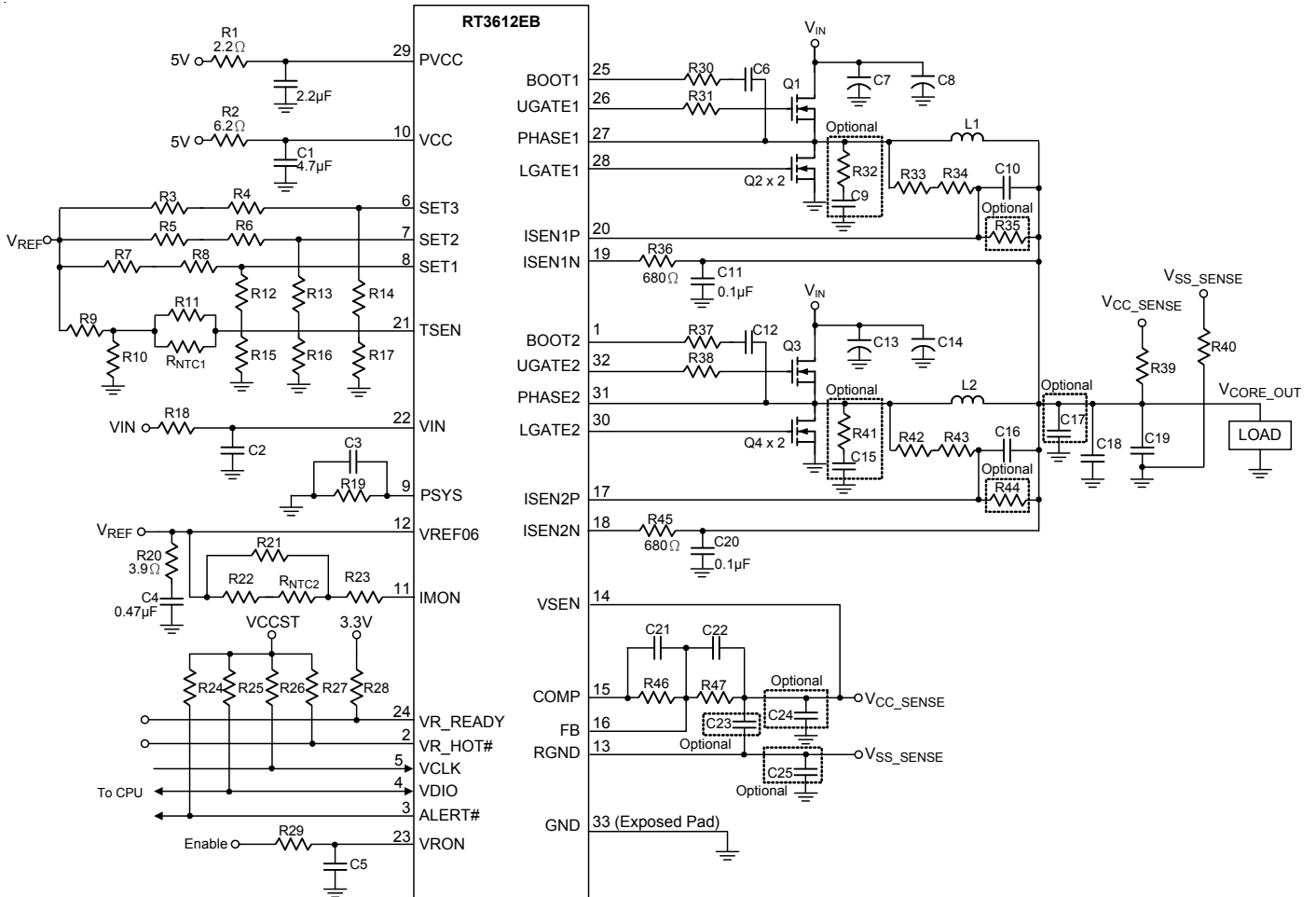
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

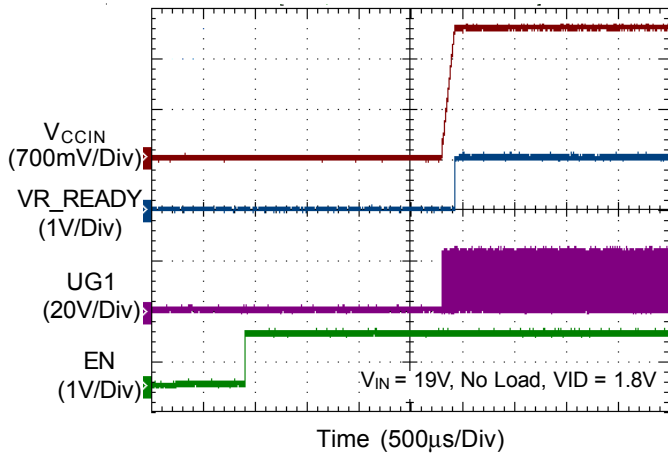
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

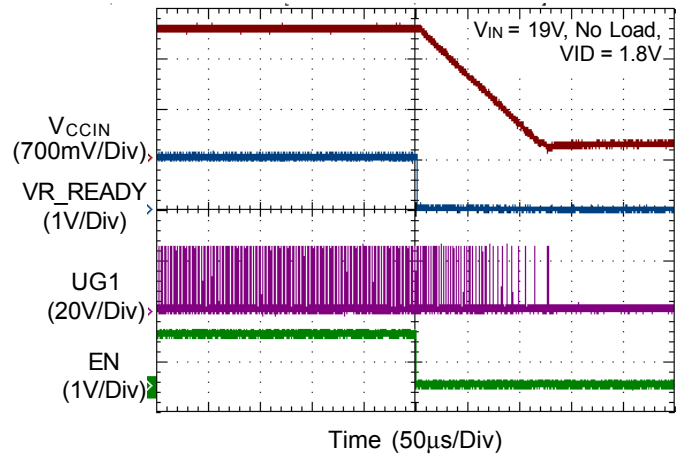


Typical Operating Characteristics

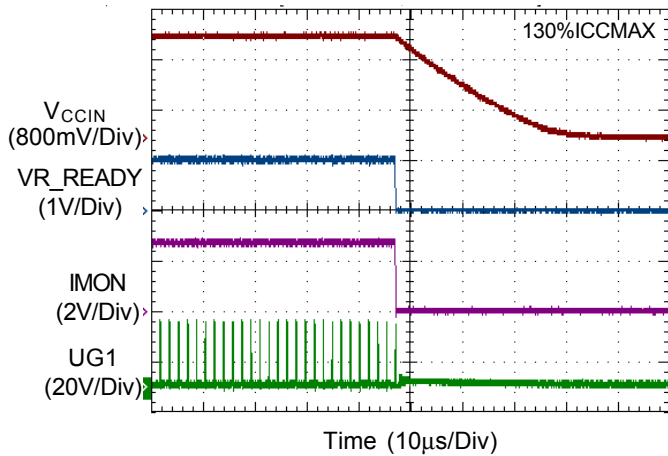
VR Power On from EN



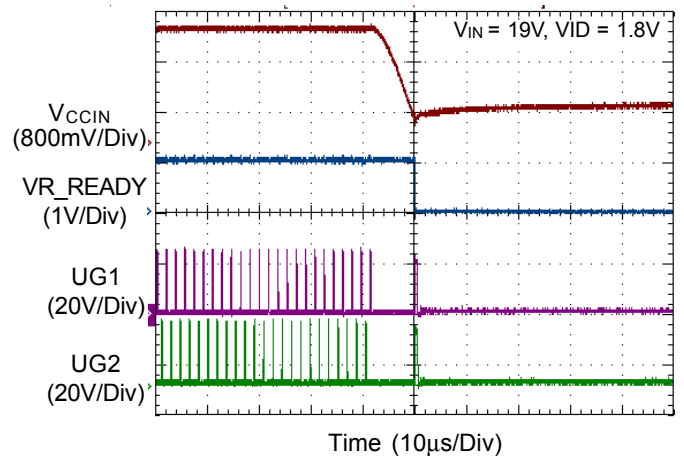
VR Power Off from EN



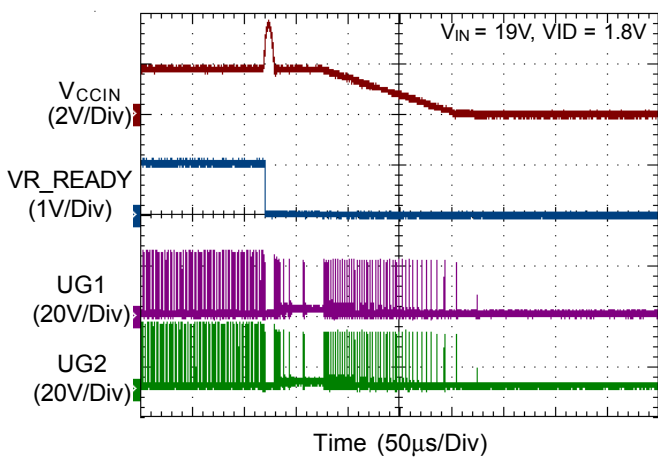
VR OCP



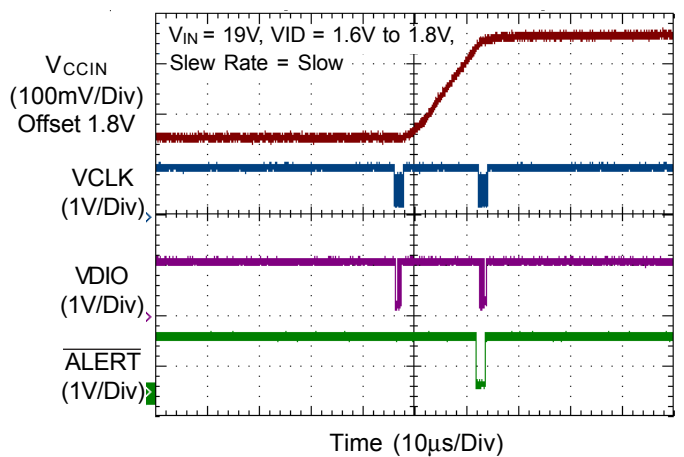
CORE VR UVP



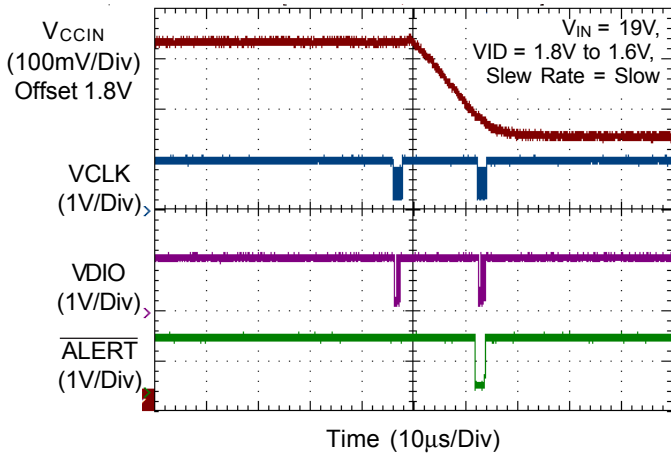
CORE VR OVP



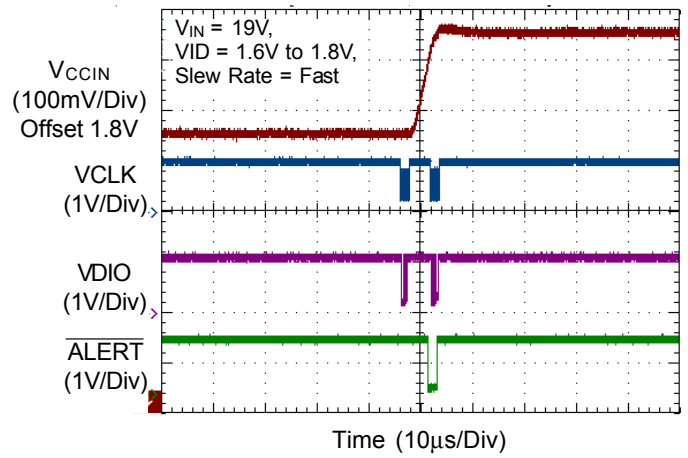
VR Dynamic VID Up



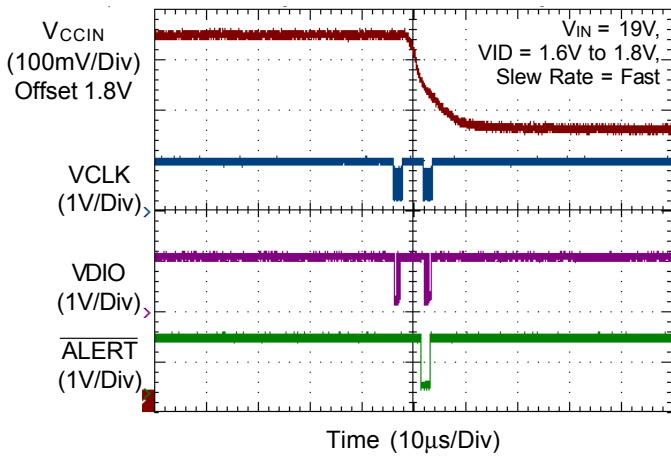
VR Dynamic VID Down



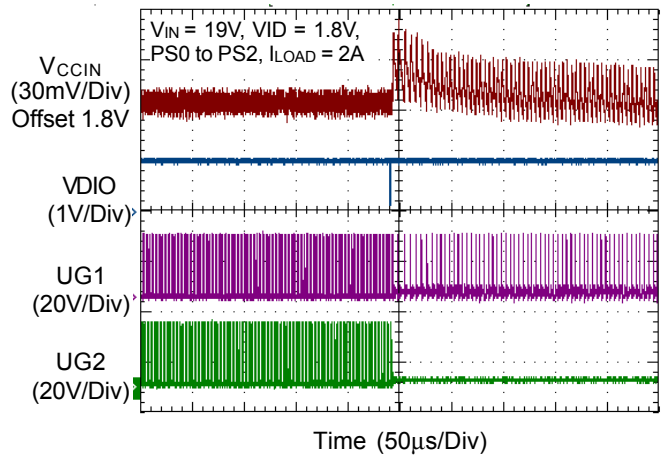
VR Dynamic VID Up



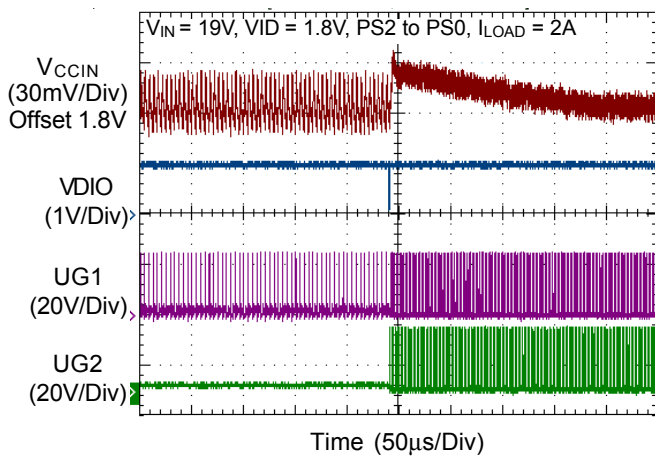
VR Dynamic VID Down



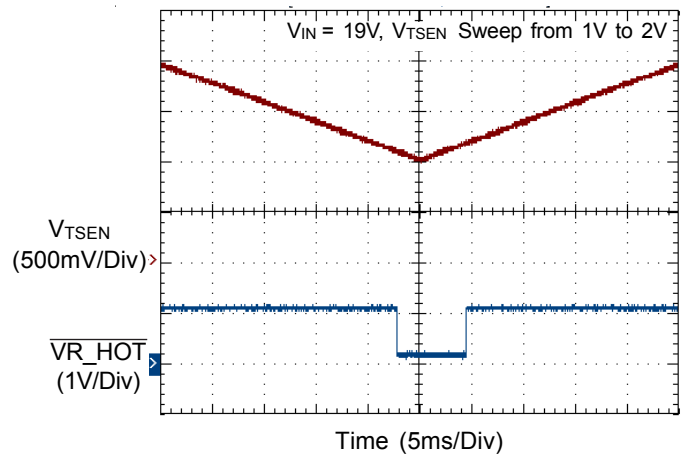
VR Mode Transient

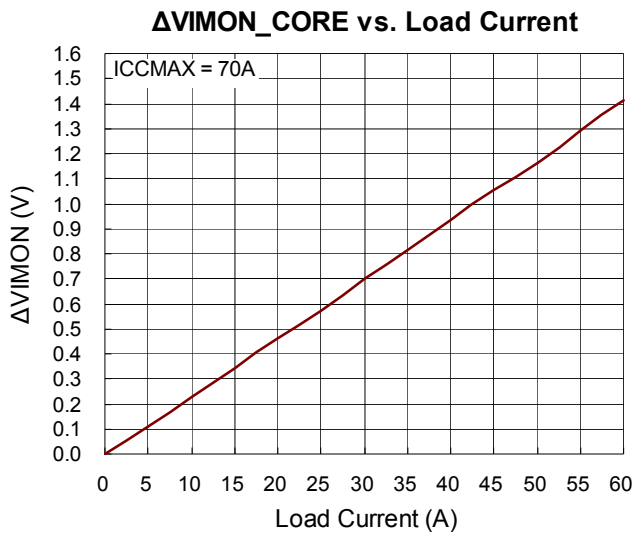


VR Mode Transient



Thermal Monitoring





Application Information

Power-ON Sequence

In order to confirm sufficient power supply for proper operation, the VR triggers UVLO if VCC pin drops below 4.3V (max). UVLO protection shuts down controller and forces high-side MOSFET and low-side MOSFET off. When $VCC > 4.45$, the RT3612EB issues POR = high and waits for VRON signal. After POR = high and $VRON > 0.7V$, controller powers on (Chip Enable = H) and starts VR internal settings, which include internal circuit offset correction and function settings (PIN-SETTING). Users

can set multi-functions through SETx and TSEN pins. Figure 2 shows the typical timing of controller power-on. After all internal settings are done and $VBOOT = 0V$, VR_READY asserts to inform system that controller is ready to communicate with CPU. If $VBOOT = 1.8V$, VR_READY asserts until DVID to VBOOT. VR_READY asserts within 2.5ms (max) after Chip Enable = H ($VRON = H$ and $VCC > 4.45V$). The pull-high power of VRON pin is recommended as 1.05V, the same power as SVID interface. That can ensure SVID power is ready while $VRON = H$. For the VR normal operation, VIN should be ready before VCC and VCC is strongly suggested to be ready before driver power(PVCC) to prevent current flowing back to VCC from PVCC through PWMx pin or DRVEN pin. Moreover, VRON must be the last one to asserts after both VCC and PVCC are ready (>UVLO).

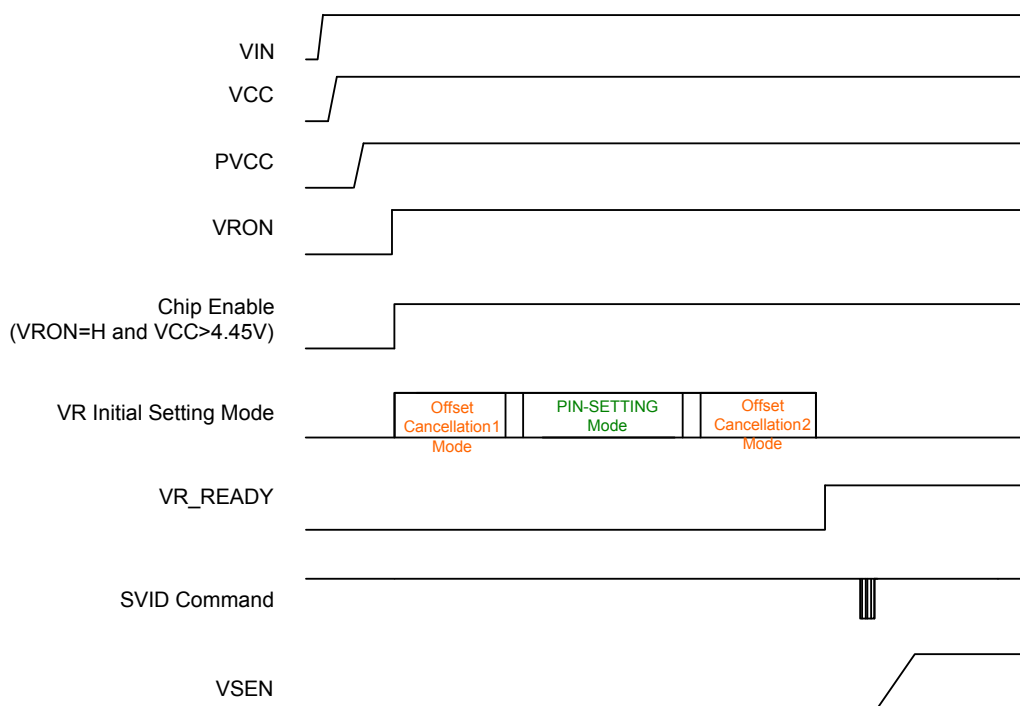


Figure 2. Typical Timing of Controller Power-On

Maximum Active Phases Number Setting

The number of active phases is determined by ISENxN voltages. The detection is only active and latched at Chip Enable rising edge (VRON = H and VCC > 4.45V). While voltage at ISENxN > (VCC - 0.7V), maximum active phase number is (x-1). For example, pulling ISEN2N to VCC programs a 1-phase operation. The unused ISENxP pins are recommended to connect to VCC and the unused PWM pins can be floating. Figure 3 is a 1-phase operation example, the pull up voltage of ISEN2N should be connected together with VCC of RT3612EB and the pull up resistor should be 10kΩ.

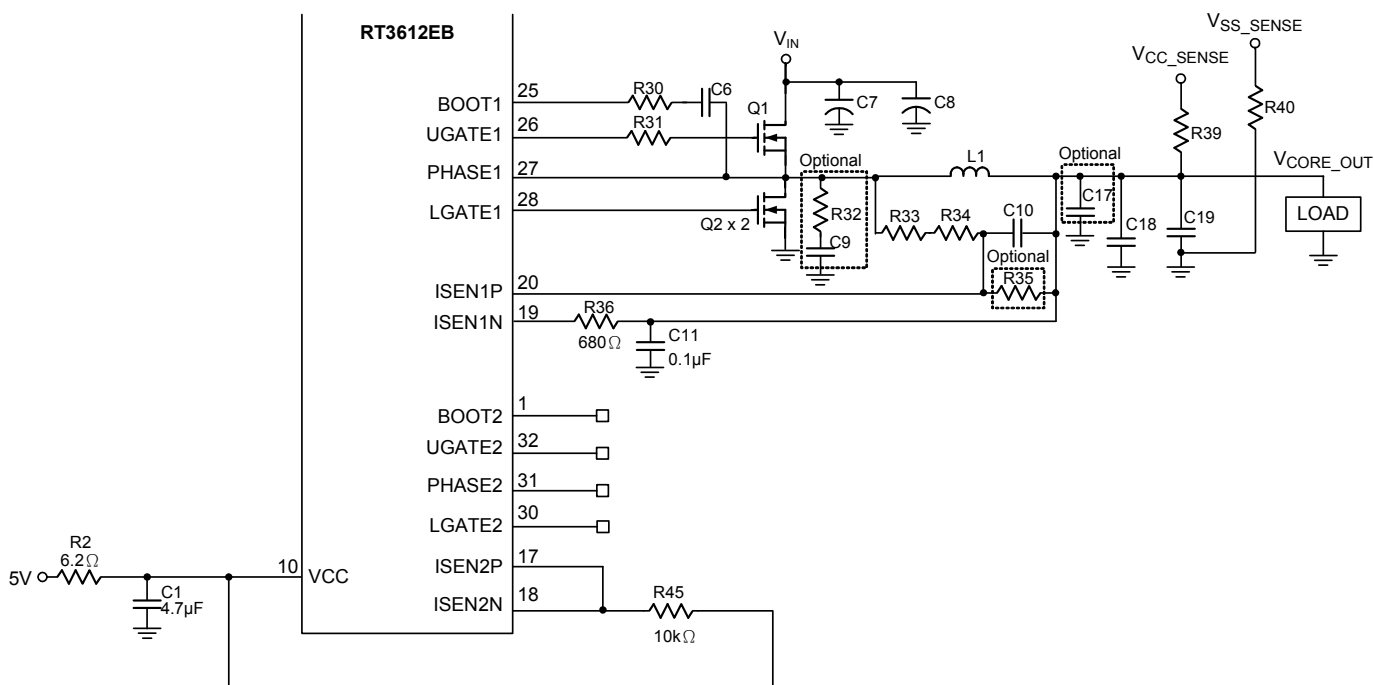


Figure 3. 1-Phases Operation Setting

PIN-SETTING Mechanism

The RT3612EB provides multiple parameters for platform setting and BOM optimization. These parameters can be set through SETx and TSEN pins. The RT3612EB adopts two-step PIN-SETTING mechanism to maximize IC pin utilization. Figure 4 shows the timing chart of PIN-SETTING mechanism. Figure 5 illustrates this operating mechanism for SETx.

The voltage at VREF06 pin ramps up to 3.2V after Chip Enable = H. First, external divider voltage is sensed as $V_{divider}$. ADC codes $V_{divider}$ and stores in the Divider-Register. Second, internal current $80\mu A$ sources the divider and generates another voltage as $V_{current}$. $V_{IXR} = (V_{current} - V_{divider})$ is coded and stored in the IXR-Register. $V_{divider}$ and $V_{current}$ can be represented as follows :

$$V_{divider} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{current} = \frac{R2}{R1+R2} \times 3.2V + 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

Divider-Register and IXR-Register set specified functions. For example, Divider-Register of SET1 sets ICCMAX and TON width setting; IXR-Register of SET1 sets TON width setting and VBOOT. All setting functions are summarized in Table 1.

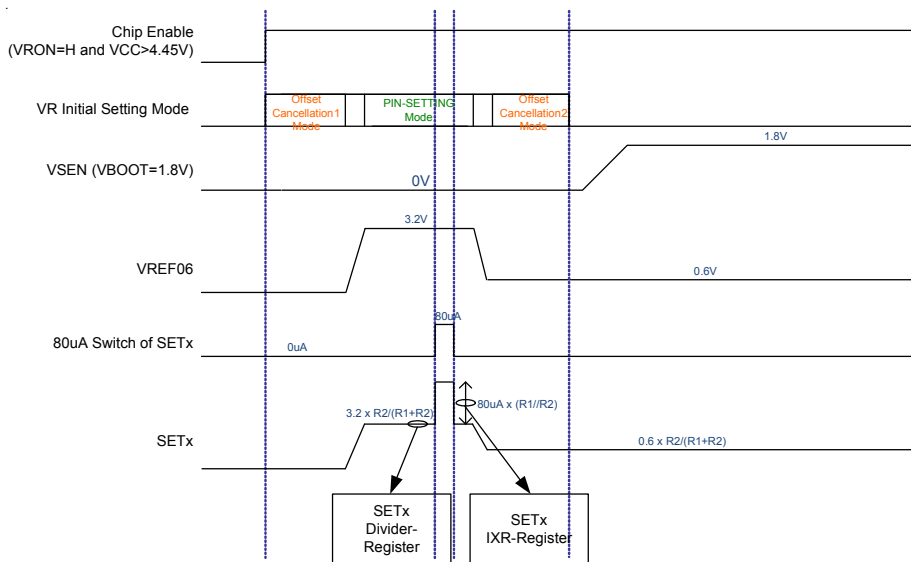


Figure 4. Timing Chart of PIN-SETTING Mechanism

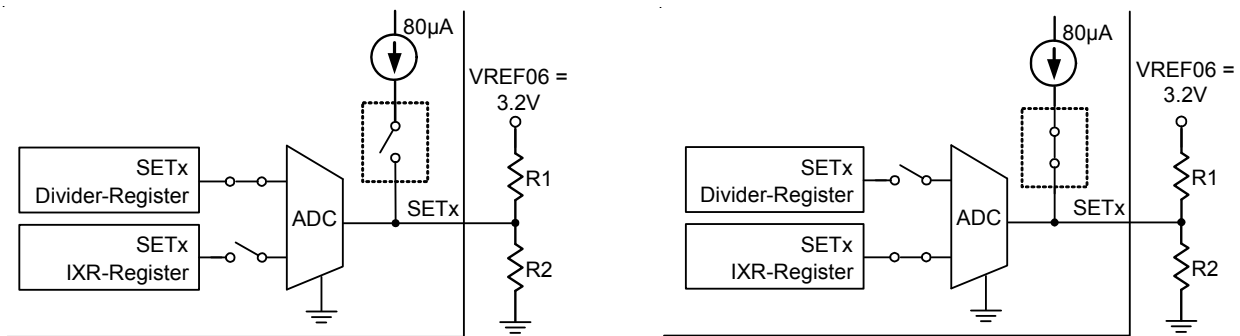


Figure 5. Operating Mechanism for SETx

Table 1. Summary of Pin Setting Functions

		Function Setting	Symbol	Description
SET1	Divider Register[4]	TON width setting (Switching frequency)	TONSET[3]	According to required frequency, to select TON width.
	Divider Register[3:0]	ICCMAX	ICCMAX[3:0]	According to platform, to set corresponding ICCMAX.
	IXR Register[4:2]	TON width setting (Switching frequency)	TONSET[2:0]	According to required frequency, to select TON width.
	IXR Register[1]	VBOOT	VBOOT_SET	VBOOT_SET= 0: VBOOT = 0V, wait for SVID command after controller power on. VBOOT_SET= 1: Automatically DVID to VBOOT=1.8V after controller power on.
SET2	Divider Register[4:2]	Anti-overshoot trigger level	ANTIOVS_TH[2:0]	ANTIOVS for reduction of overshoot at loading falling edge. To set trigger level.
	Divider Register[1:0]	Current gain	Ai[1:0]	Current gain setting
	IXR Register[4]	DVID fast slew rate	DVID Fast_SR	DVID Fast_SR = 0 : 48mV/us; for Y/U/H-line.
	IXR Register[3]	Acoustic noise suppression	ANS_EN	ANS_EN=0 : Disable. ANS_EN=1 : Enable. To reduce acoustic noise.
	IXR Register[2:1]	High frequency ACLL voltage compensation in PS1	HFACLL_LIFT_PS1[1:0]	To provide positive offset in high frequency ACLL.
SET3	Divider Register[4:2]	Adaptive quick response(AQR) trigger level	AQR_TH[2:0]	AQR for loop response speed-up of loading rising edge. To set trigger level.
	Divider Register[1:0]	Zero current detection threshold	ZCD_TH[1:0]	Detects whether each phase current crosses zero current. To set trigger level.
	IXR Register[4]	Sum OCP ratio	SUM_OC	SUM_OC = 0 : 160% x ICCMAX SUM_OC = 1 : 130% x ICCMAX
	IXR Register[3:1]	Undershoot suppression	UDS[2:0]	To improve undershoot by applying a positive offset at loading edge. To set trigger level.
TSEN	Divider Register[5]	Advanced ramp magnitude in PS1	FLRAMP_PS1	Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on.
	Divider Register[4:3]	Advanced ramp magnitude in PS0	FLRAMP_PS0[1:0]	Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on.
	Divider Register[2]	Zero load line	Zero LL_EN	Zero LL_EN = 0 : Disable zero load line. Zero LL_EN = 1 : Enable zero load line.
	Divider Register[1]	DVID voltage compensation level	DVID_LIFT	DVID_LIFT = 0 : Disable. DVID_LIFT = 1 : 5uA current source sinks from FB pin.

Referring to PIN-SETTING tables Table 2 to 7, users can search corresponding V_{divider} or V_{IXR} according to the desired function setting combinations. Then SETx external resistors can be calculated as follows :

$$R1 = \frac{3.2V \times V_{\text{IXR}}}{80\mu A \times V_{\text{divider}}}$$

$$R2 = \frac{R1 \times V_{\text{divider}}}{3.2V - V_{\text{divider}}}$$

Richtek provides a Microsoft Excel-based design tool to calculate the desired PIN-SETTING resistors.

TSEN pin also has function settings except for thermal monitoring function. It only utilizes divider part of PIN-SETTING mechanism. The functions TSEN sets include, zero loadline and DVID voltage-compensation. The detailed operation is described in Thermal Monitoring and Indicator section.

Table 2. SET1 Pin Setting for ICCMAX, KTON and VBOOT

$V_{\text{divider_SET1}}$ (mV)			ICCMAX (A)		$V_{\text{IXR_SET1}}$ (mV)			KTON	VBOOT
Min.	Typ.	Max.	1 Phase	2 Phase	Min.	Typ.	Max.		
6.5	25	43	26	30	6.5	50	91.5	0.64	0V
57	75	92.5	27	33	108.5	150	189.5		1.8V
107.5	125	142	28	36	210.5	250	287.5	0.73	0V
158	175	191.5	29	39	312.5	350	385.5		1.8V
208.5	225	241	30	42	414.5	450	483.5	0.82	0V
259	275	290.5	31	45	516.5	550	581.5		1.8V
309.5	325	340	32	48	618.5	650	679.5	0.91	0V
360	375	389.5	33	51	720.5	750	777.5		1.8V
410.5	425	439	34	54	822.5	850	875.5	1	0V
461	475	488.5	35	57	924.5	950	973.5		1.8V
511.5	525	538	36	60	1026.5	1050	1071.5	1.09	0V
562	575	587.5	37	63	1128.5	1150	1169.5		1.8V
612.5	625	637	38	66	1230.5	1250	1267.5	1.18	0V
663	675	686.5	39	69	1332.5	1350	1365.5		1.8V
713.5	725	736	40	72	1434.5	1450	1463.5	1.27	0V
764	775	785.5	41	75	1536.5	1550	1590		1.8V
814.5	825	835	26	30	6.5	50	91.5	1.36	0V
865	875	884.5	27	33	108.5	150	189.5		1.8V
915.5	925	934	28	36	210.5	250	287.5	1.45	0V
966	975	983.5	29	39	312.5	350	385.5		1.8V
1016.5	1025	1033	30	42	414.5	450	483.5	1.64	0V
1067	1075	1082.5	31	45	516.5	550	581.5		1.8V
1117.5	1125	1132	32	48	618.5	650	679.5	1.82	0V
1168	1175	1181.5	33	51	720.5	750	777.5		1.8V
1218.5	1225	1231	34	54	822.5	850	875.5	2.09	0V
1269	1275	1280.5	35	57	924.5	950	973.5		1.8V
1319.5	1325	1330	36	60	1026.5	1050	1071.5	2.36	0V
1370	1375	1379.5	37	63	1128.5	1150	1169.5		1.8V
1420.5	1425	1429	38	66	1230.5	1250	1267.5	2.55	0V
1471	1475	1478.5	39	69	1332.5	1350	1365.5		1.8V
1521.5	1525	1528	40	72	1434.5	1450	1463.5	2.91	0V
1572	1575	1577.5	41	75	1536.5	1550	1590		1.8V

Table 3. SET2 Pin Setting for ANTIOVS_TH and Ai Gain

Vdivider_SET2 (mV)			ANTIOVS_TH (mV)	Ai
Min.	Typ.	Max.		
6.5	25	43	90	0.125
57	75	92.5		0.25
107.5	125	142		0.375
158	175	191.5		0.5
208.5	225	241	120	0.125
259	275	290.5		0.25
309.5	325	340		0.375
360	375	389.5		0.5
410.5	425	439	150	0.125
461	475	488.5		0.25
511.5	525	538		0.375
562	575	587.5		0.5
612.5	625	637	180	0.125
663	675	686.5		0.25
713.5	725	736		0.375
764	775	785.5		0.5
814.5	825	835	210	0.125
865	875	884.5		0.25
915.5	925	934		0.375
966	975	983.5		0.5
1016.5	1025	1033	240	0.125
1067	1075	1082.5		0.25
1117.5	1125	1132		0.375
1168	1175	1181.5		0.5
1218.5	1225	1231	270	0.125
1269	1275	1280.5		0.25
1319.5	1325	1330		0.375
1370	1375	1379.5		0.5
1420.5	1425	1429	Disable	0.125
1471	1475	1478.5		0.25
1521.5	1525	1528		0.375
1572	1575	1577.5		0.5

Table 4. SET2 Pin Setting for DVID Fast Slew Rate, Acoustic Noise Suppression and High Frequency ACLL Voltage Compensation in PS1

VIXR_SET2 (mV)			DVID Fast Slew Rate	Acoustic Noise Suppression	High Frequency ACLL Voltage compensation in PS1 (index)
Min.	Typ.	Max.			
6.5	50	91.5	48mV/us (Y/U/H-line)	Disable	60
108.5	150	189.5			80
210.5	250	287.5			100
312.5	350	385.5			Disable
414.5	450	483.5		Enable	60
516.5	550	581.5			80
618.5	650	679.5			100
720.5	750	777.5			Disable

Table 5. SET3 Pin Setting for AQR_TH and ZCD_TH

V _{divider_SET3} (mV)			AQR_TH (mV)	ZCD_TH [V _{CX} (mV)]
Min.	Typ.	Max.		
6.5	25	43	440	1.81
57	75	92.5		2.57
107.5	125	142		3.17
158	175	191.5		3.93
208.5	225	241	520	1.81
259	275	290.5		2.57
309.5	325	340		3.17
360	375	389.5		3.93
410.5	425	439	600	1.81
461	475	488.5		2.57
511.5	525	538		3.17
562	575	587.5		3.93
612.5	625	637	680	1.81
663	675	686.5		2.57
713.5	725	736		3.17
764	775	785.5		3.93
814.5	825	835	760	1.81
865	875	884.5		2.57
915.5	925	934		3.17
966	975	983.5		3.93
1016.5	1025	1033	840	1.81
1067	1075	1082.5		2.57
1117.5	1125	1132		3.17
1168	1175	1181.5		3.93
1218.5	1225	1231	920	1.81
1269	1275	1280.5		2.57
1319.5	1325	1330		3.17
1370	1375	1379.5		3.93
1420.5	1425	1429	Disable	1.81
1471	1475	1478.5		2.57
1521.5	1525	1528		3.17
1572	1575	1577.5		3.93

Table 6. SET3 Pin Setting for Sum OCP Ratio and Undershoot Suppression

V _{IXR_SET3} (mV)			Sum OCP Ratio	Undershoot suppression	
Min.	Typ.	Max.		PS0(index)	PS1(index)
6.5	50	91.5	160%	Disable	Disable
108.5	150	189.5		Disable	175
210.5	250	287.5		200	125
312.5	350	385.5		200	150
414.5	450	483.5		200	175
516.5	550	581.5		250	125
618.5	650	679.5		250	150
720.5	750	777.5		250	175
822.5	850	875.5		130%	Disable
924.5	950	973.5	Disable		175
1026.5	1050	1071.5	200		125
1128.5	1150	1169.5	200		150
1230.5	1250	1267.5	200		175
1332.5	1350	1365.5	250		125
1434.5	1450	1463.5	250		150
1536.5	1550	1590	250		175

Table 7. TSEN Pin Setting for Advanced Ramp Magnitude in PS1, Advanced Ramp Magnitude in PS0, Zero LL and DVID_LIFT

VTSEN (mV)			Advanced ramp magnitude in PS1(index)	Advanced ramp magnitude in PS0(index)	Zero LL	DVID_LIFT
Min.	Typ.	Max.				
6.5	50	92.5	125	125	Disable	Disable
107.5	150	191.5			5uA	
208.5	250	290.5			Disable	Disable
309.5	350	389.5			5uA	
410.5	450	488.5			Disable	Disable
511.5	550	587.5			5uA	
612.5	650	686.5		175	Disable	Disable
713.5	750	785.5			5uA	
814.5	850	884.5			Disable	Disable
915.5	950	983.5		225	5uA	
1016.5	1050	1082.5			Disable	Disable
1117.5	1150	1181.5			5uA	
1218.5	1250	1280.5			Disable	Disable
1319.5	1350	1379.5		Disable	5uA	
1420.5	1450	1478.5			Disable	Disable
1521.5	1550	1577.5	5uA			
1622.5	1650	1676.5	Disable		Disable	
1723.5	1750	1775.5	175	125	5uA	
1824.5	1850	1874.5			Disable	Disable
1925.5	1950	1973.5			5uA	
2026.5	2050	2072.5		175	Disable	Disable
2127.5	2150	2171.5			5uA	
2228.5	2250	2270.5			Disable	Disable
2329.5	2350	2369.5			5uA	
2430.5	2450	2468.5		225	Disable	Disable
2531.5	2550	2567.5			5uA	
2632.5	2650	2666.5			Disable	Disable
2733.5	2750	2765.5			5uA	
2834.5	2850	2864.5		Disable	Disable	Disable
2935.5	2950	2963.5	5uA			
3036.5	3050	3062.5	Disable		Disable	
3137.5	3150	3161.5	5uA			

Per Phase Current Sense

To achieve higher efficiency, the RT3612EB adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 6. An external low-pass filter R_{X1} and C_X reconstruct the current signal. The low-pass filter time constant $R_{X1} \times C_X$ should match time constant $\frac{L_X}{DCR}$ of Inductance and DCR. It's fine to fine tune R_{X1} and C_X for transient performance and current reporting. If RC network time constant matches inductor time constant $\frac{L_X}{DCR}$, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant $\frac{L_X}{DCR}$, V_{CORE} waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant $\frac{L_X}{DCR}$, V_{CORE} waveform sags to create an undershooting to fail the specification and mis-trigger over current protections (sum OCP and per phase OCP). Figure 7 shows the output waveforms according to the RC network time constant. The resistance of R_{CSx} is restricted to 680Ω and the accuracy is within 1%. R_{X1} is highly recommended as two 0603 size resistors in series to enhance the Iout reporting accuracy. X7R type capacitor is suggested for C_X in the application.

$$I_{CS,PERx} = \frac{V_{CSIN}}{680\Omega} = \frac{I_{Lx} \times DCR}{680\Omega}$$

R_{X2} is optional for prevent V_{CSIN} exceeding current sense amplifier input range. The time constant of $(R_{X1} // R_{X2}) * C$ should match $\frac{L_X}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{680\Omega} = \frac{I_{Lx} \times DCR}{680\Omega} \times \frac{R_{X2}}{R_{X1} + R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for loadline control/ current reporting, current balance, zero current detection and over current protection. The mirrored current to IMON pin is one time of $I_{CS,PER}$.

$$(I_{MON} = A_{MIRROR} \times I_{CS,PERx}, A_{MIRROR} = 1)$$

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

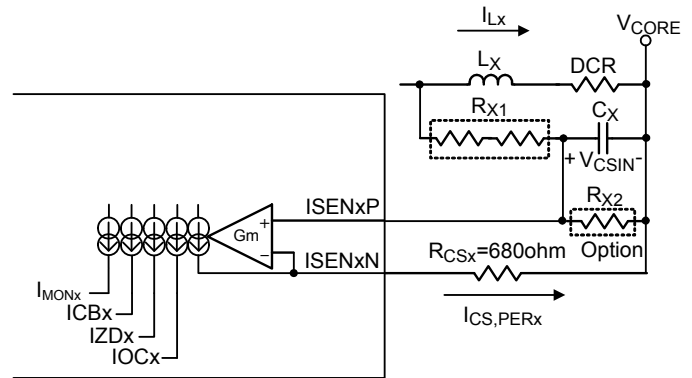


Figure 6. Inductor DCR Current Sensing Method

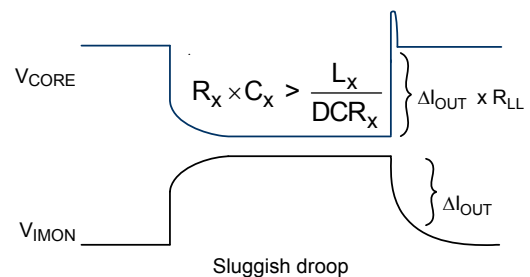
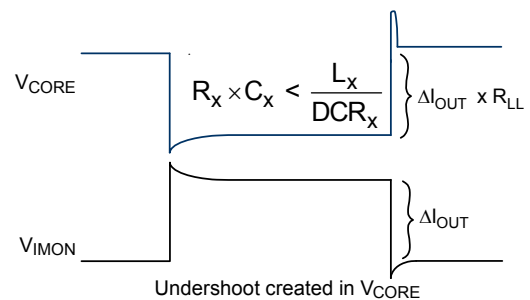
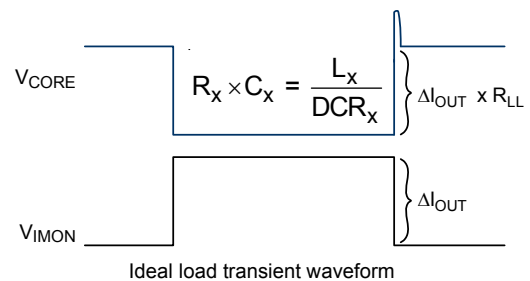


Figure 7. All Kinds of R_C Network Time Constant

Total Current Sense/ICCMAX Setting/Current Monitoring

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The RT3612EB adopts a patented total current sense method that requires only one NTC resistor for thermal compensation. The NTC resistor is designed within IMON resistor network on IMON pin. It is suggested to be placed near the inductor of the first phase. Figure 8 shows the configuration. All phase current signals are gathered to IMON pin and converted to a voltage signal V_{IMON} by $R_{IMON,EQ}$ based on V_{REF06} pin. V_{REF06} pin provides 0.6V voltage source (as presented as V_{VREF06}) while normal operation. The relationship between V_{IMON} and inductor current I_{Lx} is :

$$V_{IMON} - V_{VREF06} = (I_{L1} + I_{L2}) \times \frac{DCR}{R_{CSx}} \times R_{IMON,EQ}$$

$V_{IMON} - V_{VREF06}$ is proportional to output current. $V_{IMON} - V_{VREF06}$ is used for output current reporting and loadline loop-control. $V_{IMON} - V_{VREF06}$ is averaged by analog low-pass filter and then transferred to 8-bit ADC. The digitized reporting value is scaled such that FFh=ICCMAX. $R_{IMON,EQ}$ should be designed that $V_{IMON} - V_{VREF06} = 1.6V$ while $(I_{L1} + I_{L2}) = ICCMAX$. Additionally, sets the desired ICCMAX by ICCMAX[3:0] of PIN-SETTING table. The PIN-SETTING value determines intel ICCMAX register (21h) value. The Alert# is asserted while output current exceeds ICCMAX ($V_{IMON} - V_{VREF06} > 1.6V$). The behavior is masked during DVID. For loadline loop-control, $V_{IMON} - V_{VREF06}$ is scaled by a percentage of A_i , that can be selected by PIN-SETTING of $A_i[1:0]$. The detailed application is described in the loadline setting section.

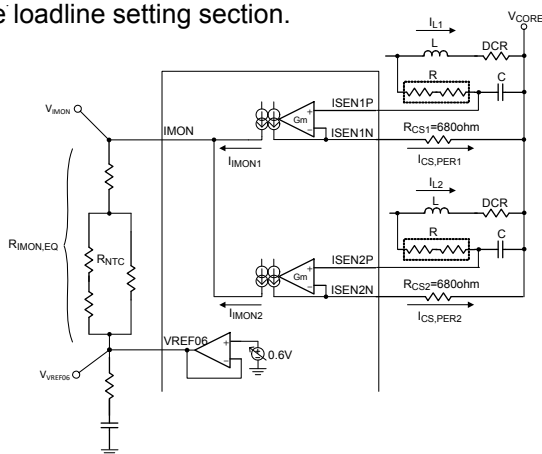


Figure 8. Total Current Sense Method

Loadline Setting (R_{LL})

An output voltage loadline (Adaptive Voltage Positioning) are specified in CPU VR for power saving and output capacitance reduction. The characteristic of loadline is that the output voltage decreases by an amount proportional to the increasing loading current, i.e. the slope between output voltage and loading current (R_{LL}) is shown in Figure 9. Figure 10 shows how the voltage and current loop parameters of RT3612EB achieve loadline. The detailed equation is described as below :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{R_{CSx}} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times \frac{3}{4}$$

A_i is current gain. R_{EA2} / R_{EA1} is defined as ERROR AMP gain. In order to have better transient performance, the ERROR AMP gain is suggested to be within 2.2 to 3.6 when $ICCMAX \geq 45A$ and within 2.2 to 5 when $ICCMAX < 45A$. R_{LL} can be programmed by A_i and R_{EA2} / R_{EA1} . A_i can be selected by PIN-SETTING of $A_i[1:0]$ as listed in Table 8.

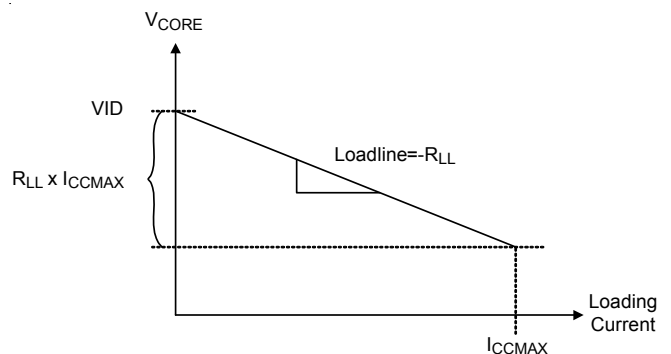


Figure 9. Load-Line (Droop)

Table 8. PIN-SETTING of $A_i[1:0]$

$A_i[1:0]$	Current Gain Setting
00	0.125
01	0.25
10	0.375
11	0.5

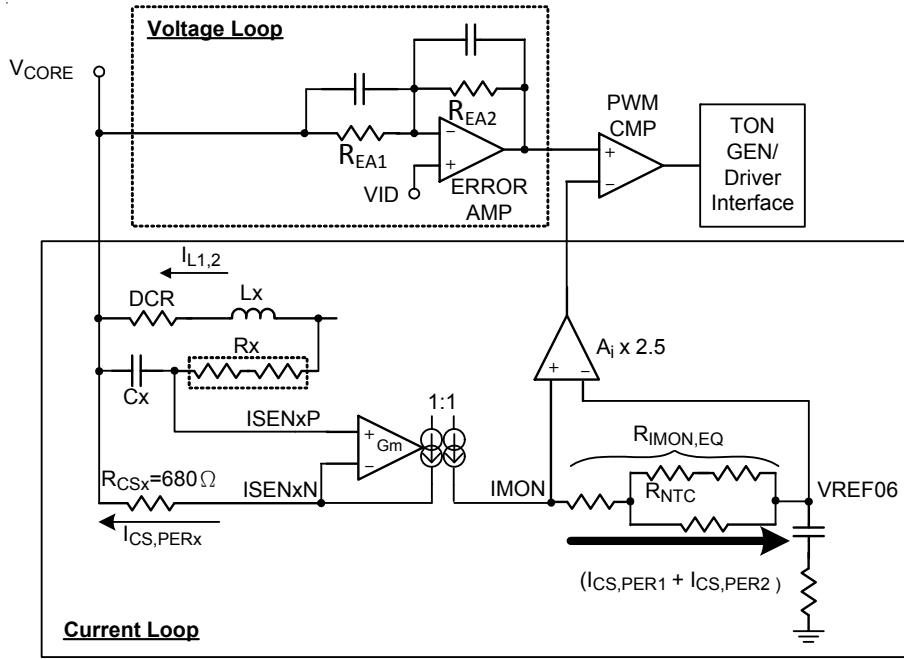


Figure 10. Voltage Loop and Current Loop for Load Line

Dynamic VID (DVID) Compensation

During DVID transition, an extra current is required to charge output capacitance for increasing voltage. The charging current approximates to the product of the DVID slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach target within the specified time. The extra voltage drop approximates to $DVID \text{ Slew Rate} \times Output \text{ Capacitance} \times R_{LL}$ (R_{LL} is the loadline slope, Ω). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 11. The RT3612EB provides one DVID compensation function as shown in Figure 12. An internal current I_{DVID_LIFT} is sinking internally from FB pin to generate DVID compensation $I_{DVID_LIFT} \times R_{EA1}$. I_{DVID_LIFT} for 50mV/ μ s DVID SR can be set from TSEN PIN-SETTING of DVID_LIFT, disabled or 5uA. For different scale of DVID SR, I_{DVID_LIFT} is internally

adjusted. Compensating magnitude can also be adjusted by R_{EA1} . For IMVP9 specification, output voltage should be within target TOB at 3us after Alert# assertion. While DAC just arrives target (Alert issue timing), inductor current is still high and needs a time to settle down to the DC loading current. In the settling time, the falling down current keeps to charge output capacitance (The magnitude is related with inductor, capacitance and VID). Thus DVID compensation can be less than $DVID \text{ Slew Rate} \times Output \text{ Capacitance}$ (Capacitance degeneration should be considered). While output capacitance is so large that DVID compensation cannot cover, adding resistor and capacitance from FB to GND also can provide similar function. ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects DVID behavior. The final setting should be based on actual measurement.

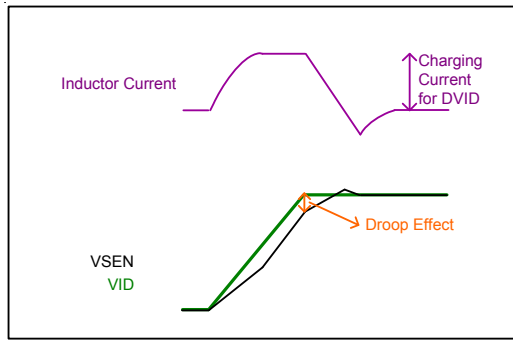


Figure 11. Droop Effect in VID Transition

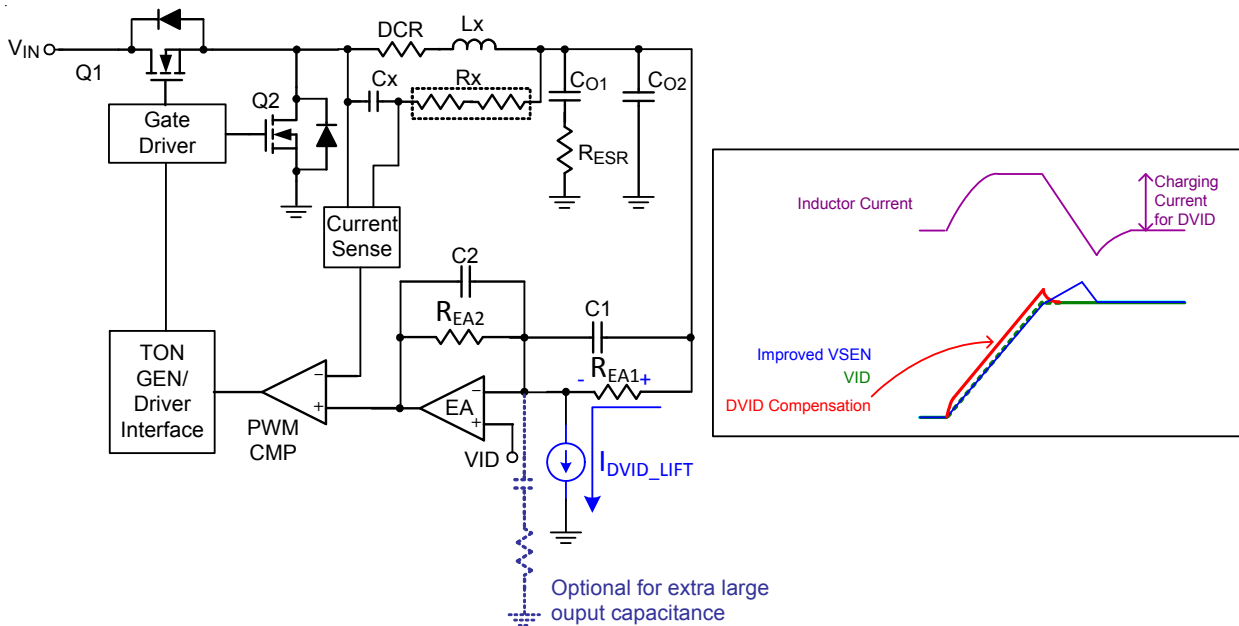


Figure 12. DVID Compensation

Compensator Design

The compensator of the RT3612EB doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP™ topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 13. For IMVP9 ACLL specification, it is recommended to adjust compensator according to load transient ring back level. Default compensator values are referred to design tool.

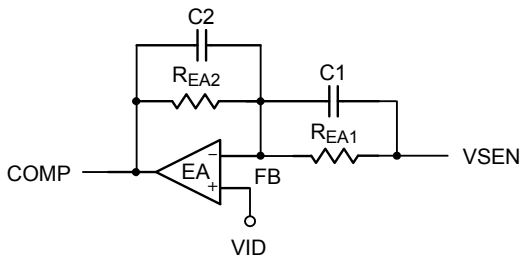


Figure 13. Type I Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. The related connection is shown in Figure 14. The VID voltage (DAC) is referred to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

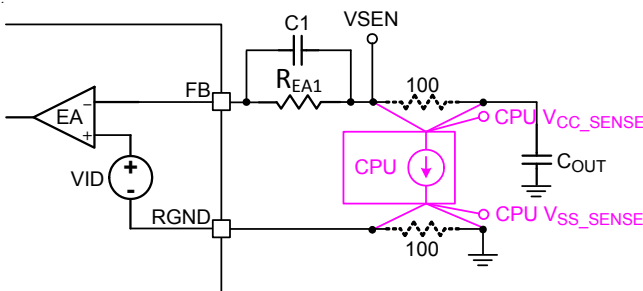


Figure 14. Remote Sensing Circuit

Switching Frequency Setting

The RT3612EB topology G-NAVP™ (Green Native AVP) is one kind of current-mode constant on-time control. It generates an adaptive T_{ON} (PWM) with input voltage (V_{IN}) for better line regulation. The T_{ON} is also adaptive to VID voltage. For VID < 1.8V, the adaptive T_{ON} is based on constant current ripple concept for better output voltage ripple size control. For VID ≥ 1.8V, the adaptive T_{ON} is based on constant frequency concept for better efficiency performance. Figure 15 is the conceptual chart showing the relationships between switching frequency vs. VID and current ripple vs. VID. The RT3612EB provides a parameter setting of k_{TON} to design T_{ON} width. k_{TON} is set by PIN-SETTING of TONSET[3:0]. The related setting table is listed in Table 9.

The equations of T_{ON} are listed as below (k_{TON} should be referred to Table 9) :

VID ≥ 1.8V

$$T_{ON(UG)} = 2.206\mu \times \frac{VID}{k_{TON} \times (V_{IN} - 1.8V)} - 5ns$$

0.3V ≤ VDACC < 1.8V

$$T_{ON(UG)} = 3.971\mu \times \frac{1}{k_{TON} \times (V_{IN} - VDACC)} - 5ns$$

VDACC < 0.3V

$$T_{ON(UG)} = 3.971\mu \times \frac{1}{k_{TON} \times (V_{IN} - 0.3)} - 5ns$$

Table 9. PIN-SETTING of TONSET

TONSET[3:0]	KTON
0000	0.64
0001	0.73
0010	0.82
0011	0.91
0100	1
0101	1.09
0110	1.18
0111	1.27
1000	1.36
1001	1.45
1010	1.64
1011	1.82
1100	2.09
1101	2.36
1110	2.55
1111	2.91

The switching frequency can be derived from T_{ON} as shown below. The losses in the main power stage and driver characteristics are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times \left(DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL} \right)}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}} \right) \right] \times (T_{ON} - T_D + T_{ONVAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times T_D}$$

- VID : VID voltage
- V_{IN} : input voltage
- I_{CC} : loading current
- N : total phase number
- R_{ONLS,max} : maximum equivalent low-side R_{DS(ON)}
- n_{HS}: number of high-side MOSFETs
- R_{ONHS,max} : maximum equivalent high-side R_{DS(ON)}
- n_{LS} : number of low-side MOSFETs.
- T_D : summation of the high-side MOSFET delay time and rising time
- T_{ONVAR} : TON variation value
- DCR : inductor DCR
- R_{LL} : loadline setting (Ω).

Although T_{ON} is designed for constant frequency target while VID ≥ 1.8, the actual frequency is still impacted by main power stage's loss and driver dead time. The switching frequency rises as loading current increases. Recommend to design the switching frequency based on the optimized efficiency and thermal performance at thermal design current (I_{CC}TDC). For example, at I_{CC} = I_{CC}TDC, VID = 1.8V and VIN = 19V, the switching frequency is 850kHz. Then substitute these values into equations to get T_{ON} and relative k_{T_{ON}}.

Richtek provides a Microsoft Excel-based design tool to help design R_{T_{ON}} and k_{T_{ON}} setting for the desired switching frequency at TDC.

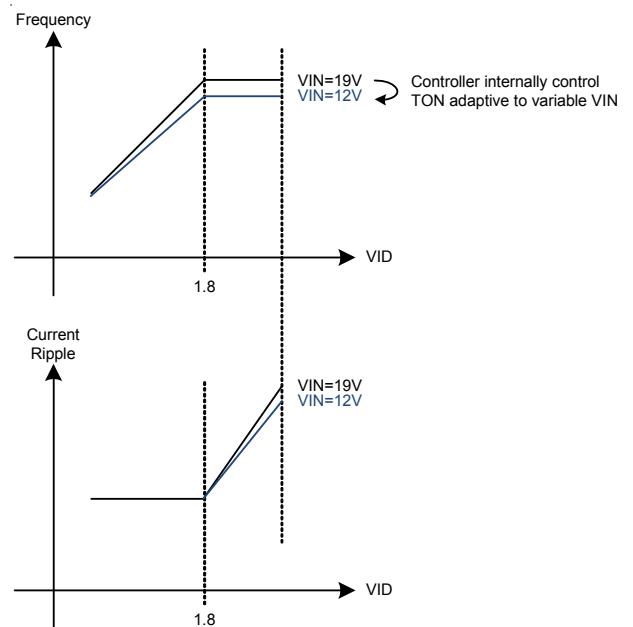


Figure 15. Switching Frequency and Current with Different VID

Adaptive Quick Response (AQR)

The RT3612EB features adaptive quick response (AQR) function to optimize transient response. The mechanism concept is illustrated in Figure 16. Controller detects output voltage drop slew rate. While the slew rate exceeds the AQR threshold, all PWMs turn on until output voltage slew rate significantly slows down. The output voltage slew rate transition also indicates that inductor current almost reaches the loading current. Under such mechanism, AQR PWM width is adaptive to variable loading step. The RT3612EB provides various AQR threshold through PIN-SETTING of AQR_TH[2:0]. The following equation can initially decide the AQR starting trigger threshold. Smaller threshold indicates larger AQR PWM. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid miss triggering AQR.

$$\text{AQR starting trigger threshold} = -200k \times 20p \times \frac{dV_{SEN}}{dt}$$

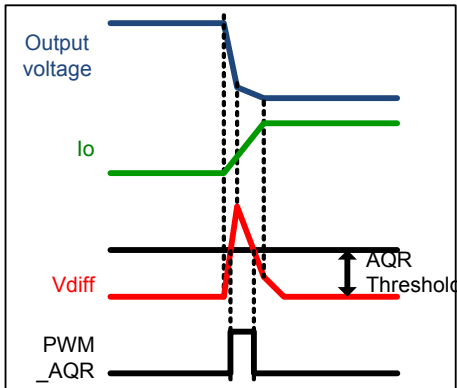
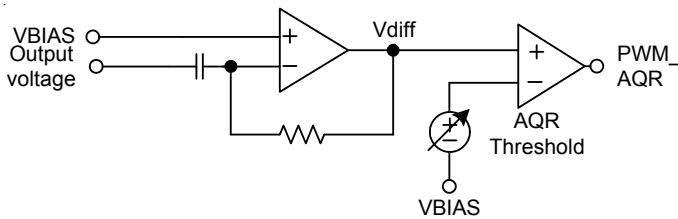


Figure 16. Adaptive Quick Response Mechanism

Table 10. PIN-SETTING of AQR_TH

AQR_TH[2:0]	AQR Starting Trigger Threshold(mV)
000	440
001	520
010	600
011	680
100	760
101	840
110	920
111	Disable

Anti-overshoot (ANTI-OVS)

The RT3612EB provides Anti-overshoot Function to depress output voltage overshoot. Controller detects overshoot by signals relating to output voltage. The overshoot trigger level can be adjusted by PIN-SETTING as listed in Table 11. The main detecting signal comes from COMP. However, COMP varies with compensation. Initial trigger level setting can be based on the following equation :

$$\Delta COMP \times \frac{4}{3} = \Delta V_{SEN} \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3}$$

> Antiovershoot Threshold of ANTIOVS_TH[2:0]

The final setting should be according to actual Error AMP compensator design and measurement.

While overshoot exceeds the setting trigger level, all PWMs keep in tri-state until the zero current is detected. Turning off LGs forces positive current flow through body diode to cause diode forward voltage. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

Table 11. PIN-SETTING of Anti-Overshoot Threshold

ANTIOVS_TH[2:0]	Anti-Overshoot Threshold (mV)
000	90
001	120
010	150
011	180
100	210
101	240
110	270
111	Disable

Dual Ramp Mechanism

Normal controllers easily suffer jitter and stability issues under low equivalent series resistance (ESR) of capacitor application and large loop delay condition. The large Loop delay often comes from PCB parasitic inductance. Figure 17 illustrates how PCB parasitic inductance impact the load transient response. The PCB parasitic inductance delays energy delivering and causes VSEN to keep falling. The dropping VSEN induces several successive PWM pulses and then VSEN ring-back occurs. While load current release at the ring back region, it will generate large overshoot. Thus more capacitors will use for the overshoot reduction.

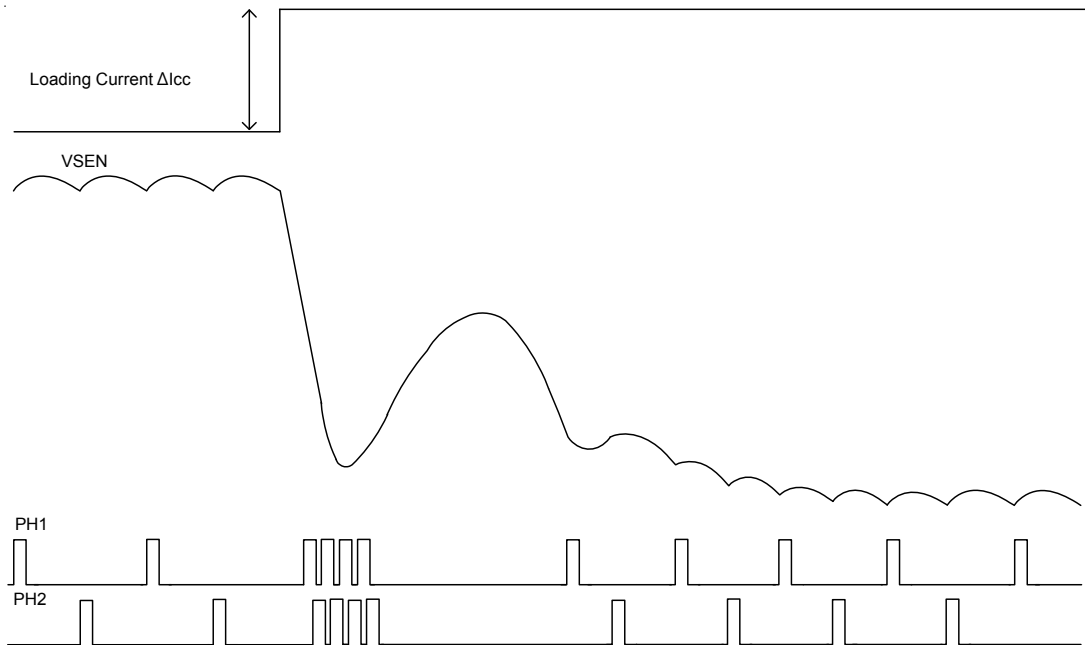


Figure 17. Load Transient Response with PCB Parasitic Inductance

RT3612EB provides a new generation of dual ramp mechanism to enhance performance. Except original ramp to minimize jitter, additional Advanced Ramp is developed to solve loop natural lag due to PCB parasitic inductance and prevent adjacent PWM turn-on. That has current signal meaning and prediction. The transient ring-back can be effectively suppressed. Figure 18 and Figure 19 show the apparent difference between single ramp and dual ramp with PCB parasitic inductance condition.

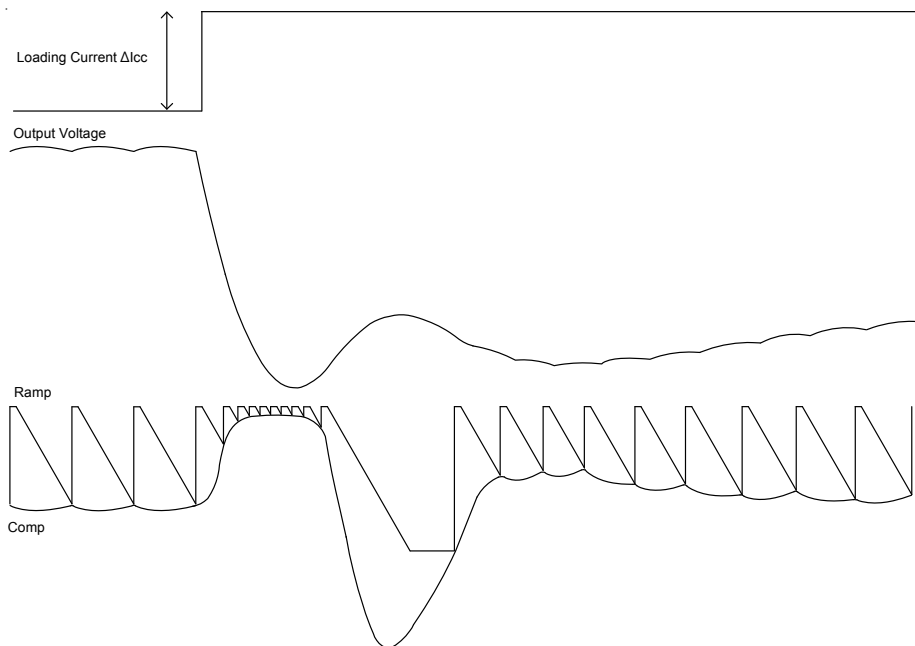


Figure 18. Single Ramp Behavior with PCB Parasitic Inductance Condition

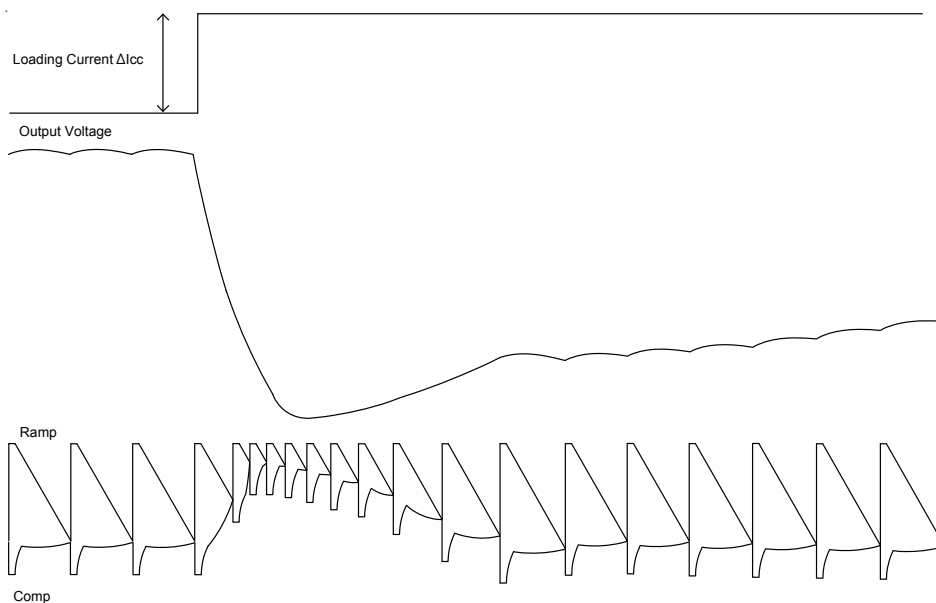


Figure 19. Dual Ramp Behavior with PCB Parasitic Inductance Condition

Through PIN-SETTING, RT3612EB provides advanced ramp magnitude tuning. FLRAMP_PS0[1:0] and FLRAMP_PS1 are for PS0 and PS1, respectively. According to different application conditions, the setting of parameters are listed in Table 12 and Table 13. The larger magnitude indicates larger parasitic inductance suppression. However, larger magnitude also affects loop response speed and reduce PWM output frequency at loading edge. For normal PCB layout, FLRAMP_PS0[1:0] = 00 or FLRAMP_PS0[1:0] = 11 are recommended. The final setting must be based on actual measurement.

Table 12. PIN-SETTING of Advanced Ramp Magnitude in PS0

FLRAMP_PS0 [1:0]	Internal Advanced Ramp Magnitude (index)
00	125
01	175
10	225
11	Disable

Table 13. PIN-SETTING of Advanced Ramp Magnitude in PS1

FLRAMP_PS1	Internal Advanced Ramp Magnitude (index)
0	125
1	175

ACLL Performance Enhancement

RT3612EB provides another optional function to improve undershoot by applying a positive offset at loading edge. Controller detects COMP signal and compared it with steady state. While V_{COMP} variation exceeds a threshold, an additional positive offset will apply to the output voltage. The threshold can be set through PIN-SETTING and separately for PS0 and PS1, as listed in Table 14. The smaller index indicates the easier detection being triggered. The positive offset is related to the compensation. It can approximate to $60mV / \left(\frac{R_{EA2}}{R_{EA1}} \right)$. In PS0, the slew rate of V_{RAMP} would increase when the V_{COMP} intersect the positive offset. In order to send out another on-time earlier to improve undershoot. In PS1, besides the positive offset, an additional 10mV is applied to the DAC and one pulse of PWM is also forced turn on while the function is triggered. The positive offset and the 10mV DAC offset is released gradually with about hundred microsecond. Figure 20 and Figure 21 show undershoot suppression behavior in PS0 and PS1. For different platform, the optimized setting is different. The final setting must be based on actual measurement.

Table 14. PIN-SETTING of Undershoot Suppression

UDS[2:0]	PS0 (index)	PS1 (index)
000	Disable	Disable
001	Disable	175
010	200	125
011	200	150
100	200	175
101	250	125
110	250	150
111	250	175

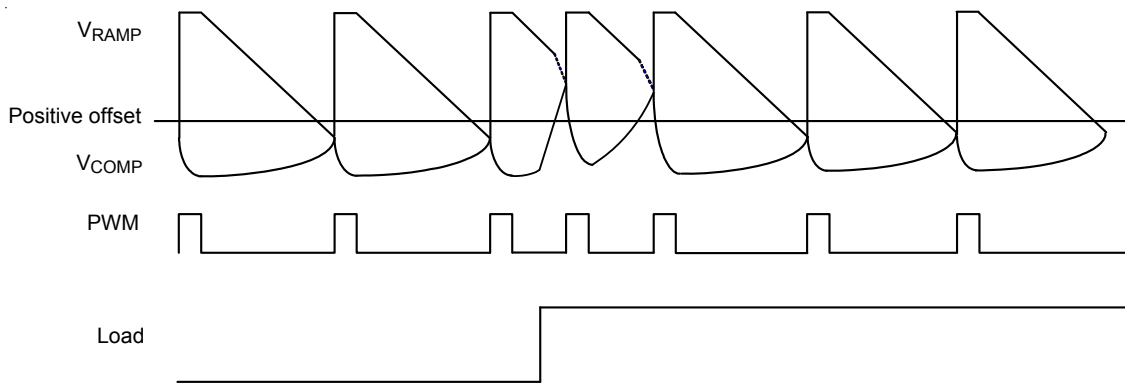


Figure 20. Undershoot Suppression Behavior in PS0

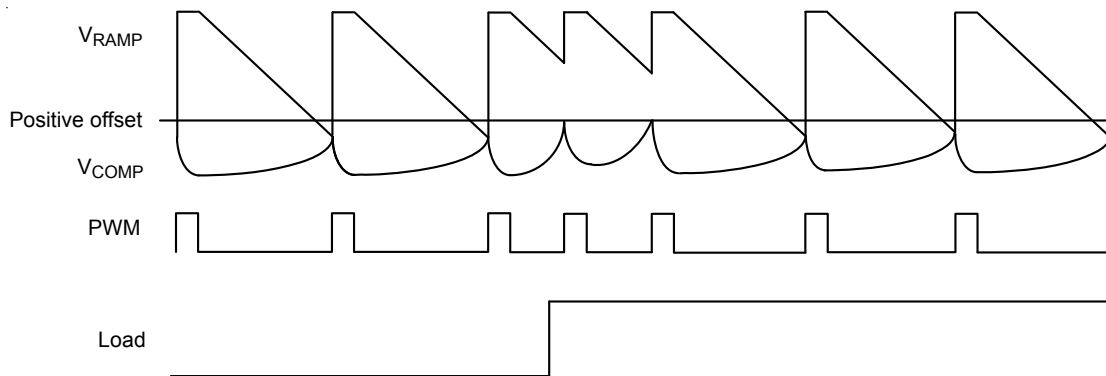


Figure 21. Undershoot Suppression Behavior in PS1

High Frequency ACLL Voltage Compensation

RT3612EB provides positive offset to enhance performance that only applies to high frequency ACLL. The positive offset can be set through PIN-SETTING in PS1. HFACLL_LIFT_PS1[1:0] is the related settings. The related setting table is listed in Table 15. The default set of HFACLL_LIFT_PS1[1:0]=00. Note that smaller setting value represents higher positive offset. The final setting must be based on actual measurement.

Table 15. PIN-SETTING of High Frequency ACLL Voltage Compensation in PS1

HFACLL_LIFT_PS1 [1:0]	High Frequency ACLL Voltage Compensation in PS1 (index)
00	60
01	80
10	100
11	Disable

Thermal Monitoring and Indicator

TSEN pin processes two functions of PIN-SETTING (function setting) and thermal monitoring as shown in Figure 22. The timing chart and related signals are shown in Figure 23. After power on, TSEN has three operation modes : PIN-SETTING, Pre-Thermal Sense and Thermal Sense Mode. The corresponding function blocks of the three modes are shown in Figure 22. In PIN-SETTING Mode, TSEN pin voltage = $3.2V \times R2 / (R1 + R2)$ with $VREF06 = 3.2V$ and is coded by ADC and stored in PIN-SETTING register. In Pre-Thermal Sense Mode, TSEN pin voltage = $0.6V \times R2 / (R1 + R2)$ with $VREF06 = 0.6V$ and is coded and stored in Pre-Thermal Register. This part helps Thermal Sense Mode calculation. In Thermal Sense Mode, TSEN pin voltage = $0.6V \times R2 / (R1 + R2) + 80\mu A \times [(R1 // R2) + R3]$ with $VREF06 = 0.6V$ and is coded. Pre-Thermal Register code is subtracted from the result and the value is stored in Thermal Register (The corresponding TSEN voltage = $80\mu A \times [(R1 // R2) + R3]$ that's defined as Thermal Voltage. R3 is the NTC thermistor network to sense temperature.) NTC thermistor is recommended to be placed near the MOSFET, the hottest area in the PCB. Higher temperature causes smaller R3 and lower TSEN. According to NTC thermistor temperature curve, design Thermal Voltage v.s Temperature with proper Rx network to meet Table 16. $100^{\circ}C$ Thermal Voltage = $80\mu A \times [(R1 // R2) + R3, 100^{\circ}C] = 1.092V$ must be met. Controller processes TSEN pin voltage to report temperature zone register (12h). While TSEN pin voltage is less than 1.092V, VR_HOT# is pulled low to indicate thermal alert. The VR_HOT# signal is an open-drain signal. Thermal Register data is updated every 100μs and averaged every 800μs. The resistance accuracy of TSEN network is recommended to be less than 1% error.

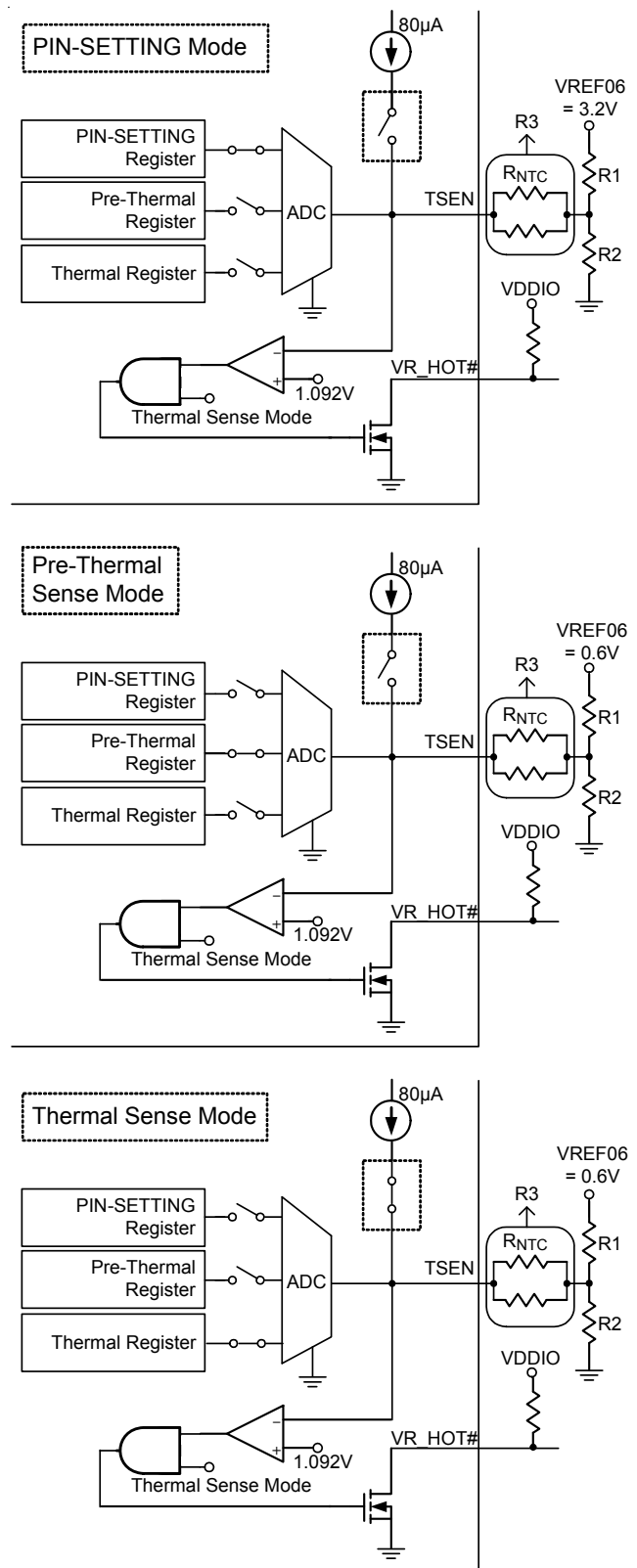


Figure 22. Multi-Function Pin Setting Mechanism for TSEN

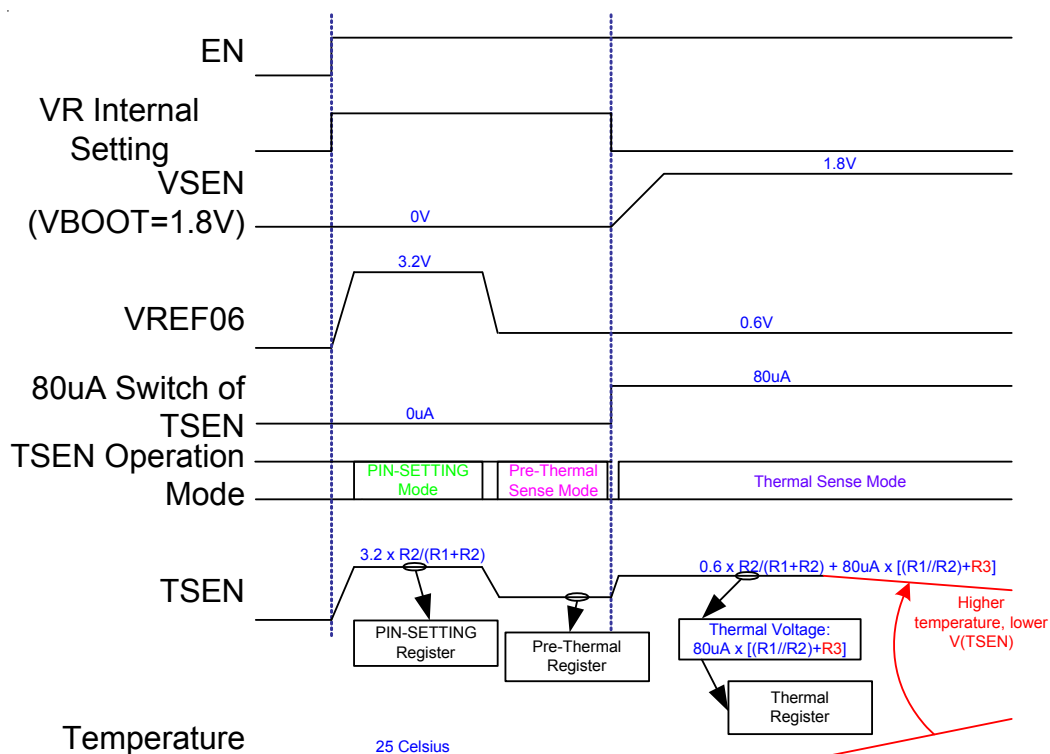


Figure 23. Timing Chart for Thermal Monitoring

Table 16. Thermal Zone and Detection Encoding with $R_{NTC} = 100k\Omega$, $\text{Beta} = 4485K$

Temperature	Thermal Voltage $80\mu A \times [(R1 // R2) + R3]$	Temperature Zone Register (12h)
100°C	1.092V	FFh
97°C	1.132V	7Fh
94°C	1.176V	3Fh
91°C	1.226V	1Fh
88°C	1.283V	0Fh
85°C	1.346V	07h
82°C	1.418V	03h
75°C	1.624V	01h

System Input Power Monitoring (PSYS)

RT3612EB provides PSYS function to monitor total platform system power and report to the CPU via SVID interface. The PSYS function can be illustrated as in Figure 24. PSYS meter measures system input current and outputs a proportional current signal I_{PSYS} . R_{PSYS} is designed for the PSYS voltage = 1.6V with maximum I_{PSYS} for 100% system input power. 1.6V is a full-scale analog signal for FFh digitized code.

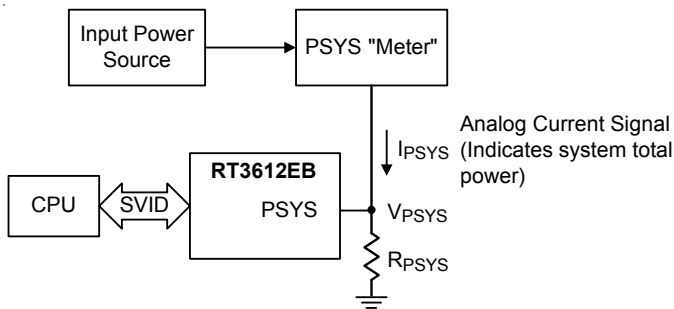


Figure 24. PSYS Function Block Diagram

Zero Loadline

RT3612EB also can support zero loadline function. It can be enabled by PIN-SETTING of Zero LL_EN = 1. When zero loadline function is enabled, the output voltage is determined only by VID and does not vary with the loading current like loadline system behavior. RT3612EB adopts a new feature, i.e. AC-droop, to effectively suppress load transient ring back and to control overshoot well for zero loadline application. Figure 25 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back $\Delta V2$ due to C area charge. Figure 26 shows the condition with AC-droop control. While loading occurs, controller temporarily changes VID target to short-term voltage target. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as the following :

$$\text{Short_Term_Voltage_Target} = \text{VID} - \Delta I_{CC} \times R_{LL}$$

The setting method of R_{LL} is the same as loadline system. The short-term voltage target reverts to VID target slowly after a period of time. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back can be suppressed. The overshoot amplitude is reduced to only $\Delta V3$.

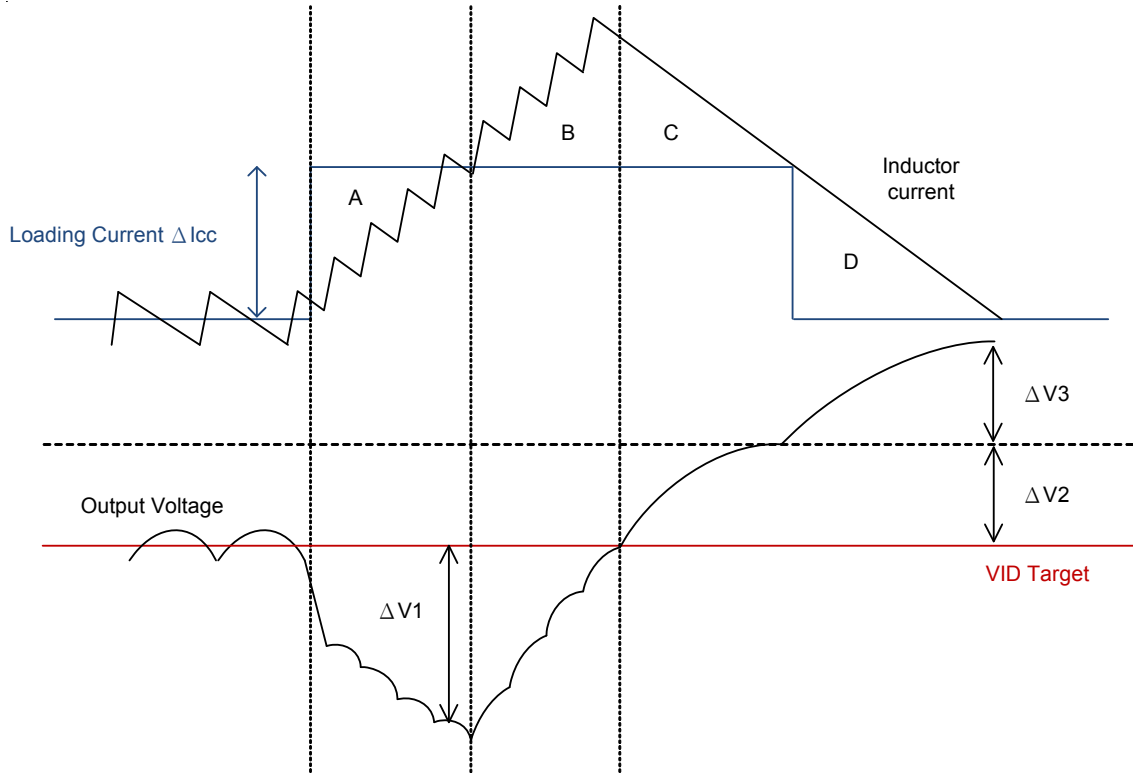


Figure 25. Zero Loadline without AC-droop Control

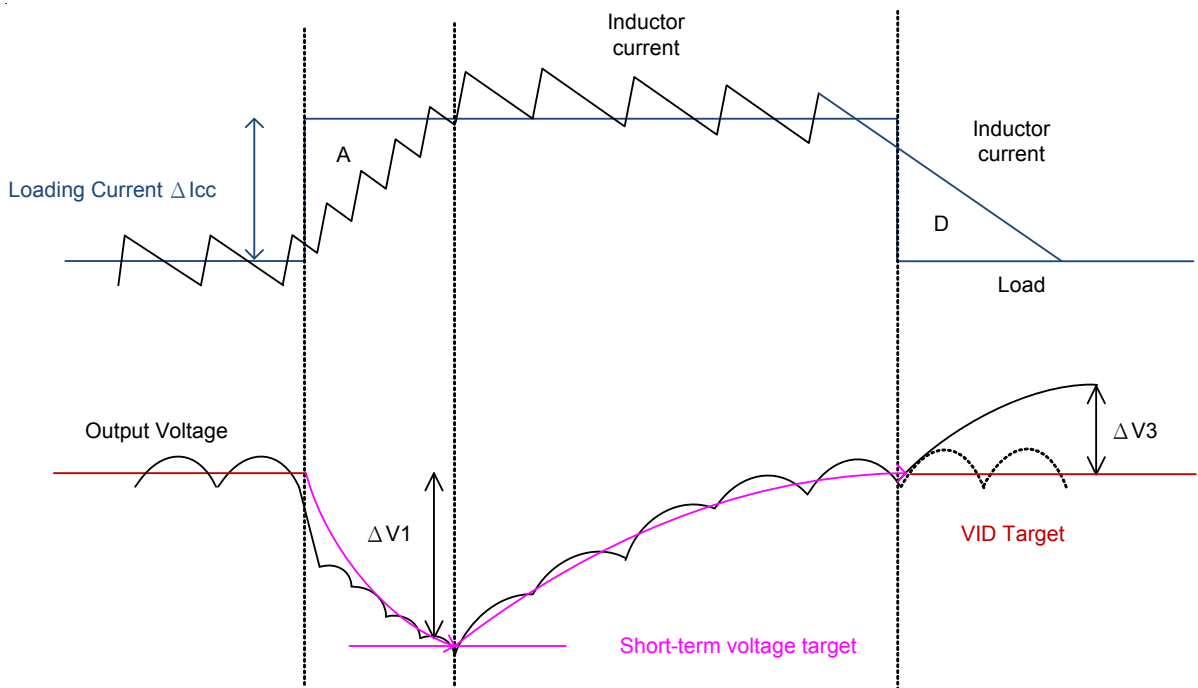


Figure 26. Zero Loadline with AC-droop Control

Acoustic Noise Suppression

The RT3612EB support acoustic noise suppression function for reducing acoustic noise induced by Piezoelectric Effect from MLCC. As output voltage transition, especially in Dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falling into audible band and the noise level is related to the output voltage transition amplitude ΔV . Therefore, the RT3612EB adapts acoustic noise suppression function which is enabled by PIN-SETTING of ANS_EN = 1.

Over Current Protection (OCP)

The RT3612EB has two OCP mechanisms, sum OCP and per phase OCP.

Sum OCP

The threshold of sum OCP for PS0 is defined as

$$I_{SUM_OC,PS0} = K_{SOCP} \times V_{MON_ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{MON,EQ}}$$

PS1/2/3 sum OCP is defined as

$$I_{SUM_OC,PS1} = 0.5 \times K_{SOCP} \times V_{MON_ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{MON,EQ}}$$

While $R_{MON,EQ}$ is designed exactly for

$$V_{MON_ICCMAX} = ICCMAX \times \frac{DCR}{R_{CSx}} \times R_{MON,EQ}$$

$$V_{MON_ICCMAX} = 1.6V$$

And $K_{SOCP} = 1.3$ and 1.6 . It is set by Pin Setting Function of SET3.

Sum OCP threshold can be simplified as $I_{SUM_OC,PS0} = K_{SOCP} \times ICCMAX$ and $I_{SUM_OC,PS1} = 0.5 \times K_{SOCP} \times ICCMAX$ when $ICCMAX \geq 45A$. and $I_{SUM_OC,PS0} = I_{SUM_OC,PS1} = K_{SOCP} \times ICCMAX$ when $ICCMAX < 45A$. While inductor current above sum OCP threshold lasts $40\mu s$, controller de-asserts VR_READY and latches PWM in tri-state to turn off high-side and low-side power MOSFETs.

Per Phase OCP

Per phase OCP is mainly for short circuit protection. Per phase OCP threshold is directly linked with ICCMAX. The relations between per phase OCP threshold, I_Max register setting and total phase numbers N are listed in Table 17. While inductor current exceeds per phase OCP threshold, PWMs high pulse are blanked until the inductor current is pulled below per phase OCP threshold. If the POCP indicator keeps high for $40\mu s$ (with $10\mu s$ deglitch), the controller de-asserts VR_READY and latches PWM in tri-state to turns off both the high-side and low-side MOSFETs. OCP_SUM is masked during DVID period and $80\mu s$ after VID settles. All of the OCP protections are illustrated in Figure 27 and Figure 28.

Table 17. Per Phase OC Threshold

$\frac{ICCMAX}{N}$ (A)	Per phase OCP TH (A)	While $R_{IMON,EQ}$ design meets the following conditions $1.6V = ICCMAX \times \frac{DCR}{R_{CSx}} \times R_{IMON,EQ}$
≥ 31	$\frac{2.25}{N} \times 1.6V \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$	$\frac{2.25}{N} \times ICCMAX$
23 - 30	$\frac{2.625}{N} \times 1.6V \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$	$\frac{2.625}{N} \times ICCMAX$
18 - 22	$\frac{3.9375}{N} \times 1.6V \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$	$\frac{3.9375}{N} \times ICCMAX$
≤ 17	$\frac{5.25}{N} \times 1.6V \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$	$\frac{5.25}{N} \times ICCMAX$

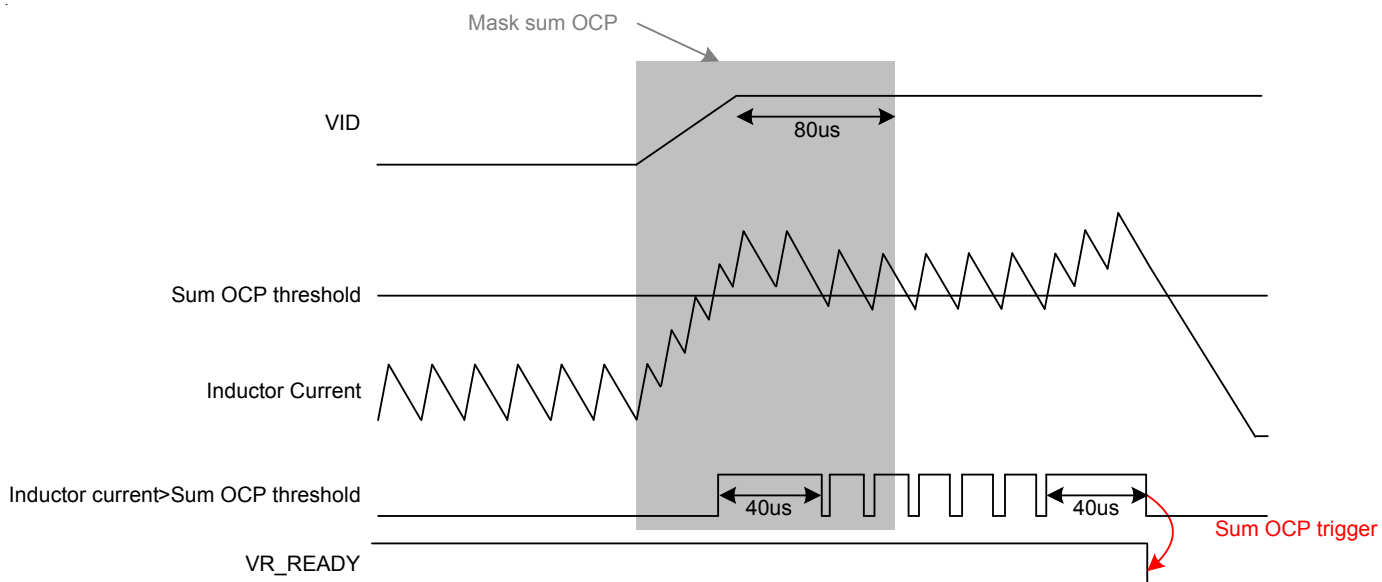


Figure 27. Sum OC Protection Mechanism

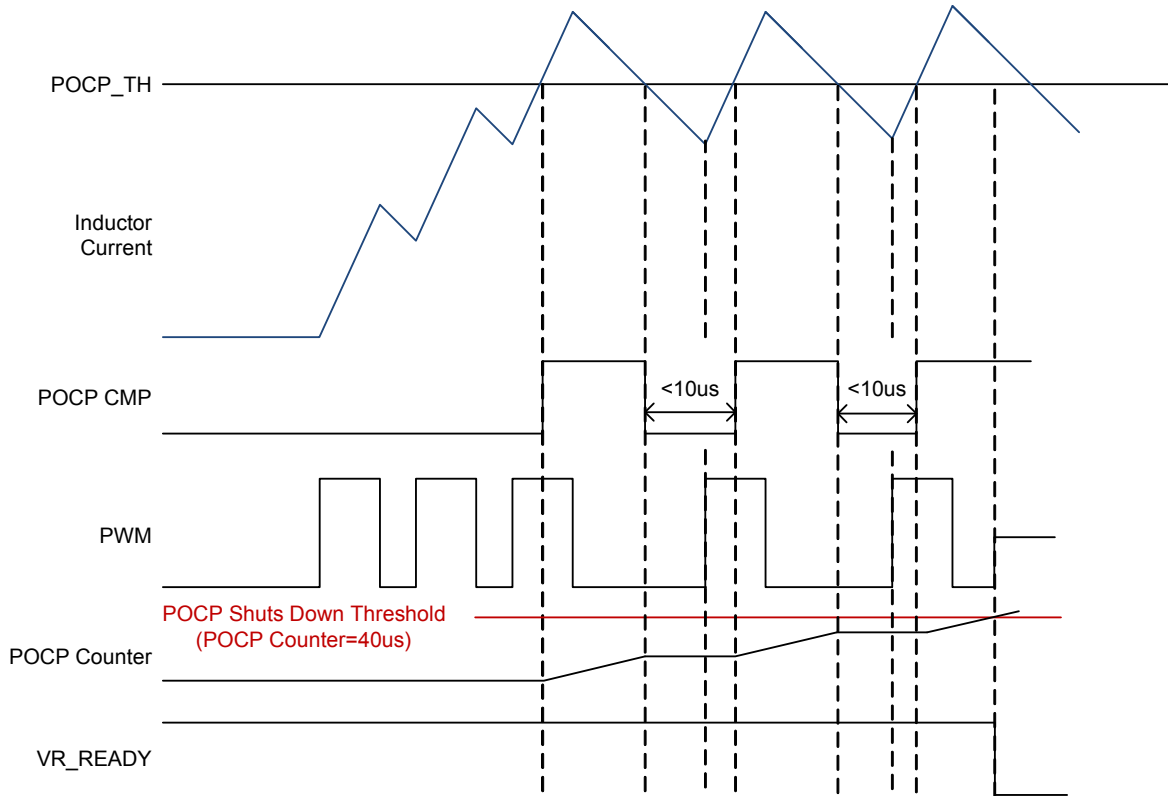


Figure 28. (a). $<10\mu s</math>, the POCP Counter No Reset$

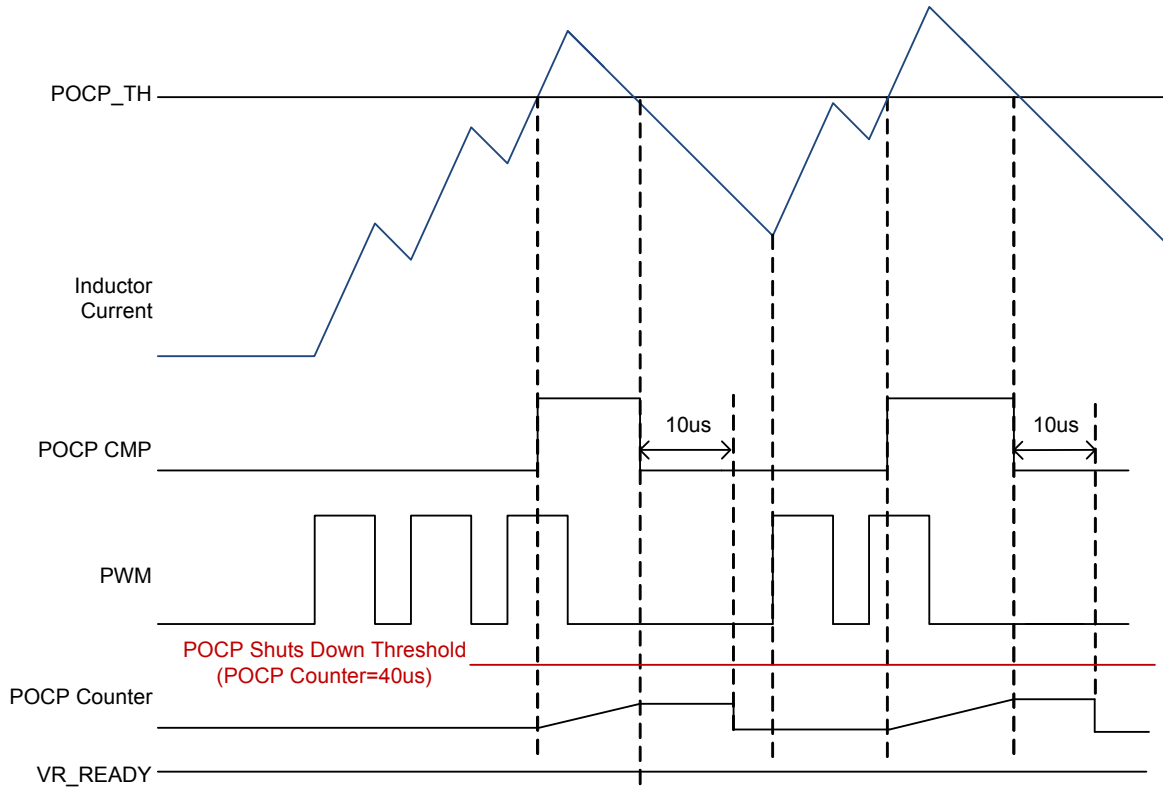


Figure 28. (b). $>10\mu s</math>, the POCP Counter Reset$

Figure 28. Per Phase OC Limit Mechanism

Over Voltage Protection (OVP)

The OVP threshold is linked with VID. The classification table and waveform are illustrated in Table 18 and Figure 29. While VID = 0V in case of VR internal setting mode or DACOFF or PS4, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, OVP threshold is 2.45V to allow not-fully-discharged VSEN. Otherwise, the OVP threshold is relative to VID and equals to VID+350mV with minimum limit = 2.23V. While VID<1.88V, the OVP threshold is limited at 2.23V.

The OV protection mechanism is illustrated in Figure 30. When OVP is triggered with 0.5us filter time, controller de-asserts VR_READY and forces all PWMs low to turn on low-side power MOSFETs. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWMx is not allowed to turn on.

Table 18. Summary of Over Voltage Protection

VID Condition	OVP Threshold	Example	Protection Action	Protection Reset
VID = 0 (VRON = L or VR internal setting mode or DACOFF or PS4)	OVP is masked		VR_READY latched low.	VCC/EN Toggle
DVID up period from 0V to 1st PWM pulse after VID settles	2.45V			
DVID period from non-zero VID	VID+350mV minimum threshold = 2.23V	VID = 2V, OVP threshold = 2.35V VID = 1.2V, OVP threshold = 2.23V		
VID ≠ 0	VID+350mV minimum threshold = 2.23V			

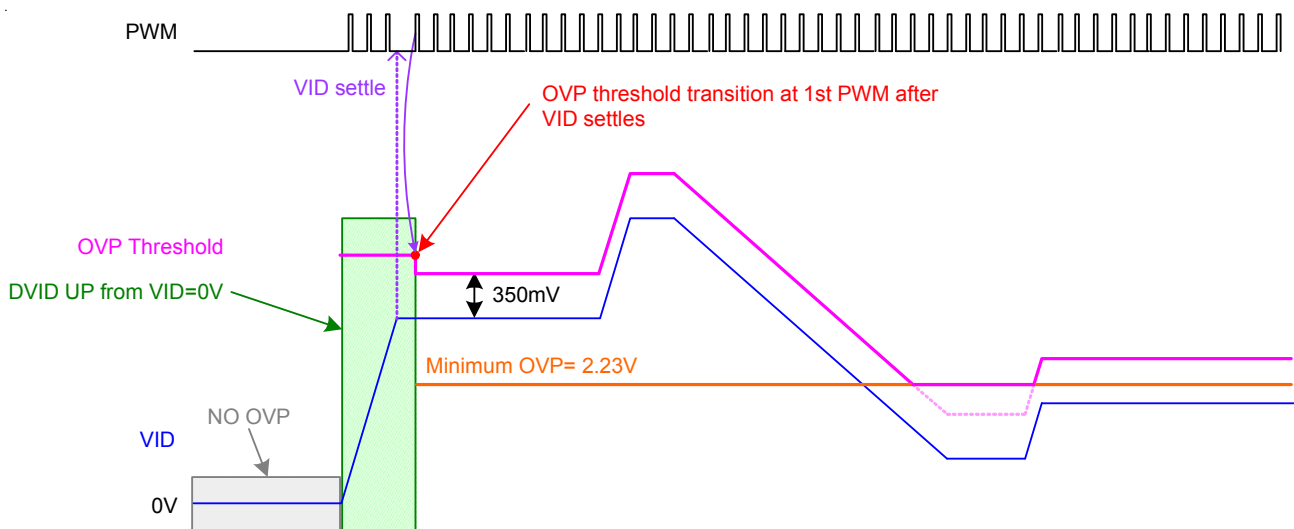


Figure 29. Timing Chart for Over Voltage Threshold

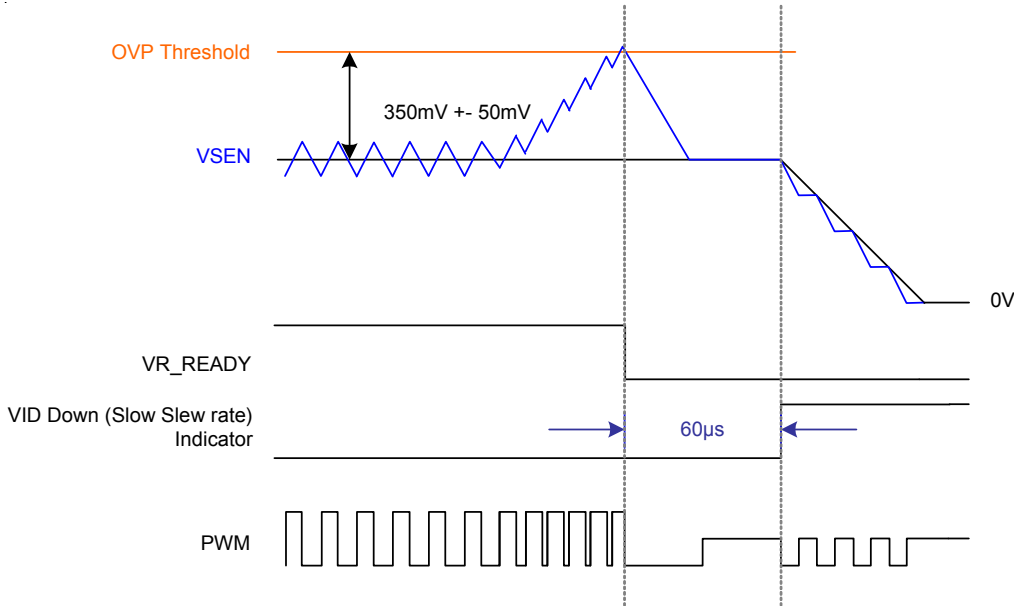


Figure 30. Over Voltage Protection Mechanism

Under Voltage Protection

When the output voltage is lower than VID-660mV with 3µs filter time, UVP is triggered and PWMx are in tri-state to turn off high-side and low-side power MOSFETs. UVP is masked during DVID period and 80µs after VID settles. The mechanism is illustrated in Figure 31.

All protections are reset only by VCC/EN toggle. UVP and OCP protections are listed in Table 19.

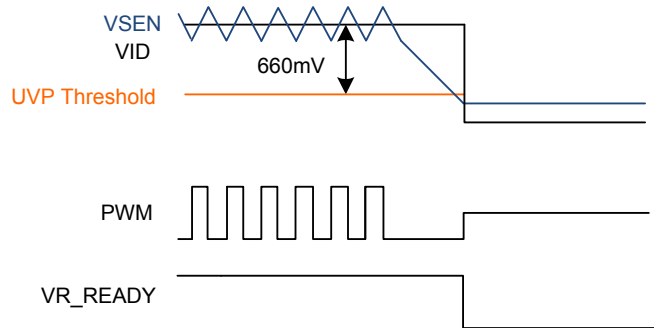


Figure 31. Under Voltage Mechanism

Table 19. Summary of UVP and OCP Protection

Protection Type	Protection Threshold	Protection Action	DVID Mask Time	Protection Reset
Sum OC for PS0	$I_{SUM_OC,PS0}$ $= K_{SOCP} \times V_{IMON,ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$	PWM tri-state, VR_READY latched low	DVID+80us	VCC/EN Toggle
Sum OC for non PS0	$I_{SUM_OC,PS1}$ $= 0.5 \times K_{SOCP} \times V_{IMON,ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$			
UV	VID - 660mV			

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-32L 4x4 package, the thermal resistance, θ_{JA} , is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (27.8^\circ\text{C/W}) = 3.59\text{W for a WQFN-32L 4x4 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 32 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

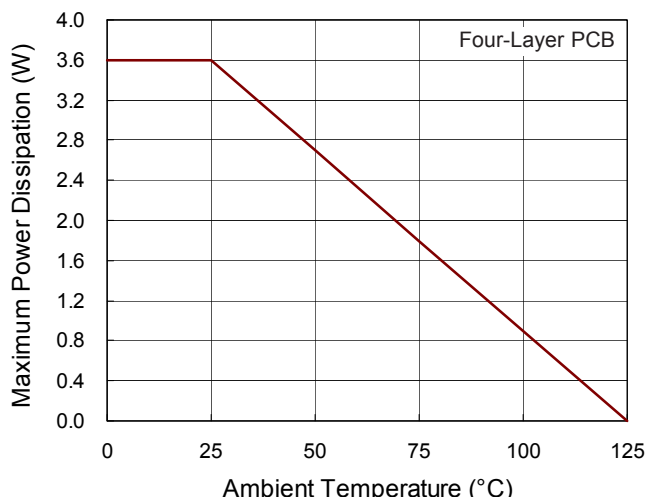
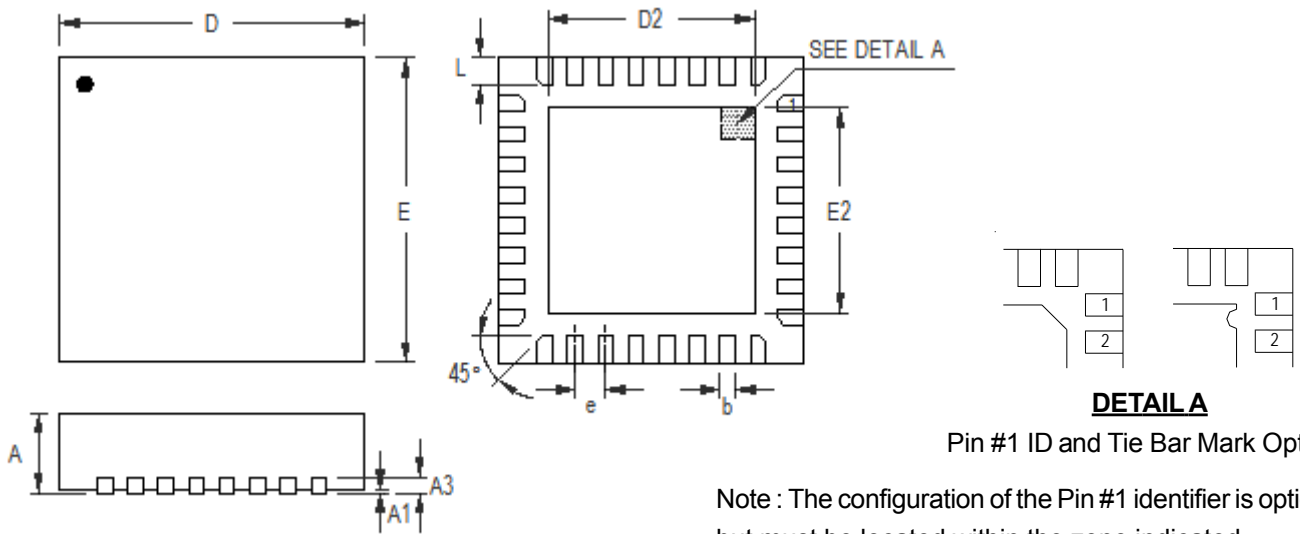


Figure 32. Derating Curve of Maximum Power Dissipation

Outline Dimension



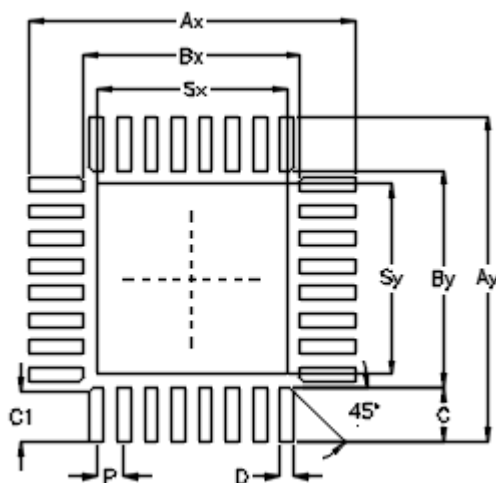
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*32	C1*8	D	Sx	Sy	
V/W/U/XQFN4*4-32	32	0.40	4.80	4.80	3.20	3.20	0.80	0.75	0.20	2.80	2.80	±0.05

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