RICHTEK®

RT3624PE

Dual Channel PWM Controller for IMVP9.1 CPU Core Power Supply

1 General Description

The RT3624PE is a synchronous buck controller that supports two output rails and fully meets the Intel IMVP9.1 requirements. The RT3624PE adopts G-NAVP^{TM} (Green Native AVP), which is Richtek's proprietary topology derived from the finite DC gain of an EA amplifier with current mode control. This design makes it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). The RT3624PE integrates a high-accuracy ADC for platform and function settings, such as ICCMAX, switching frequency, DVID fast slew rate, and DVID compensation. The RT3624PE provides VR Ready and thermal indicators. It also features complete fault protection functions, including overvoltage (OV), undervoltage (UV), overcurrent (OC), and undervoltage lockout (UVLO). The recommended junction temperature range is from –40°C to 125°C.

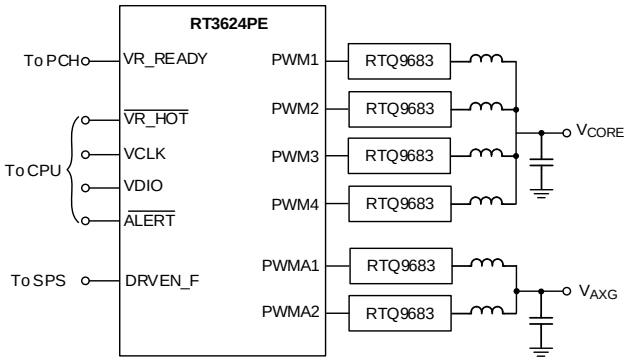
2 Applications

- IMVP9.1 Intel CORE/AXG Power Supply
- Desktop and Notebook Computers
- AVP Step-Down Converter

3 Features

- **Compliant with Intel IMVP9.1 Standards**
- **Configurable 4/3/2/1 Phase (CORE VR) + 2/1 Phase (AXG VR) PWM Controller**
- **G-NAVP^{TM} (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-In ADC for Platform Programming and Reporting**
- **Accurate Current Balance**
- **Diode Emulation Mode under Light Load Conditions**
- **VR Ready Indicator**
- **OVP, OCP, and UVP with Flag**
- **Switching Frequency Setting**
- **DVID Enhancement**
- **Acoustic Noise Suppression**
- **Zero Load-Line**
- **Rail Disable Feature**
- **Support Phase Doubler RT9637 for CORE Rail Up to 6-Phase Operation (Optional)**
- **Support SPS Application**
- **Soldering Good Detection**
- **RT3624PE: Support Addresses 00 and 01**
- **Small 52-Lead WQFN Package**

4 Simplified Application Circuit



5 Ordering Information

RT3624PE □□

Package Type(1)
QW: WQFN-52L 6x6 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information

RT3624PEGQW: Product Code
YMDAN: Date Code

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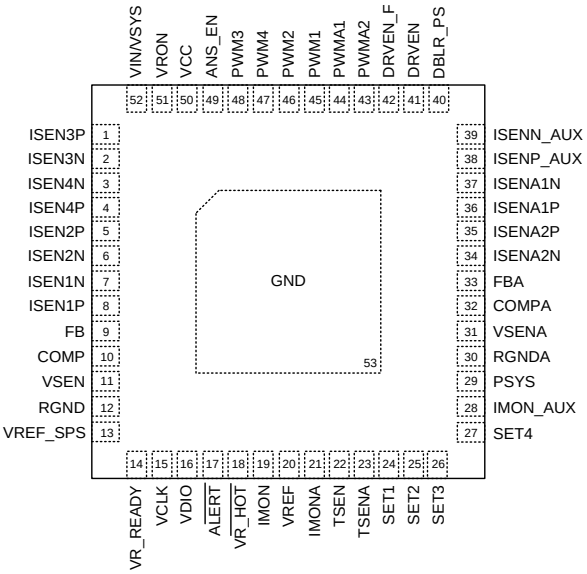
7 Pin Configuration

(TOP VIEW)



WQFN-52L 6x6

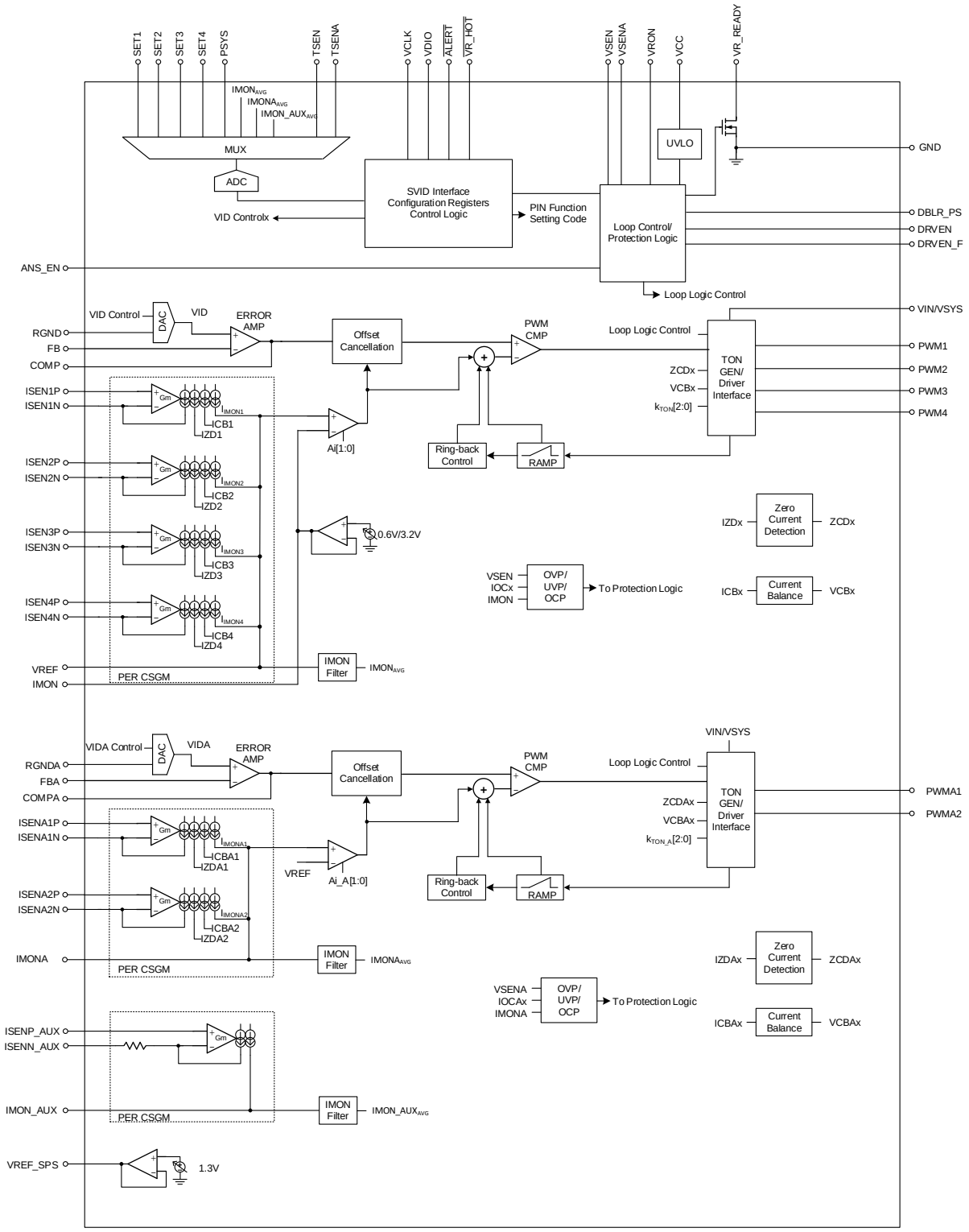
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
8, 5, 1, 4	ISEN[1:4]P	Positive inputs to current-sense amplifier for Phase 1 to 4 of VR CORE rail.
7, 6, 2, 3	ISEN[1:4]N	Negative inputs to current-sense amplifier for Phase 1 to 4 of VR CORE rail.
9	FB	Negative input of the error amplifier. This pin is for CORE rail VR output voltage feedback to the controller.
10	COMP	CORE rail VR compensation. This pin is an error amplifier output pin.
11	VSEN	CORE rail VR voltage sense input. This pin is connected to the terminal of CORE rail VR output voltage.
12	RGND	Return ground for CORE rail VR. This pin is the negative node of the differential remote voltage sensing.
13	VREF_SPS	Fixed 1.3V output reference voltage. This voltage is used to offset the smart power stage. An exact 0.22μF decoupling capacitor must be placed between this pin and GND.
14	VR_READY	VR ready indicator.
15	VCLK	Synchronous clock from the CPU.
16	VDIO	VR and CPU data transmission interface.
17	$\overline{\text{ALERT}}$	SVID alert. (Active low)
18	$\overline{\text{VR\_HOT}}$	Thermal monitor output. (Active low)
19	IMON	CORE rail VR current monitor output. This pin provides a current proportional to the output current.

Pin No.	Pin Name	Pin Function
20	VREF	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of all IMON pins. The voltage source shuts down when the controller is off or when all rails are set to PS4. An exact 0.47μF decoupling capacitor and a 3.9Ω resistor must be placed between this pin and GND.
21	IMONA	AXG rail VR current monitor output. This pin outputs a current proportional to the output current.
22	TSEN	CORE rail VR thermal sense input connects to the smart power stage (SPS) temperature sensor.
23	TSENA	AXG rail VR thermal sense input connects to the smart power stage (SPS) temperature sensor.
24	SET1	Function settings for ICCMAX, VBOOT of CORE rail and ICCMAX of AXG rail. For soldering check, connect the SET1 pin to 5V and pull the VRON high. If the soldering is good, both rail outputs are non-zero VBOOT.
25	SET2	Function settings for VBOOT of AXG rail, on-time width setting (switching frequency) of CORE rail, selectable VID table, zero load-line, and ICCMAX of AUX rail.
26	SET3	Function settings for undershoot suppression, DVID fast slew rate, DVID voltage compensation and $\overline{\text{VR\_HOT}}$ assertion during DVID current limit.
27	SET4	Function settings for phase number with the RT9637 of CORE rail, on-time width setting (switching frequency) of AXG rail and current gain (Ai).
28	IMON_AUX	AUX rail VR current monitor output. This pin outputs a current proportional to the output current.
29	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible. The input power domain (SVID Address 0x0Dh) rail can be disabled by pulling the voltage at the PSYS pin > (VCC – 0.5V). The RT3624PE rejects any commands to the input power domain rail. If the platform does not support the PSYS function, it is recommended to connect the PSYS pin to GND to avoid affecting system performance.
30	RGNDA	Return ground for AXG rail VR. This pin is the negative node of the differential remote voltage sensing.
31	VSENA	AXG rail VR voltage sense input. This pin is connected to the terminal of AXG rail VR output voltage.
32	COMPA	AXG rail VR compensation. This pin is an error amplifier output pin.
33	FBA	Negative input of the error amplifier. This pin is for AXG rail VR output voltage feedback to controller.
37, 34	ISENA[1:2]N	Negative inputs to current-sense amplifier for Phase 1 to 2 of VR AXG rail.
36, 35	ISENA[1:2]P	Positive inputs to current-sense amplifier for Phase 1 to 2 of VR AXG rail.
38	ISENP_AUX	Positive input to current-sense amplifier of VR AUX rail.
39	ISENN_AUX	Negative input to current-sense amplifier of VR AUX rail.
40	DBLR_PS	External driver mode control. When the PS4 command is received, this pin enters a high state. This pin can work with the RT9637 to drive two power stages using a single PWM signal. When the PS0 command is received, this pin enters a low state. When the PS1 command is received, this pin enters a floating state. When the PS2/3 command is received, this pin enters a high state.
41	DRVEN	External driver mode control. When the PS4 command is received, this pin enters a low state. The output high level is VCC.

Pin No.	Pin Name	Pin Function
42	DRVEN_F	External driver mode control. As the PS4 command is received, this pin enters a floating state. The output high level is VCC.
44, 43	PWMA[1:2]	PWM outputs for AXG rail VR. The tri-state window = 1.4V to 2.1V.
45, 46, 48, 47	PWM[1:4]	PWM outputs for CORE rail VR. The tri-state window = 1.4V to 2.1V.
49	ANS_EN	Acoustic Noise Suppression function setting. When the pin is pulled to VCC, this function can be enabled. This pin is not allowed to be floating.
50	VCC	Controller power supply. Connect this pin to a 5V source and attach an RC filter with R = 2.2Ω and C = 4.7μF. The decoupling capacitor should be placed as close to the PWM controller as possible. The recommended size of R_{VCC} is 0603.
51	VRON	VR enable control input.
52	VIN/VSYS	VIN/VSYS input pin. Connect a low pass filter to this pin to set on-time.
53 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

10 Functional Block Diagram



11 Absolute Maximum Ratings

(Note 2)

- VIN/VSYS to GND ---------- –0.3V to 28V
- VCC to GND - ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-52L 6x6 ---------- 3.77W
- Package Thermal Resistance (Note 3)

  WQFN-52L 6x6, θ_{JA} ---------- 26.5°C/W

  WQFN-52L 6x6, θ_{JC} ---------- 6.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- VIN/VSYS to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating condition.

13 Electrical Characteristics

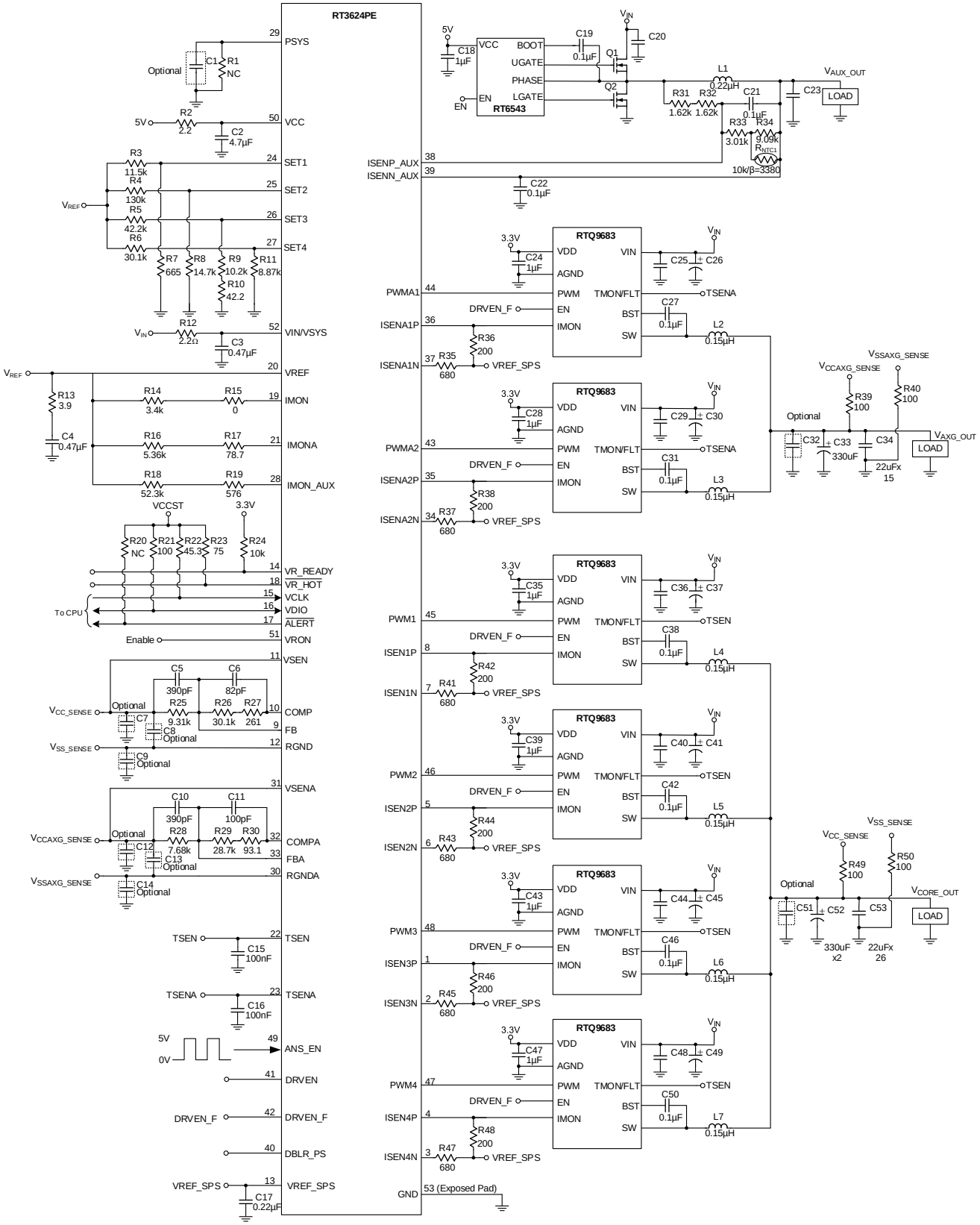
(V_{CC} = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from –20°C to 105°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	VRON = H, not switching	--	14	--	mA
Supply Current at PS4	I_{CC_PS4}	VRON = H, not switching	--	85	--	μA
Shutdown Current	I_{SHDN}	VRON = L	--	--	15	μA
EA Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ	70	--	--	dB
Gain-Bandwidth Product	G_{BW}	C_{LOAD} = 5pF	--	10	--	MHz
Slew Rate	SR_{EA}	C_{LOAD} = 10pF (Gain = –4, Rf = 47kΩ, VOUT = 0.5V to 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.3	--	3.6	V
Maximum Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Current Sensing Amplifier (CORE/AXG/AUX)						
Impedance at Positive Input	R_{ISENxP}		1	--	--	MΩ
CS Input Voltage	V_{CSIN}	Differential voltage range of DCR sense. (V_{CSIN} = Inductor current x DCR x DCR divider)	–10	--	80	mV
Current Sense Gain Error	A_{MIRROR}	Internal current mirror gain of per phase current sense $I_{IMON}/I_{CS,PERx}$	0.97	1	1.03	A/A
TON Setting						
On-Time Setting	t_{ON}	V_{IN} = 19V, VID = 0.9V, k_{TON} = 1.36	--	93	--	ns
Minimum Off-Time	t_{OFF_MIN}	VID = 1V under PS1 condition	--	130	300	ns
Minimum On-Time	t_{ON_MIN}		--	50	--	ns
Protections						
Undervoltage Lockout Rising Threshold	V_{UVLO_R}	Rising edge	4.1	--	4.45	V
Undervoltage Lockout Falling Threshold	V_{UVLO_F}	Falling edge	3.9	--	4.2	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	Rising edge hysteresis	100	170	250	mV
Output Overvoltage Protection Threshold	V_{OVP}	Respect to VID voltage	VID	VID	VID	mV
		VID > 1V	+320	+350	+380	
		VID ≤ 1V	1.3	1.35	1.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Undervoltage Protection Threshold	V_{UVP}	Respect to VID voltage	–680	–650	–620	mV
VRON and VR_READY						
VRON Input Voltage Rising Threshold	V_{VRON_R}		0.7	--	--	V
VRON Input Voltage Falling Threshold	V_{VRON_F}		--	--	0.3	V
Leakage Current of VRON	I_{LEAK_IN}		–1	--	1	µA
VR_READY Pull Low Voltage	V_{VR_READY}	I_{VR_READY} = 10mA	--	--	0.13	V
Serial VID and $\overline{VR\_HOT}$						
VCLK, VDIO Input Voltage Logic-High	V_{IH}		0.65	--	--	V
VCLK, VDIO Input Voltage Logic-Low	V_{IL}		--	--	0.45	V
Leakage Current of VCLK and VDIO	I_{LEAK_IN}		–1	--	1	µA
Pull Low Voltage of V_{VDIO}		I_{VDIO} = 10mA	--	--	0.13	V
Pull Low Voltage of $V_{\overline{ALERT}}$		$I_{\overline{ALERT}}$ = 10mA	--	--	0.13	V
Pull Low Voltage of $V_{\overline{VR\_HOT}}$		$I_{\overline{VR\_HOT}}$ = 10mA	--	--	0.13	V
Leakage Current of $\overline{ALERT}$, $\overline{VR\_HOT}$	I_{LEAK_OUT}		–1	--	1	µA
ANS_EN						
Input Voltage Logic-High	V_{IH}		VCC – 0.5	--	--	V
Input Voltage Logic-Low	V_{IL}		--	--	1	V
VREF						
VREF Voltage	V_{REF}	Normal operation	0.59	0.6	0.61	V
VREF SPS Voltage	V_{REF_SPS}	Normal operation	1.2	1.3	1.4	V
ADC						
Digital IMON Set of CORE	dV_{IMON_ICCMAX}	$V_{IMON} - V_{REF}$ = 0.8V @ ICCMAX ≥ 80A $V_{IMON} - V_{REF}$ = 0.4V @ ICCMAX ≥ 40A $V_{IMON} - V_{REF}$ = 0.2V @ ICCMAX < 40A	--	255	--	Decimal
Digital IMON Set of AXG	dV_{IMONA_ICCMAX}	$V_{IMONA} - V_{REF}$ = 0.4V @ ICCMAX ≥ 40A $V_{IMONA} - V_{REF}$ = 0.2V @ ICCMAX < 40A	--	255	--	Decimal
Digital IMON Set of AUX	$dV_{IMON\_AUX\_ICCMAX}$	$V_{IMON\_AUX} - V_{REF}$ = 1.6V	--	255	--	Decimal
PSYS Maximum Input Voltage	PSYS	V_{PSYS} = 1.6V	--	255	--	Decimal

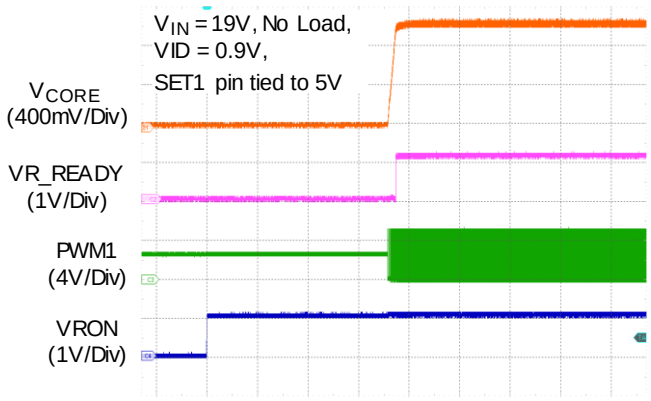
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSYS Maximum Input Voltage	VSYS	VIN/VSYS = 24V	--	255	--	Decimal
Averaging Period of IMON	t_{IMON}		--	150	--	μs
Averaging Period of TSEN	t_{TSEN}		--	600	--	μs
TSEN Input Voltage Rising Threshold to Pull Low $\overline{VR\_HOT}$ (Asserts $\overline{VR\_HOT}$)	$V_{TSEN\_\overline{VR\_HOT}\_R}$	Rising	--	1.4	--	V
TSEN Input Voltage Falling Threshold to Pull High $\overline{VR\_HOT}$ (De-Asserts $\overline{VR\_HOT}$)	$V_{TSEN\_\overline{VR\_HOT}\_F}$	Falling	--	1.376	--	V
TSEN Input Voltage Rising Threshold to Pull Low $\overline{ALERT}$	$V_{TSEN\_\overline{ALERT}\_R}$	$\overline{ALERT}$ = Low	--	1.376	--	V
TSEN Input Voltage Falling Threshold to Pull Low $\overline{ALERT}$	$V_{TSEN\,\overline{ALERT}\_F}$	$\overline{ALERT}$ = Low	--	1.352	--	V
Input Power Domain Disable Voltage	V_{PSYS}		VCC – 0.5	--	--	V

14 Typical Application Circuit



15 Typical Operating Characteristics

CORE VR Power On from EN



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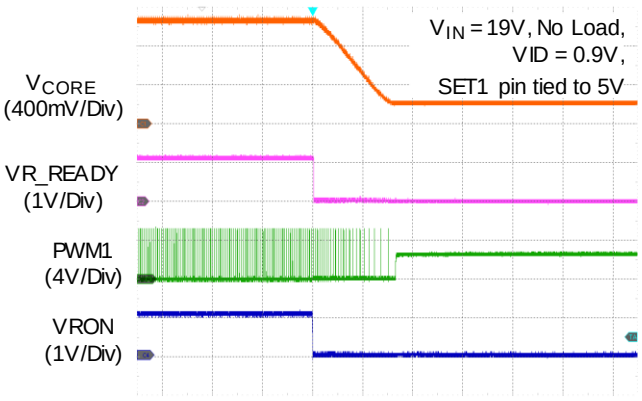
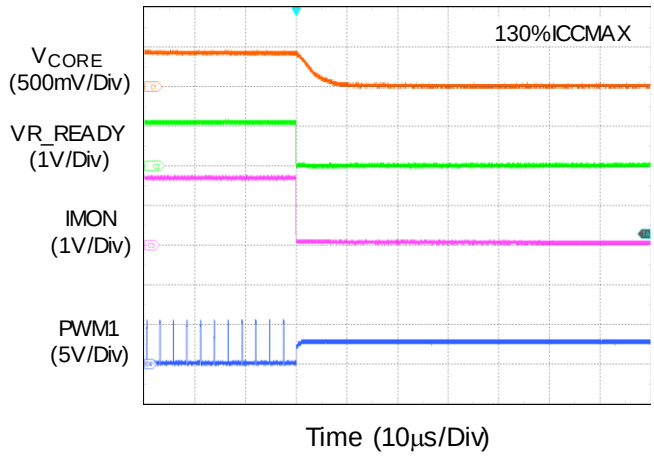
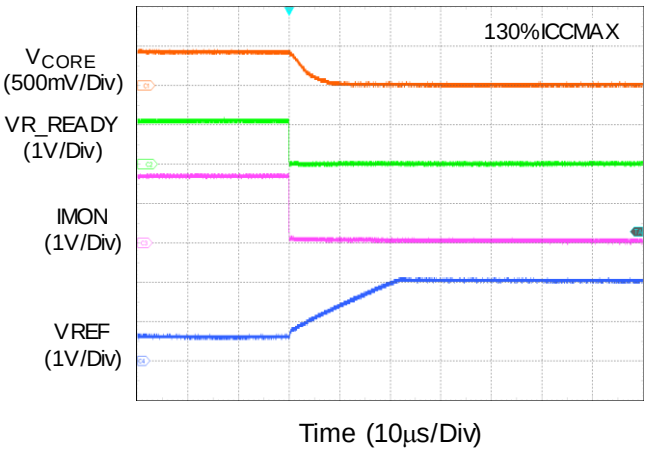


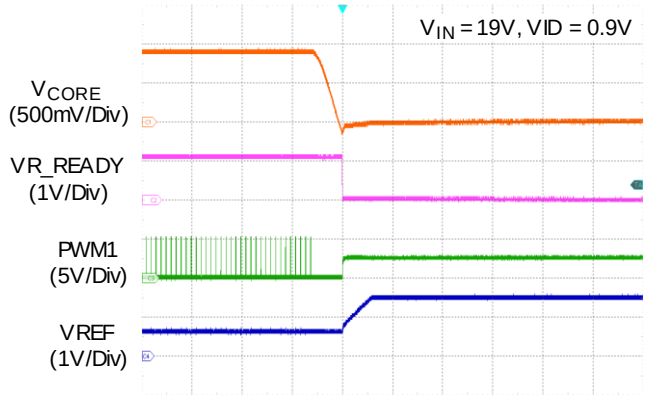
CORE VR OCP



CORE VR OCP



CORE VR UVP



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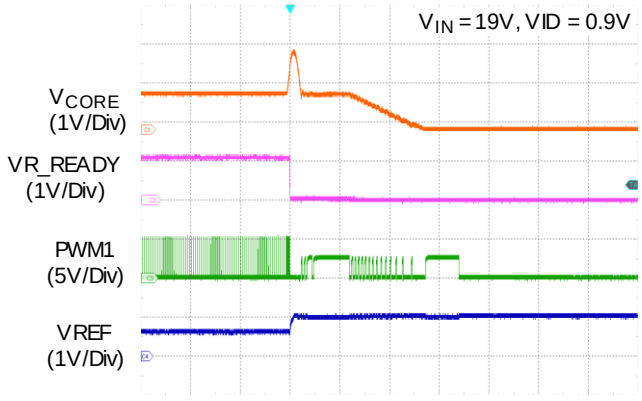
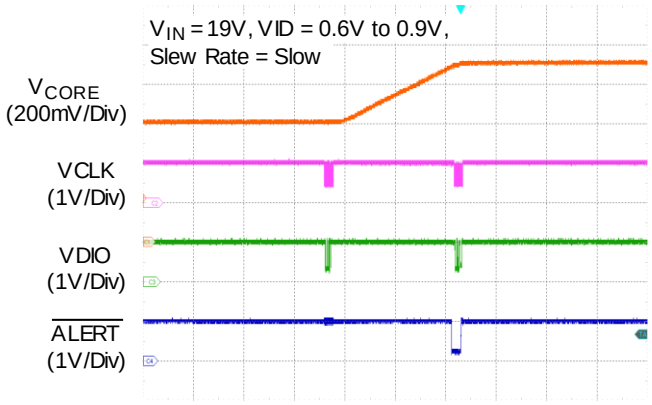
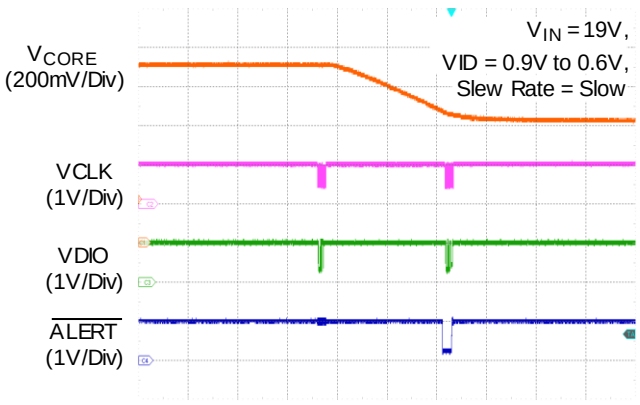


CORE VR Dynamic VID Up



CORE VR Dynamic VID Down



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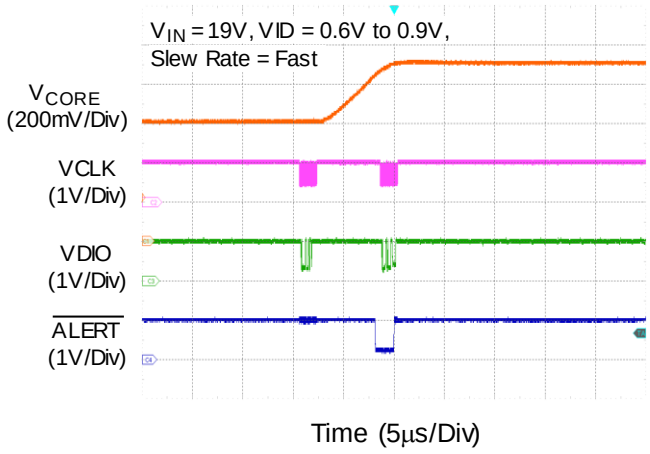

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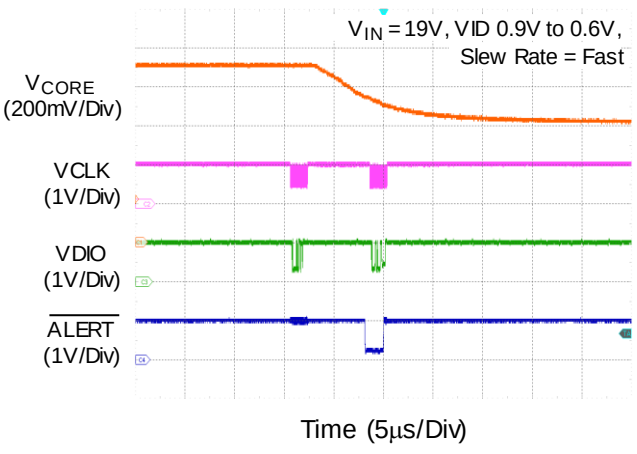
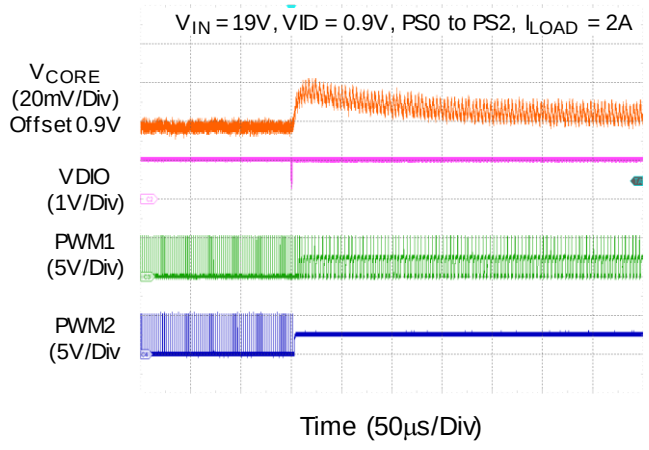
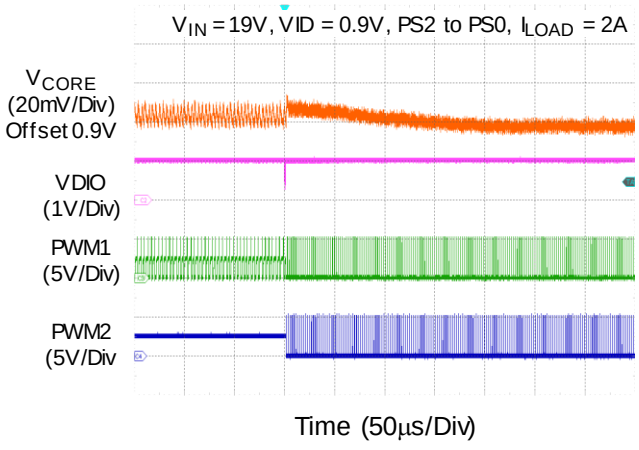


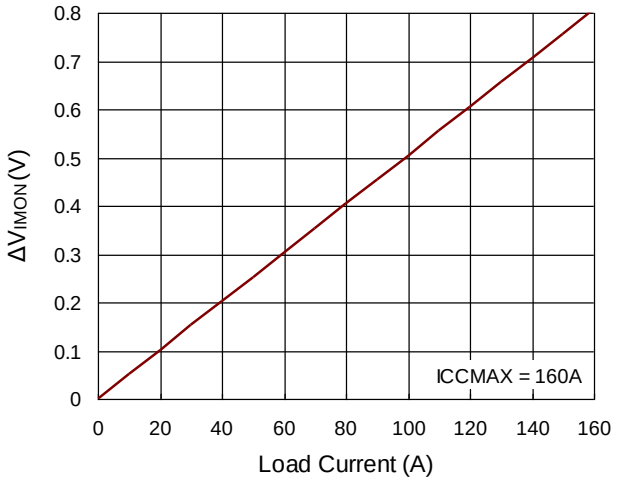
CORE VR Mode Transient



CORE VR Mode Transient



ΔV_{IMON} vs. Load Current



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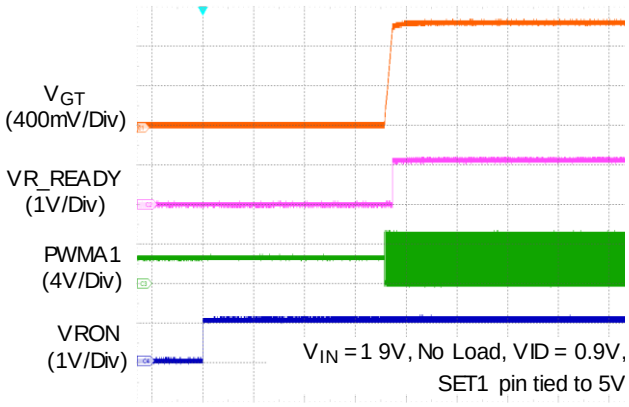
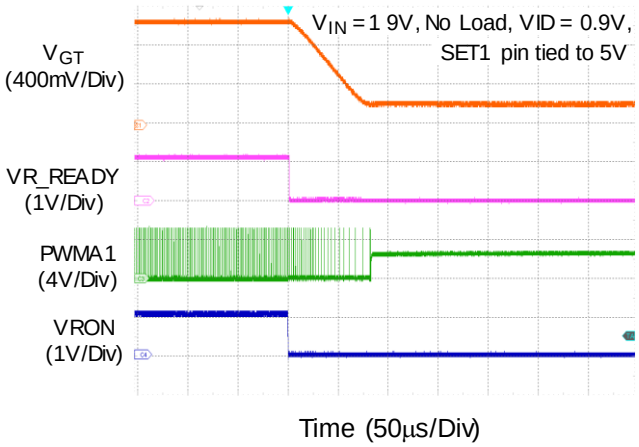
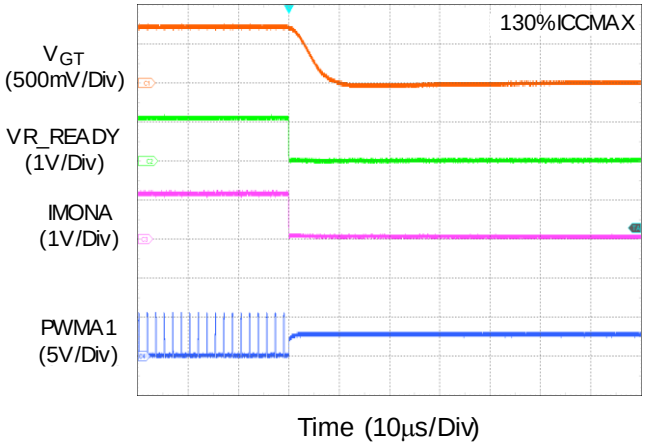


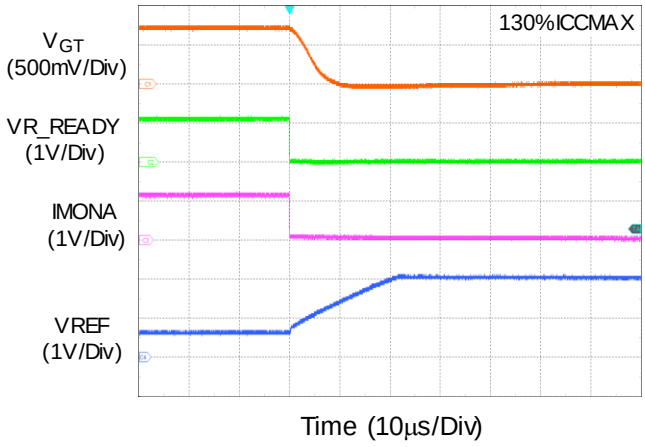
GT VR Power Off from EN



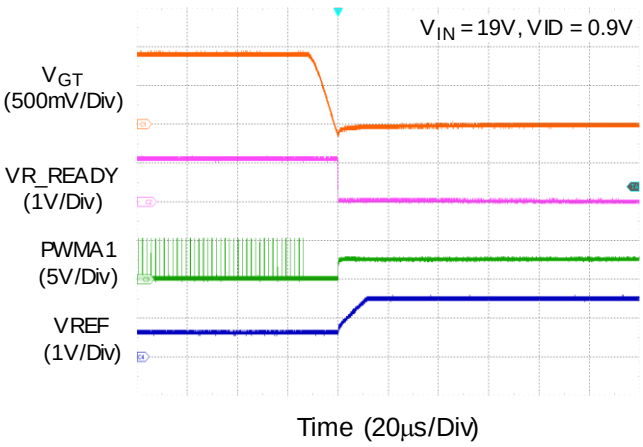
GT VR OCP



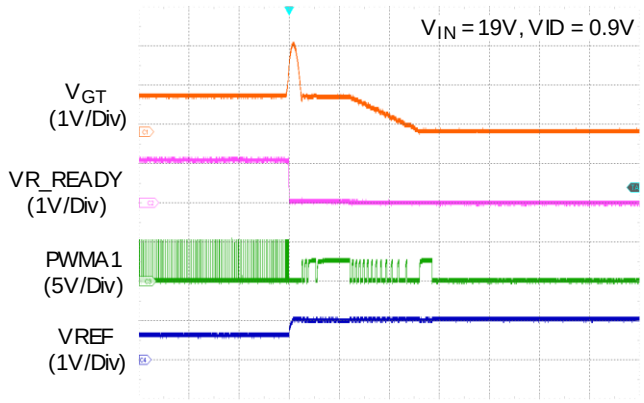
GT VR OCP



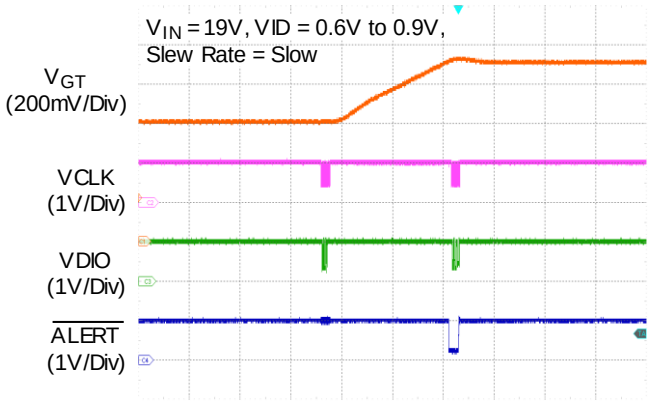
GT VR UVP



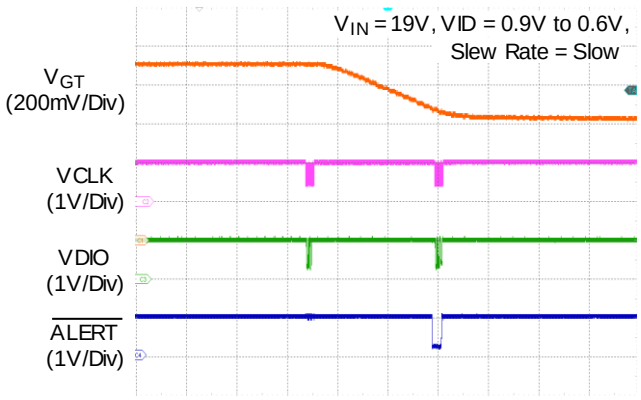
GT VR OVP



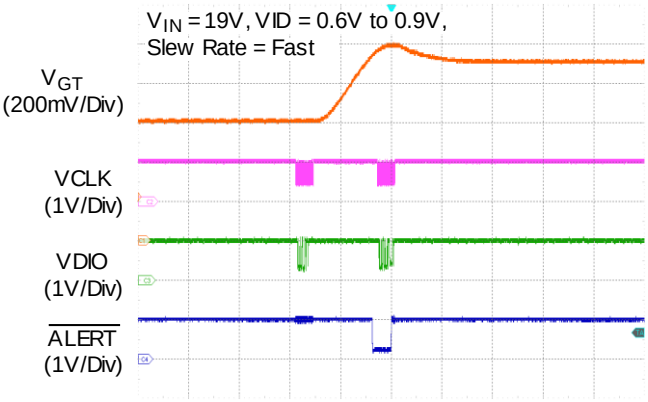
GT VR Dynamic VID Up



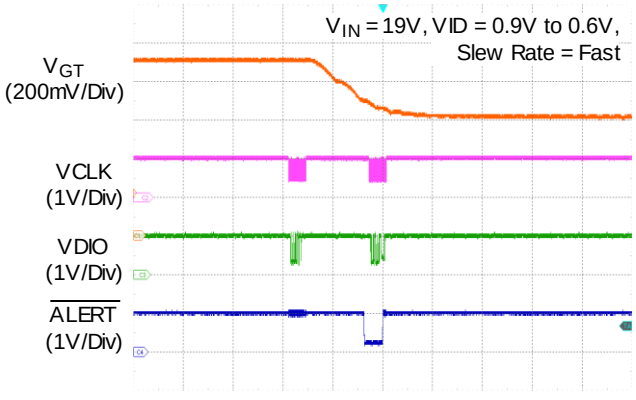
GT VR Dynamic VID Down



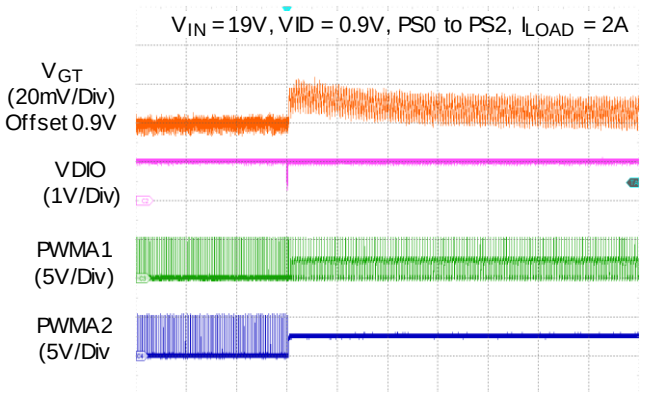
GT VR Dynamic VID Up



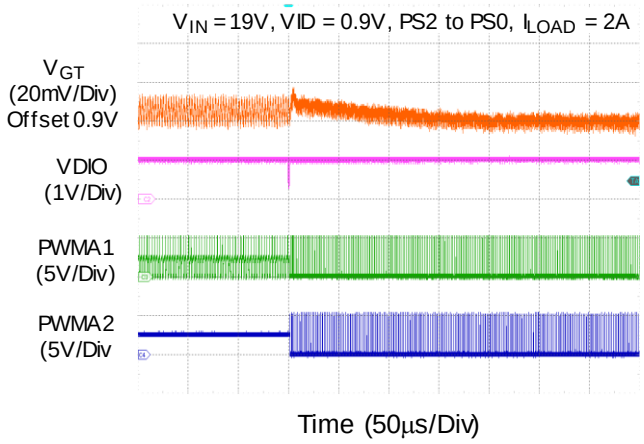
GT VR Dynamic VID Down



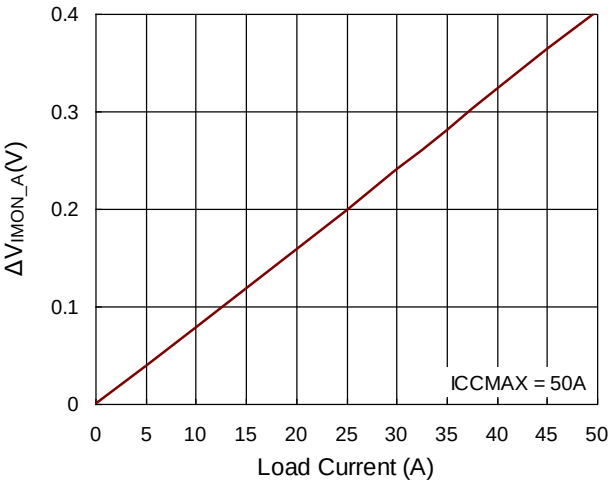
GT VR Mode Transient



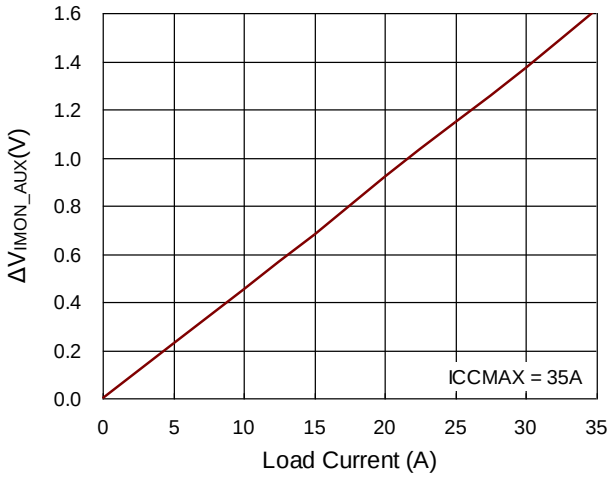
GT VR Mode Transient



ΔV_{IMON_A} vs. Load Current



ΔV_{IMON_AUX} vs. Load Current



16 Operation

16.1 G-NAVP™ Control Mode

The RT3624PE adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When the sensed current signal reaches the sensed voltage signal, the RT3624PE generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage that is inverted and amplified signal of the output voltage while current loading increases. The COMP rises due to output voltage drop. Then rising COMP forces PWM turn-on earlier and closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage, and the corresponding output voltage is in the steady state of lower voltage. The load-line, output voltage droping which is proportional to loading current, is achieved.

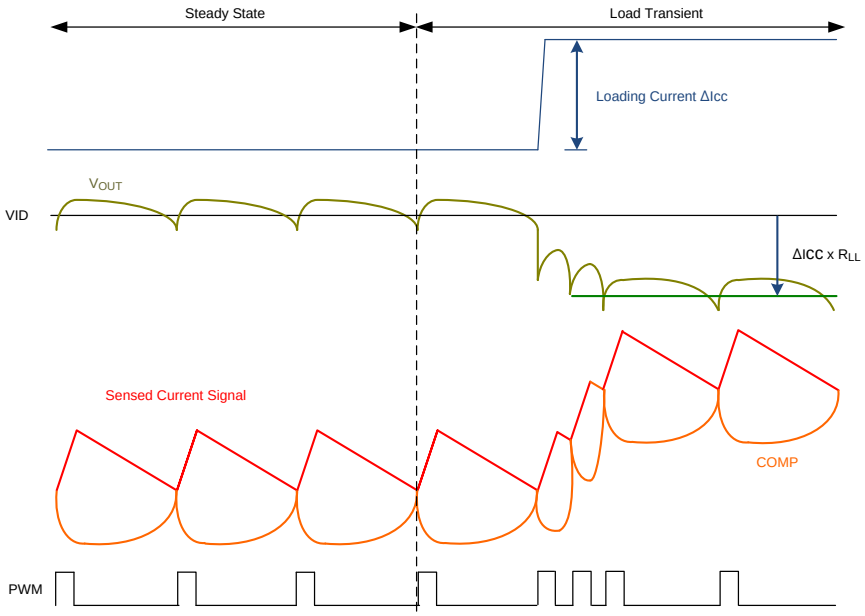


Figure 1. G-NAVP™ Behavior Waveform

16.2 SVID Interface/Control Logic/Configuration Registers

SVID Interface receives or transmits SVID signal with CPU. Control Logic executes commands (Read/Write registers, setVID, setPS) and sends related signals to control VR. Configuration Registers include function setting registers and CPU required registers.

16.3 IMON Filter

IMON Filter is used to average current signal by an analog low-pass filter. It outputs $IMON_{AVG}$ to the MUX of ADC for current reporting.

16.4 MUX and ADC

The MUX supports the inputs for SET1, SET2, SET3, SET4, TSEN, TSENA, PSYS, $IMON_{AVG}$, $IMONA_{AVG}$, and $IMON\_AUX_{AVG}$. The ADC converts these analog signals to digital codes for reporting or function settings.

16.5 UVLO

The UVLO detects the VCC voltage. As VCC exceeds threshold, controller issues POR = high and waits VRON. After both POR and VRON are ready, the controller is enabled.

16.6 Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition, and PWM sequence.

16.7 DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to the setVID command, Control Logic dynamically changes the VID voltage to the target voltage with required slew rate.

16.8 ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally set finite DC gain. The output signal is COMP for PWM trigger.

16.9 PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, current balance, zero current detection, current reporting and overcurrent protection.

16.10 SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be set by PIN-SETTING(Ai[1:0]). It helps wide application range of DCR and load-line. SUM CSGM output is used for PWM trigger.

16.11 RAMP

The RAMP helps loop stability and transient response.

16.12 PWM CMP

The PWM comparator compares COMP signal with sum current signal based on RAMP to trigger PWM.

16.13 Offset Cancellation

The offset cancellation is based on VID, COMP voltage and current signal from SUM CSGM to control output voltage accurately.

16.14 Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

16.15 Zero Current Detection

Detects whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (anti-overshoot function).

16.16 OCP

The RT3624PE has two overcurrent protection mechanisms, sum OCP and OC limit.

16.17 OVP

The overvoltage protection threshold is linked to VID. Please refer to classification table and waveform in Table 13, Figure 20, and Figure 21.

16.18 UVP

When the output voltage is lower than VID-650mV with 3μs filter time, UVP is triggered and all PWMs are in tri-state to turn off high-side power MOSFETs.

17 Application Information

(Note 6)

The RT3624PE includes two voltage rails: a 4/3/2/1 phase synchronous buck controller, the CORE VR, and a 2/1 phase synchronous buck controller, the AXG VR, designed to meet Intel IMVP9.1 compatible CPUs specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save total pin number for easy use increasing PCB space utilization. The RT3624PE is used in desktop computers or notebook computers.

17.1 Power-ON Sequence

In order to confirm sufficient power supply for proper operation, the VR triggers UVLO if VCC voltage drops below 4.2V (max). UVLO protection shuts down controller and forces high-side MOSFET and low-side MOSFET off. When VCC > 4.45V(max), RT3624PE issues POR = high and waits for VRON signal. After POR=high and VRON > 0.7V, controller powers on (Chip Enable = H) and starts VR internal settings, which include internal circuit offset correction and function settings (PIN-SETTING). The VRON is recommended to be ready after SPS VDD POR. Users can set multi-functions through SETx, TSEN and TSENA pins. Figure 2 shows the typical timing of controller power-on. The pull-high power of VRON pin is recommended as 1.05V, the same power for SVID interface. That can ensure SVID power is ready while VRON = H. Driver power (VDD) is strongly suggested to be ready after VCC. This can prevent current flow back to VCC from VDD through PWMx pin or DRVEN pin.

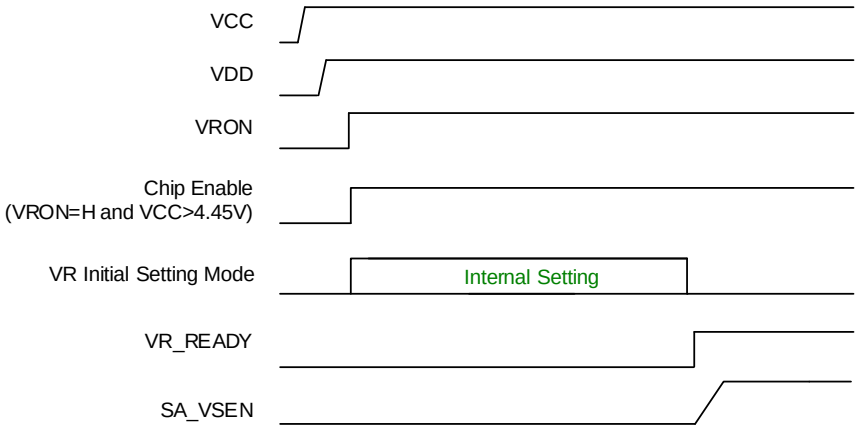


Figure 2. Typical Timing of Controller Power-ON

17.2 Maximum Active Phases Number Setting

The number of active phases is determined by ISENxN voltages. The detection is only active and latched at Chip Enable rising edge (VRON = H and VCC > 4.45V). While voltage at ISENxN > (VCC – 0.5V), maximum active phase number is (x-1). For example, pulling ISEN4N to VCC programs is a 3-phase operation, while pulling ISEN3N to VCC programs a 2-phase operation. The unused ISENxP pins are recommended to connect to VCC and the unused PWM pins can be floating. Figure 3 is a 3-phase operation example.

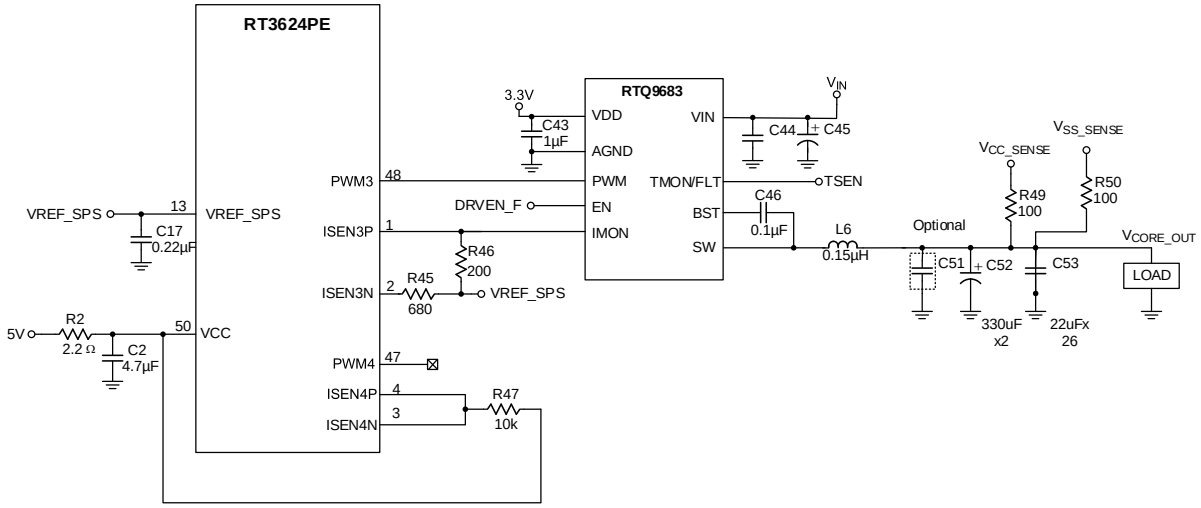


Figure 3. 3-Phases Operation Setting

17.3 Rail Disable

Pulling ISEN1N to VCC programs CORE rail disabled. The unused ISENxP pins are recommended to connect to VCC and the unused PWMx pins can be floating. Pulling ISENA1N to VCC programs AXG rail disabled. The unused ISENAxP pins are recommended to connect to VCC and the unused PWMAx pins can be floating. Pulling the PSYS pin to (VCC – 0.5V) programs input power domain rail disabled. RT3624PE rejects any commands to the input power domain rail. The unused ISENP_AUX pin and ISENN_AUX pin are recommended to connect to VCC.

17.4 Acoustic Noise Suppression

The RT3624PE supports acoustic noise suppression function for reducing acoustic noise induced by piezoelectric effect from MLCC. As output voltage transition occurs, especially in dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band and the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3624PE adopts acoustic noise suppression function which is enabled by pulling ANS pin to VCC to reduce ΔV when SetVID down and SetVID Decay down in DEM mode.

17.5 PIN-SETTING Mechanism

The RT3624PE provides multiple parameters for platform setting and BOM optimization. These parameters can be set through SETx and TSEN pins. The RT3624PE adopts two-step PIN-SETTING mechanism to maximize IC pin utilization. Figure 4 illustrates this operating mechanism for SETx.

The Vdivider and Vcurrent can be represented as follows:

$$V_{divider} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{current} = \frac{R2}{R1+R2} \times 3.2V + 80uA \times \frac{R1 \times R2}{R1+R2}$$

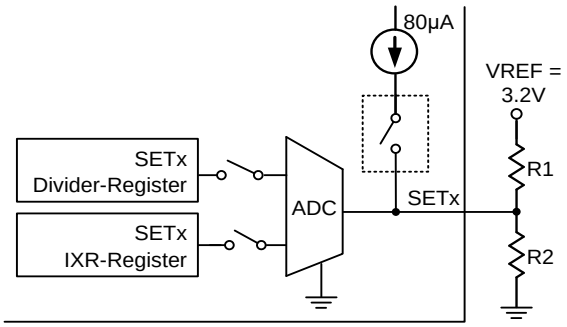


Figure 4. Operating Mechanism for SETx

Divider-Register and IXR-Register set the specified functions. For example, Divider-Register of SET1 sets VBOOT and ICCMAX of CORE rail; IXR-Register of SET1 sets AXG rail ICCMAX. All setting functions are summarized in Table 1.

Table 1. Summary of Pin Setting Functions

		Function Setting	Symbol	Description
SET1	Divider Register [4]	Setting VBOOT of CORE rail	VBOOT[4]	VBOOT[4] = 0, 0V VBOOT[4] = 1, non-zero
	Divider Register[3:0]	CORE VR ICCMAX	ICCMAX[3:0]	According to Platform, set CORE VR's corresponding ICCMAX.
	IXR Register[4:1]	AXG VR ICCMAX	ICCMAX_A[4:1]	According to Platform, set AXG VR's corresponding ICCMAX.
SET2	Divider Register[4]	Setting VBOOT of AXG rail	VBOOT_A[4]	VBOOT_A[4] = 0, 0V VBOOT_A[4] = 1, non-zero
	Divider Register[3]	Selectable VID table	VIDT[3]	VIDT[3] = 0, VID1(0V~1.52V) VIDT[3] = 1, VID2(0V~2.74V)
	Divider Register[2:0]	CORE VR TON width setting (switching frequency)	k_{TON}[2:0]	According to required frequency, select adaptive k_{TON} parameter.
	IXR Register[4:2]	AUX VR ICCMAX	ICCMAX_AUX[4:2]	According to Platform, set AUX VR's corresponding ICCMAX.
	IXR Register[1]	Enable zero load-line for CORE and AXG VR	0LL[1]	0LL[1] = 0: Disable zero load-line 0LL[1] = 1: Enable zero load-line
SET3	Divider Register[4:3]	CORE VR undershoot suppression	UDS[4:3]	To improve undershoot by applying a positive offset at loading edge. Set trigger level.
	Divider Register[2]	DVID Fast slew rate	DVID fast_SR[2]	DVID fast_SR[2][0] = 00, 1/2*Fast_P DVID fast_SR[2][0] = 01, 3/4*Fast_P DVID fast_SR[2][0] = 10, Fast_P DVID fast_SR[2][0] = 11, Fast_S
	Divider Register[1]	CORE VR DVID voltage-compensation level	DVID_LIFT[1]	DVID_LIFT[1] = 0: 10uA DVID_LIFT[1] = 1: 20uA Current sink from FB pin
	Divider Register[0]	DVID Fast slew rate	DVID fast_SR[0]	DVID fast_SR[2][0] = 00, 1/2*Fast_P DVID fast_SR[2][0] = 01, 3/4*Fast_P DVID fast_SR[2][0] = 10, Fast_P DVID fast_SR[2][0] = 11, Fast_S
	IXR Register[4:3]	AXG VR undershoot suppression	UDS_A[4:3]	To improve undershoot by applying a positive offset at loading edge. Set trigger level.

		Function Setting	Symbol	Description
	IXR Register[2]	VR_HOT# assertion during DVID current limit	VR_HOT#_DVID[2]	VR_HOT#_DVID[2] = 0,Enable VR_HOT#_DVID[2] = 1,Disable
	IXR Register[1]	AXG VR DVID voltage-compensation level	DVID_LIFT_A[1]	DVID_LIFT_A[1] = 0: 10μA DVID_LIFT_A[1] = 1: 20μA Current sink from FB pin
SET4	Divider Register[4:3]	CORE VR Phase Extension	DBLR[4:3]	DBLR[4:3] = 00: Enable, Phase = 8 DBLR[4:3] = 01: Disable, Phase = 1~4 DBLR[4:3] = 10: Enable, Phase = 5 DBLR[4:3] = 11: Enable, Phase = 6
	Divider Register[2:0]	AXG VR TON width setting (switching frequency)	k_{TON_A}[2:0]	According to required frequency, select adaptive k_{TON_A} parameter.
	IXR Register[4:3]	CORE VR Current Gain	Ai[4:3]	Current gain setting
	IXR Register[2:1]	AXG VR Current Gain	Ai_A[2:1]	Current gain setting

Referring to PIN-SETTING tables, Table 2 to 9, users can search corresponding $V_{divider}$ or V_{IXR} according to the desired function setting combinations. Then SETx external resistors can be calculated as follows:

$$R1 = \frac{3.2V \times V_{IXR}}{80\mu A \times V_{divider}}$$

$$R2 = \frac{R1 \times V_{divider}}{3.2V - V_{divider}}$$

Richtek provides a Microsoft Excel-based design tool to calculate the desired PIN-SETTING resisters.

Table 2. SET1 Pin Setting for VBOOT and ICCMAX

$V_{divider\_SET1}$ (mV)	VBOOT	ICCMAX (A)						
		8 phase	6 phase	5 Phase	4 Phase	3 Phase	2 Phase	1 Phase
25	0V	240	180	160	142	105	50	20
75		248	186	166	148	110	55	23
125		256	192	172	154	115	60	26
175		264	198	178	160	120	65	29
225		272	204	184	166	125	70	32
275		280	210	190	172	130	75	35
325		288	216	196	178	135	80	38
375		296	222	202	184	140	85	41
425		304	228	208	190	145	90	44
475		312	234	214	196	150	95	47
525		320	240	220	202	155	100	50
575		328	246	226	208	160	105	53
625		336	252	232	214	165	110	56
675		344	258	238	220	170	115	59
725		352	264	244	226	175	120	62
775		Reserve						
825	non-zero	240	180	160	142	105	50	20
875		248	186	166	148	110	55	23
925		256	192	172	154	115	60	26
975		264	198	178	160	120	65	29
1025		272	204	184	166	125	70	32
1075		280	210	190	172	130	75	35
1125		288	216	196	178	135	80	38
1175		296	222	202	184	140	85	41
1225		304	228	208	190	145	90	44
1275		312	234	214	196	150	95	47
1325		320	240	220	202	155	100	50
1375		328	246	226	208	160	105	53
1425		336	252	232	214	165	110	56
1475		344	258	238	220	170	115	59
1525		352	264	244	226	175	120	62
1575		Reserve						

Table 3. SET1 Pin Setting for ICCMAX_A

V_{IXR_SET1} (mV)	ICCMAX_A (A)	
	2 Phase	1 Phase
50	50	20
150	55	23
250	60	26
350	65	29
450	70	32
550	75	35
650	80	38
750	85	41
850	90	44
950	95	47
1050	100	50
1150	105	53
1250	110	56
1350	115	59
1450	120	62
1550	Reserve	

Table 4. SET2 Pin Setting for VBOOT_A, VIDT and k_{TON}

$V_{divider\_SET2}$ (mV)	VBOOT_A	VIDT	k_{TON}
25	0V	VID1	0.64
75			0.82
125			1
175			1.18
225			1.36
275			1.55
325			1.73
375			2.27
425		VID2	0.64
475			0.82
525			1
575			1.18
625			1.36
675			1.55
725			1.73
775			2.27
825	non-zero	VID1	0.64
875			0.82
925			1
975			1.18
1025			1.36
1075			1.55
1125			1.73
1175			2.27
1225		VID2	0.64
1275			0.82
1325			1
1375			1.18
1425			1.36
1475			1.55
1525			1.73
1575			2.27

Table 5. SET2 Pin Setting for ICCMAX_AUX and 0LL

V_{IXR_SET2} (mV)	ICCMAX_AUX (A)	0LL
50	10	Disable
150		Enable
250	15	Disable
350		Enable
450	20	Disable
550		Enable
650	25	Disable
750		Enable
850	30	Disable
950		Enable
1050	35	Disable
1150		Enable
1250	40	Disable
1350		Enable
1450	55	Disable
1550		Enable

Table 6. SET3 Pin Setting for UDS, DVID_LIFT and DVID fast_SR

$V_{divider\_SET3}$ (mV)	UDS		DVID_LIFT	DVID fast_SR
	PS0	PS1		
25	Disable	Disable	10μA	1/2*Fast_P
75				3/4*Fast_P
125			20μA	1/2*Fast_P
175				3/4*Fast_P
225			10μA	Fast_P
275				Fast_S
325			20μA	Fast_P
375				Fast_S
425	200	125	10μA	1/2*Fast_P
475				3/4*Fast_P
525			20μA	1/2*Fast_P
575				3/4*Fast_P
625			10μA	Fast_P
675				Fast_S
725			20μA	Fast_P
775				Fast_S
825	200	175	10μA	1/2*Fast_P
875				3/4*Fast_P
925			20μA	1/2*Fast_P
975				3/4*Fast_P
1025			10μA	Fast_P
1075				Fast_S
1125			20μA	Fast_P
1175				Fast_S
1225	250	150	10μA	1/2*Fast_P
1275				3/4*Fast_P
1325			20μA	1/2*Fast_P
1375				3/4*Fast_P
1425			10μA	Fast_P
1475				Fast_S
1525			20μA	Fast_P
1575				Fast_S

Table 7. SET3 Pin Setting for UDS_A, $\overline{VR_HOT}$_DVID and DVID_LIFT_ A

V_{IXR_SET3} (mV)	UDS_A		$\overline{VR_HOT}$_DVID	DVID_LIFT_A
	PS0	PS1		
50	Disable	Disable	Enable	10μA
150				20μA
250			Disable	10μA
350				20μA
450	200	125	Enable	10μA
550				20μA
650			Disable	10μA
750				20μA
850	200	175	Enable	10μA
950				20μA
1050			Disable	10μA
1150				20μA
1250	250	150	Enable	10μA
1350				20μA
1450			Disable	10μA
1550				20μA

Table 8. SET4 Pin Setting for DBLR and k_{TON_A}

$V_{divider\_SET4}$ (mV)	DBLR	k_{TON_A}
25	Enable DBLR 8phase	0.64
75		0.82
125		1
175		1.18
225		1.36
275		1.55
325		1.73
375		2.27
425	Disable DBLR	0.64
475		0.82
525		1
575		1.18
625		1.36
675		1.55
725		1.73
775		2.27
825	Enable DBLR 5 phase	0.64
875		0.82
925		1
975		1.18
1025		1.36
1075		1.55
1125		1.73
1175		2.27
1225	Enable DBLR 6 phase	0.64
1275		0.82
1325		1
1375		1.18
1425		1.36
1475		1.55
1525		1.73
1575		2.27

Table 9. SET4 Pin Setting for Ai and Ai_A

V_{TSEN} (mV)	Ai	Ai_A
50	0.25	0.25
150		0.5
250		0.75
350		1
450	0.5	0.25
550		0.5
650		0.75
750		1
850	0.75	0.25
950		0.5
1050		0.75
1150		1
1250	1	0.25
1350		0.5
1450		0.75
1550		1

17.6 Thermal Monitoring and Indicator

The RT3624PE supports smart power stages (SPS) with dedicated temperature monitors. VTSEN voltage represents temperature information at 8mV/°C + 0.6V.

The Controller processes the TSEN pin voltage to report temperature zone register.

When the TSEN pin voltage is higher than 1.4V, the $\overline{VR\_HOT}$ is pulled low to indicate thermal hot. The signal is an open-drain signal, and an external pull-up resistor is required. Thermal Register data is updated every 75μs and the averaging interval is 600μs. The $\overline{VR\_HOT}$ signal can be used to inform the system that the temperature of the voltage regulator is too high and the load should reduce its power consumption. $\overline{VR\_HOT}$ only indicates a thermal warning, not a fault.

17.7 System Input Power Monitoring (PSYS)

The RT3624PE provides PSYS function to monitor total platform system power and report to the CPU via SVID interface. The PSYS function can be illustrated as in Figure 5. PSYS meter measures system input current and outputs a proportional current signal I_{PSYS}. R_{PSYS} is designed for the P_{SYS} voltage = 1.6V with maximum I_{PSYS} for 100% system input power. 1.6V is a full-scale analog signal for FFh digitized code.

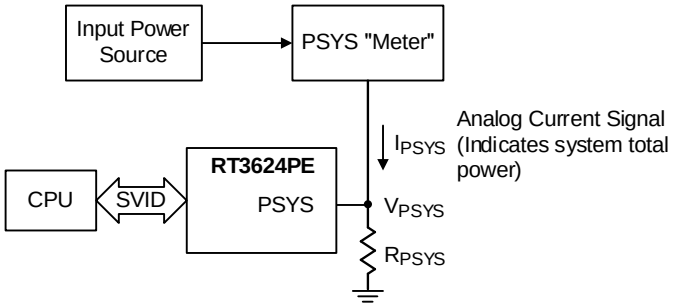


Figure 5. PSYS Function Block Diagram

17.8 System Input Voltage Monitoring (VSYS)

The RT3624PE provides optional VSYS function to monitor system input voltage. The threshold can be set through SVID interface and FFh digitized code indicates for 24V input voltage (24V/255 pre code). If input voltage is lower than critical threshold, controller asserts $\overline{VR\_HOT}$.

17.9 Zero Load-Line

The RT3624PE can also support enable zero load-line function. When zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current like load-line system behavior. The RT3624PE adopts AC-droop to effectively suppress load transient ring back and control overshoot for zero load-line application. Figure 6 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back $\Delta V2$ due to C area charge. Figure 7 shows the condition with AC-droop control. While loading occurs, controller changes VID target to short-term voltage target temporarily. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as the following:

$$Short\_Term\_Voltage\_Target = VID - \Delta I_{CC} \times R_{LL}$$

The setting method of R_{LL} is the same as load-line system. The short-term voltage target reverts to VID target slowly after a period of time. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back $\Delta V2$ can be suppressed. The overshoot amplitude is reduced to only $\Delta V3$.

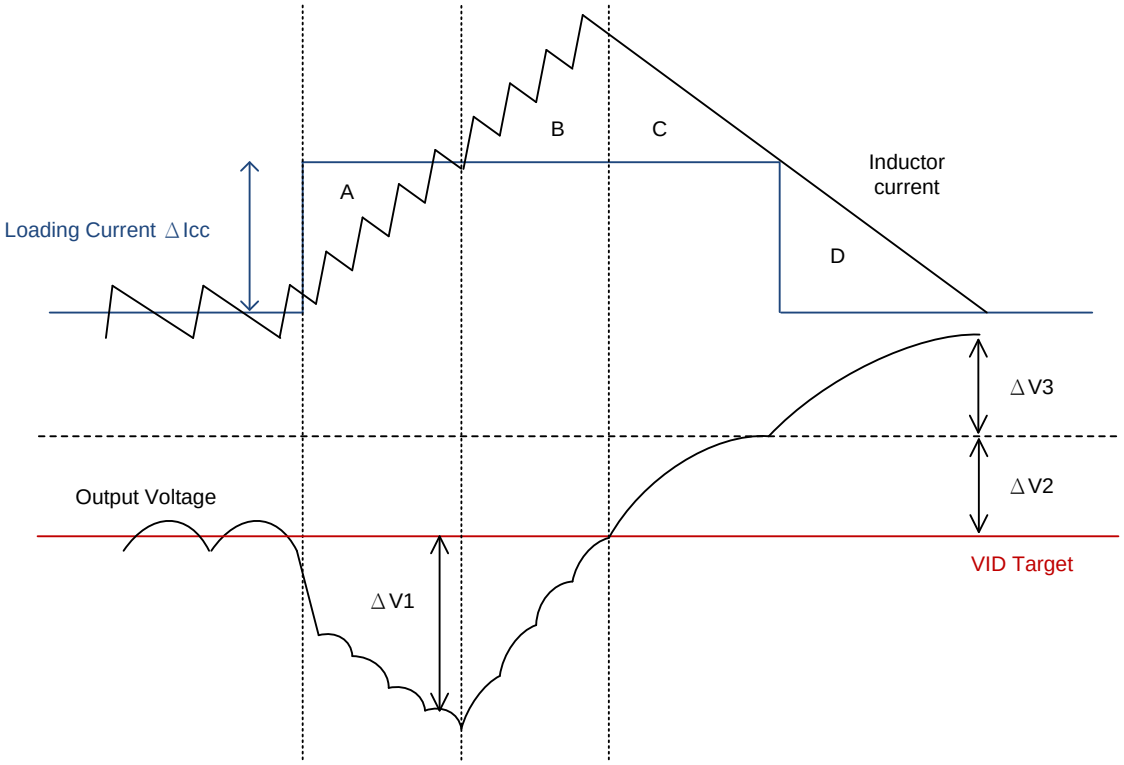


Figure 6. Zero Load-line without AC-droop Control

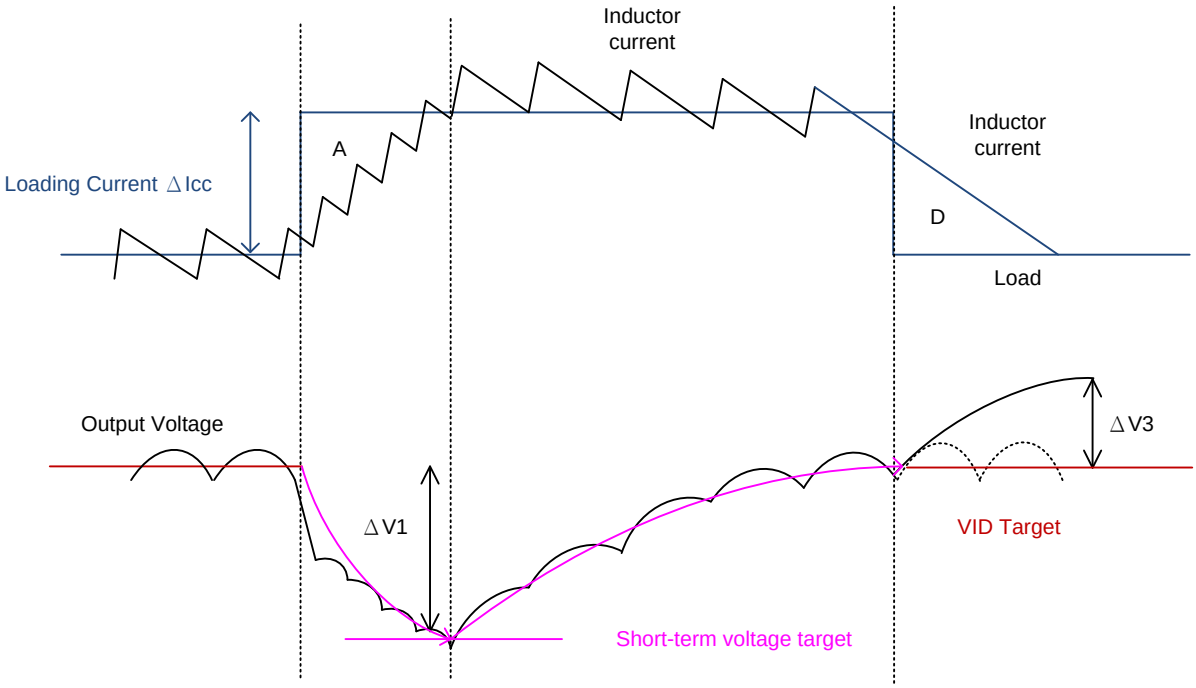


Figure 7. Zero Load-line with AC-droop Control

17.10 Per Phase Current Sense

To achieve higher efficiency, the RT362PE adopts SPS current sensing to get each phase current signal, as illustrated in Figure 8. SPS current sense is accomplished by sensing each SPS IOUT output individually using a 1.3V buffer VREF_SPS pin to provide biasing for the current sense signal. Differential voltage range of current sense input (VCSIN = ISENxP - ISENxN) is -10mV~80mV.

For I-type SPS, SPS IOUT output current represents current information at 5μA/A.

For I-type SPS,

$$I_{CS,PERx} = \frac{V_{CSIN}}{680} = \frac{I_{Lx} \times I_{SPS} \times R_{X2}}{680}$$

The current signal $I_{CS,PERx}$ is mirrored for load-line control/current reporting, current balance and zero current. The mirrored current to IMON pin is one time of $I_{CS,PER}$. ($I_{IMON}=A_{MIRROR} \times I_{CS,PERx}$, $A_{MIRROR}=1$)

The current sense lines should be run as differential pairs from the SPS back to the RT3624PE on the same layer.

The AUX current sense is demonstrated in Figure 9. In this design, the R_{CS} is 1kΩ and the mirror-gain is 1.25 ($I_{IMON\_AUX} = A_{MIRROR} \times I_{CS\_AUX}$, $A_{MIRROR} = 1.25$)

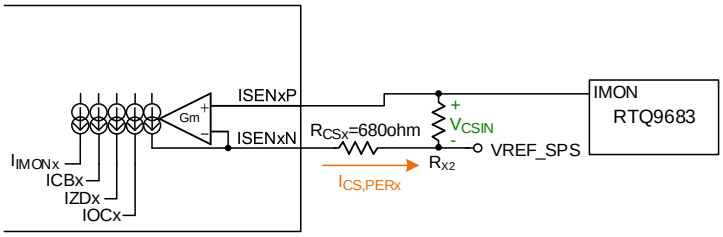


Figure 8. Current Type SPS Current Sensing Method for CORE/AXG

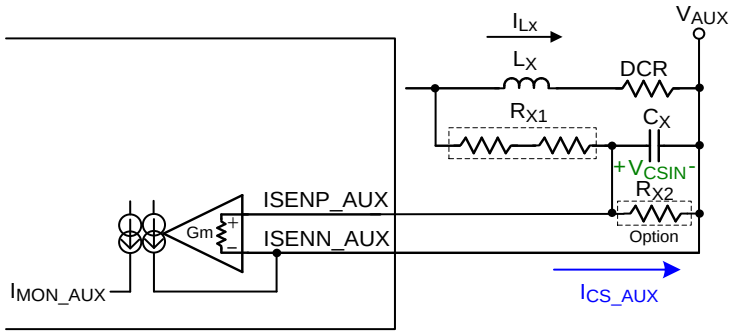


Figure 9. Inductor DCR Current Sensing Method for AUX

17.11 Total Current Sense/ICCMAX Setting/Current Monitoring

All phase current signals are gathered to IMON pin and converted to a voltage signal V_{IMON} by $R_{IMON,EQ}$ based on VREF pin. The VREF pin provides 0.6V voltage source (as presented as V_{REF}) during normal operation. The relationship between V_{IMON} and inductor current I_{Lx} is:

For I-type SPS,

$$V_{IMON} - V_{REF} = (I_{L1} + I_{L2} + ...) \times \frac{I_{SPS} \times R_{X2}}{680} \times R_{IMON,EQ}$$

$V_{IMON} - V_{REF}$ is proportional to output current. $V_{IMON} - V_{REF}$ is used for output current reporting and load-line loop-

control and sum over-current protection. For the reporting, V_{IMON} - V_{REF} is averaged by analog low-pass filter and then coded by 8-bit ADC. The digitized reporting value is scaled so that FFh = ICCMAX. The $R_{IMON, EQ}$ should be designed so that V_{IMON} − V_{REF} = V_{ICCMAX} while (I_{L1}+I_{L2}+…) = $ICCMAX_{CORE}$ = CORE ICC_MAX register value, where V_{ICCMAX} setting for each rail is shown below:

For CORE rail,

V_{ICCMAX}=0.8V, when ICCMAX>80A

V_{ICCMAX}=0.4V, when 80A≥ICCMAX≥40A

V_{ICCMAX}=0.2V, when 40A>ICCMAX

For AXG rail,

V_{ICCMAX}=0.4V, when ICCMAX≥40A

V_{ICCMAX}=0.2V, when 40A>ICCMAX

For AUX,

V_{ICCMAX}=1.6V for all ICCMAX setting

For load-line loop control, V_{IMON} − V_{REF} is scaled by Ai, that can be selected by Ai[1:0] of PIN-SETTING. The detailed application is described in the load-line setting section.

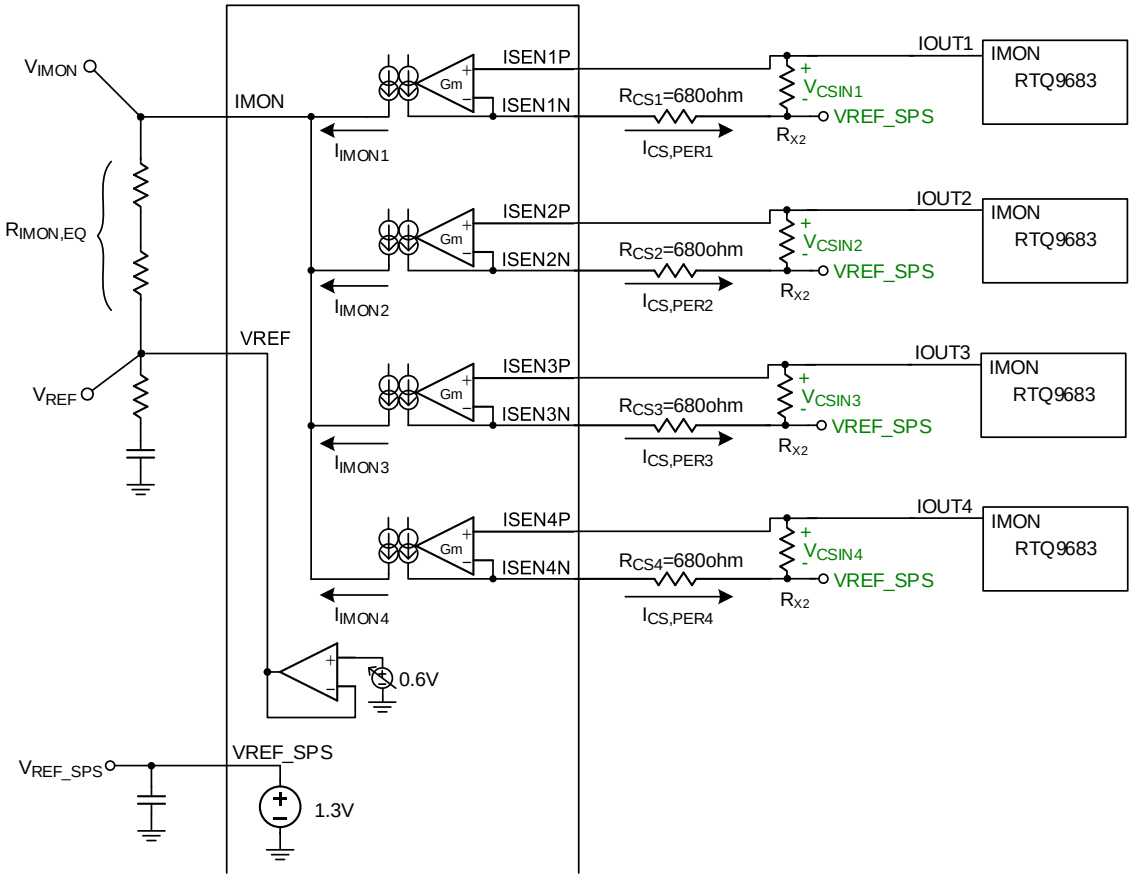


Figure 10. Total Current Sense Method

17.12 Load-line Setting (R_{LL})

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount proportional to the increasing loading current. The slope between output voltage and loading current (R_{LL}) is shown in Figure 11. Figure 12 shows the voltage and current loop circuits of the RT3624PE for the load-line control. The detailed equation is described as below:

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{680\Omega} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times \frac{3}{2}$$

Ai is current gain. $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested to be greater than 2 for better transient response. R_{LL} can be programmed by Ai and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be selected by PIN-SETTING of Ai[1:0] as listed in Table 10.

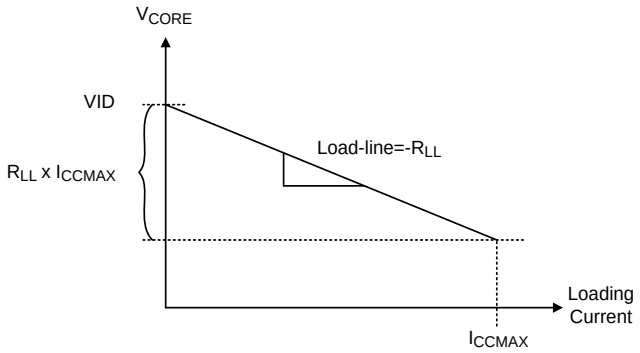


Figure 11. Load-line (Droop)

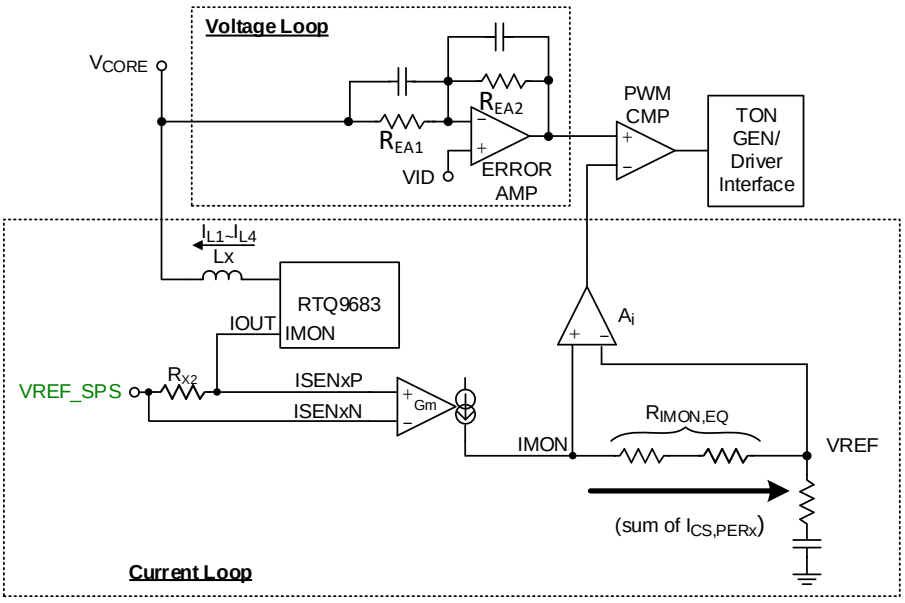


Figure 12. Voltage Loop and Current Loop for Load-line

Table 10. PIN-SETTING of Ai

Ai[1:0]	Current Gain Setting
00	0.25
01	0.50
10	0.75
11	1.00

17.13 Dynamic VID (DVID) Compensation

During DVID transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates the product of the DVID slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. The extra voltage drop approximates to DVID Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the load-line slope, Ω). This phenomenon is called the droop effect. How charging current affects loop is illustrated in Figure 13. The RT3624PE provides one DVID compensation function as shown in Figure 14. An internal current I_{DVID_LIFT} sinks internally from FB pin to generate DVID compensation, $I_{DVID\_LIFT} \times R_{EA1}$. I_{DVID_LIFT} for fast DVID SR can be set from SET3 PIN-SETTING of DVID_LIFT[1], 10μA and 20μA. For different scales of DVID SR, I_{DVID_LIFT} is internally adjusted. Compensating magnitude can also be adjusted by R_{EA1}. When DAC output reaches the target ($\overline{\text{ALERT}}$ issue timing), inductor current is still high and needs a time to settle down to the DC loading current. In the settling time, the falling down current keeps charging output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, DVID compensation can be less than DVID Slew Rate x Output Capacitance (Capacitance degeneration should be considered). While output capacitance is so large that DVID compensation cannot cover, adding a resistor and capacitor from FB to GND can also provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects DVID behavior. The final setting should be based on actual measurement.

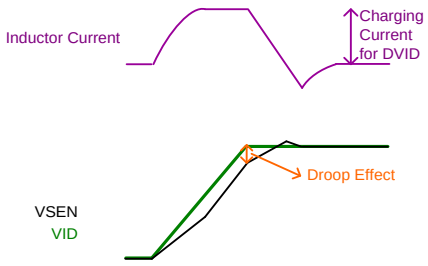


Figure 13. Droop Effect in VID Transition

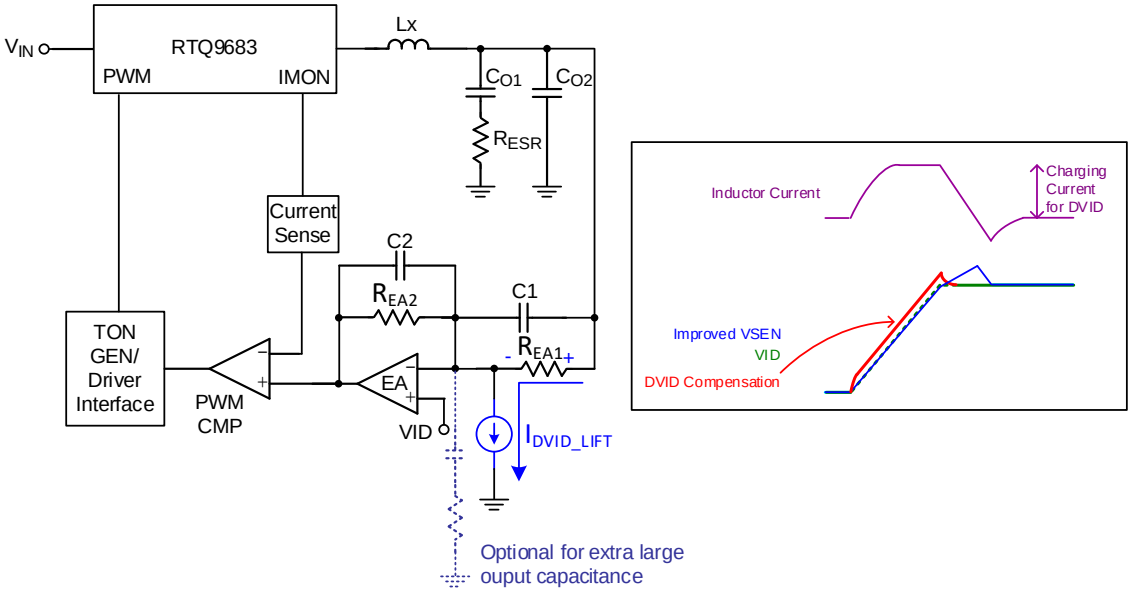


Figure 14. DVID Compensation

17.14 Compensator Design

The compensator of the RT3624PE does not need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP^{TM} topology to fine tune ACLL performance. The one pole and one zero compensator are shown in Figure 15. For IMVP9.1 ACLL specification, it is recommended to adjust compensator according to load transient ring back level. Refer to the design tool for default compensator values.

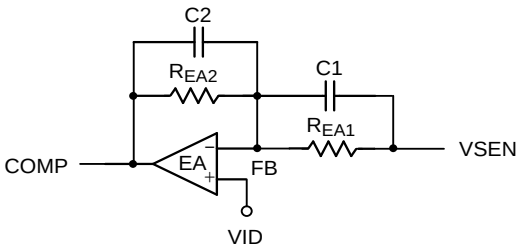


Figure 15. Type I Compensator

17.15 Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. The related connection is shown in Figure 16. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

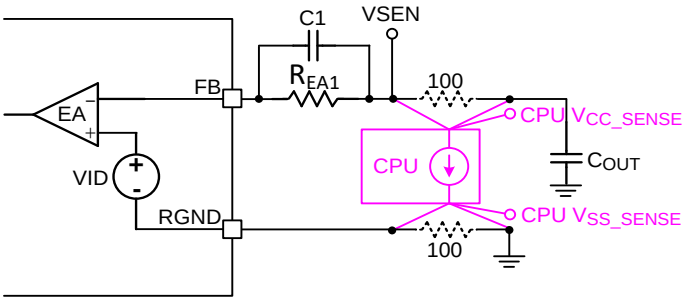


Figure 16. Remote Sensing Circuit

17.16 Switching Frequency Setting

The RT3624PE G-NAVP™ (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive TON (PWM) with input voltage (VIN) for better line regulation. The TON is also adaptive to VID voltage to achieve constant frequency concept. The constant switching frequency operation makes thermal estimation easy. The RT3624PE provides a parameter setting of kTON to design TON width. kTON is set by PIN-SETTING of kTON[2:0]. The related setting table is listed in Table 11.

The equations of TON are listed as below:

VID $\geq$ 0.93V

$$Ton=2.206u\times\frac{VID}{k_{TON}\cdot(VIN)}+14ns$$

VID $<$ 0.93V

$$Ton=2.05158u\times\frac{1}{k_{TON}\cdot(VIN)}+14ns$$

Table 11. PIN-SETTING of kTON

kTON[2:0]	kTON
000	0.64
001	0.82
010	1
011	1.18
100	1.36
101	1.55
110	1.73
111	2.27

The switching frequency can be derived from TON as shown below. The losses in the CORE power stage and driver characteristics are considered.

$$Freq=\frac{VID+\frac{I_{CC}}{N}\times\left(DCR+\frac{R_{ONLS,max}}{n_{LS}}-N\times R_{LL}\right)}{\left[V_{IN}+\frac{I_{CC}}{N}\times\left(\frac{R_{ONLS,max}}{n_{LS}}-\frac{R_{ONHS,max}}{n_{HS}}\right)\right]\times\left(T_{ON}-T_D+T_{ON,\,VAR}\right)+\frac{I_{CC}}{N}\times\frac{R_{ONLS,max}}{n_{LS}}\times T_D}$$

VID: VID voltage

VIN: input voltage

I_{CC}: loading current

N: total phase number

$R_{ON_{HS,max}}$: maximum equivalent high-side $R_{DS(ON)}$

n_{HS}: number of high-side MOSFETs

$R_{ON_{LS,max}}$: maximum equivalent low-side $R_{DS(ON)}$

n_{LS}: number of low-side MOSFETs.

T_D: summation of the high-side MOSFET delay time and rising time

$T_{ON, VAR}$: on-time variation value

DCR: inductor DCR

R_{LL}: load-line setting (Ω)

17.17 ACLL Performance Enhancement

The RT3624PE provides another optional function to improve undershoot by applying a positive offset at loading edge. Controller detects the COMP signal and compares it with steady state. While V_{COMP} variation exceeds a threshold, an additional positive offset is added to the output voltage. The threshold can be set through PIN-SETTING separately for PS0 and PS1 as listed in Table 12. The smaller index indicates that the detection is triggered easily. The positive offset is related to the compensation.

The ACLL performance enhancement threshold can approximate to $60mV/\frac{V_{EA2}}{V_{EA1}}$. In PS0, the slew rate of V_{RAMP} increases when the V_{COMP} intersects the positive offset in order to send out another on-time earlier to improve undershoot. In PS1, except for the positive offset, an additional 10mV is applied to the DAC and one pulse of PWM is also forced to turn on while the function is triggered. The positive offset is released gradually in about a hundred micro-second. Figure 17 and Figure 18 show undershoot suppression behavior in PS0 and PS1. For different platforms, the optimized setting is different. The final setting must be based on actual measurement.

Table 12. PIN-SETTING of Undershoot Suppression

UDS[1:0]	PS0 (Index)	PS1 (Index)
00	Disable	Disable
01	200	125
10	200	175
11	250	150

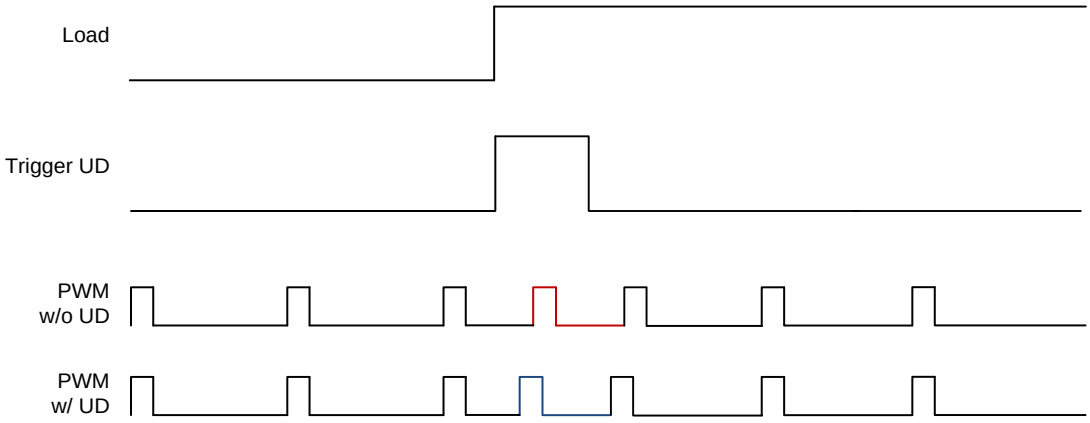


Figure 17. Undershoot Suppression Behavior in Multi Phase

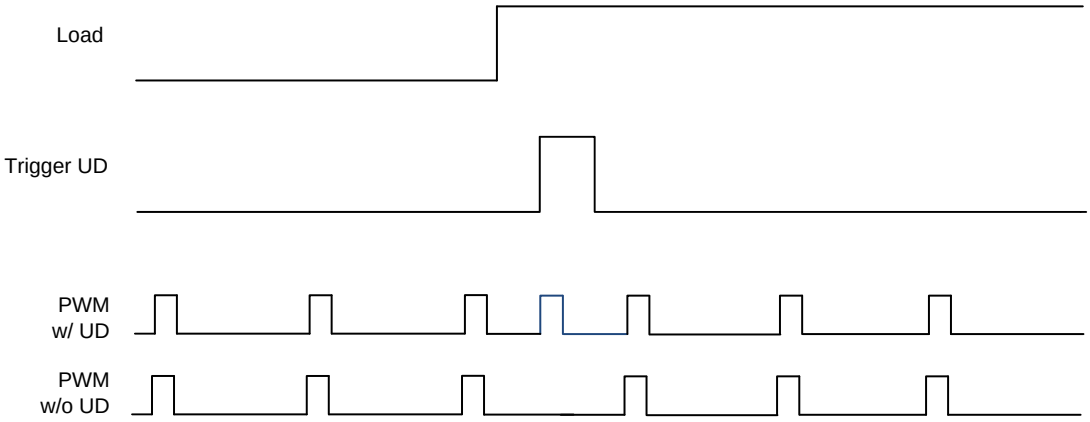


Figure 18. Undershoot Suppression Behavior in Single Phase

17.18 Overcurrent Protection (OCP)

The RT3624PE has sum OCP mechanisms and the threshold of sum OCP for PS0 is defined as

$$I_{SUM\_OC,PS0}=K_{SOCP}\times VIMON_{ICCMAX}\times\frac{R_{CS}}{DCR}\times\frac{1}{R_{IMON,EQ}}$$

$$I_{SUM\_OC,PS1,2,3}=K_{SOCP1}\times VIMON_{ICCMAX}\times\frac{R_{CS}}{DCR}\times\frac{1}{R_{IMON,EQ}}$$

ICCMAX<40, $K_{SOCP}=K_{SOCP1}=1.6$

ICCMAX≥40, $K_{SOCP}=1.3$, $K_{SOCP1}=\frac{1}{\text{phase number x }K_{SOCP}}$

While $R_{IMON,EQ}$ is designed exactly to meet $VIMON_{ICCMAX}$=ICCMAX register value$\times\frac{DCR}{680\Omega}\times R_{IMON,EQ}$, ICCMAX register value=ICCMAX, and $VIMON_{ICCMAX}$=0.2V, 0.4V or 0.8V according to ICCMAX.

Sum OCP threshold can be simplified as $I_{SUM\_OC,PS0}=K_{SOCP}\times ICCMAX$ and $I_{SUM\_OC,PS1,2,3}=K_{SOCP1}\times ICCMAX$. Note that the modification of ICCMAX register value cannot change sum OCP threshold.

While inductor current above sum OCP threshold lasts 40µs, controller de-asserts VR_READY and latches PWM in tri-state to turn off high-side and low-side power MOSFETs. Sum OCP is masked during DVID period plus 80µs after VID settles. it is also masked when VID = 0V condition.

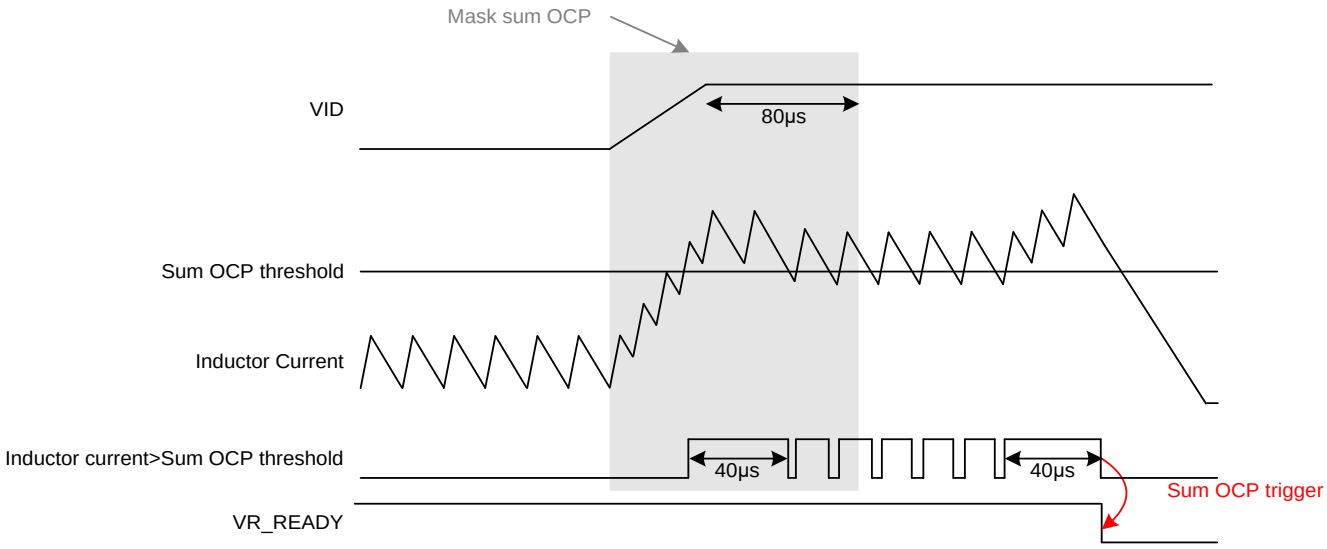


Figure 19. SUM OC Protection Mechanism

17.19 Overvoltage Protection (OVP)

The OVP threshold is linked with VID. The classification table is illustrated in Table 13. While VID = 0V, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, OVP threshold is 2.45V to allow not-fully-discharged VSEN. Otherwise, the OVP threshold is relative to VID and equals to VID+350mV with minimum limit = 1.35V. While VID ≤ 1.0V, the OVP threshold is limited at 1.35V.

The OV protection mechanism is illustrated in Figure 20 and Figure 21. When OVP is triggered with 0.5µs filter time, controller de-asserts VR_READY and forces all PWMs low to turn on low-side power MOSFETs. PWM remains low until the output voltage is pulled down to below 2.1V for DVID up from 0V and below VID for other conditions. After 60µs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWM is not allowed to turn on. Controller controls PWM to be low or tri-state to pull down the output voltage along with VID.

Table 13. Summary of Overvoltage Protection

VID Condition	OVP Threshold	Example	Protection Flag	Protection Action	Protection Reset
VID=0	OVP is masked.		VREF=1V		VCC/VRON Toggle
DVID up period from 0V to 1st PWM pulse after VID settles	2.45V			VR_READY latched low. The output voltage is pulled down to below 2.1V and then ramps down to 0V.	
DVID period from non-zero VID	VID+350mV if VID > 1.0V, 1.35V if VID ≤ 1.0V	VID = 1.2V, OVP threshold = 1.55V VID = 0.9V, OVP threshold = 1.35V		VR_READY latched low. The output voltage is pulled down to below VID and then ramps down to 0V.	
VID≠0	VID+350mV if VID > 1.0V, 1.35V if VID ≤ 1.0V	VID = 1.2V, OVP threshold = 1.55V VID = 0.9V, OVP threshold = 1.35V			

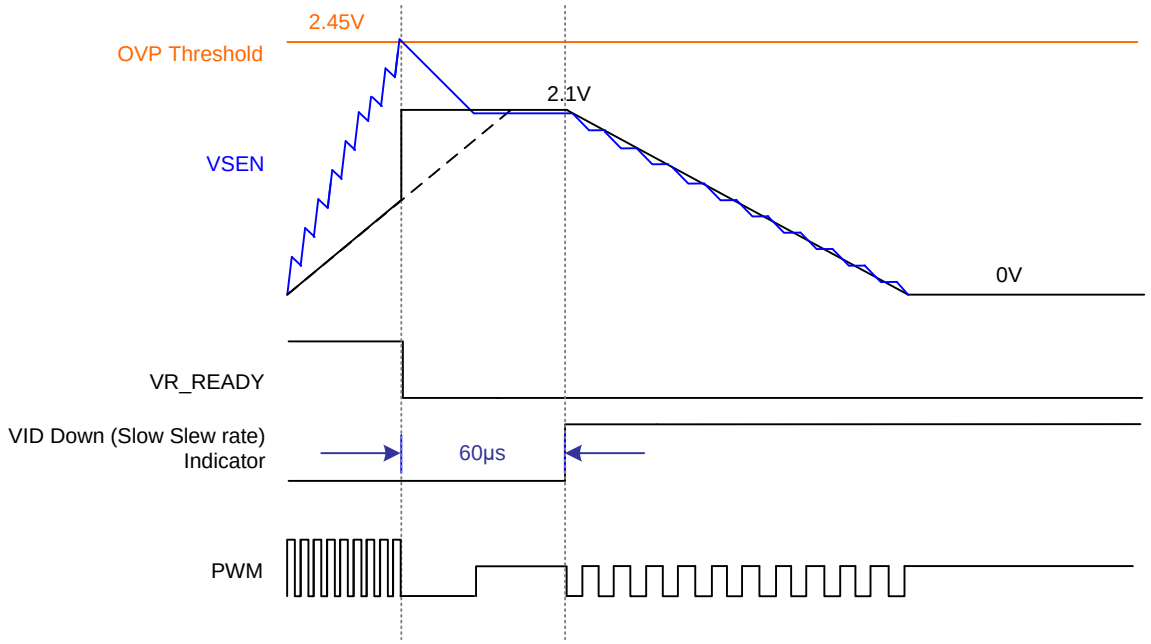


Figure 20. Overvoltage Protection Mechanism for DVID up from 0V

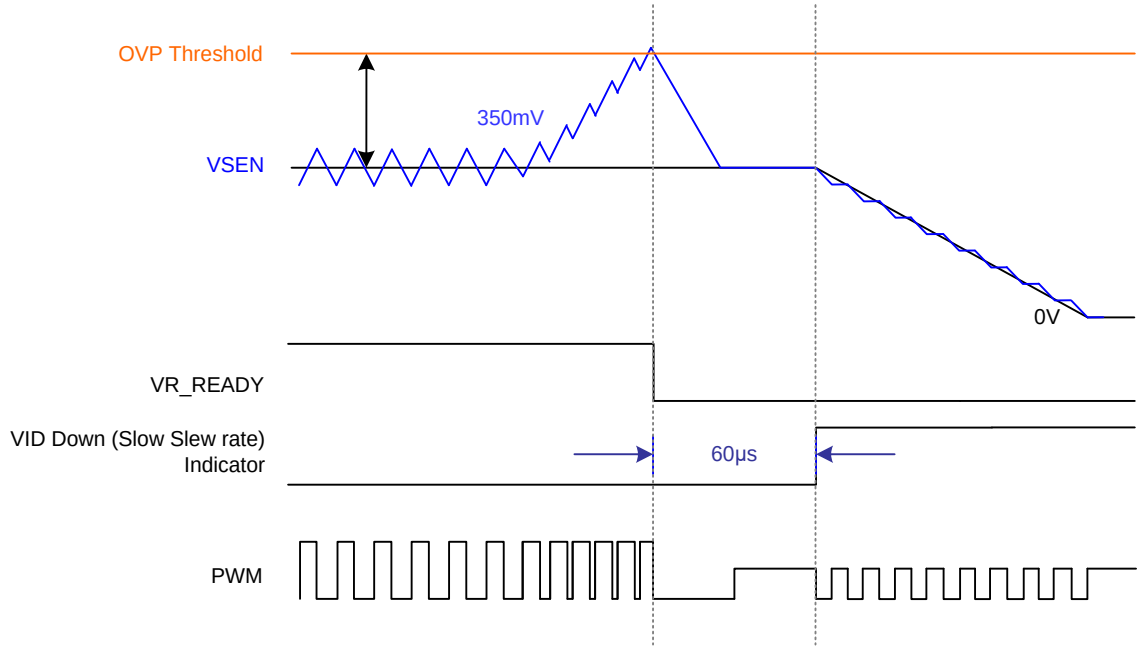


Figure 21. Overvoltage Protection Mechanism

17.20 Undervoltage Protection

When the output voltage is lower than VID-650mV with 3µs filter time, UVP is triggered and all PWMs are in tri-state to turn off high-side and low-side power MOSFETs. UVP is masked during DVID period and 80µs after VID settles. The mechanism is illustrated in Figure 22.

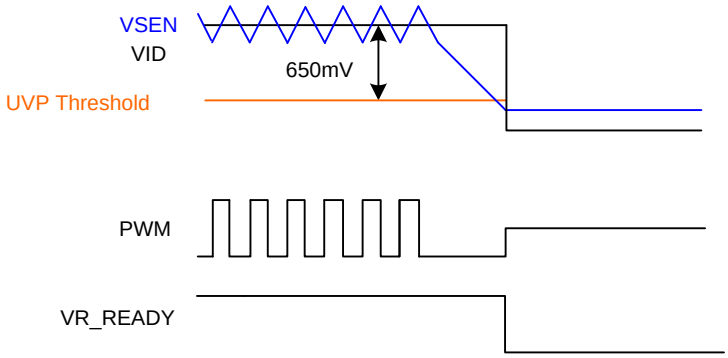


Figure 22. Undervoltage Protection Mechanism

All protections are reset only by VCC/VRON toggle. UVP and OCP protections are listed in Table 14. Note that the real filter time also depends on the magnitude of detected signal. The signal magnitude affects analog comparator's overdrive voltage and output slew rate. The RT3624PE provides a protection flag to promptly determine which kind of protection is triggered. As protection happens, VREF is forced to be 1V/1.5V/2V for OVP/UVP/SUM_OCP, respectively.

Table 14. Summary of UVP and OCP Protection

Protection Type	Protection Threshold	Protection Flag	Protection Action	DVID mask time	Protection Reset
Sum OCP for PS0	$I_{SUM\_OC,PS0}=K_{SOCP}\times VIMON_{ICCMAX}\times\frac{R_{CS}}{DCR}\times\frac{1}{R_{IMON,EQ}}$	VREF=2V	PWM tri-state, VR_READY latched low	DVID +80µs	VCC/ VRON Toggle
Sum OCP for non PS0	$I_{SUM\_OC,PS1,2,3}=K_{SOCP1}\times VIMON_{ICCMAX}\times\frac{R_{CS}}{DCR}\times\frac{1}{R_{IMON,E}}$	VREF=2V			
UVP	VID-650mV	VREF=1.5V			

17.21 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-
ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-52L 6x6 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (26.5°C/W) = 3.77W for a WQFN-52L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 23 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

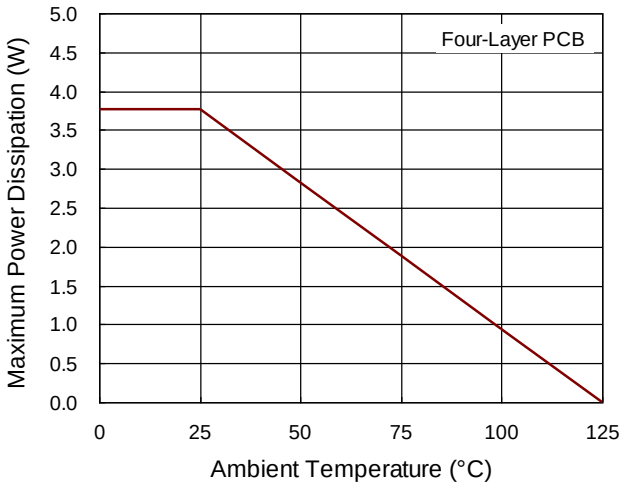
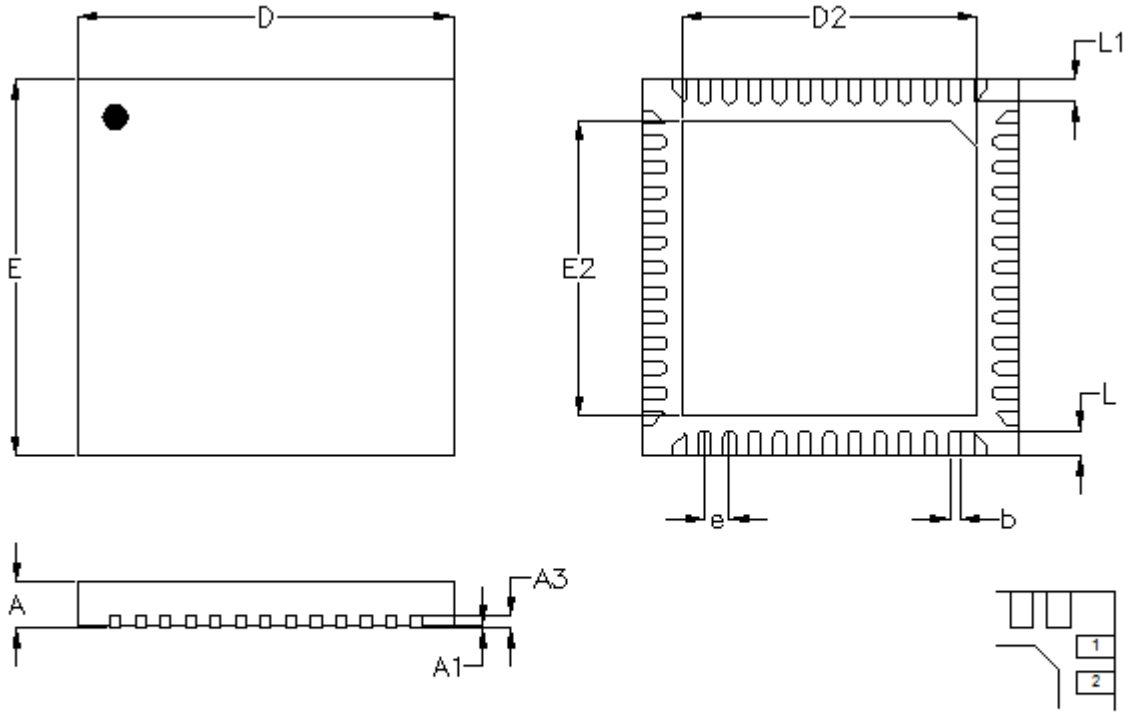


Figure 23. Derating Curve of Maximum Power Dissipation

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

18 Outline Dimension



DETAIL A

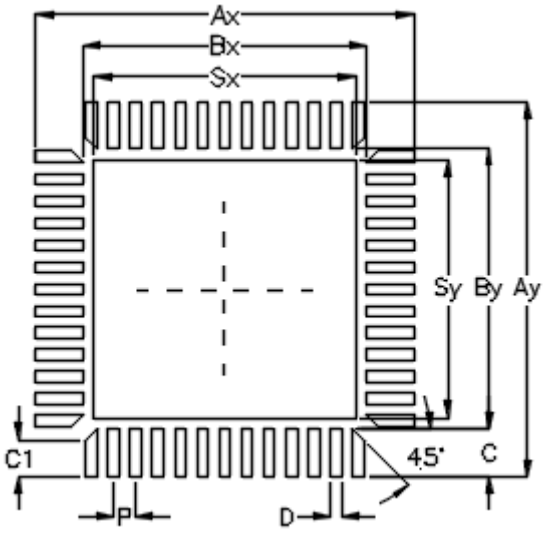
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

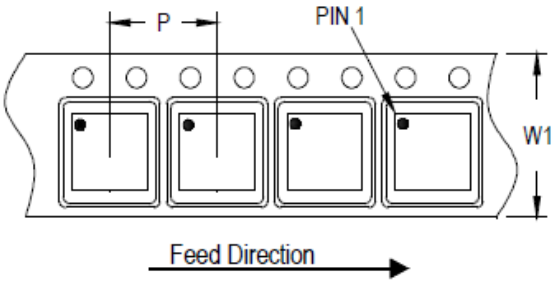
19 Footprint Information

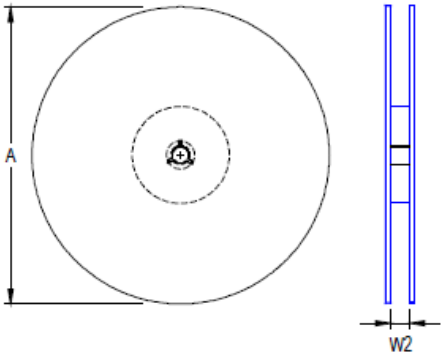


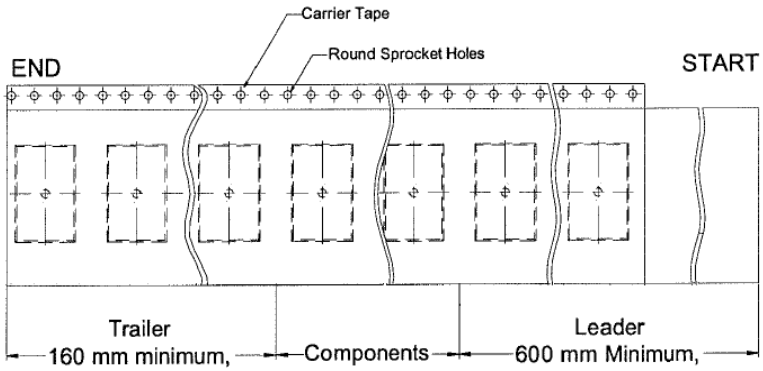
Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*52	C1*8	D	Sx	Sy	
V/W/U/XQFN6*6-52	52	0.40	6.80	6.80	5.10	5.10	0.85	0.65	0.20	4.70	4.70	±0.05

20 Packing Information

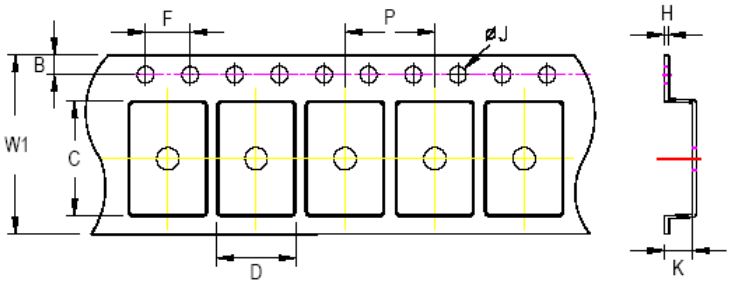
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 6x6	16	12	330	13	2,500	160	600	16.4/18.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
QFN and DFN 6x6	13”	2,500	Box G	1	2,500	Carton A	6	15,000

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/6/28	Final	