Quadruple Channel PWM Controller with I²C Interface for IMVP9.3 CPU Core Power Supply

1 General Description

The RT3645BE is a synchronous VR controller with quadruple output rails and is fully compliant with Intel IMVP9.3 PWM specification. The RT3645BE adopts Richtek's new generation of hybrid control architecture. The hybrid control achieves fast dynamic response without using external passive components for loop compensation. The control loop settings can be easily programmed through the I²C interface, simplifying the process of setting the droop control to meet all AVP (Adaptive Voltage Positioning) requirements for CPU core power.

The RT3645BE features Richtek's new generation transient technique, AQR (Adaptive Quick Response), to optimize AVP performance during load transients and reduce output capacitance. The RT3645BE controller adopts SPM (Smart Phase Management) technique with programmable current thresholds and hysteresis to optimize system efficiency. The RT3645BE incorporates a high-accuracy ADC for multiple signal telemetry, including input voltage, output current, temperature sensing for each rail and system power monitoring. An MTP NVM (Multiple-Time Programmable Non-Volatile Memory) is integrated into the RT3645BE to store custom configurations, such as droop control settings, ICCMAX current, switching frequency, and SPM current thresholds. The configurations can be selected by placing a specified resistor between the ADDR pin and GND. The RT3645BE also supports fault protections, including undervoltage-lockout (UVLO), undervoltage (UV), overvoltage (OV), overcurrent (OC), and SPS fault indication. The recommended junction temperature range is –40°C to 125°C.

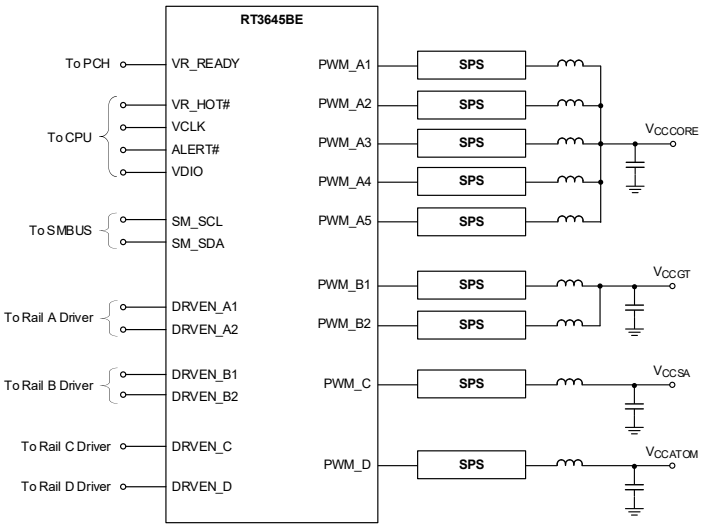
2 Features

- **Compliant with Intel IMVP9.3 Specification**
- **5/4/3/2/1 Phases (CORE VR) + 2/1 Phases (GT VR) + 1 Phase (SA VR) + 1 Phase (ATOM VR)**
- **Hybrid Control Architecture without External RC Components**
- **Good Stability and Fast Dynamic Performance: Adaptive Ramp and Quick Response**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-In ADC for Signal Monitoring and Telemetry**
- **DVID Enhancement**
- **Zero Load-Line**
- **Smart Phase Control for Efficiency Optimization**
- **Support Fast V-Mode (FVM)**
- **VR Ready and Thermal Indicator**
- **Soldering Good Detection**
- **Standard I2C Protocol Interface**
  - **Flexible Address Options**
  - **Built-In Multiple-Time Programmable Non-Volatile Memory to Store Custom Configurations**
  - **Current Balance Control for Thermal Balance**
  - **Easy Internal Hybrid Control Loop Setting**
  - **Switching Frequency Setting**
  - **Fault Status and Protection Flags**

3 Applications

- Intel IMVP9.3 CPU Core Power
- Notebook and Desktop Computers
- AVP Buck Converters

4 Simplified Application Circuit



5 Ordering Information

RT3645BE □-□-□

- The configuration code identifier for the register setting stored in the internal NVM(2)
- **Packing**
  A: Standard
- **Package Type**(1)
  N: WQFN-52L 6x6 (W-Type)

Note 1.

- Marked with (1) indicates that Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates the default code does not have a configuration code identifier.

6 Marking Information

RT3645BEN-A

RT3645BEN: Product Code
YMDAN: Date Code

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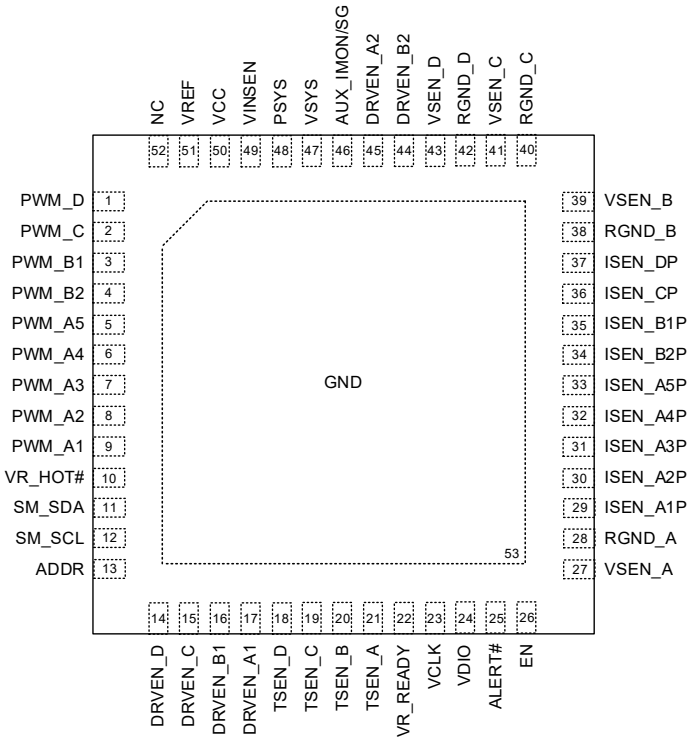
7 Pin Configuration

(TOP VIEW)



WQFN-52L 6x6

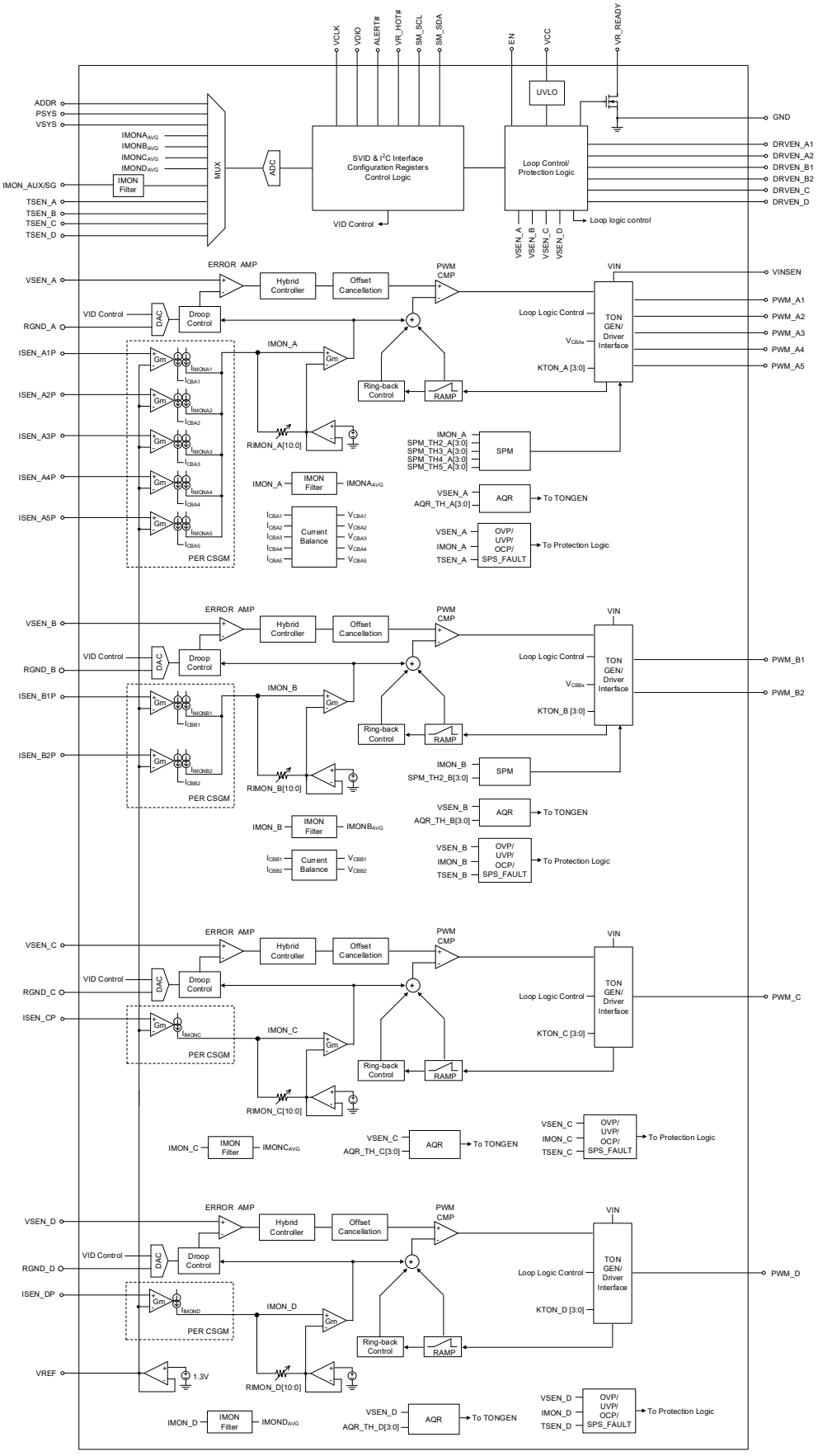
8 Functional Pin Description

Pin No.	Pin Name	Pin Description
1	PWM_D	PWM output for rail D. Refer to the pin description for PWM_D.
2	PWM_C	PWM output for rail C. Refer to the pin description for PWM_C.
3	PWM_B1	PWM output for phase 1 of rail B. Refer to the pin description for PWM_B1.
4	PWM_B2	PWM output for phase 2 of rail B. Refer to the pin description for PWM_B2.
5	PWM_A5	PWM output for phase 5 of rail A. Refer to the pin description for PWM_A5.
6	PWM_A4	PWM output for phase 4 of rail A. Refer to the pin description for PWM_A4.
7	PWM_A3	PWM output for phase 3 of rail A. Refer to the pin description for PWM_A3.
8	PWM_A2	PWM output for phase 2 of rail A. Refer to the pin description for PWM_A2.
9	PWM_A1	PWM output for phase 1 of rail A. The tri-state level of the PWM output can be selected in NVM. This signal is used to drive the PWM input of FET driver ICs. Any unused PWM pin(s) should be left floating.
10	VR_HOT#	Thermal monitor output pin
11	SM_SDA	Data line for I^2C interface

Pin No.	Pin Name	Pin Description
12	SM_SCL	Clock input for I^2C interface
13	ADDR	This pin is used to set I^2C address. Connect the ADDR pin to GND with the specified resistor. Refer to the Application Information for the table of resistance values.
14	DRVEN_D	External driver mode control pin for rail D. Refer to the pin description for DRVEN_D.
15	DRVEN_C	External driver mode control pin for rail C. Refer to the pin description for DRVEN_C.
16	DRVEN_B1	External driver mode control pin for rail B. Refer to the pin description for DRVEN_B1. Connect DRVEN_B1 to the 1st phase of rail B.
17	DRVEN_A1	External driver mode control pin for rail A. The output high level is VCC. This pin becomes floating when a PS4 command is received. Connect DRVEN_A1 to the 1st phase of rail A.
18	TSEN_D	Thermal sense input for rail D
19	TSEN_C	Thermal sense input for rail C
20	TSEN_B	Thermal sense input for rail B
21	TSEN_A	Thermal sense input for rail A
22	VR_READY	VR ready indicator. This open-drain output requires an external pull-up resistor. VR_READY is pulled low when EN goes low or when a fault event is detected in the active output rails.
23	VCLK	SVID synchronous clock input pin
24	VDIO	SVID synchronous data transmission line
25	ALERT#	SVID alert signal (active low). This open-drain output requires an external pull-up resistor.
26	EN	Controller enable pin. A logic high level enables the controller.
27	VSEN_A	Remote voltage sense input of rail A
28	RGND_A	Remote voltage sense return ground of rail A.
29	ISEN_A1P	Positive current sense input for phase 1 of rail A. Any unused ISEN pin(s) should be left floating.
30	ISEN_A2P	Positive current sense input for phase 2 of rail A
31	ISEN_A3P	Positive current sense input for phase 3 of rail A
32	ISEN_A4P	Positive current sense input for phase 4 of rail A
33	ISEN_A5P	Positive current sense input for phase 5 of rail A
34	ISEN_B2P	Positive current sense input for phase 2 of rail B
35	ISEN_B1P	Positive current sense input for phase 1 of rail B
36	ISEN_CP	Positive current sense input for rail C

Pin No.	Pin Name	Pin Description
37	ISEN_DP	Positive current sense input for rail D
38	RGND_B	Remote voltage sense return ground of rail B
39	VSEN_B	Remote voltage sense input of rail B
40	RGND_C	Remote voltage sense return ground of rail C
41	VSEN_C	Remote voltage sense input of rail C
42	RGND_D	Remote voltage sense return ground of rail D
43	VSEN_D	Remote voltage sense input of rail D
44	DRVEN_B2	External driver mode control pin for rail B. The output high level is VCC. This pin becomes floating when a PS4 command is received. Connect DRVEN_B2 to the 2nd phase of rail B.
45	DRVEN_A2	External driver mode control pin for rail A. The output high level is VCC. This pin becomes floating when a PS4 command is received. Connect DRVEN_A2 to the 2nd phase of rail A.
46	AUX_IMON/SG	Multi-function pin. • **Current monitoring**: Input pin for AUX VR rail current reporting. • **Soldering good**: When this pin is pulled high to over 3.0V during power-on and EN is at a logic high level, all rails ramp up to VBOOT if the controller soldering is good. • **Fault indicator**: Indicates OVP, OCP, UVP, and SPS faults.
47	VSYS	System input voltage monitoring pin. No external attenuator is required. Do not connect a low-pass filter to this pin to ensure correct detection of fast VSYS events.
48	PSYS	System power monitoring input pin
49	VINSEN	Input voltage sense input pin. Connect an external low-pass filter with a corner frequency less than one-tenth of the switching frequency to attenuate noise.
50	VCC	Controller power supply input pin. Connect this pin to 5V with an external RC filter (R = 1Ω, C = 4.7μF). The decoupling capacitor should be placed as close to the controller as possible.
51	VREF	Fixed 1.3V voltage source output. Connect this pin to GND with a 0.47 μF decoupling capacitor. The decoupling capacitor should be placed as close to the controller as possible.
52	NC	No connection
53 (Exposed pad)	GND	Grounding connection. The exposed pad should be soldered to a large ground pad with a sufficient number of vias to ensure proper power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VINSEN, VSYS to GND ---------- –0.3V to 28V
- VCC to GND ---------- –0.3V to 6.5V
- VCLK, VDIO, ALERT# to GND
  - DC ---------- –0.3V to 6.8V
  - < 10ns ---------- –0.45V to 7.5V
- RGND_A/B/C/D to GND ---------- –0.3V to 0.3V
- Other pins ---------- –0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –40°C to 125°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Susceptibility

(Note 3)

- HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- VINSEN, VSYS to GND ---------- 4.5V to 24V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5)

- WQFN-52L, 6x6, θ_{JA} ---------- 26.34°C/W
- WQFN-52L, 6x6, $\theta_{JC(Top)}$ ---------- 13.3°C/W

Note 5. For more information about thermal parameters, refer to the "Application and Definition of Thermal Resistances" report, AN061.

14 Electrical Characteristics

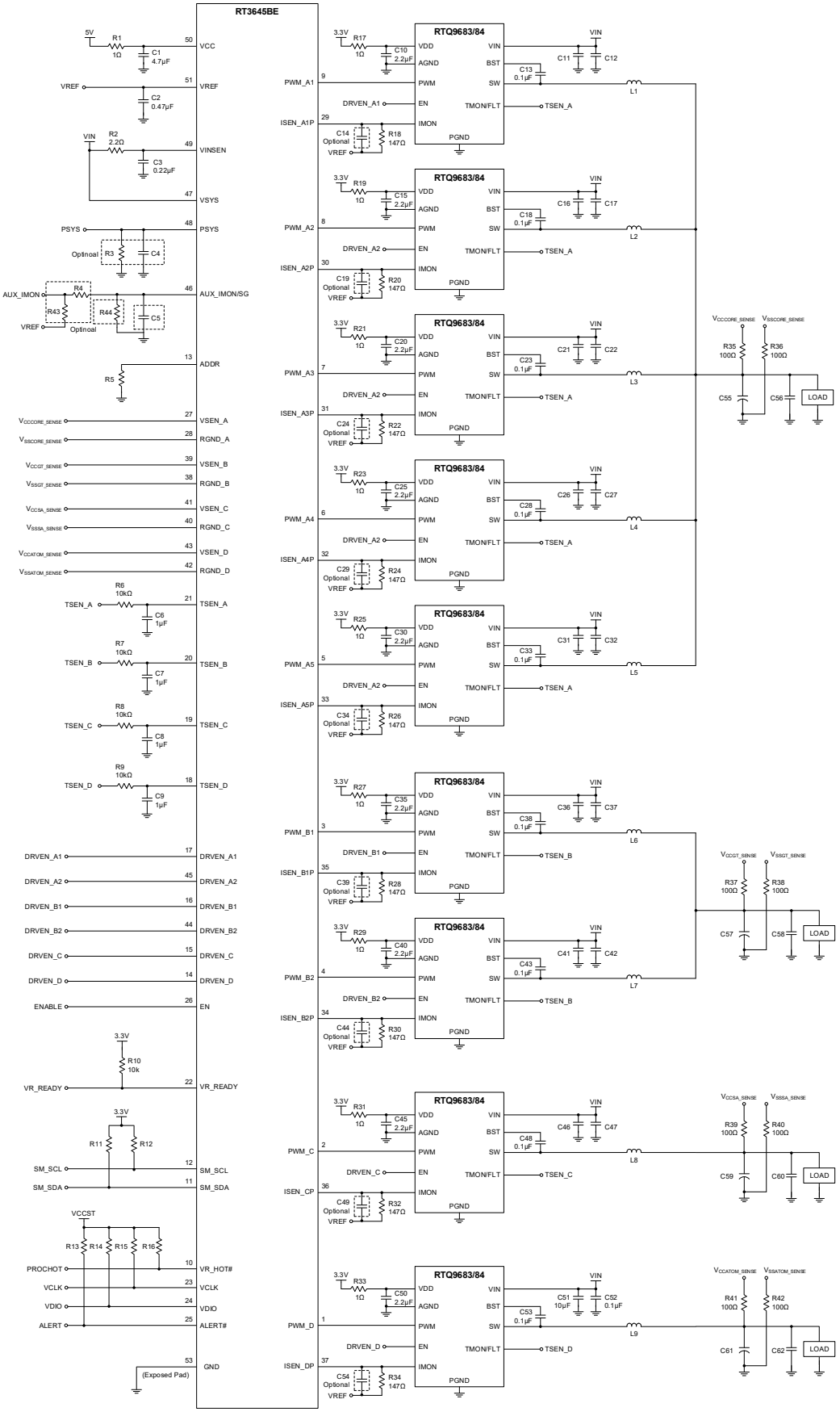
(V_{CC} = 5V, typical values are referenced to T_J = 25°C, Min/Max values are referenced to T_J from −10°C to 105°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{VCC}	EN = H, no switching	--	5.5	--	mA
Supply Current at PS2, VID = 0	I_{VCC_PS2}	EN = H, no switching	--	4.7	--	mA
Supply Current at PS3, VID = 0	I_{VCC_PS3}	EN = H, no switching	--	4.3	--	mA
Supply Current at PS4	I_{VCC_PS4}	EN = H, no switching	--	63	--	μA
Shutdown Current	I_{SHDN}	EN = L	--	53	--	μA
TON Setting (Rail A, B, C, and D)						
On-Time Setting	t_{ON}	V_{IN} = 12V, VID = 1.05V, K_{TON} = 3.2	--	105	--	ns
Minimum On-Time	$t_{ON(MIN)}$		40	--	--	ns
Minimum Off-Time	$t_{OFF(MIN)}$		--	160	--	ns
VREF						
Reference Voltage Output	V_{REF1p3}	Normal operation	1.2	1.3	1.4	V
Current Sensing Amplifier						
CS Input Voltage	V_{CSIN}	Recommended input range for high accuracy	–10	--	80	mV
Protections						
VCC Undervoltage Lockout	V_{UVLO_R}	Rising edge	4.2	--	4.45	V
	V_{UVLO_F}	Falling edge	4	--	4.3	V
	ΔV_{UVLO_HYS}	Rising edge hysteresis	100	170	250	mV
Undervoltage Protection	V_{UVP}	With respect to VID	–700	–650	–600	mV
Overvoltage Protection	V_{ROVP}	VID > 1V	320	350	380	mV
	V_{AOVP}	VID ≤ 1V	1.30	1.35	1.40	V
SPS Fault	V_{SPS_FAULT}		2.15	2.20	2.25	V
EN and VR_READY						
EN Input Voltage Rising Threshold	V_{EN_R}		0.7	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.3	V
EN Leakage Current	I_{LEAK_EN}	T_J = 25°C	–1	--	1	μA
VR_READY Pull Low Voltage	V_{RDY_L}		--	--	--	V
Serial VID and VR_HOT#						
VCLK, VDIO Logic High Level	V_{IH_SVID}		0.65	--	--	V
VCLK, VDIO Logic Low Level	V_{IL_SVID}		--	--	0.45	V
Leakage Current of VCLK, VDIO, ALERT# and VR_HOT#	I_{LEAK_SVID}		–1	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Low Voltage of VDIO, ALERT# and VR_HOT#	V_{OL_SVID}	I = 10mA	--	--	0.13	V
I²C Interface						
SCL, SDA Logic High Level	V_{IH_I2C}		1	--	--	V
SCL, SDA Logic Low Level	V_{IL_I2C}		--	--	0.6	V
SCL Clock Rate	f_{SCL}	Standard mode	--	100	--	kHz
		Fast mode	--	400	--	kHz
Rising Time of SCL, SDA	t_R	Standard mode	--	--	1000	ns
		Fast mode	20	--	300	ns
Falling Time of SCL, SDA	t_F	Standard mode	--	--	300	ns
		Fast mode	20	--	300	ns
Data Setup Time	$t_{SU,DAT}$	Standard mode	--	--	250	ns
		Fast mode	--	--	100	ns
Data Hold Time	$t_{HD,DAT}$	Standard mode	0	--	--	µs
		Fast mode	0	--	--	µs
Low Period of SCL Clock	t_{LOW}	Standard mode	4.7	--	0.9	µs
		Fast mode	1.3	--	--	µs
High Period of SCL Clock	t_{HIGH}	Standard mode	4.0	--	--	µs
		Fast mode	0.6	--	--	µs
Setup Time for Repeated START Condition	$t_{SU,STA}$		0.6	--	--	µs
Hold Time for Repeated START Condition	$t_{HD,STA}$		0.6	--	--	µs
Setup Time for STOP Condition	$t_{SU,STO}$		0.6	--	--	µs
Bus Free Time between STOP and START Condition	t_{BUF}		1.3	--	--	µs
SDA Output Low Sink Current	I_{OL}	SDA Voltage = 0.4V	2	--	--	mA
ADC						
ADC Resolution			--	10	--	bits
ADC Reference Voltage			--	3.2	--	V
PSYS Maximum Input Voltage	PSYS	V_{PSYS} = 1.6V	--	255	--	Decimal
VSYS Maximum Input Voltage	VSYS	V_{VSYS} = 24V	--	255	--	Decimal
Thermal Monitor						
TSEN Voltage for VR_HOT# Assertion	$V_{TSEN\_VRHOT\_L}$	TSEN_TYPE = 0 TSEN_VRHOT_TH = 0xA TSEN_VRHOT_HYS = 0x3 TSEN_ALERT_TH = 0x9 TSEN_ALERT_HYS = 0x3	--	1.4	--	mV
TSEN Voltage for VR_HOT# De-Assertion	$V_{TSEN\_VRHOT\_H}$		--	1.376	--	mV
TSEN Voltage for SVID ALERT# Assertion	$V_{TSEN\_ALERT\_L}$		--	1.376	--	mV
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω

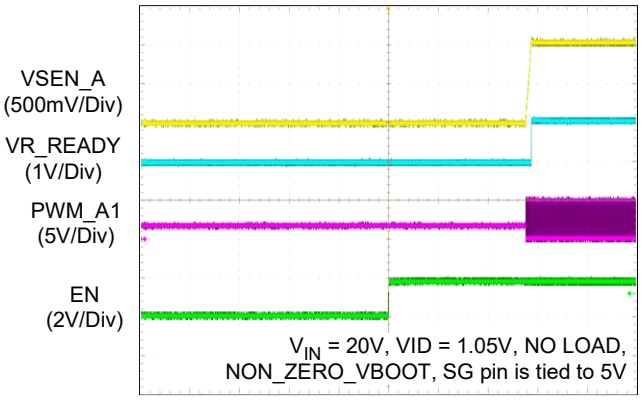
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
PWM Output						
PWMx Output High Level		I_{PWM_OUT} = 4mA	VCC – 0.16	--	--	V
PWMx Output Low Level		I_{PWM_OUT} = 4mA	--	--	0.08	V

15 Typical Application Circuit



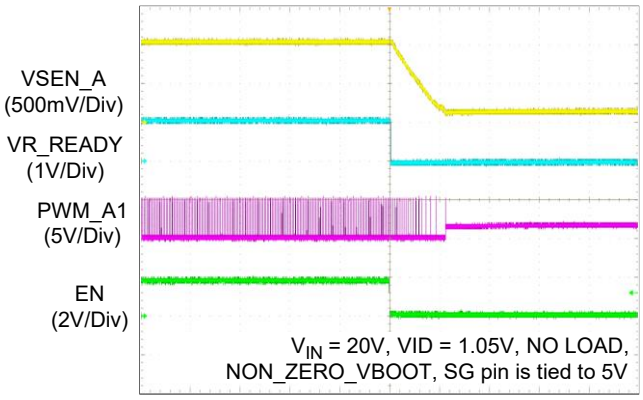
16 Typical Operating Characteristics

CORE VR Power On from EN



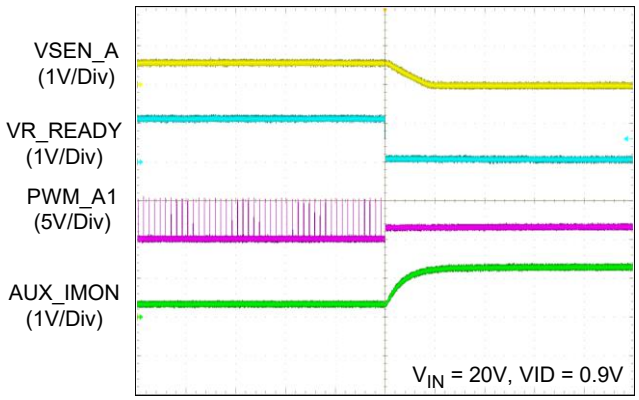
Time (500μs/Div)

CORE VR Power Off from EN



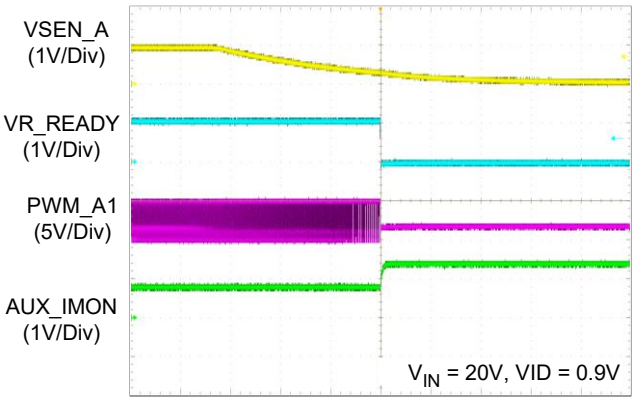
Time (50μs/Div)

CORE VR OCP



Time (20μs/Div)

CORE VR UVP



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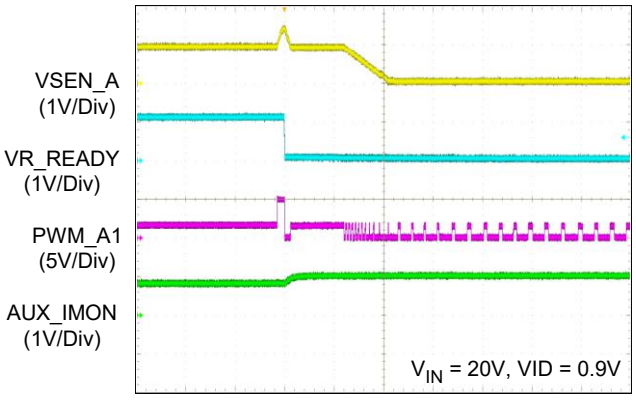
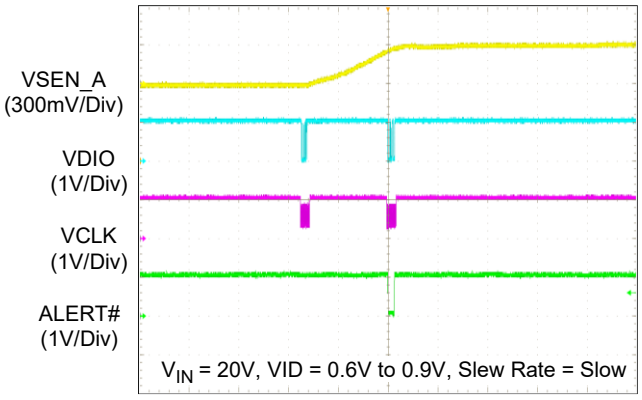
CORE VR OVP



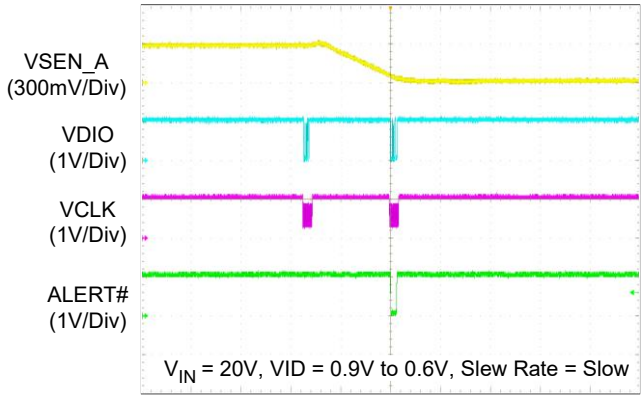
Time (50μs/Div)

CORE VR Dynamic VID Up



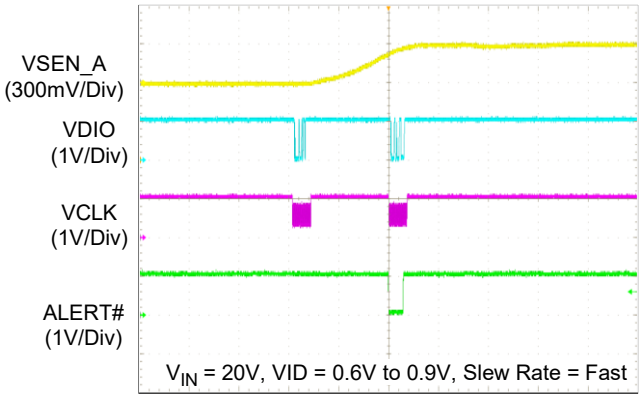
Time (10μs/Div)

CORE VR Dynamic VID Down



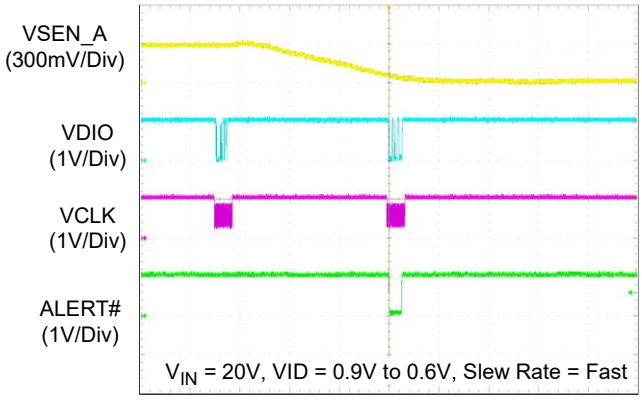
Time (10μs/Div)

CORE VR Dynamic VID Up



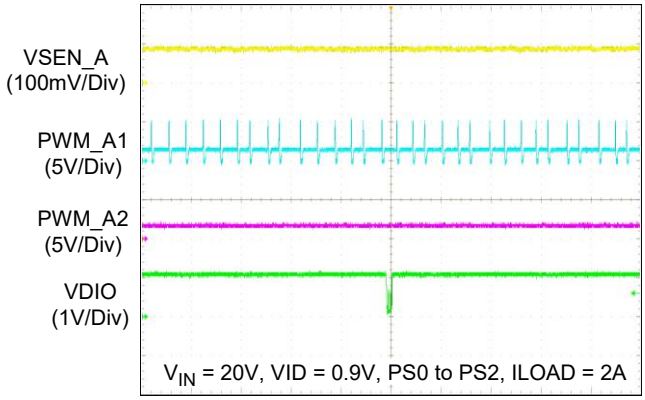
Time (5μs/Div)

CORE VR Dynamic VID Down



Time (5μs/Div)

CORE VR Mode Transient



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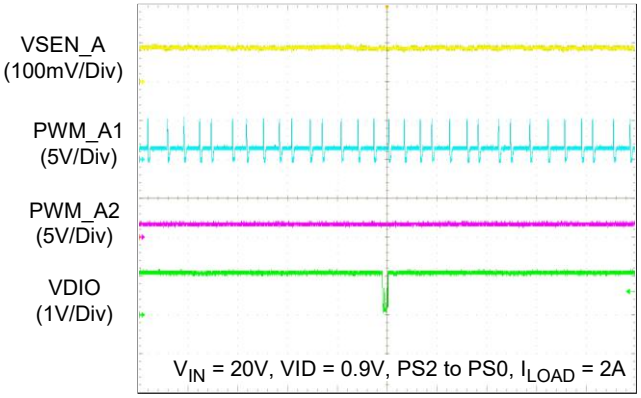
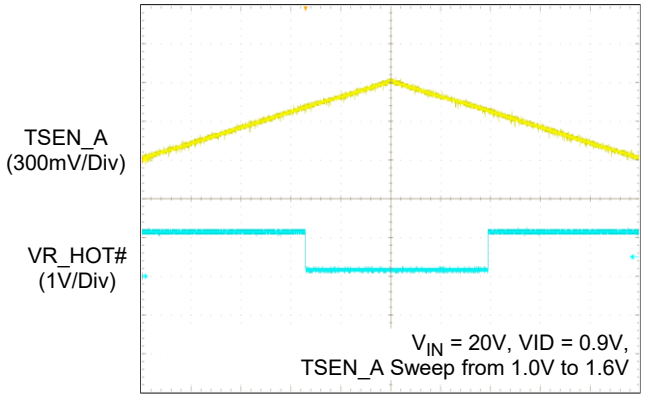
CORE VR Mode Transient



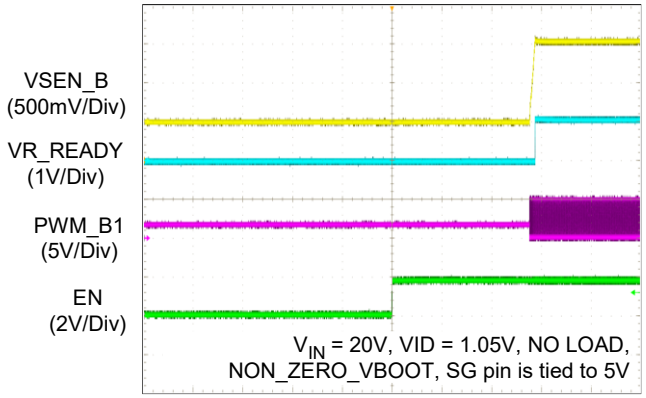
Time (5μs/Div)

CORE VR Thermal Monitoring



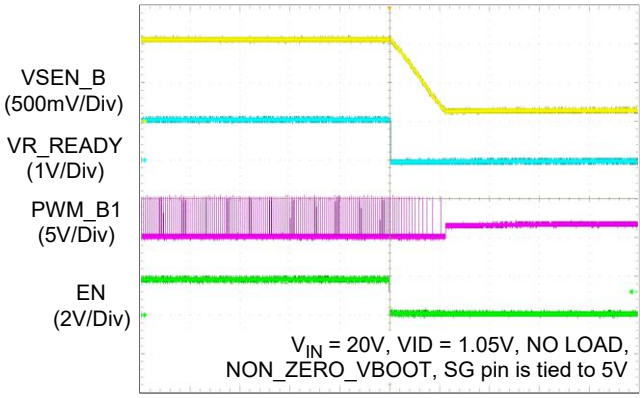
Time (10ms/Div)

GT VR Power On from EN



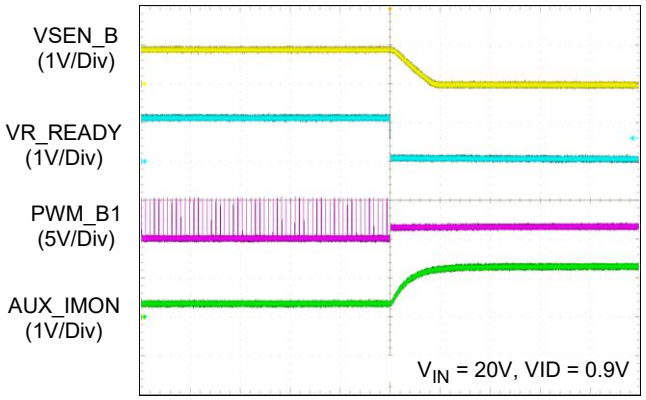
Time (500μs/Div)

GT VR Power Off from EN



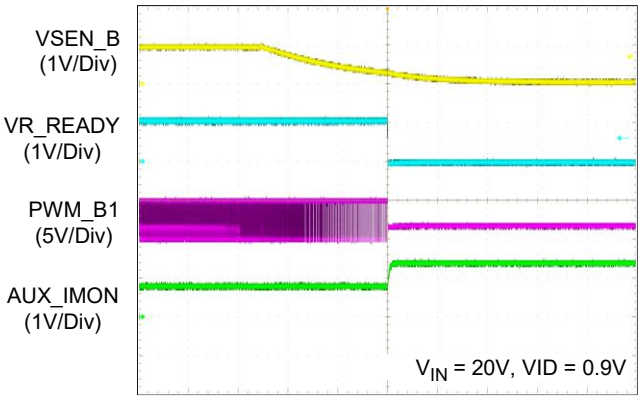
Time (50μs/Div)

GT VR OCP



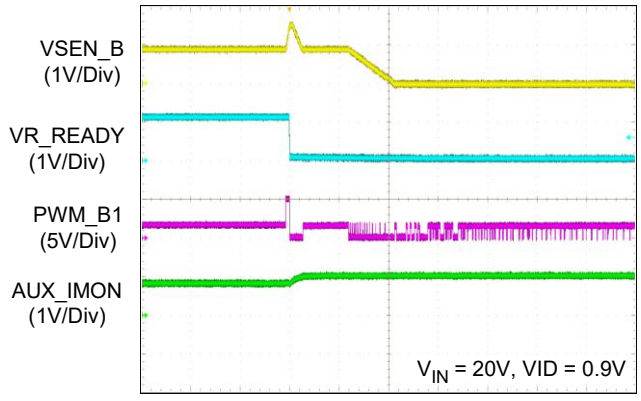
Time (20μs/Div)

GT VR UVP



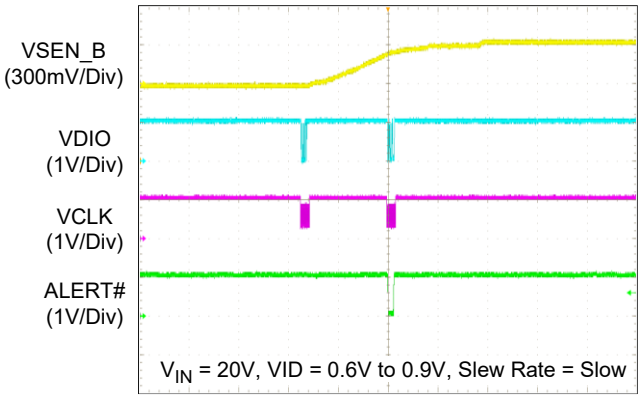
Time (200μs/Div)

GT VR OVP



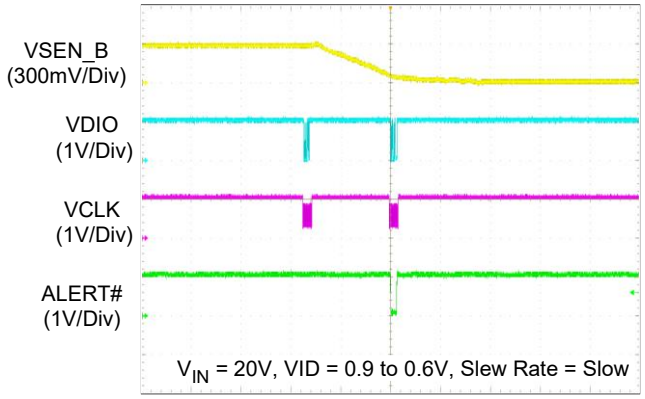
Time (50μs/Div)

GT VR Dynamic VID Up

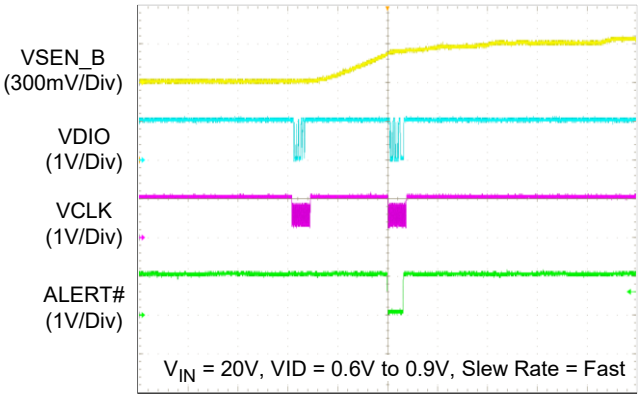


Time (10μs/Div)

GT VR Dynamic VID Down



GT VR Dynamic VID Up



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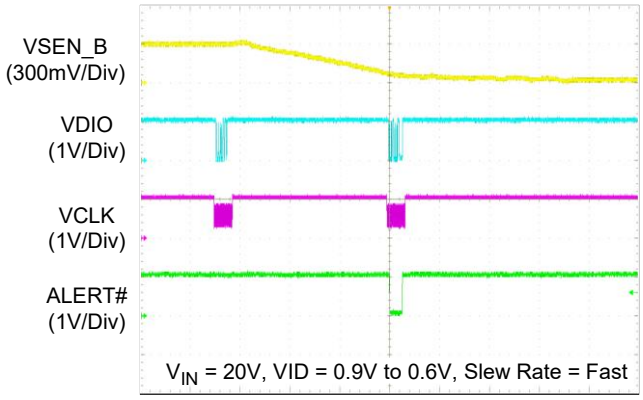

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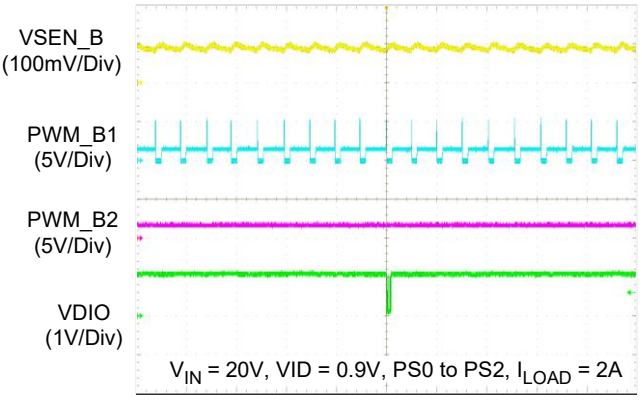

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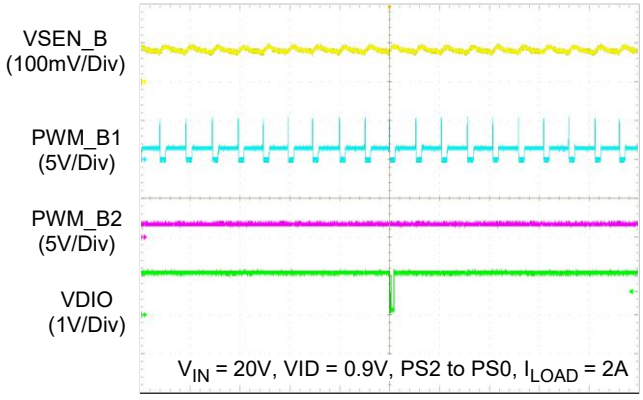
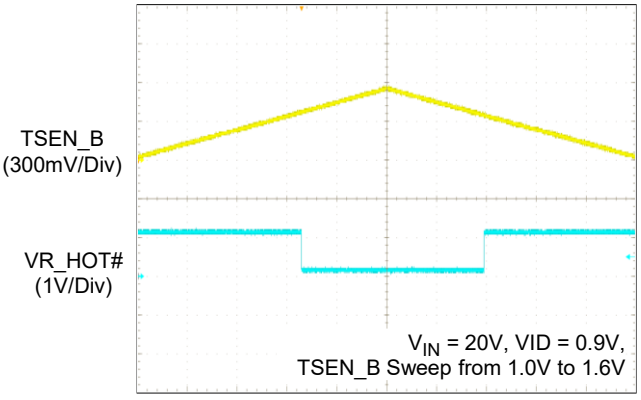
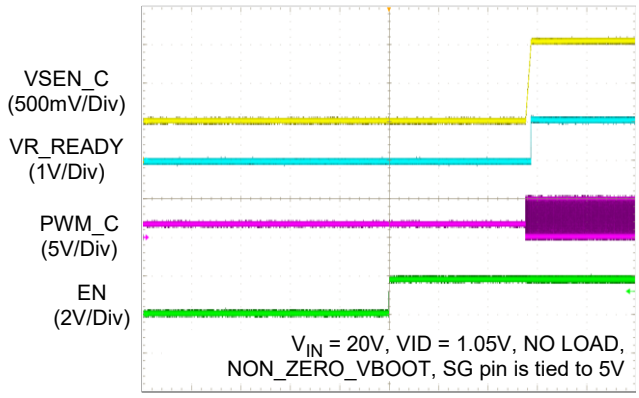


GT VR Thermal Monitoring

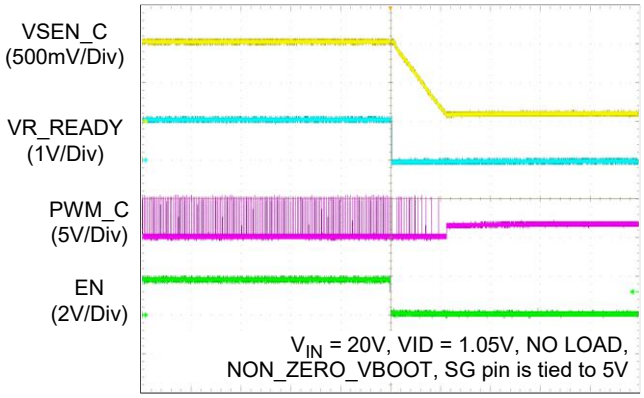


SA VR Power On from EN



Time (500μs/Div)

SA VR Power Off from EN



Time (50μs/Div)

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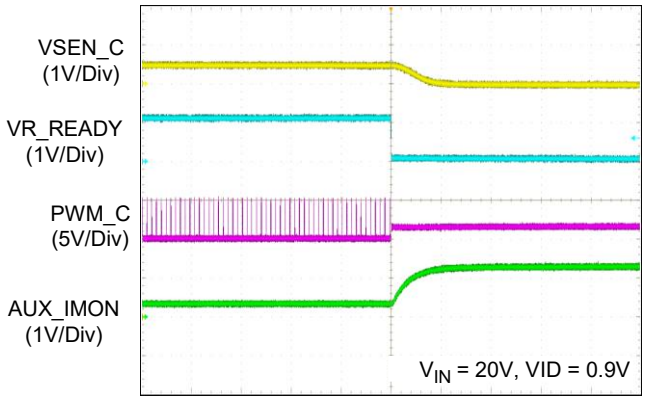

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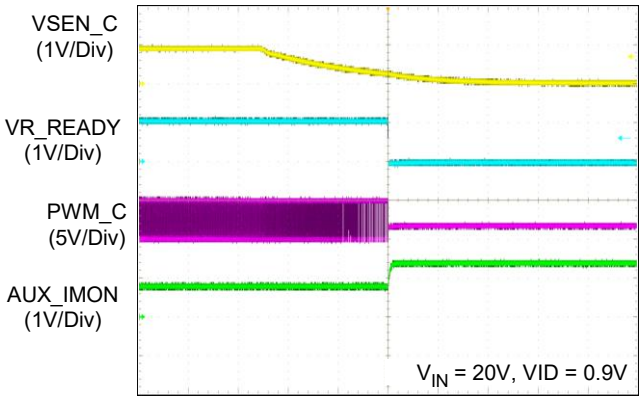

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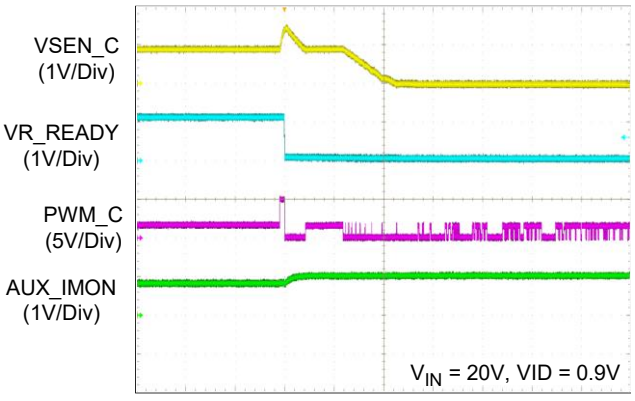

Time (50μs/Div)

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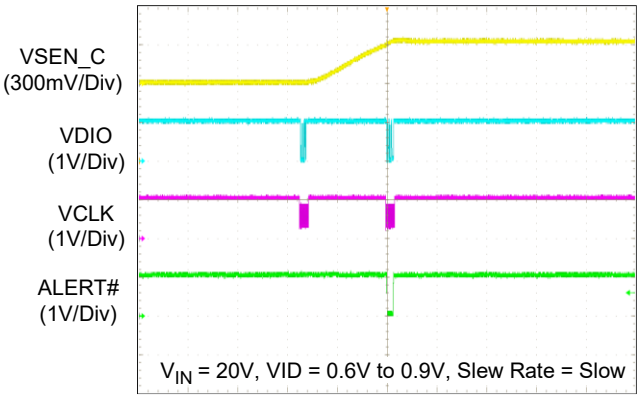

Time (10μs/Div)

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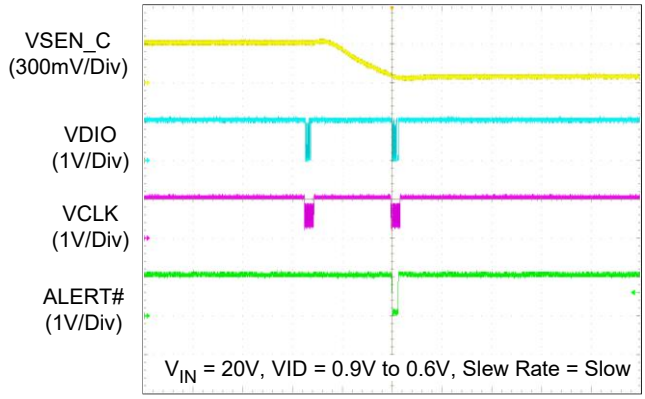

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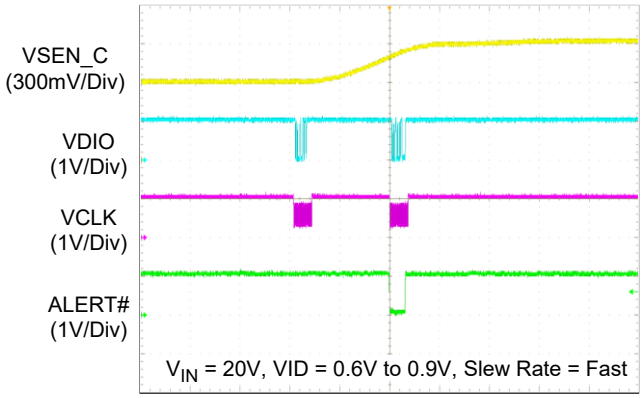

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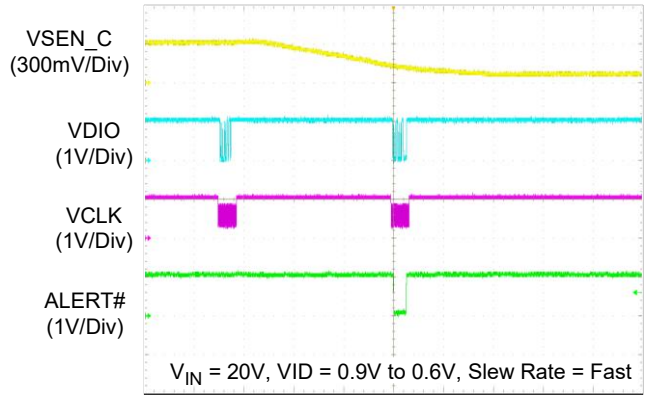
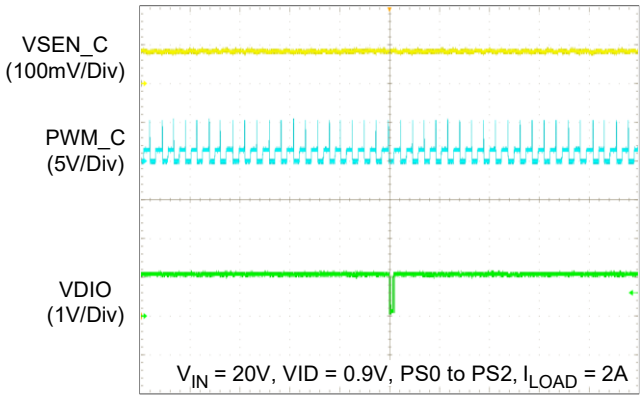


SA VR Mode Transient



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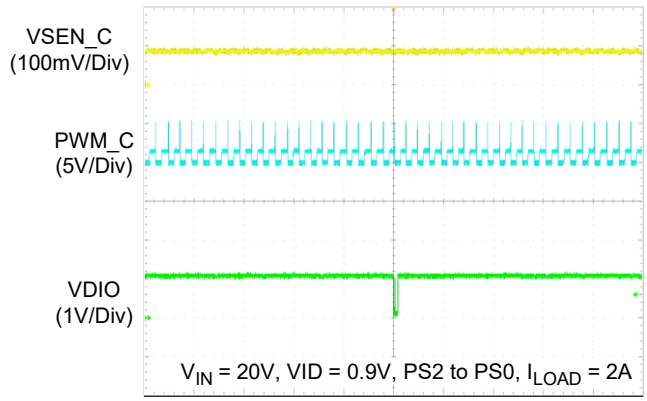
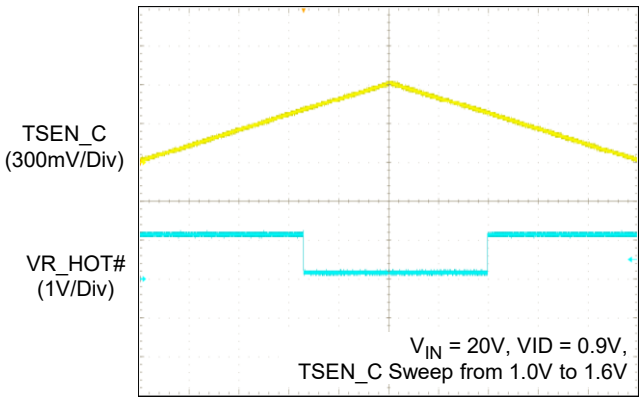
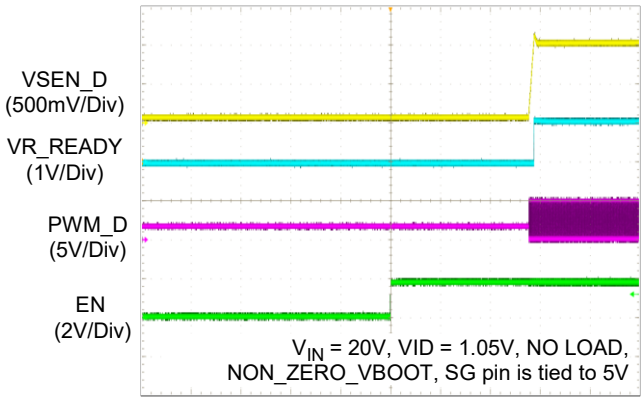


SA VR Thermal Monitoring

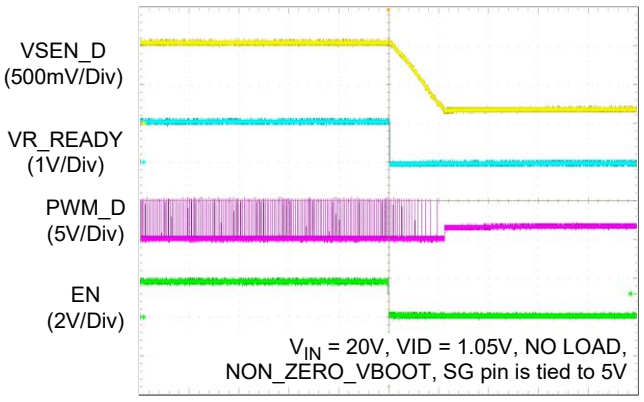


ATOM VR Power On from EN



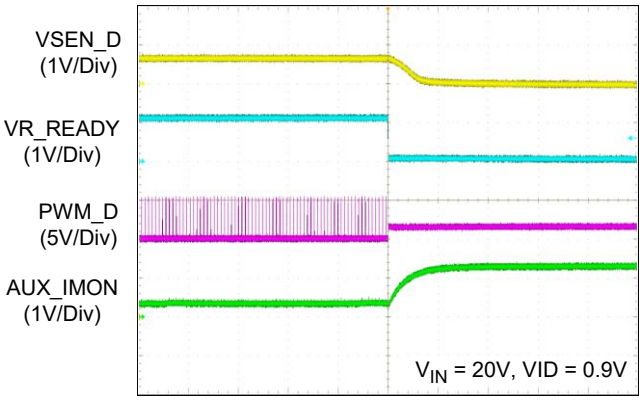
Time (500μs/Div)

ATOM VR Power Off from EN



Time (50μs/Div)

ATOM VR OCP



Time (20us/Div)

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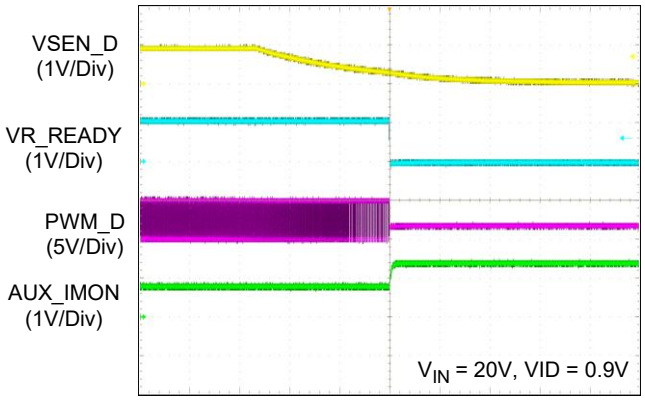

Time (200us/Div)

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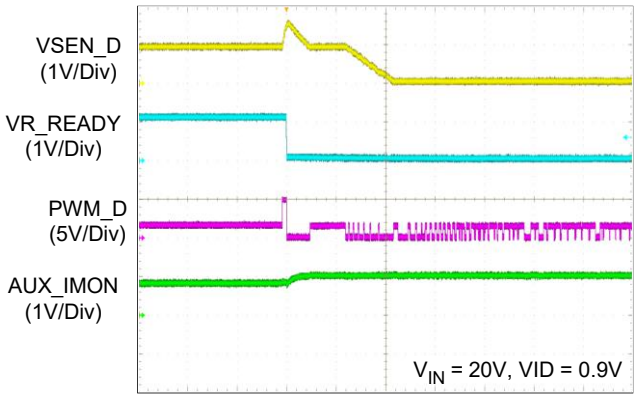
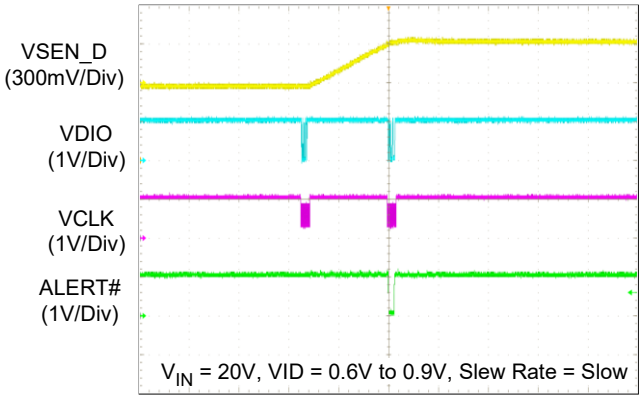


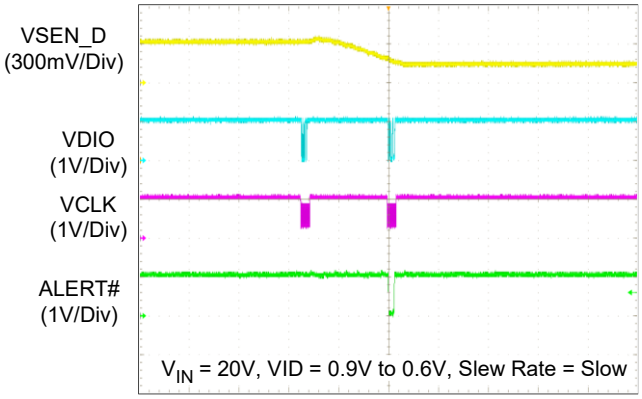
Time (50μs/Div)

ATOM VR Dynamic VID Up



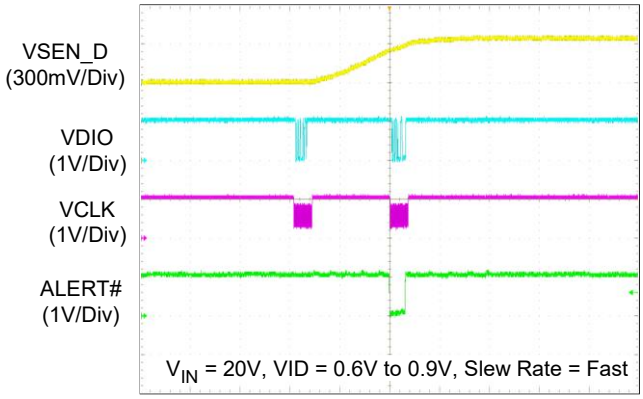
Time (10μs/Div)

ATOM VR Dynamic VID Down



Time (10μs/Div)

ATOM VR Dynamic VID Up



Time (5μs/Div)

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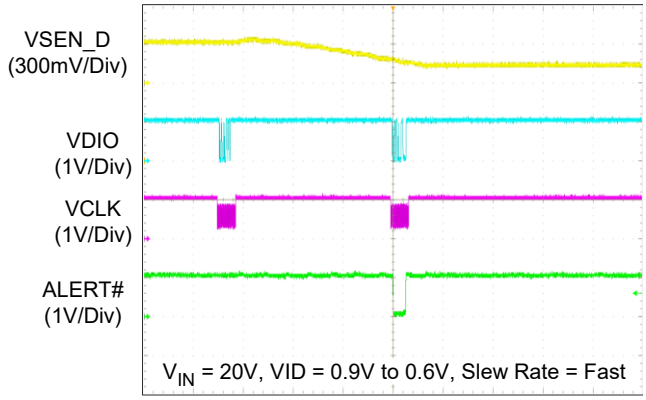
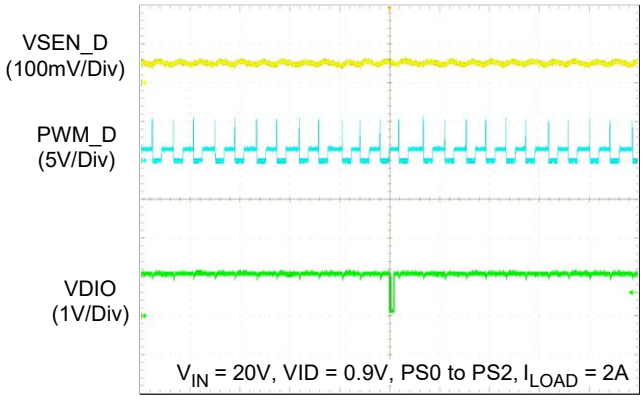


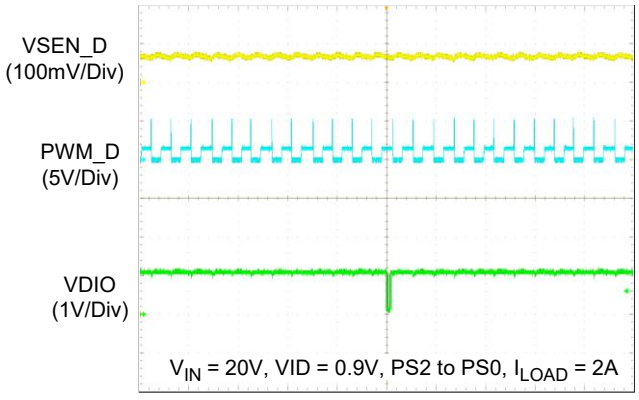
Time (5μs/Div)

ATOM VR Mode Transient



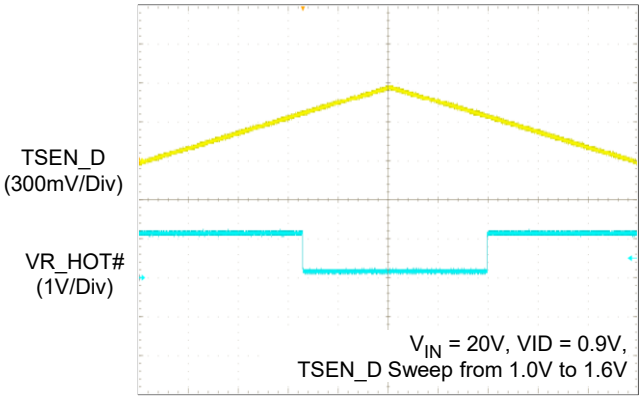
Time (10μs/Div)

ATOM VR Mode Transient



Time (10μs/Div)

ATOM VR Thermal Monitoring



Time (10ms/Div)

17 Operation

17.1 SVID Interface/Control Logic

The SVID interface receives and transmits Serial VID signal between the CPU and the VR controller. The Control logic executes SVID commands and sends the related signals to control the VR.

17.2 I²C Interface and Configuration Registers

The I²C interface can be used to fine-tune controller performance and function settings. Configuration registers include CPU required registers, necessary registers for basic operation and function settings.

17.3 PER CSGM

The PER CSGM senses the per-phase inductor current reported by the SPS. The outputs of the PER CSGM are summed as the IMON signal and fed into Droop Control, Current Balance, IOUT telemetry, and overcurrent protection.

17.4 MUX and ADC

The RT3645BE supports temperature sense input and IOUT telemetry for each rail, as well as input voltage and input power (VSYS and PSYS) monitoring, and AUX_IMON. The MUX controls the sampling sequence, and the ADC converts analog signal to digital codes for telemetry or function settings.

17.5 DAC

The DAC generates a reference VID voltage based on the VID code from the control logic. According to the SetVID command issued by the CPU, the control logic dynamically changes the VID target voltage with the required slew rate.

17.6 Droop Control

Droop Control generates the required droop voltage based on the DAC output and the summed current. The output of Droop Control is fed into the ERRPR AMP for loop regulation.

17.7 ERROR AMP

The ERROR AMP inverts and amplifies the difference between output and target voltage based on the control loop settings in Hybrid Control block.

17.8 Hybrid Control

Hybrid Control is a finite DC gain architecture that features fast dynamic response. The control mode can be selected in NVM. The output of the Hybrid Control is fed into Offset Cancellation to ensure output accuracy.

17.9 Offset Cancellation

The offset cancellation ensures precise droop control to meet the required load-line accuracy. It is based on a low-pass filter to achieve an infinite DC gain system, allowing the error between the output and the target to be eliminated.

17.10 RAMP

The RAMP signal helps to improve the signal-to-noise ratio, enhance loop stability, and transient response.

17.11 PWM CMP

The PWM CMP compares the inductor current signal and the RAMP signal with the output of the Offset Cancellation to trigger TONGEN.

17.12 TONGEN and Driver Interface

The output of the PWM comparator triggers TONGEN to produce the PWM signal. The PWM on-time is determined by the input voltage, frequency setting, current balance output, and AQR settings. The driver interface provides high, low, and tri-state levels to drive external MOSFET drivers.

17.13 Current Balance

The sensed per-phase inductor current is compared with the average current to adjust the PWM on-time of each phase. Thermal balance of a multi-phase VR can be achieved with proper Current Balance settings.

17.14 Zero Current Detection

The ZCD detects the zero crossing of the inductor current for each phase. The ZCD output is used for diode-emulation mode (DEM) to improve light-load efficiency, and for overshoot reduction (ANTIOVS).

17.15 Adaptive Quick Response (AQR)

AQR is a new-generation of quick response mechanism. It detects the falling edge of the output voltage and allows all phase PWMs to turn on simultaneously. The AQR trigger level and pulse width can be set in NVM.

17.16 Anti-Overshoot (ANTIOVS)

ANTIOVS detects the output voltage during load release and controls all PWM signals in tri-state to force current flow through the body diode of low-side switches until zero current is reached. This can attenuate voltage overshoot and reduce the output capacitance.

17.17 Protection Logic

Protection Logic detects potential fault events including undervoltage-lockout (UVLO), undervoltage (UV), overvoltage (OV), overcurrent (OC), and SPS fault flags. VR_READY is pulled low if a fault event is detected in active output rails.

18 Application Information

(Note 6)

18.1 General Description

The RT3645BE controller is designed for CPU power solutions in consumer electronics such as laptop and desktop computers. The RT3645BE includes four VR domains: VCCCORE, VCCGT, VCCSA, and VCC_LP_ECORE. Each rail can be configured to support the desired phase number with a maximum phase count of 5-phase for VCCCORE, 2-phase for VCCGT, 1-phase for VCCSA, and 1-phase for VCC_LP_ECORE. Phase configurations such as 5+2+1+1, 4+2+1+1, 2+1+1+1, and others., are supported. The RT3645BE can fully meet the Intel IMVP9.3 specification with a serial VID control interface. The RT3645BE features several function settings for performance optimization, which can be accessed via the I^2C interface. The RT3645BE controller incorporates a Multiple-Time Programmable (MTP) Non-Volatile Memory (NVM) to store customized configurations.

18.2 Power-On Sequence

The RT3645BE controller requires a VCC supply of 5V. To ensure sufficient power for proper VR operation, the controller triggers UVLO if the VCC voltage drops below 4.2V (maximum). The UVLO protection shuts down the controller and forces all PWM signals into tri-state to turn off power switches. When VCC > 4.45V (maximum), the RT3645BE issues POR = high and waits for the EN signal. After POR = high and EN > 0.7V, the controller starts power-on initialization, including internal offset calibration and loading NVM data to functional registers. It takes 2ms for the RT3645BE controller to complete internal settings. It is suggested to set EN to logic high after VCC is stable. Figure 1 shows a typical timing diagram of the controller power-on sequence. For proper operation and output accuracy, it is strongly recommended that the driver power (PVCC) be ready after the controller VCC is established.

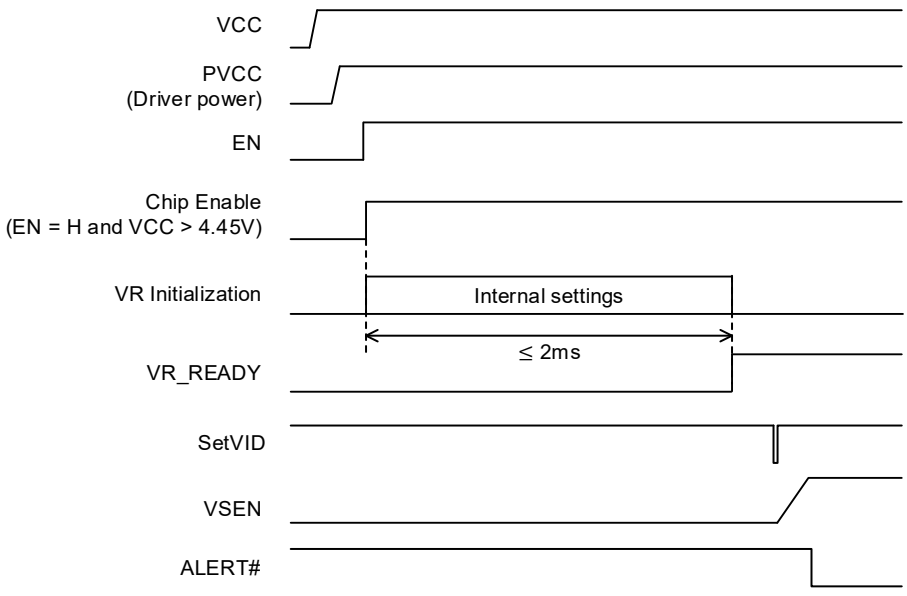


Figure 1. Typical Timing of Controller Power-On Sequence

18.3 Active Phase Number Setting

For the RT3645BE controller, the active phase count of each rail can be configured either through NVM or by the hardware connection of the ISENxP pin(s). When the ISENxP voltage is greater than > (VCC − 0.5V), the hardware-programmed active phase count is (x−1). The detection is executed during power-on initialization and is latched when the internal settings are finished. Figure 2 below shows an example of a 3-phase configuration for VCCCORE set by the ISENxP pin(s). The active phase number can also be configured in NVM with the register MAX_PH_A for VCCCORE, and MAX_PH_B for VCCGT. For more details, refer to the Functional Register Description. If the NVM setting conflicts with the ISENxP connection, the controller uses the smaller phase count as the active phase number.

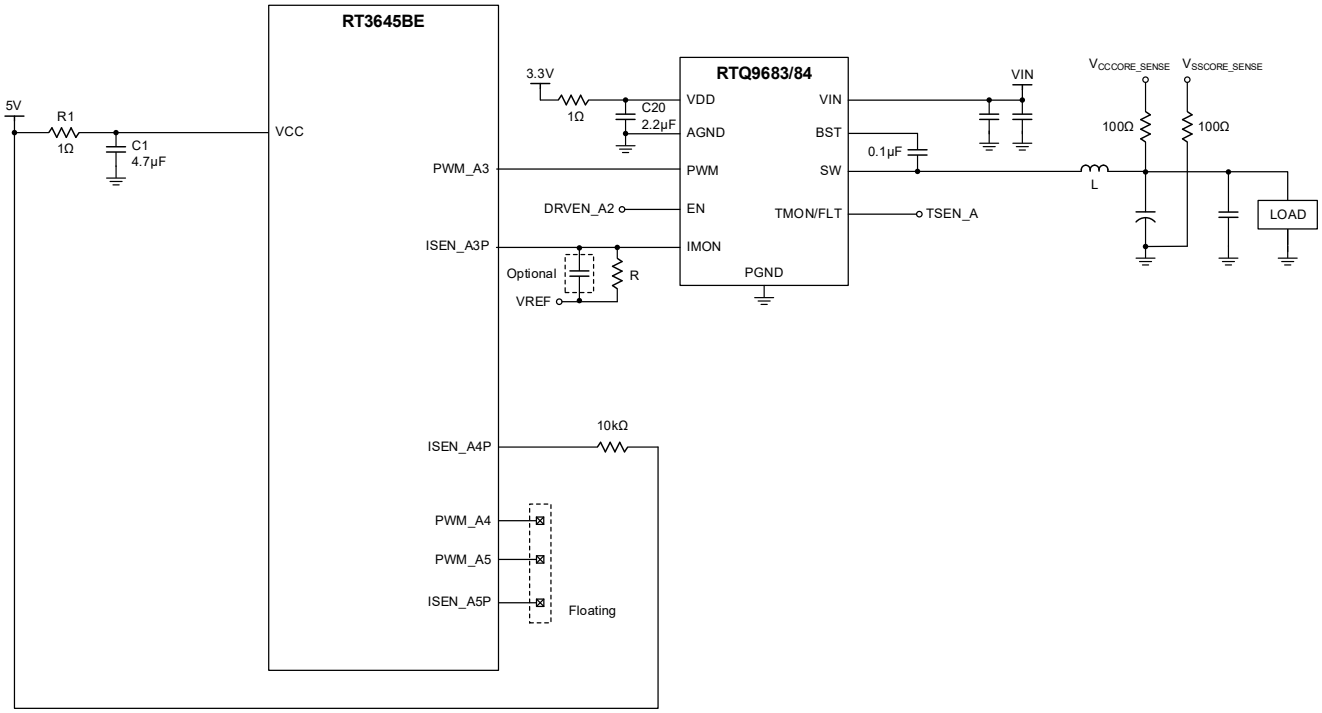


Figure 2. Three-Phase Configuration for VCCCORE Set by ISENxP Hardware Connection

18.4 Rail Disable

For the RT3645BE controller, each rail can be disabled by hardware connection or internal NVM settings. By pulling ISEN_A1P above (VCC − 0.5V), rail A is disabled. The same methodology is applicable for rails B, C, and D, that is, pulling ISEN_B1P to VCC disables rail B, pulling ISEN_CP to VCC disables rail C, and pulling ISEN_DP to VCC disables rail D. Each rail can also be disabled by NVM. The corresponding registers are EN_RAIL_A, EN_RAIL_B, EN_RAIL_C, and EN_RAIL_D, respectively. Note that the VR domain is disabled when one of the disabling conditions is satisfied. For the PSYS domain, it can be disabled by setting the NVM register EN_PSYS_DOMAIN. The PSYS domain is also disabled when all VR domains enter PS4 or are disabled.

18.5 NVM Programming Mechanism

The RT3645BE provides several function settings for performance tuning and BOM optimization. These registers can be accessed via the I^2C interface and can be programmed into NVM using specific programming instructions. Figure 3 shows a simplified timing diagram of the NVM programming. As VCC ramps up higher than the power-on reset (POR) threshold, the controller starts to load data from NVM to the functional registers. It takes approximately 500µs to complete the NVM download. After the NVM download is finished, users can write the

functional registers via the I²C interface to adjust control parameters. When a program instruction is issued by the host, the controller starts to program the data from functional registers into NVM. The NVM programming process takes approximately450ms. The EN pin should remain in a LOW state during NVM programming. DO NOT program the NVM while output regulation is active, as this may cause unexpected PWM behavior and voltage errors. RICHTEK provides a software-based NVM programming tool to help users perform the programming task more easily.

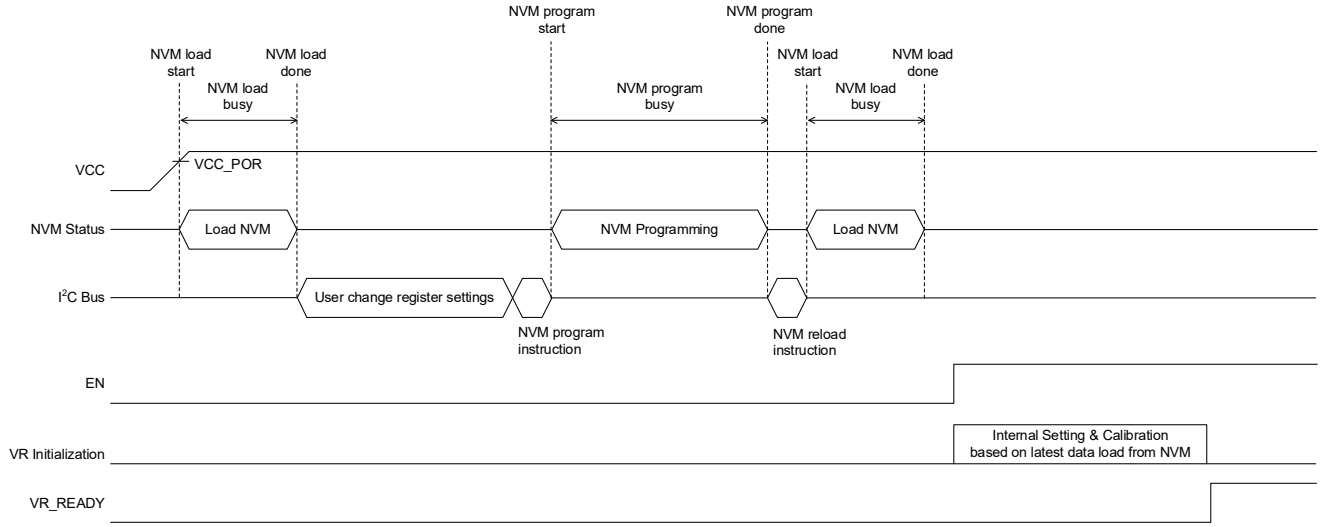


Figure 3. Timing Diagram of VR Initialization and NVM Programming

18.6 ADDR Pin and I²C Slave Address

The RT3645BE controller can store customized configurations in NVM. Users can program different parameters for different platforms and set the I²C slave address by connecting a single resistor from the ADDR pin to ground. The ADDR pin strapping is executed and latched during power-on initialization. The I²C address can also be changed by programming the NVM register I2C_ADDR_SET1 or I2C_ADDR_SET2. After NVM programming, the change in the I²C address will take effect by cycling the VCC power. The RT3645BE provides several address options to support multiple devices connected on a single I²C bus. To ensure the I²C slave address is set properly, a resistor with 1% tolerance or smaller is preferred. Refer to Table 1 for I²C slave address settings.

Table 1. Resistance for Configuration Selection and I²C Slave Address

Resistance (kΩ)	Slave Address (7-bit)		I²C Slave address
	[6:2]	[1:0]	
90.9	I2C_ADDR_SET1	00	0x20
100		01	0x21
110		10	0x22
121		11	0x23
133	I2C_ADDR_SET2	00	0x60
147		01	0x61
162		10	0x62
Tie to VCC		11	0x63

18.7 Differential Remote Voltage Sense

The RT3645BE provides a differential remote-sense pair for each rail to eliminate voltage drops across PCB traces and socket contacts. The CPU contains on-die sense pins and the connection between the CPU and the VR controller is shown in Figure 4. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at the CPU remote-sense node. If the CPU is not mounted on the PCB during the initial design phase, two resistors of typical 100Ω are required to provide a feedback path for output regulation.

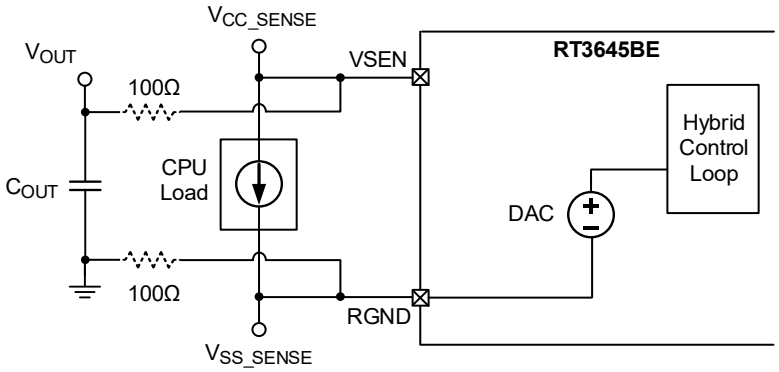


Figure 4. Connection of Differential Remote Voltage Sense Pin

18.8 Thermal Monitoring

The RT3645BE has four TSEN pins for thermal monitoring of each rail. The TSEN pins should be connected to the TMON pins of the SPS with a positive temperature coefficient. The TMON voltage should follow the equation:

V_{TSEN_x} = Temperature(°C) · 8mV/ °C + 600mV

The minimum V_{TSEN} from the SPS TMON that can be decoded is 0V. It is strongly suggested to add a 1μF capacitor (C_{TSEN}) between the TSEN pin and ground for SPS applications to ensure accurate temperature sensing.

If the sensed temperature is higher than the SVID ThermAlert bit assertion threshold, the RT3645BE controller asserts the ThermAlert bit in the SVID status1 (10h) register. The assertion threshold and de-assertion hysteresis of the ThermAlert bit can be set by NVM using the registers TSEN_ALERT_TH and TSEN_ALERT_HYS. If the sensed temperature is higher than the VR_HOT# assertion threshold, the RT3645BE asserts the VR_HOT# pin. The assertion threshold and de-assertion hysteresis of the VR_HOT# pin can be set by NVM using the registers TSEN_VRHOT_TH and TSEN_VRHOT_HYS. It is suggested to set the VR_HOT# assertion threshold higher than the assertion threshold of the SVID ThermAlert bit to ensure proper system operation.

18.9 System Input Power Monitoring (PSYS)

The RT3645BE provides a PSYS function to monitor system input power and report it to the CPU via the SVID interface. The PSYS function is illustrated in Figure 5. The PSYS meter outputs a current signal (I_{PSYS}) proportional to the system input power. The R_{PSYS} should be designed to meet $I_{PSYS(MAX)}$ x R_{PSYS} = $V_{PSYS(MAX)}$. The full-scale voltage $V_{PSYS(MAX)}$ can be set via the register PSYS_SCALE_SEL and the maximum digital code reported via SVID is 0xFF. If V_{PSYS} is higher than the critical threshold set in the SVID register, the controller asserts the VR_HOT# pin.

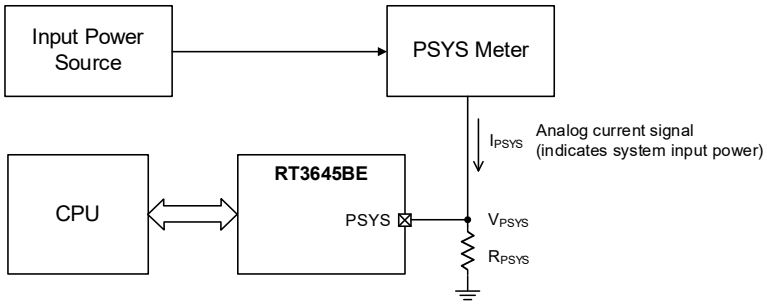


Figure 5. Block Diagram of PSYS Monitoring

18.10 System Input Voltage Monitoring

The RT3645BE provides two input voltage sense pins: the VINSEN pin for system input voltage monitoring, and the VSYS pin dedicated to fast V_{SYS} droop detection. It is recommended to connect a low-pass filter with a corner frequency around the PWM switching frequency to ensure proper PWM on-time pulse width setting and telemetry. The maximum input voltage that can be decoded is 24V with a digitized code of 0xFF reported via SVID. If the system input monitoring setting of the SVID register 34h is set to detect input voltage, the RT3645BE controller asserts the VR_HOT# when V_{SYS} is lower than the critical threshold. It is strongly recommended NOT to filter the VSYS signal to ensure proper detection of fast V_{SYS} droop.

18.11 Auxiliary VR Output Current Monitoring

The RT3645BE provides an analog input pin for auxiliary VR output current monitoring. The auxiliary VR outputs a current signal, that is linearly proportional to its loading current and should be referenced to VREF with a termination resistor, R_{AUX}, located at the controller. Figure 6 below shows an example of auxiliary VR output current monitoring. The RT3645BE senses the differential voltage between the AUX_IMON pin and VREF and converts it into a digital code for telemetry. The maximum differential input voltage is 0.8V, with a digitized code of 0xFF reported via the SVID interface. The termination resistor R_{AUX} should be properly designed to satisfy the equation:

$$0.8V = K \cdot ICCMAX_{AUX} \cdot R_{AUX}$$

The ICCMAX value and the corresponding high current capability bit of the auxiliary VR can be set in the registers ICCMAX_AUX and ICCMAX_HC_AUX. The current telemetry of the auxiliary VR can be enabled or disabled by the register IMON_AUX. When disabled, the RT3645BE acknowledges the SVID command with a payload of 0x00, and the AUX_IMON pin serves as a fault indicator. Refer to Table 5 for a summary of the fault indicator.

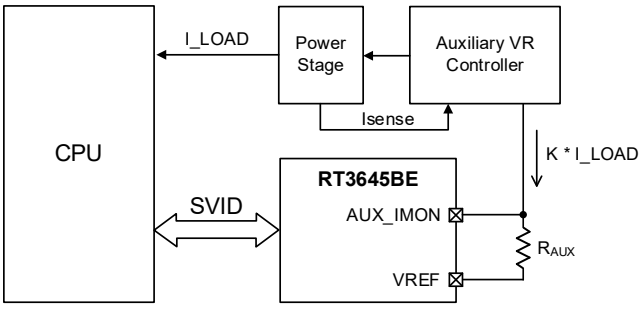


Figure 6. Block Diagram of Auxiliary VR Current Monitoring

18.12 Per-Phase Current Sensing and RIMON

The RT3645BE controller adopts SPS IMON current sensing. All the ISENxP pins should be connected to the IMON pin of the SPS with a termination resistor, R_{SPS}, referenced to VREF, as shown in Figure 7.

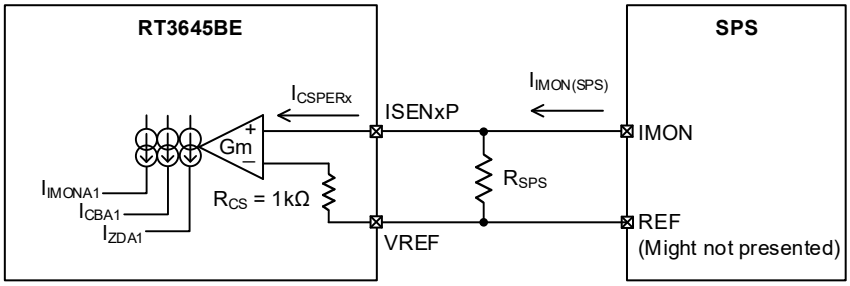


Figure 7. Per-Phase Current Sensing Using SPS IMON

For SPS IMON current sensing, the equivalent DCR seen by the controller is given by:

$DCR_{eq} = I_{IMON(SPS)} \times R_{SPS}$

The symbol $I_{IMON(SPS)}$ indicates the IMON gain of SPS. The equivalent DCR should meet the following constraint to ensure accurate load-line control and output telemetry.

$0.2m\Omega \le DCR_{eq} \le 0.8m\Omega$

The sensed per-phase current signals are mirrored and summed together with the current mirror gain A_{MIRROR} = 0.125A/A. The internal R_{IMON} converts the summed current into a voltage signal V_{IMON}, as shown in Figure 8. The symbol ΔV_{IMON} represents the differential voltage between V_{IMON} and VREF and can be expressed as:

$$\Delta V_{IMON} = (I_{L1} + I_{L2} + \ldots) \times \frac{DCR_{eq}}{R_{CS}} \times A_{MIRROR} \times R_{IMON}[10:0]$$

ΔV_{IMON} is proportional to the output current and is used for droop control, IOUT telemetry and overcurrent protection. The internal resistor R_{IMON} should be properly set to satisfy $\Delta V_{IMON} = V_{ICCMAX}$ when ($I_{L1} + I_{L2} + \cdots$) = ICCMAX. The V_{ICCMAX} voltage of each rail is determined based on ICCMAX as follows:

V_{ICCMAX} = 0.8V, when ICCMAX > 160A

V_{ICCMAX} = 0.4V, when 60A < ICCMAX ≤ 160A

V_{ICCMAX} = 0.2V, when 15A < ICCMAX ≤ 60A

V_{ICCMAX} = 0.1V, when ICCMAX ≤ 15A

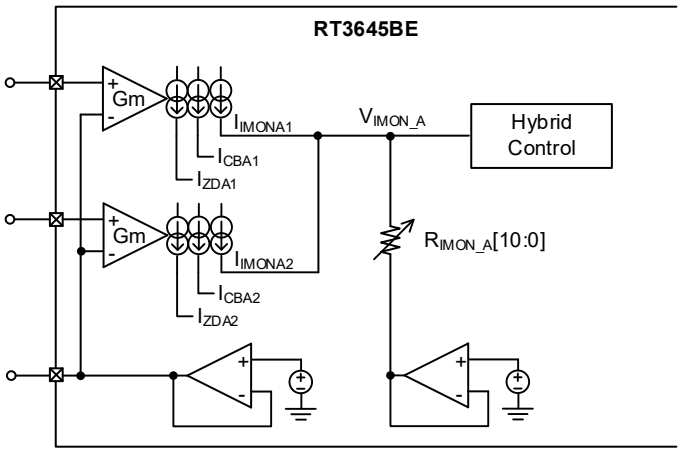


Figure 8. Internal RIMON and VIMON

Based on the equations above, the internal RIMON can be calculated as:

$$R_{IMON}[10:0] = \frac{V_{ICCMAX}}{\frac{DCR_{eq}}{R_{CS}} \cdot ICCMAX \cdot A_{MIRROR} \times 0.25k\Omega}$$

The resistor RIMON is set using the 11-bit register RIMON_MSB_SET<rail> and RIMON_SET<rail> with a resolution of 0.25kΩ/LSB. It should be noted that the EN pin should remain in a LOW state while programming the RIMON registers. DO NOT program RIMON during active output regulation, as it may cause unexpected PWM behavior and voltage errors.

18.13 Load-Line Setting

The load-line feature is specified in CPU power to reduce power consumption and output capacitance. The VR output voltage decreases linearly as the loading current increases, as shown in Figure 9. The RT3645BE controller uses the ΔVIMON signal to produce the desired droop, as show in Figure 10. The ΔVIMON signal is proportional to the output current and is mirrored to produce a droop voltage across RLL [7:0], with a current mirror gain of 0.125 A/A. The droop voltage is subtracted from the DAC voltage to generate the VTARGET for loop regulation. The value of RLL can be calculated as:

$$R_{LL}[7:0] = ICCMAX \cdot LL \times \frac{R_{CSLL}}{V_{ICCMAX} \times A_{MIRROR\_LL} \times 1k\Omega}$$

The symbol LL stands for the desired Load-Line. The RLL register can be set to zero for zero load-line applications. It should be noticed that the EN pin should remain in a LOW state while programming the load-line register. DO NOT program the load-line registers during active output regulation, as it may cause unexpected PWM behaviors and voltage errors.

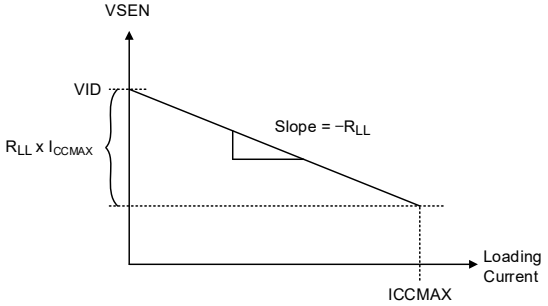


Figure 9. Characteristic of Load-Line

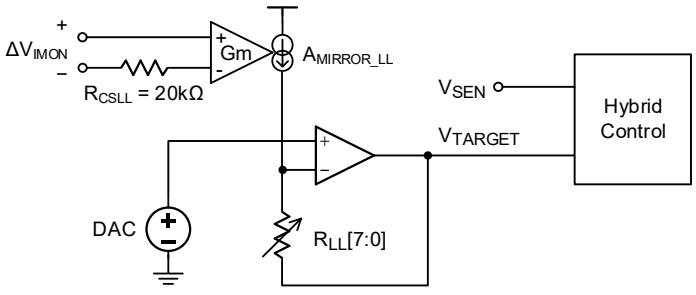


Figure 10. Droop Settings for Load-Line Control

18.14 Hybrid Control and Offset Cancellation

The RT3645BE controller adopts a hybrid control and offset cancellation loop to achieve precise load-line control with fast transient response. Figure 11 below shows a simplified control block diagram. The positive feedback loop formed by a low-pass filter (LPF) can effectively produce an infinite DC gain to mitigate the steady-state error. The hybrid control loop is composed of a high-pass filter (HPF) with finite DC gain. When a load transient occurs, the HPF path can respond rapidly to generate the required control signal and trigger the PWM comparator. The RT3645BE controller supports two types of control modes: Mode 1 for 2 pole 2 zero (2P2Z), and Mode 2 for 3 pole 3 zero (3P3Z). For non-zero load-line applications, Mode 1 is sufficient for the VR to satisfy all AVP requirements. However, for zero load-line applications, the VR with Mode 1 control may struggle in transient tests due to strict AC specifications. The RT3645BE controller offers the flexibility to further extend the bandwidth in Mode 2. In Mode 2, an additional pole-zero pair is induced in the HPF path to compensate for the high-frequency response of the system.

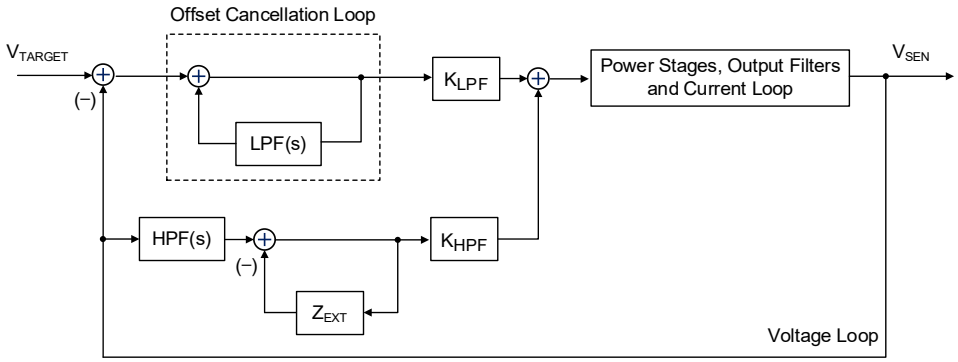
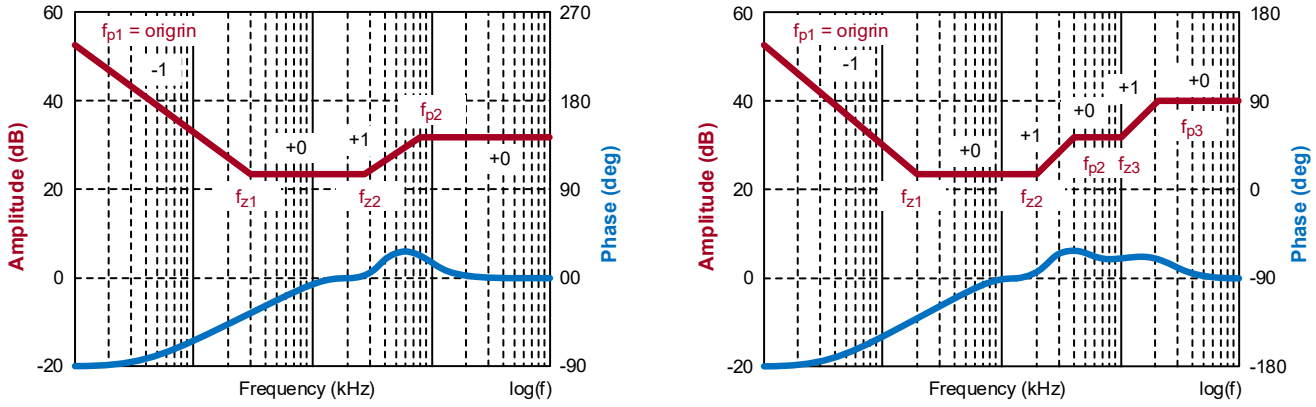


Figure 11. Simplified Block Diagram of Hybrid Control and Offset Cancellation Loop



(a) Mode 1 Control

(b) Mode 2 Control

Figure 12. Pole-Zero Illustration of Mode 1 and Mode 2 Controls

The resistance and capacitance in the offset cancellation loop can be set in the NVM register LPF_TAU_SET_<rail>. The resistance and capacitance in the high-pass filter path can be set in the NVM registers HPF_R_SET_<rail> and HPF_C_SET_<rail>. KLPF and KHPF determine the DC gain of the corresponding filter and can be set in the NVM registers LPF_GAIN_SET_<rail> and HPF_GAIN_SET_<rail>. For Mode 2, the additional pole-zero pair can be set in the NVM registers EXT_R_SET_<rail> and EXT_C_SET_<rail>, respectively. Table 2 below summarizes the approximation of the pole-zero locations for Mode 1 and Mode 2.

Table 2. Approximation of Pole-Zero Locations for Mode 1 and Mode 2 Controls

	Mode 1 (2P2Z)	Mode 2 (3P3Z)
fp1	0 (Origin pole)	
fp2	$\frac{1}{2\pi R_{HPF} C_{HPF}}$	
fp3	--	$\frac{1}{2\pi R_{EXT} C_{EXT}}$
fz1	$\frac{1}{2\pi R_{LPF} C_{LPF}}$	
fz2	$\frac{1}{2\pi \cdot \frac{R_{LPF}C_{LPF}R_{HPF}C_{LPF}}{R_{LPF}C_{LPF} + R_{HPF}C_{LPF}} \cdot \frac{K_{LPF} + K_{HPF}}{K_{LPF}}}$	
fz3	--	$\frac{1}{2\pi (R_{EXT} + 80k\Omega) C_{EXT}}$

18.15 Adaptive Quick Response (AQR)

The RT3645BE controller features the Adaptive Quick Response (AQR) technique to optimize transient response. The controller monitors the derivative of the output voltage, and if it exceeds the AQR threshold, all PWM signals are forced to turn on simultaneously. The AQR threshold can be set by the NVM register AQR_TH_<rail>. The pulse width triggered by AQR is 50% of nominal t_{ON} defined by the KTON equation. Figure 13(a) shows a waveform comparison with and without AQR. As shown in Figure 13(b), when AQR is enabled, all active phases turn on their high-side switches simultaneously to quickly deliver power from input to output, resulting in significantly improved voltage waveform.

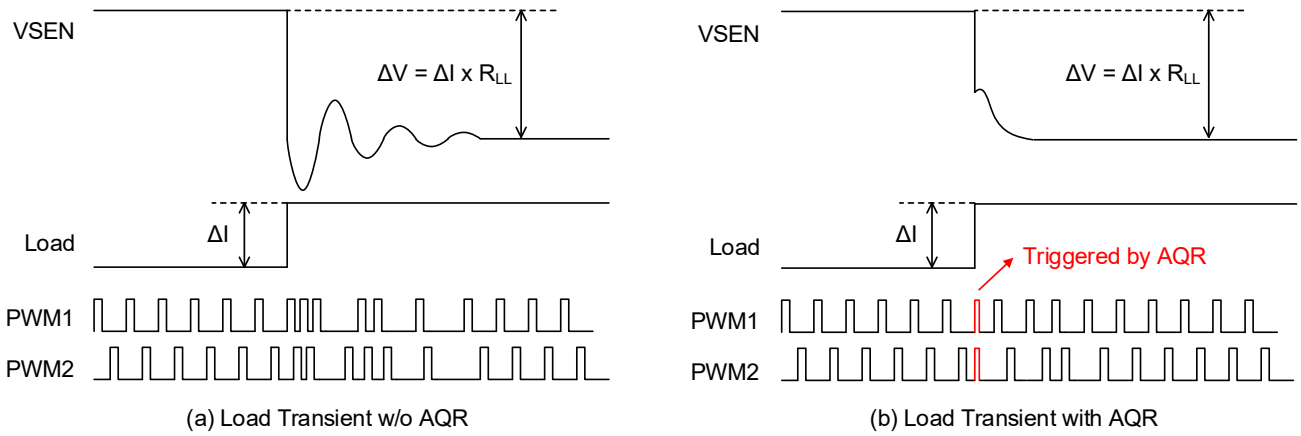


Figure 13. Load Transient Waveform (a) without AQR, (b) with AQR

18.16 Anti-Overshoot (ANTIOVS)

The RT3645BE controller provides an anti-overshoot function to suppress output voltage overshoot. The output voltage is compared with the ANTIOVS trigger level. If an overshoot occurs, the controller holds the LPF in the offset cancellation loop and forces all PWM signals into tri-state until the inductor current reaches zero. By turning off both the high-side and low-side switches, the inductor current is forced to flow through the low-side body diode. The forward voltage drop of the low-side body diode is induced across the inductor to accelerate the discharging slope and reduce the overshoot. Holding the LPF can block the overshoot voltage from being accumulated in the offset cancellation loop, preventing undesired voltage droop after the overshoot. The trigger level of the ANTIOVS function can be set in the register ANTIOVS_TH_<rail>. Figure 14 shows the basic operating principle of the ANTIOVS function. The ANTIOVS trigger level should be properly set to avoid false triggering from steady-state output ripple. Note that the ANTIOVS function might not take effect when SPS is used. Refer to the datasheet of the selected SPS part for a detailed description of PWM operation.

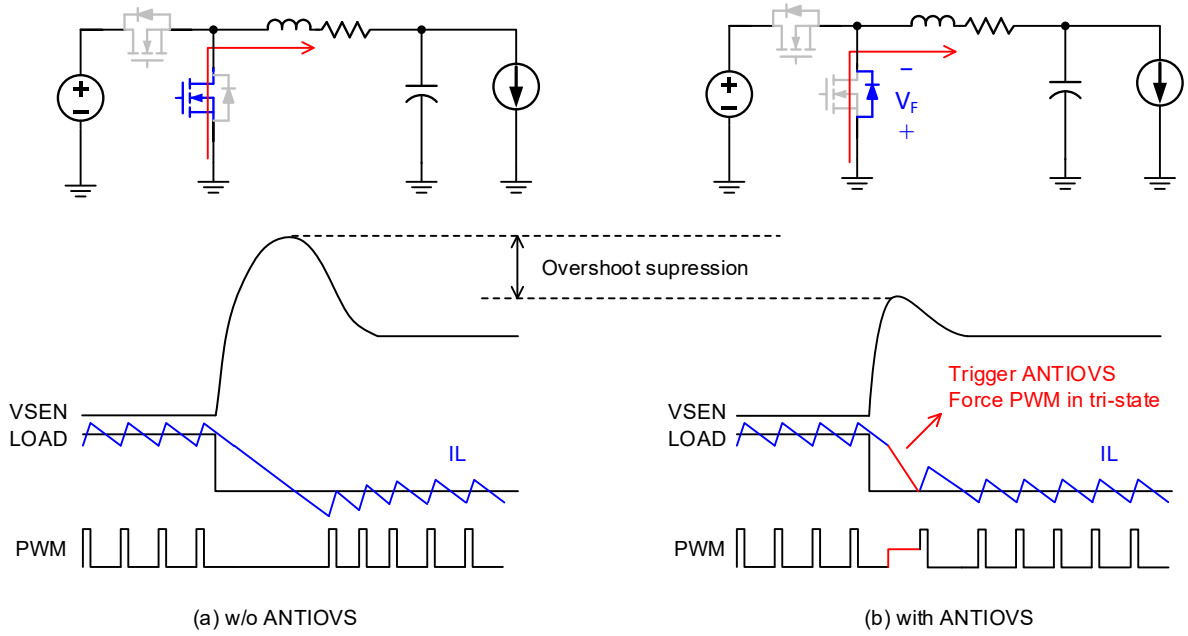


Figure 14. Load Release Waveform (a) without ANTIOVS, (b) with ANTIOVS

18.17 PWM On-Time and Switching Frequency

The RT3645BE controller adopts constant on-time (COT) control, generating an adaptive t_{ON} based on the input voltage to ensure line regulation capability. The t_{ON} is adaptive to VID to achieve nearly constant switching frequency for high duty ratio application. The constant switching frequency helps to simplify the design of EMI filter and thermal estimation of the system. The RT3645BE provides a parameter K_{TON} to set the t_{ON} width. The equations to set t_{ON} width are as follows:

Rail A and Rail B:

$$t_{ON} = \frac{VID}{VIN \times 300000 \times KTON} + 18ns + DEADTIME\_SET\_<rail>, \text{ if } VID \geq 0.9V$$

$$t_{ON} = \frac{0.9}{VIN \times 300000 \times KTON} + 18ns + DEADTIME\_SET\_<rail>, \text{ if } VID < 0.9V$$

Rail C and Rail D:

$$t_{ON} = \frac{VID}{VIN \times 300000 \times KTON} + 14ns + DEADTIME\_SET\_<rail>, \text{ if } VID \geq 0.9V$$

$$t_{ON} = \frac{0.9}{VIN \times 300000 \times KTON} + 14ns + DEADTIME\_SET\_<rail>, \text{ if } VID < 0.9V$$

t_{ON} is fixed when VID is lower than 0.9V. This feature helps to reduce the switching frequency and power losses during low VID operation. The NVM register DEADTIME_SET_<rail> is used to compensate for the deadtime of the power switches, ensuring that the actual on-time at the switching node closely matches the intended PWM on-time. The minimum PWM on-time that can be generated by the RT3645BE controller is 40ns and the minimum off-time is 130ns. When the PWM on-time is determined, the switching frequency can be derived from the equation below. The equation is applicable for CCM operation and the losses in the power stage and driver characteristics are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times \left(DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL} \right)}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}} \right) \right] \times \left(t_{ON} - t_D + t_{ON,VAR} \right) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times t_D}$$

VID: VID voltage

V_{IN}: Input voltage

I_{CC}: Loading current

N: Total phase number

$R_{ONHS,max}$: Maximum equivalent resistance of high-side switch $R_{DS(ON)}$

n_{HS}: Number of high-side switches

$R_{ONLS,max}$: Maximum equivalent resistance of low-side switch $R_{DS(ON)}$

n_{LS}: Number of low-side switches

t_D: Summation of high-side switch delay time and rising time

$t_{ON,VAR}$: On-time variation value

DCR: Inductor DCR

R_{LL}: Load-line setting (Ω)

18.18 PWM On-Time Extension for Asymmetric VR Design

The RT3645BE supports asymmetric VR design to further extend battery life during light-load operation. In an asymmetric VR design, a power switch with relatively large $R_{DS(ON)}$ and a larger inductance will be used for the 1st phase to boost system efficiency. The RT3645BE controller supports asymmetric t_{ON} mode for the 1st phase. In asymmetric t_{ON} mode, the PWM on-time is scaled to reduce the switching frequency, reducing switching loss and improving light-load efficiency. The scaling factor of the PWM on-time can be set by the NVM registers ASYM_TON_PSx<rail>, where x = 1, 2, and 3, respectively. Table 3 below summarizes the PWM on-time extension for different conditions.

It should be noted that in an asymmetric VR design, smaller power switch usually indicates lower current capability. And higher inductance results in a lower saturation current of the inductor. Therefore, it is necessary to limit the phase 1 current using the current balancing setting to prevent the device from being damaged or overstressed.

Table 3. PWM On-Time Extension for Asymmetric VR Design

	EN_SPM = 1 & EN_ASYM_TON = 1 & EN_ASYM_TON_SPM_DEM = 0	EN_SPM = 1 & EN_ASYM_TON = 1 & EN_ASYM_TON_SPM_DEM = 1
PS0 t_{ON}	Nominal t_{ON}	Nominal t_{ON} * ASYM_TON_SPM_DEM
PS1 t_{ON}	If EN_PS1_SLOW_CCM = 1: Nominal t_{ON} If EN_PS1_SLOW_CCM = 0: Nominal t_{ON} * ASYM_TON_PS1	If EN_PS1_SLOW_CCM = 1: Nominal t_{ON} * ASYM_TON_SPM_DEM If EN_PS1_SLOW_CCM = 0: Nominal t_{ON} * ASYM_TON_PS1
PS2 t_{ON}	Nominal t_{ON} * ASYM_TON_PS2	
PS3 t_{ON}	Nominal t_{ON} * ASYM_TON_PS3	

18.19 Smart Phase Management

The RT3645BE controller adopts the new generation of Smart Phase Management (SPM) technique to improve efficiency with fast phase adding and shedding operations. The SPM function can be enabled or disabled by the NVM registers EN_SPM_<rail>. The controller compares the sensed output current with the SPM current threshold and hysteresis to determine the operating phase number. The NVM registers for SPM threshold are defined as a percentage of ICCMAX, and the hysteresis register is defined as a linear fraction of V_{ICCMAX}. For the VCCCORE rail, the SPM threshold can be set in registers SPM_THx_A, with x = 2, 3, 4, and 5. The SPM hysteresis can be set in SPM_HYS_A. For the VCCGT rail, the SPM threshold can be set in SPM_TH2_B and the hysteresis can be set in SPM_HYS_B. It is strongly suggested to set the hysteresis higher than half of the inductor current ripple to prevent oscillation between phase adding and shedding. When SPM is enabled, the controller enters DEM automatically when the inductor current is lower than the ZCD threshold. Figure 15 shows the operating principle of SPM for the VCCCORE rail. There is no delay time for phase adding; that is, the operating phase number can increase immediately if the loading current is higher than the SPM thresholds defined in the NVM registers. The delay time for phase shedding is 5μs.

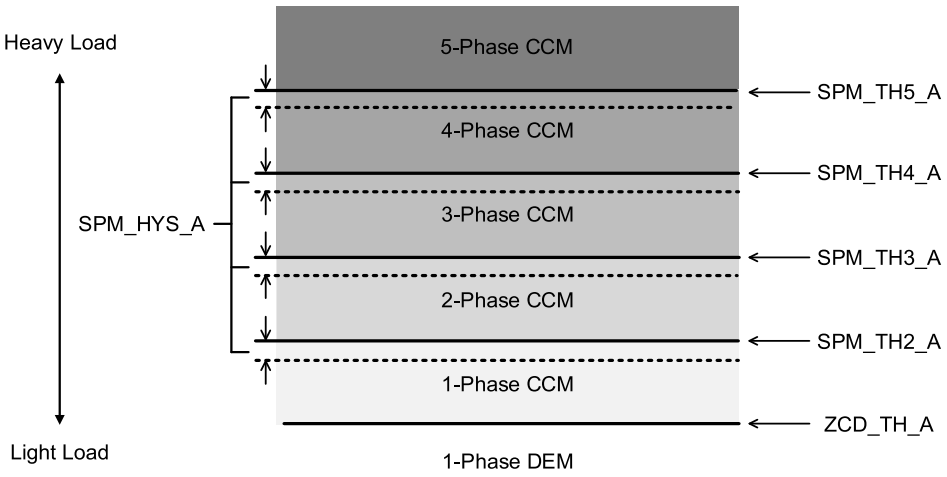


Figure 15. Operating Principle of SPM for VCCCORE rail

18.20 Dynamic VID (DVID) Compensation

When a DVID up command is issued by the CPU, the VR output current starts to charge the output capacitors. For a non-zero load-line system, the charging current induces extra voltage droop, which may prevent the output voltage from reaching the target VID within the required timing. The charging current and the droop voltage can be estimated as follows:

I_{Charge} = DVID_SR x C_{OUT}

V_{Droop} = I_{Charge} x LL = DVID_SR x C_{OUT} x LL

The same methodology is also applicable for downward DVID, where the VR output current discharges the output capacitors. The RT3645BE controller provides DVID lift/pull offset to compensate for the droop effect.

The register DVID_UP_LIFT_<rail> offers a positive offset to lift the target voltage during DVID up, and DVID_DN_PULL_<rail> provides a negative offset to pull the target voltage during downward DVID. The NVM register DVID_COMP_TAU_<rail> allows configuration of the time constant used to gradually release the DVID lift/pull offset after the target VID is reached. Figure 16 shows the DVID lift/pull compensation. Note that the equations above can provide an initial value for DVID lift/pull compensation, however, final settings should be based on actual measurements.

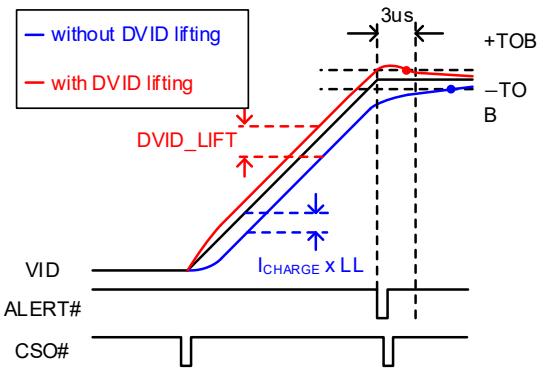


Figure 16. DVID Lift Compensation

18.21 Overcurrent and Soft-Start Overcurrent Protection (OCP and SSOCP)

The RT3645BE controller provides soft-start overcurrent protection (SSOCP) for the initial startup from 0V. Figure 17 illustrates the SSOCP behavior. When the inductor current exceeds the SSOCP threshold, the controller forces all PWM signals into tri-state, turning off both the high-side and low-side switches. It also asserts the OCP bit in the FAULT_STATUS register and de-asserts VR_READY. The SSOCP threshold is 200% of ICCMAX. After the SSOCP event is resolved, the controller can be restarted by toggling the VCC power or the EN pin.

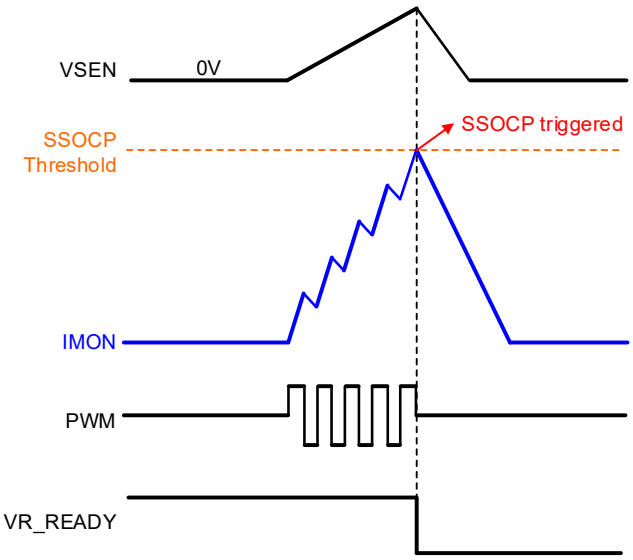


Figure 17. Soft-Start OCP Behavior

The RT3645BE also provides sum overcurrent protection (SOCP) to prevent the power stage from being damaged. The threshold of SCOP can be set by the register SOC_TH_SEL_<rail> as a percentage of ICCMAX. The default value of the SOCP threshold is 130% of ICCMAX. Figure 18 shows the behavior of SOCP. SOCP is masked during DVID events and for an additional 80µs after the VID has settled. The de-glitch time for SOCP is 20µs. If the loading current is higher than the SOCP threshold and continues over the de-glitch time, the controller will force all PWM signals into tri-state, turning off both the high-side and low-side switches. It also asserts the OCP bit in the FAULT_STATUS register and de-asserts VR_READY. After the SOCP event is resolved, the controller can be restarted by toggling the VCC power or the EN pin.

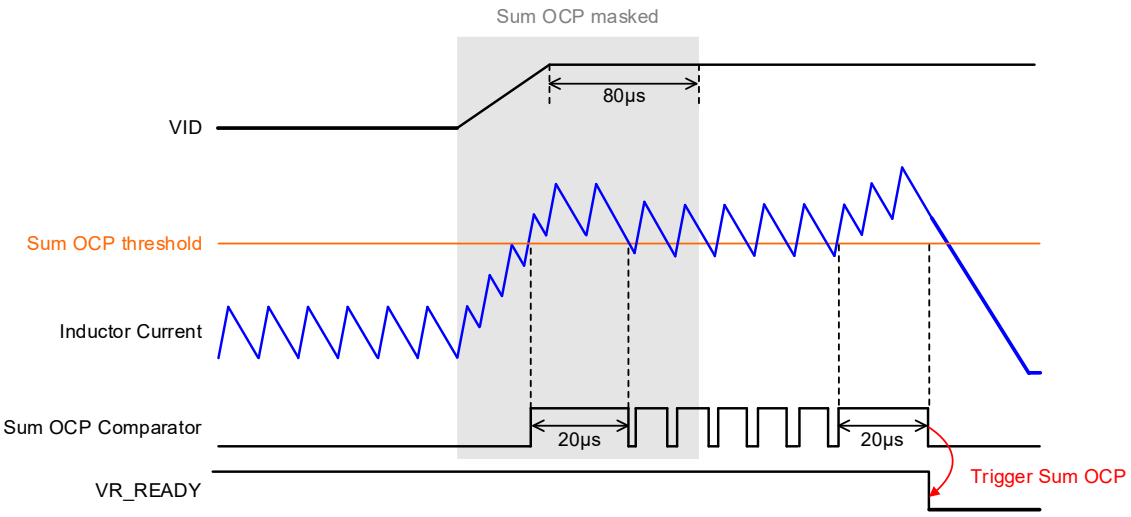


Figure 18. Sum OCP Behavior

18.22 Overvoltage Protection (OVP)

The RT3645BE provides both relative and absolute OVP based on the operating VID. OVP is masked when VID = 0V. For 5mV VID step, the OVP threshold is 2.45V during the initial startup from 0V. For 10mV VID step, the OVP threshold is 3.05V during the initial startup from 0V when startup from 0V. In normal operation, including steady-state and DVID up/down from a non-zero VID, the OVP thresholds are defined as follows:

OVP_TH = VID + 350mV if VID ≥ 1V

OVP_TH = 1.35V if VID < 1V.

Figure 19 and Figure 20 illustrate the OVP threshold and behavior. The de-glitch time for OVP is 0.5µs. When OVP is triggered, the controller will force all PWM signals low to turn off the high-side switches, assert the OVP bit in the FAULT_STATUS register and de-asserts VR_READY. All PWM signals remain low until the output voltage is pulled down to the target VID. The VID starts to ramp down at a slow slew rate, 60µs after the OVP event. The output voltage is shut down softly with all PWM signals toggling between low and tri-state. Table 4 summarizes the OVP behavior and thresholds for different conditions.

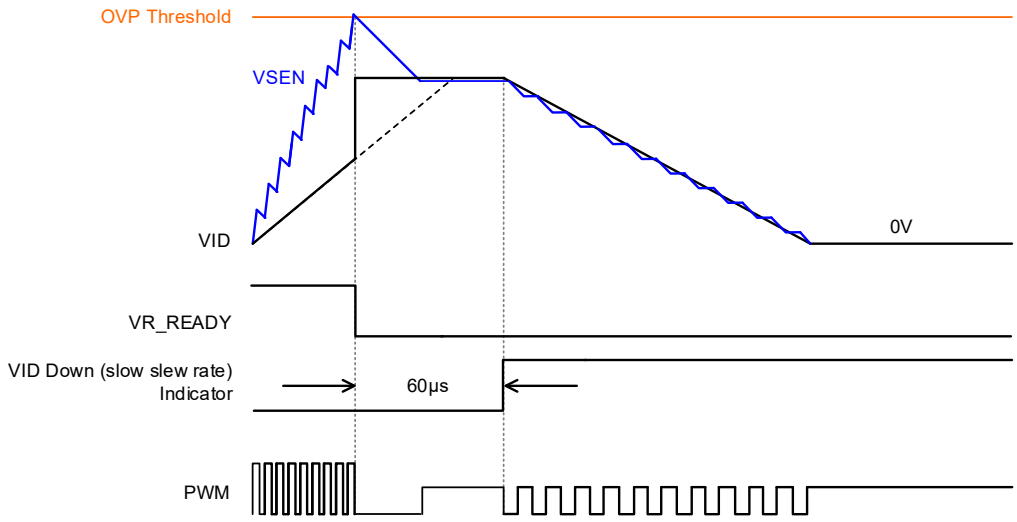


Figure 19. OVP for Startup from 0V

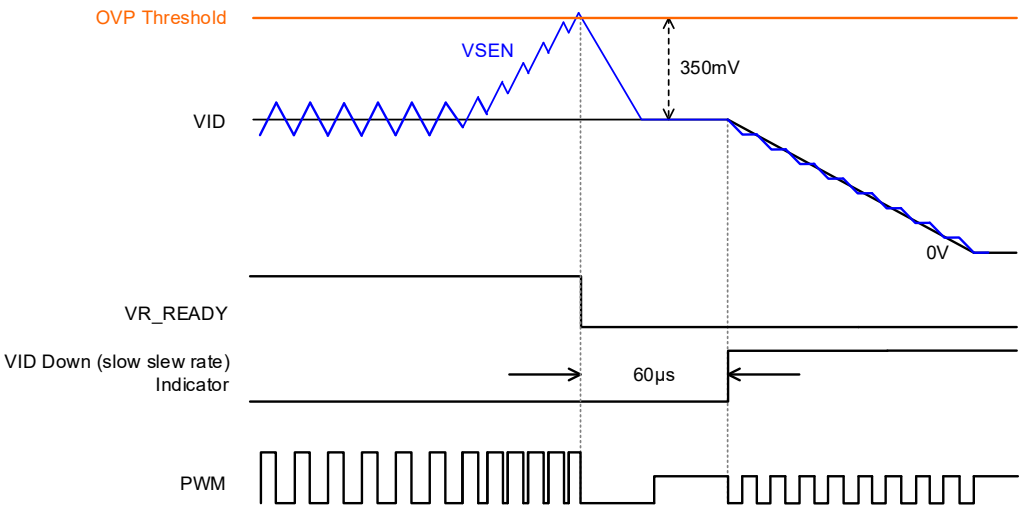


Figure 20. OVP Behavior for Normal Operation

Table 4. Summary of OVP Threshold and Behavior

VID Condition	OVP Threshold	Protection Behavior	Reset
VID = 0V	OVP masked	NA	Toggle VCC power or EN pin
Initial Startup from 0V	For 5mV VID step: OVP_TH = 2.45V For 10mV VID step: OV_TH = 3.05V	VR_READY de-assertion. VSEN is pulled down to below 2.1V and then soft shuts down to 0V	
DVID from Non-Zero VID	If VID ≥ 1V OVP_TH = VID + 350mV	VR_READY de-assertion. VSEN is pulled down to below VID and then soft shuts down to 0V	
VID ≠ 0V	If VID < 1V OVP_TH = 1.35V		

18.23 Undervoltage Protection (UVP)

The RT3645BE controller provides undervoltage protection. UVP is masked during DVID events and for an additional 80μs after the VID has settled. The de-glitch time for UVP is 3μs. When the output voltage is lower than (VID – 650mV), the controller forces all PWM signals into tri-state, turning off both the high-side and low-side switches, asserts the UVP bit in the FAULT_STATUS register and de-asserts VR_READY. Figure 21 shows the UVP threshold and behavior.

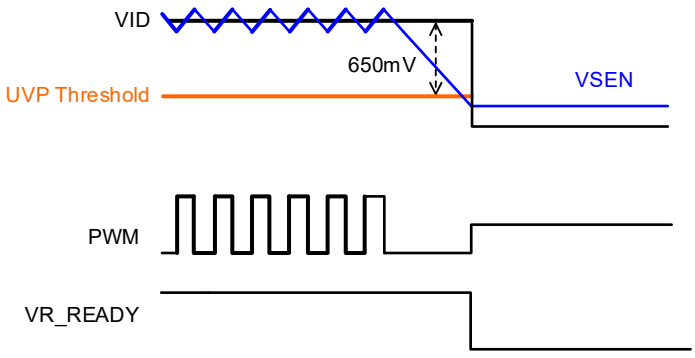


Figure 21. UVP Threshold and Behavior

18.24 SPS/DrMOS Fault Detection

The RT3645BE provides SPS/DrMOS fault detection by monitoring the TMON signal. When a fault event is detected by the SPS or DrMOS, the TMON voltage is pulled to a typical 3.3V. The SPS/DrMOS fault detection threshold for the RT3645BE controller is 2.2V with a de-glitch time of 600ns. When the SPS/DrMOS fault is detected, the controller forces all PWM signals into tri-state, turning off both the high-side and low-side switches. It also asserts the SPS_FAULT bit in the FAULT_STATUS register and de-asserts VR_READY.

18.25 Fault Event Indicator

The RT3645BE provides a fault indicator when AUX_IMON telemetry is disabled. The AUX_IMON pin serves fault indicator and outputs different voltage levels based on different protection events as summarized in Table 5. The RT3645BE controller also provides a FAULT_STATUS register that can be read via the I^2C interface. The FAULT_STATUS register is read-only, with bit 7 to bit 4 indicating the rail that triggered the protection, and bit 3 to 0 showing the specific fault event. Refer to the Functional Register Description of the FAULT_STATUS register.

Table 5. Fault Indicator Summary
(IMON_AUX = Disable)

Protection Type	Fault Flag	Protection Reset
OVP	1.0V ± 50mV	VCC/EN toggle
UVP	1.4V ± 50mV	
SOCP	1.8V ± 50mV	
SSOCP		
SPS Fault	2.2V ± 50mV	

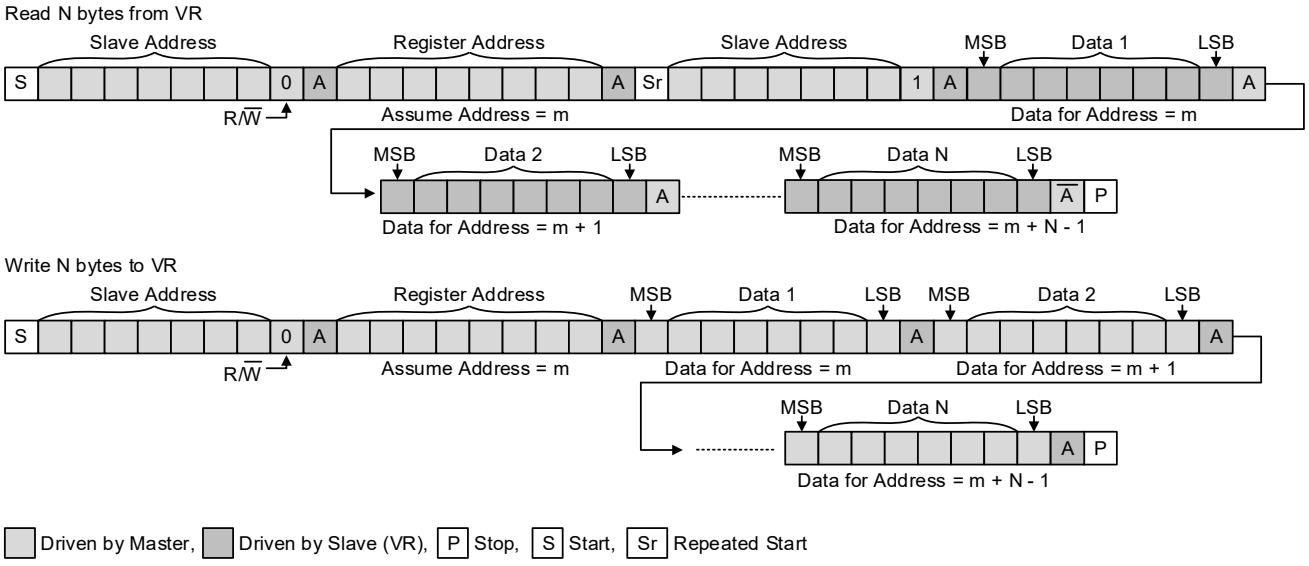
Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

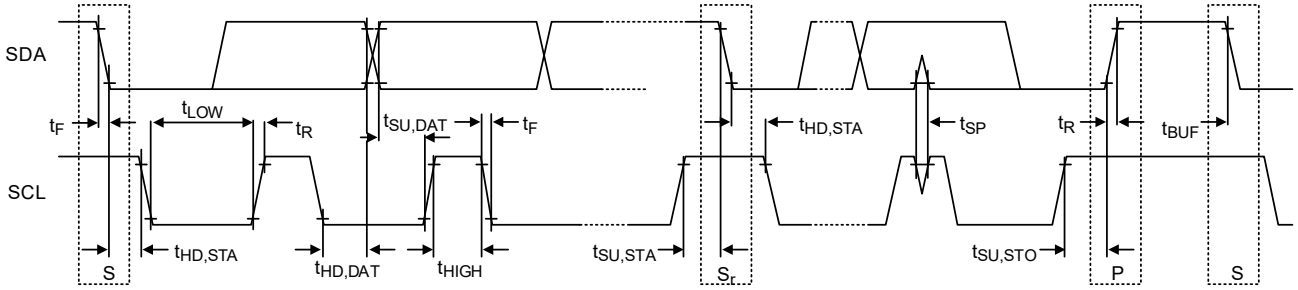
19 Functional Register Description

Refer to the Application Information section for details on slave address settings.

The I^2C interface of the RT3645BE controller does not support the clock stretching function.

The RT3645BE controller supports standard mode (100kbps) and fast mode (400kbps) with the standard I^2C protocol. The write or read bit stream (N > 1) is shown in the following figure:





All reserved bit(s) must be kept at their default values.

Table 6. Register Attribute Mapping

Attribute	Meaning
Page	Specifies the page on which the register is located
Default	Represents the default value of the register in hexadecimal
Type	Access type of the register. R = Read-only W = Write-only RW = Read-write
NVM	The register supports NVM programming or not. Y = Support NVM programming N = Not applicable
CONFIG	The register supports different CONFIG settings or not. Y = Support different CONFIG settings N = Not applicable
KEY	The register requires key to access or not. Y = Specific key required N = No key required to access the register

Table 7. Register Table Summary

Page	Address	Register Name	Default	Type	NVM
Global	0xEC	NVM_PROGRAM_STATUS	--	R	N
	0xED	NVM_PROGRAM_CTRL	--	W	N
	0xEF	PAGE	0x08	RW	N
	0xF1	ENTER_CONFIG_MODE	--	W	N
	0xF9	FAULT_STATUS	--	R	N
	0xFE	PRODUCT_ID	0x45	R	N

Table 8 to Table 13 provide bit field description of global registers. Global registers can be accessed without writing to the PAGE register. No specific key is required to access global registers.

Table 8. Bit Field Description of Register NVM_PROGRAM_STATUS

Page: Global **Address:** 0xEC **Description:** NVM status indicator								
Bit	7	6	5	4	3	2	1	0
Field	RELOAD_FINISH	PROGRAM_FINISH	PROGRAM_ALLOW	RELOAD_BUSY	PROGRAM_BUSY	CRC_FAIL	RESERVED	
Default	N/A							
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
7	RELOAD_FINISH	0: NVM reload in progress 1: NVM reload finished
6	PROGRAM_FINISH	0: NVM programming in progress 1: NVM programming finished
5	PROGRAM_ALLOW	0: NVM is NOT allowed to be programmed. 1: NVM is allowed to be programmed.
4	RELOAD_BUSY	0: NVM reload NOT busy 1: NVM reload busy
3	PROGRAM_BUSY	0: NVM programming NOT busy 1: NVM programming busy
2	CRC_FAIL	0: NVM CRC check pass 1: NVM CRC check fail
1:0	RESERVED	Reserved bit(s)

Table 9. Bit Field Description of Register NVM_PROGRAM_CTRL

Page: Global
Address: 0xED
Description: NVM store and restore instructions. When the controller receives a program command, the controller copies the content of functional registers into the corresponding address of non-volatile memory. A reload command instructs the controller to load data from non-volatile memory into the functional registers. This command should NOT be used during active output regulations. Note that the program command should be followed by a reload command with a delay time of 400ms.

Bit	7	6	5	4	3	2	1	0
Field	NVM_PROGRAM_CTRL							
Default	N/A							
Type	W	W	W	W	W	W	W	W

Bit	Name	Description
7:0	NVM_PROGRAM_CTRL	0x66: reload all data from NVM to functional registers. 0xA6: program all data from functional registers into NVM. All the other combinations are not defined.

Table 10. Bit Field Description of Register PAGE

Page: Global
Address: 0xEF
Description: Select the register page. DO NOT switch pages during active output regulation.

Bit	7	6	5	4	3	2	1	0
Field	PAGE							
Default	0	0	0	0	1	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7:0	PAGE	0x02 Enhance functional registers for general settings 0x03 Enhance functional registers for rail A 0x04 Enhance functional registers for rail B 0x05 Enhance functional registers for rail C 0x06 Enhance functional registers for rail D 0x08: Functional registers for general settings 0x09: Functional registers for rail A 0x0A: Functional registers for rail B 0x0B: Functional registers for rail C 0x0C: Functional registers for rail D 0x0D: Functional registers for I^2C settings 0x0E: Functional registers for asymmetric VR and FVM All the other combinations are not defined.

Table 11. Bit Field Description of Register ENTER_CONFIG_MODE

Page: Global **Address:** 0xF1 **Description:** Command to enter user configuration mode.								
Bit	7	6	5	4	3	2	1	0
Field	ENTER_CONFIG_MODE							
Default	N/A							
Type	W	W	W	W	W	W	W	W

Bit	Name	Description
7:0	ENTER_CONFIG_MODE	0x62 is not available. Contact RICHTEK to get the password to enter user configuration mode.

Table 12. Bit Field Description of Register FAULT_STATUS

Page: Global **Address:** 0xF9 **Description:** Fault status								
Bit	7	6	5	4	3	2	1	0
Field	FAULT_RAIL				FAULT_EVENT			
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
7:4	FAULT_RAIL	Indicate which rail triggers the fault event [7]: Rail D (VCCATOM) [6]: Rail C (VCCSA) [5]: Rail B (VCCGT) [4]: Rail A (VCCCORE)
3:0	FAULT_EVENT	Indicate which kind of fault event is triggered [3]: SPS Fault [2]: OCP (including SSOCP and SOCP) [1]: UVP [0]: OVP

Table 13. Bit Field Description of Register PRODUCT_ID

Page: Global **Address:** 0xFE **Description:** Same definition as SVID slave product ID (01h).								
Bit	7	6	5	4	3	2	1	0
Field	PRODUCT_ID							
Default	Refer to Description							
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
7:0	PRODUCT_ID	0x45 stands for the RT3645BE controller.

Table 14 to Table 29 provide bit field descriptions of NVM registers for enhanced function settings. A specific key is required to access functional registers; contact RICHTEK for the password. Make sure that the PAGE register is properly set before changing the content of functional registers.

Table 14. NVM Table Summary of Enhance_ALL Function Settings

Page	Address	Register Name	Default	Type	NVM
0x02	0x00	TSEN_TYPE	0xDE	RW	Y
0x02	0x01	RESERVED	0x02	RW	Y
0x02	0x02	RESERVED	0x88	RW	Y
0x02	0x03	RESERVED	0x90	RW	Y
0x02	0x04	RESERVED	0x83	RW	Y
0x02	0x05	PS3_IMON_RPT	0x30	RW	Y
0x02	0x06	RESERVED	0x44	RW	Y
0x02	0x07	RESERVED	0xFA	RW	Y
0x02	0x08	RESERVED	0x20	RW	Y
0x02	0x09	RESERVED	0x7E	RW	Y
0x02	0x0A	RESERVED	0x00	RW	Y
0x02	0x0B	SPM_DN_TIME_STEP_HYS	0x5C	RW	Y
0x02	0x0C	IMON_AUX	0x05	RW	Y
0x02	0x0D	RESERVED	0x8F	RW	Y
0x02	0x0E	RESERVED	0xF0	RW	Y
0x02	0x0F	RESERVED	0x09	RW	Y
0x02	0x10	RESERVED	0x60	RW	Y
0x02	0x11	RESERVED	0x00	RW	Y
0x02	0x12	RESERVED	0x00	RW	Y
0x02	0x13	RESERVED	0x00	RW	Y
0x02	0x14	RESERVED	0x00	RW	Y
0x02	0x15	RESERVED	0x00	RW	Y
0x02	0x16	RESERVED	0x00	RW	Y
0x02	0x17	CRC0_CHECK	--	R	N

Table 15. TSEN_TYPE

Page: 0x02 Address: 0x00								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED		TSEN_TYPE	RESERVED				
Default	1	1	0	1	1	1	1	0
Type	R	R	RW	R	R	R	R	R

Bit	Name	Description
7:6	RESERVED	Reserved bit(s)
5	TSEN_TYPE	SPS temperature reporting scale (TMON). 1: for 10mV/degree SPS 0: for 8mV/degree SPS
4:0	RESERVED	Reserved bit(s)

Table 16. PS3_IMON_RPT

Page: 0x02 Address: 0x05								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED						PS3_IMON_RPT	
Default	0	0	1	1	0	0	0	0
Type	R						RW	

Bit	Name	Description
7:2	RESERVED	Reserved bit(s)
1:0	PS3_IMON_RPT	Under PS3 or ultra-low load conditions, DIMON always reports a constant value. 00: 0A 01: 1A 10: 2A 11: 3A

Table 17. SPM_DN_TIME_STEP_HYS

Page: 0x02 Address: 0x0B								
Bit	7	6	5	4	3	2	1	0
Field	SPM_DN_PH_TIME		SPM_DN_PH_STEP	RESERVED			SPM_HYS_DOUBLE_CORE	SPM_HYS_DOUBLE_GT
Default	0	1	0	1	1	1	0	0

Type	RW	RW	R	RW

Bit	Name	Description
7:6	SPM_DN_PH_TIME	Set the CORE/GT SPM down-phase delay time.00: 1us 01: 2us 10: 3us 11: 4us
5	SPM_DN_PH_STEP	According to SPM, when the current decreases, the number of phases drops either immediately or step by step. 1: step by step 0: directly down to the target phase
4:2	RESERVED	Reserved bit(s)
1	SPM_HYS_DOUBLE_CORE	1: Enable 0: Disable
0	SPM_HYS_DOUBLE_GT	1: Enable 0: Disable

Table 18. IMON_AUX

Page: 0x02 **Address: 0x0C**								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED					IMON_AUX	RESERVED	
Default	0	0	0	0	0	1	0	1
Type	R					RW	R	

Bit	Name	Description
7:3	RESERVED	Reserved bit(s)
2	IMON_AUX	1: Fault indicator 0: IMON_AUX
1:0	RESERVED	Reserved bit(s)

Table 19. CRC0_CHECK

Page: 0x02 **Address: 0x17**								
Bit	7	6	5	4	3	2	1	0
Field	CRC0_CHECK							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description

7:0	CRC0_CHECK	The cyclic redundancy code (CRC) of all functional registers from PAGE 0x02 to 0x06

Table 20. NVM Table Summary of Enhanced Functional Registers

Page	Address	Register Name	Default	Type	NVM
0x03	0x00	RESERVED	0x94	RW	Y
0x03	0x01	RESERVED	0xA1	RW	Y
0x03	0x02	RESERVED	0x9C	RW	Y
0x03	0X03	RESERVED	0x85	RW	Y
0x03	0x04	CCM_CLAMP_A	0x3F	RW	Y
0x03	0x05	PS_LIFT_VID_A	0x03	RW	Y
0x03	0x06	DEM_LIFT_5MV_A	0xDC	RW	Y
0x03	0x07	AQR_TH_MSB_A	0x64	RW	Y
0x03	0x08	DVID_DN_UP_LPF_A	0x5A	RW	Y
0x03	0x09	RESERVED	0xCF	RW	Y
0x03	0x0A	AQR_WIDTH_A	0x7E	RW	Y
0x03	0x0B	DVID_DECAY_OFS_COMP_A	0x9D	RW	Y
0x03	0x0C	RESERVED	0xD0	RW	Y
0x03	0x0D	RESERVED	0x12	RW	Y
0x03	0x0E	RESERVED	0xEF	RW	Y
0x03	0x0F	RESERVED	0x07	RW	Y
0x03	0x10	DEM_HOLD_LPF_DLY_A	0x3A	RW	Y
0x03	0x11	DVID_ALERT_DLY_A	0x00	RW	Y
0x04	0x00	RESERVED	0xBA	RW	Y
0x04	0x01	RESERVED	0xA1	RW	Y
0x04	0x02	RESERVED	0x9B	RW	Y
0x04	0X03	RESERVED	0x87	RW	Y
0x04	0x04	CCM_CLAMP_B	0x33	RW	Y
0x04	0x05	PS_LIFT_VID_B	0x93	RW	Y
0x04	0x06	DEM_LIFT_5MV_B	0xCC	RW	Y
0x04	0x07	AQR_TH_MSB_B	0x24	RW	Y
0x04	0x08	DVID_DN_UP_LPF_B	0x58	RW	Y
0x04	0x09	RESERVED	0xC7	RW	Y

Page	Address	Register Name	Default	Type	NVM
0x04	0x0A	AQR_WIDTH_B	0x7E	RW	Y
0x04	0x0B	DVID_DECAY_OFS_COMP_B	0x7D	RW	Y
0x04	0x0C	RESERVED	0xD0	RW	Y
0x04	0x0D	RESERVED	0xD6	RW	Y
0x04	0x0E	RESERVED	0x61	RW	Y
0x04	0x0F	RESERVED	0x07	RW	Y
0x04	0x10	DEM_HOLD_LPF_DLY_B	0x3A	RW	Y
0x04	0x11	DVID_ALERT_DLY_B	0x00	RW	Y
0x05	0x00	RESERVED	0xBA	RW	Y
0x05	0x01	RESERVED	0xA1	RW	Y
0x05	0x02	RESERVED	0x9B	RW	Y
0x05	0X03	RESERVED	0x87	RW	Y
0x05	0x04	CCM_CLAMP_C	0x34	RW	Y
0x05	0x05	PS_LIFT_VID_C	0x92	RW	Y
0x05	0x06	DEM_LIFT_5MV_C	0xCC	RW	Y
0x05	0x07	AQR_TH_MSB_C	0x6C	RW	Y
0x05	0x08	DVID_DN_UP_LPF_C	0x58	RW	Y
0x05	0x09	RESERVED	0xC7	RW	Y
0x05	0x0A	AQR_WIDTH_C	0x7E	RW	Y
0x05	0x0B	DVID_DECAY_OFS_COMP_C	0x7D	RW	Y
0x05	0x0C	RESERVED	0xD0	RW	Y
0x05	0x0D	RESERVED	0xD6	RW	Y
0x05	0x0E	RESERVED	0xE1	RW	Y
0x05	0x0F	RESERVED	0x07	RW	Y
0x05	0x10	DEM_HOLD_LPF_DLY_C	0x3A	RW	Y
0x05	0x11	DVID_ALERT_DLY_C	0x00	RW	Y
0x06	0x00	RESERVED	0xBA	RW	Y
0x06	0x01	RESERVED	0xA1	RW	Y
0x06	0x02	RESERVED	0x9F	RW	Y
0x06	0X03	RESERVED	0x87	RW	Y
0x06	0x04	CCM_CLAMP_D	0xB5	RW	Y

Page	Address	Register Name	Default	Type	NVM
0x06	0x05	PS_LIFT_VID_D	0x92	RW	Y
0x06	0x06	DEM_LIFT_5MV_D	0xCE	RW	Y
0x06	0x07	AQR_TH_MSB_D	0x64	RW	Y
0x06	0x08	DVID_DN_UP_LPF_D	0x5A	RW	Y
0x06	0x09	RESERVED	0xC7	RW	Y
0x06	0x0A	AQR_WIDTH_D	0x7E	RW	Y
0x06	0x0B	DVID_DECAY_OFS_COMP_D	0x7D	RW	Y
0x06	0x0C	RESERVED	0xD0	RW	Y
0x06	0x0D	RESERVED	0xD6	RW	Y
0x06	0x0E	RESERVED	0x61	RW	Y
0x06	0x0F	RESERVED	0x07	RW	Y
0x06	0x10	DEM_HOLD_LPF_DLY_D	0x3A	RW	Y
0x06	0x11	DVID_ALERT_DLY_D	0x00	RW	Y

Table 21. CCM_CLAMP_A

Page: 0x03 **Address: 0x04**								
Bit	7	6	5	4	3	2	1	0
Field	ENTER_DEM_LIFT_VID	RESERVED			CCM_RAMP_CLAMP			
Default	0	0	1	1	1	1	1	1
Type	RW	R			RW			

Bit	Name	Description
7	ENTER_DEM_LIFT_VID	Entering PSK lift VID 1: Enable 0: Disable
6:4	RESERVED	Reserved bit(s)
3:0	CCM_RAMP_CLAMP	Select the ramp clamping level in CCM operation. Ramp clamping level = 2.4V – [3:0] x 40mV 0000: 2400mV 0001: 2360mV 0010: 2320mV 1101: 1880mV 1110: 1840mV 1111: 1800mV

Table 22. PS_LIFT_VID_A

Page: 0x03 Address: 0x05								
Bit	7	6	5	4	3	2	1	0
Field	PS0 to PS1_Lift VID	RESERVED	PS1 to PS0_Lift VID	RESERVED	Exit PS23_lift_VID	RESERVED		
Default	0	0	0	0	0	0	1	1
Type	RW	R	RW	R	RW	R		

Bit	Name	Description
7	PS0 to PS1_Lift VID	1: Enable 0: Disable
6	RESERVED	Reserved bit(s)
5	PS1 to PS0_Lift VID	1: Enable 0: Disable
4	RESERVED	Reserved bit(s)
3	Exit PS23_lift_VID	1: Enable 0: Disable
2:0	RESERVED	Reserved bit(s)

Table 23. DEM_LIFT_5MV_A

Page: 0x03 Address: 0x06								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED	DEM_LIFT_5mV	RESERVED					
Default	1	1	0	1	1	1	0	0
Type	R	RW	R					

Bit	Name	Description
7	RESERVED	Reserved bit(s)
6	RESERVED	1: Enable 0: Disable
5:0	RESERVED	Reserved bit(s)

Table 24. AQR_TH_MSB_A

Page: 0x03 Address: 0x07								
Bit	7	6	5	4	3	2	1	0
Field	AQR_TH		RESERVED					
Default	0	1	1	0	0	1	0	0
Type	RW		R					

Bit	Name	Description
7:6	AQR_TH	Set the trigger level of AQR for the rail. AQR_TH = 40mV/per step **00**000: 40mV **00**001: 80mV ..... **01**110: 600mV **01**111: Disable **10**000: 280mV **10**001: 320mV ..... **11**110: 840mV **11**111: Disable
5:0	RESERVED	Reserved bit(s)

Table 25. DVID_DN_UP_LPF_A

Page: 0x03 Address: 0x08								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED		DVID_DN_HOLD_LPF	DVID_DN_SHUTDN_LPF	DVID_UP_HOLD_LPF	DVID_UP_SHUTDN_LPF	RESERVED	
Default	0	1	0	1	1	0	1	0
Type	R		RW				R	

Bit	Name	Description
7:6	RESERVED	Reserved bit(s)
5	DVID_DN_HOLD_LPF	Hold LPF during DVIDDN. 1: Enable 0: Disable
4	DVID_DN_SHUTDN_LPF	Shutdown LPF during DVIDDN. 1: Enable 0: Disable

3	DVID_UP_HOLD_LPF	Hold LPF during DVIDUP. 1: Enable 0: Disable
2	DVID_UP_SHUTDN_LPF	Shutdown LPF during DVIDUP. 1: Enable 0: Disable
1:0	RESERVED	Reserved bit(s)

Table 26. AQR_WIDTH_A

Page: 0x03 **Address: 0x0A**								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED						AQR_WIDTH	
Default	0	1	1	1	1	1	1	0
Type	R						RW	

Bit	Name	Description
7:2	RESERVED	Reserved bit(s)
1:0	AQR_WIDTH	The PWM TON width when AQR is triggered. 00: 66.66% x TON 01: 57% x TON 10: 50% x TON 11: 40% x TON

Table 27. DVID_DECAY_OFS_COMP_A

Page: 0x03 **Address: 0x0B**								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED	DVID_DECAY_OFS_COMP			RESERVED			
Default	1	0	0	1	1	1	0	1
Type	R	RW			R			

Bit	Name	Description
7	RESERVED	Reserved bit(s)
6:4	DVID_DECAY_OFS_COMP	000:0 001:5mV 010:10mV 011:15mV 100:0 101:-5mV 110:-10mV 111: -15mV
3:0	RESERVED	Reserved bit(s)

Table 28. DEM_HOLD_LPF_DLY_A

Page: 0x03 Address: 0x10								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED				DEM_HOLD_LPF_OFS		DEM_HOLD_LPF_DLY	
Default	0	0	1	1	1	0	1	0
Type	R				RW			

Bit	Name	Description
7:4	RESERVED	Reserved bit(s)
3:2	DEM_HOLD_LPF_OFS	100: 0 101: -2.5mV 110: -5mV 111: -7.5mV
1:0	DEM_HOLD_LPF_DLY	00: 5us 01: 10us 10: 20us 11: 40us

Table 29. DVID_ALERT_DLY_A

Page: 0x03 Address: 0x11								
Bit	7	6	5	4	3	2	1	0
Field	DVID_ALERT_DLY		RESERVED					
Default	0	0	0	0	0	0	0	0
Type	RW		R					

Bit	Name	Description
7:6	DVID_ALERT_DLY	When the decay voltage reaches the target voltage, the ALERT delay time can be set as: 00: 0us 01: 2us 10: 4us 11: 6us
5:0	RESERVED	Reserved bit(s)

Table 30 to Table 41 provide bit field description of NVM registers for general settings. A specific key is required to access functional registers; contact RICHTEK for the password. Make sure the PAGE register is properly set before changing the content of functional registers.

Table 30. NVM Table Summary of General Function Settings

Page	Address	Register Name	Default	Type	NVM
0x08	0x00	ICCMAX_AUX	0x80	RW	Y
0x08	0x01	AUX_HC_PSYS_SCALE_RAIL_EN	0x00	RW	Y
0x08	0x02	MAX_PH_DVID_INTLV	0x00	RW	Y
0x08	0x03	PM_DISA_DCM_DRVEN_IMPV_SEL	0x3E	RW	Y
0x08	0x04	EN_VR_I2C_ADDR_SET1	0xE8	RW	Y
0x08	0x05	DISA_FASTDN_FVM_HOLD_VID_VRHOT_I2C_ADDR_SET2	0xF8	RW	Y
0x08	0x06	PWM_HIZ_SEL	0xFF	RW	Y
0x08	0x07	DEADTIME_SET_A_B	0x00	RW	Y
0x08	0x08	DEADTIME_SET_C_D	0x00	RW	Y
0x08	0x09	CUSTOM_FW_VERSION	0x00	RW	Y
0x08	0x0A	CRC1_CHECK	--	R	N

Table 31. ICCMAX_AUX

Page: 0x08 **Address: 0x00**								
Bit	7	6	5	4	3	2	1	0
Field	ICCMAX_AUX							
Default	1	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	ICCMAX_AUX	Set ICCMAX value for the auxiliary VR rail. 0000 0000: 0A 0000 0001: 1A 0000 0010: 2A 1111 1101: 253A 1111 1110: 254A 1111 1111: 255A

Table 32. AUX_HC_PSYS_SCALE_RAIL_EN

Page: 0x08 Address: 0x01								
Bit	7	6	5	4	3	2	1	0
Field	ICCMAX_HC_AUX		PSYS_SCALE_SEL	EN_PSYS_DOMAIN	EN_RAIL_A	EN_RAIL_B	EN_RAIL_C	EN_RAIL_D
Default	0	0	0	0	0	0	0	0
Type	RW		RW	RW	RW	RW	RW	RW

Bit	Name	Description
7:6	ICCMAX_HC_AUX	Set the high current capability for ICCMAX of auxiliary VR rail. 00: 1A/LSB 01: 2A/LSB 10: 4A/LSB 11: 8A/LSB
5	PSYS_SCALE_SEL	Select PSYS input scale. 0: 1.6V 1: 3.2V
4	EN_PSYS_DOMAIN	Enable/disable PSYS domain 0: Enable 1: Disable
3	EN_RAIL_A	Enable/disable rail A 0: Enable 1: Disable
2	EN_RAIL_B	Enable/disable rail B 0: Enable 1: Disable
1	EN_RAIL_C	Enable/disable rail C 0: Enable 1: Disable
0	EN_RAIL_D	Enable/disable rail D 0: Enable 1: Disable

Table 33. MAX_PH_DVID_INTLV

Page: 0x08 Address: 0x02								
Bit	7	6	5	4	3	2	1	0
Field	MAX_PH_A			MAX_PH_B	EN_DVIDUP_INTLV_A	Reserved		EN_DVIDUP_INTLV_B
Default	0	0	0	0	0	0	0	0
Type	RW			RW	R			

Bit	Name	Description
7:5	MAX_PH_A	Set the active phase number for rail A. 000: 5-phase 100: 4-phase

		101: 3-phase 110: 2-phase 111: 1-phase All the other combinations are not defined.
4	MAX_PH_B	Set the active phase number for rail B. 0: 2-phase 1: 1-phase
3:	EN_DVIDUP_INTLV_A	Accelerate PWM interleaving for rail A when DVID up. 0: Disable 1: Enable
2:1	Reserved	Reserved bit(s)
0	EN_DVIDUP_INTLV_B	Accelerate PWM interleaving rail for B when DVID up. 0: Disable 1: Enable

Table 34. PM_DISA_DCM_DRVEN_IMPV_SEL

Page: 0x08 **Address: 0x03**								
Bit	7	6	5	4	3	2	1	0
Field	SPM_DISA_DCM_A	SPM_DISA_DCM_B	DRVEN_MODE_A	DRVEN_MODE_B	DRVEN_MODE_C	DRVEN_MODE_D	Reserved	IMVP_SPEC_SEL
Default	0	0	1	1	1	1	1	0
Type	RW	RW	RW	RW	RW	RW	R	RW

Bit	Name	Description
7	SPM_DISA_DCM_A	Enable/Disable DCM operation for rail A in SPM. 0: Enable DCM operation 1: Disable DCM operation
6	SPM_DISA_DCM_B	Enable/Disable DCM operation for rail B in SPM. 0: Enable DCM operation 1: Disable DCM operation
5	DRVEN_MODE_A	0: DRVEN_A remains LOW when rail A is in PS4. 1: DRVEN_A becomes FLOATING when rail A is in PS4.
4	DRVEN_MODE_B	0: DRVEN_B remains LOW when rail B is in PS4. 1: DRVEN_B becomes FLOATING when rail B is in PS4.
3	DRVEN_MODE_C	0: DRVEN_C remains LOW when rail C is in PS4. 1: DRVEN_C becomes FLOATING when rail C is in PS4.
2	DRVEN_MODE_D	0: DRVEN_D remains LOW when rail D is in PS4. 1: DRVEN_D becomes FLOATING when rail D is in PS4.
1	Reserved	Reserved bit(s)
0	IMVP_SPEC_SEL	Select the version of IMVP specification. 0: IMVP9.3 1: IMVP9.2

Table 35. EN_VR_I2C_ADDR_SET1

Page: 0x08 Address: 0x04								
Bit	7	6	5	4	3	2	1	0
Field	EN_VR	Reserved		I2C_ADDR_SET1				
Default	1	1	1	0	1	0	0	0
Type	RW	R		RW				

Bit	Name	Description
7	EN_VR	Control the ON/OFF status of the VR. 0: OFF 1: ON (VR can be activated when EN = HIGH.)
6:5	Reserved	Reserved bit(s)
4:0	I2C_ADDR_SET1	I^2C address setting. Refer to Application Information for a detailed description.

Table 36. DISA_FASTDN_FVM_HOLD_VID_VRHOT_I2C_ADDR_SET2

Page: 0x08 Address: 0x05								
Bit	7	6	5	4	3	2	1	0
Field	DISA_FASTDN	EN_FVM_HOLD_VID	EN_FVM_VRHOT	I2C_ADDR_SET2				
Default	1	1	1	1	1	0	0	0
Type	RW	RW	RW	RW				

Bit	Name	Description
7	DISA_FASTDN	Fast DVID down mitigation 0: Follow SVID command. 1: Execute the fast DVID down command with a slow slew rate.
6	EN_FVM_HOLD_VID	Control Fast-V Mode behavior during DVID. 0: VID and ALERT# follow normal operation. 1: Hold VID and delay ALERT# assertion when triggering FVM during DVID.
5	EN_FVM_VRHOT	Control Fast-V Mode behavior during DVID 0: No VR_HOT# assertion 1: Assert VR_HOT# when triggering FVM during DVID.
4:0	I2C_ADDR_SET2	I^2C address setting. Refer to the Application Information for a detailed description.

Table 37. PWM_HIZ_SEL

Page: 0x08 Address: 0x06								
Bit	7	6	5	4	3	2	1	0
Field	PWM_HIZ_LEVEL_A		PWM_HIZ_LEVEL_B		PWM_HIZ_LEVEL_C		PWM_HIZ_LEVEL_D	
Default	1	1	1	1	1	1	1	1
Type	RW		RW		RW		RW	

Bit	Name	Description
7:6	PWM_HIZ_LEVEL_A	Control the PWM tri-state level for rail A. 00: 1.66 ~ 2.17V 01: 1.43 ~ 1.90V 11: 1.27 ~ 1.66V
5:4	PWM_HIZ_LEVEL_B	Control the PWM tri-state level for rail B. 00: 1.66 ~ 2.17V 01: 1.43 ~ 1.90V 11: 1.27 ~ 1.66V
3:2	PWM_HIZ_LEVEL_C	Control the PWM tri-state level for rail C. 00: 1.66 ~ 2.17V 01: 1.43 ~ 1.90V 11: 1.27 ~ 1.66V
1:0	PWM_HIZ_LEVEL_D	Control the PWM tri-state level for rail D. 00: 1.66 ~ 2.17V 01: 1.43 ~ 1.90V 11: 1.27 ~ 1.66V

Table 38. DEADTIME_SET_A_B

Page: 0x08 Address: 0x07								
Bit	7	6	5	4	3	2	1	0
Field	DEADTIME_SET_A				DEADTIME_SET_B			
Default	0	0	0	0	0	0	0	0
Type	RW				RW			

Bit	Name	Description
7:4	DEADTIME_SET_A	Control the PWM on-time extension for Rail A to compensate for the deadtime of power switches. 0000: 0ns 0001: 10ns 0010: 15ns 0011: 20ns 0100: 25ns 0101: 30ns 0110: 35ns 0111: 40ns 1000: -5ns 1001: 5ns All the other combinations are not defined.
3:0	DEADTIME_SET_B	Control the PWM on-time extension for Rail B to compensate for the deadtime of power switches. 0000: 0ns 0001: 10ns 0010: 15ns 0011: 20ns 0100: 25ns 0101: 30ns 0110: 35ns 0111: 40ns 1000: -5ns 1001: 5ns All the other combinations are not defined.

Table 39. DEADTIME_SET_C_D

Page: 0x08 Address: 0x08								
Bit	7	6	5	4	3	2	1	0
Field	DEADTIME_SET_C				DEADTIME_SET_D			
Default	0	0	0	0	0	0	0	0
Type	RW				RW			

Bit	Name	Description
7:4	DEADTIME_SET_C	Control the PWM on-time extension for Rail C to compensate for the deadtime of power switches. 0000: 0ns 0001: 10ns 0010: 15ns 0011: 20ns 0100: 25ns 0101: 30ns 0110: 35ns 0111: 40ns 1000: -5ns 1001: 5ns All the other combinations are not defined.
3:0	DEADTIME_SET_D	Control the PWM on-time extension for Rail D to compensate for the deadtime of power switches. 0000: 0ns 0001: 10ns 0010: 15ns 0011: 20ns 0100: 25ns 0101: 30ns 0110: 35ns 0111: 40ns 1000: -5ns 1001: 5ns All the other combinations are not defined.

Table 40. CUSTOM_FW_VERSION

Page: 0x08 Address: 0x09								
Bit	7	6	5	4	3	2	1	0
Field	CUSTOM_FW_VERSION							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	CUSTOM_FW_VERSION	Reserved for customized code version control

Table 41. CRC1_CHECK

Page: 0x08 Address: 0x0A								
Bit	7	6	5	4	3	2	1	0
Field	CRC1_CHECK							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	CRC1_CHECK	The cyclic redundancy check (CRC) of all functional registers from PAGE 0x08 to 0x0D

Table 42 to Table 61 provide bit field description of NVM registers for rail A (page 0x09), rail B (page 0x0A), rail C (page 0x0B) and rail D (page 0x0C). A specific key is required to access functional registers; contact RICHTEK for the password. Make sure the PAGE register is properly set before changing the content of functional registers. For the default values of each functional register from page 0x09 (rail A) to page 0x0C (rail D), refer to Table 42.

Table 42. NVM Table Summary of Functional Registers

Page	Address	Register Name	Default	Type	NVM
0x09	0x00	ICCMAX	0x94	RW	Y
0x09	0x01	ICCMAX_HC_DVID_SR_SVID_ADDR	0x20	RW	Y
0x09	0x02	RLL_SET	0xC0	RW	Y
0x09	0x03	RAMP_KTON	0x28	RW	Y
0x09	0x04	RIMON_SET	0x74	RW	Y
0x09	0x05	RIMON_MSB_SET	0x00	RW	Y
0x09	0x06	RESERVED	0x40	RW	Y
0x09	0x07	SVID_DCLL	0x21	RW	Y
0x09	0x08	IMON_INJ_LPF_GAIN_SET_AI_GAIN	0x78	RW	Y
0x09	0x09	VID_STEP_HPF_RC_SET	0x3A	RW	Y
0x09	0x0A	LPF_RC_EXT_RC_SET	0x40	RW	Y
0x09	0x0B	IMON_LPF_DEM_TON_TSEN_SOC_SEL	0x6D	RW	Y
0x09	0x0C	AR_AQR_TH	0x27	RW	Y
0x09	0x0D	ANTIOVS_TH_DEM_RAMP_CLAMP	0xF5	RW	Y
0x09	0x0E	EN_SPM_DVID_ENHANCE	0xEE	RW	Y
0x09	0x0F	ZCD_SET_EN_VBOOT	0x76	RW	Y
0x09	0x10	SVID_VBOOT	0xA1	RW	Y
0x09	0x11	EN_SPS_OFS_LPF_INI_SET	0xDB	RW	Y
0x09	0x12	ZCD_HYS_ASYM_VID_HPF_GAIN_SET	0xC1	RW	Y
0x0A	0x00	ICCMAX	0x7C	RW	Y
0x0A	0x01	ICCMAX_HC_DVID_SR_SVID_ADDR	0x21	RW	Y
0x0A	0x02	RLL_SET	0x00	RW	Y
0x0A	0x03	RAMP_KTON	0x14	RW	Y
0x0A	0x04	RIMON_SET	0x87	RW	Y
0x0A	0x05	RIMON_MSB_SET	0x00	RW	Y
0x0A	0x06	RESERVED	0x40	RW	Y
0x0A	0x07	SVID_DCLL	0x00	RW	Y
0x0A	0x08	IMON_INJ_LPF_GAIN_SET_AI_GAIN	0xB3	RW	Y
0x0A	0x09	VID_STEP_HPF_RC_SET	0x27	RW	Y

0x0A	0x0A	LPF_RC_EXT_RC_SET	0x10	RW	Y
0x0A	0x0B	IMON_LPF_DEM_TON_TSEN_SOC_SEL	0xED	RW	Y
0x0A	0x0C	AR_AQR_TH	0x34	RW	Y
0x0A	0x0D	ANTIOVS_TH_DEM_RAMP_CLAMP	0x13	RW	Y
0x0A	0x0E	EN_SPM_DVID_ENHANCE	0xAD	RW	Y
0x0A	0x0F	ZCD_SET_EN_VBOOT	0xA4	RW	Y
0x0A	0x10	SVID_VBOOT	0xA1	RW	Y
0x0A	0x11	EN_SPS_OFS_LPF_INI_SET	0xF9	RW	Y
0x0A	0x12	ZCD_HYS_ASYM_VID_HPF_GAIN_SET	0xC6	RW	Y
0x0B	0x00	ICCMAX	0x36	RW	Y
0x0B	0x01	ICCMAX_HC_DVID_SR_SVID_ADDR	0x22	RW	Y
0x0B	0x02	RLL_SET	0xEE	RW	Y
0x0B	0x03	RAMP_KTON	0x16	RW	Y
0x0B	0x04	RIMON_SET	0xA1	RW	Y
0x0B	0x05	RIMON_MSB_SET	0x00	RW	Y
0x0B	0x06	RESERVED	0x40	RW	Y
0x0B	0x07	SVID_DCLL	0x37	RW	Y
0x0B	0x08	IMON_INJ_LPF_GAIN_SET_AI_GAIN	0x79	RW	Y
0x0B	0x09	VID_STEP_HPF_RC_SET	0x2A	RW	Y
0x0B	0x0A	LPF_RC_EXT_RC_SET	0x70	RW	Y
0x0B	0x0B	IMON_LPF_DEM_TON_TSEN_SOC_SEL	0x7D	RW	Y
0x0B	0x0C	AR_AQR_TH	0x07	RW	Y
0x0B	0x0D	ANTIOVS_TH_DEM_RAMP_CLAMP	0x13	RW	Y
0x0B	0x0E	EN_SPM_DVID_ENHANCE	0xFF	RW	Y
0x0B	0x0F	ZCD_SET_EN_VBOOT	0xF2	RW	Y
0x0B	0x10	SVID_VBOOT	0xA1	RW	Y
0x0B	0x11	EN_SPS_OFS_LPF_INI_SET	0x82	RW	Y
0x0B	0x12	ZCD_HYS_ASYM_VID_HPF_GAIN_SET	0xC7	RW	Y
0x0C	0x00	ICCMAX	0x1E	RW	Y
0x0C	0x01	ICCMAX_HC_DVID_SR_SVID_ADDR	0x23	RW	Y
0x0C	0x02	RLL_SET	0x8E	RW	Y
0x0C	0x03	RAMP_KTON	0x17	RW	Y
0x0C	0x04	RIMON_SET	0x1C	RW	Y
0x0C	0x05	RIMON_MSB_SET	0x20	RW	Y

0x0C	0x06	RESERVED	0x40	RW	Y
0x0C	0x07	SVID_DCLL	0x3A	RW	Y
0x0C	0x08	IMON_INJ_LPF_GAIN_SET_AI_GAIN	0x79	RW	Y
0x0C	0x09	VID_STEP_HPF_RC_SET	0x2A	RW	Y
0x0C	0x0A	LPF_RC_EXT_RC_SET	0x7C	RW	Y
0x0C	0x0B	IMON_LPF_DEM_TON_TSEN_SOC_SEL	0xBD	RW	Y
0x0C	0x0C	AR_AQR_TH	0x0F	RW	Y
0x0C	0x0D	ANTIOVS_TH_DEM_RAMP_CLAMP	0x13	RW	Y
0x0C	0x0E	EN_SPM_DVID_ENHANCE	0xFF	RW	Y
0x0C	0x0F	ZCD_SET_EN_VBOOT	0xFA	RW	Y
0x0C	0x10	SVID_VBOOT	0xA1	RW	Y
0x0C	0x11	EN_SPS_OFS_LPF_INI_SET	0x83	RW	Y
0x0C	0x12	ZCD_HYS_ASYM_VID_HPF_GAIN_SET	0xC7	RW	Y

Table 43. ICCMAX

Page: 0x09 **Address: 0x00**								
Bit	7	6	5	4	3	2	1	0
Field	ICCMAX							
Default	1	0	0	1	0	1	0	0
Type	RW							

Bit	Name	Description
7:0	ICCMAX	Set ICCMAX value for the rail. 0000 0000: 0A 0000 0001: 1A 0000 0010: 2A 1111 1101: 253A 1111 1110: 254A 1111 1111: 255A

Table 44. ICCMAX_HC_DVID_SR_SVID_ADDR

Page: 0x09 Address: 0x01								
Bit	7	6	5	4	3	2	1	0
Field	ICCMAX_HC		DVID_SR		SVID_ADDR			
Default	0	0	1	0	0	0	0	0
Type	RW		RW		RW			

Bit	Name	Description
7:6	ICCMAX_HC	Set ICCMAX high current capability of the rail. 00: 1A/LSB 01: 2A/LSB 10: 4A/LSB 11: 8A/LSB
5:4	DVID_SR	Select fast DVID slew rate of the rail. 00: 10mV/μs 01: 24mV/μs 10: 36mV/μs 11: 48mV/μs
3:0	SVID_ADDR	Set SVID address of the rail. 0000: 0x00 0001: 0x01 0010: 0x02 0011: 0x03 0100: 0x04 ..... 1001: 0x09 1010: 0x0A 1011: 0x0B 1100: 0x0C All values are available except 0x0D, 0x0E, and 0x0F.

Table 45. RLL_SET

Page: 0x09 **Address: 0x02**								
Bit	7	6	5	4	3	2	1	0
Field	RLL_SET							
Default	1	1	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	RLL_SET	Set the load-line of the rail. It is strongly suggested to program RLL when EN = LOW to avoid unexpected PWM behavior and voltage errors. 0000 0001: 1kΩ 0000 0010: 2kΩ 0000 0011: 3kΩ 1111 1101: 253kΩ 1111 1110: 254kΩ 1111 1111: 255kΩ

Table 46. RAMP_KTON

Page: 0x09 Address: 0x03								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	RAMP_CTRL			KTON			
Default	0	0	1	0	1	0	0	0
Type	R	RW			RW			

Bit	Name	Description
7	Reserved	Reserved bit(s)
6:4	RAMP_CTRL	Control the ramp signal amplitude of the rail. Ramp amplitude = 300mV + 100mV x [6:4] 000: 300mV 001: 400mV 110: 900mV 111: 1000mV
3:0	KTON	Select the KTON parameter for the PWM on-time of the rail. 0000: KTON = 1.6 0001: KTON = 1.8 0010: KTON = 2.0 0011: KTON = 2.2 0100: KTON = 2.4 0101: KTON = 2.6 0110: KTON = 2.8 0111: KTON = 3.0 1000: KTON = 3.2 1001: KTON = 3.4 1010: KTON = 3.6 1011: KTON = 3.8 1100: KTON = 4.0 1101: KTON = 4.4 1110: KTON = 4.8 1111: KTON = 5.2

Table 47. RIMON_SET

Page: 0x09 Address: 0x04								
Bit	7	6	5	4	3	2	1	0
Field	RIMON_SET							
Default	0	1	1	1	0	1	0	0
Type	RW							

Bit	Name	Description
7:0	RIMON_SET	Set the least significant bit 7 to bit 0 of RIMON register for IOUT telemetry of the rail. It is strongly suggested to program RIMON when EN = LOW to avoid unexpected PWM behavior and voltage errors.

Table 48. RIMON_MSB_SET

Page: 0x09 Address: 0x05								
Bit	7	6	5	4	3	2	1	0
Field	RIMON_MSB_SET			RESERVED				
Default	0	0	0	0	0	0	0	0
Type	RW			RW	RW			

Bit	Name	Description
7:5	RIMON_MSB_SET	Set the most significant bit 10 to bit 8 of RIMON register for IOUT telemetry of the rail. It is strongly suggested to program RIMON when EN = LOW to avoid unexpected PWM behavior and voltage errors.
4:0	RESERVED	Reserved bit(s)

Table 49. RESERVED

Page: 0x09 Address: 0x06								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED							
Default	0	1	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	RESERVED	Reserved bit(s)

Table 50. SVID_DCLL

Page: 0x09 **Address: 0x07**								
Bit	7	6	5	4	3	2	1	0
Field	SVID_DCLL							
Default	0	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	SVID_DCLL	Set the load-line for the SVID register 0x23 (0.1mΩ/LSB). 0000 0000: 0.0mΩ 0000 0001: 0.1mΩ 0000 0010: 0.2mΩ 1111 1101: 25.3mΩ 1111 1110: 25.4mΩ 1111 1111: 25.5mΩ

Table 51. IMON_INJ_LPF_GAIN_SET_AI_GAIN

Page: 0x09 **Address: 0x08**								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	IMON_INJ	LPF_GAIN_SET			AI_GAIN		
Default	0	1	1	1	1	0	0	0
Type	R	RW	RW			RW		

Bit	Name	Description
7	Reserved	Reserved bit(s)
6	IMON_INJ	Control the IMON injection in the compensation loop. 0: Positive 1: Negative
5:3	LPF_GAIN_SET	Set the DC gain of the LPF in the offset cancellation loop. DC gain = 1.5 + [5:3] x 0.5 000: 1.5 001: 2.0 010: 2.5 011: 3.0 100: 3.5 101: 4.0 110: 4.5 111: 5.0
2:0	AI_GAIN	Set the current gain for the IMON injection. Current gain = [2:0] x 0.25 000: 0.00 001: 0.25 010: 0.50 011: 0.75 100: 1.00 101: 1.25 110: 1.50 111: 1.75

Table 52. VID_STEP_HPF_RC_SET

Page: 0x09 Address: 0x09								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	VID_STEP	HPF_C_SET		HPF_R_SET			
Default	0	0	1	1	1	0	1	0
Type	R	RW	RW		RW			

Bit	Name	Description
7	Reserved	Reserved bit(s)
6	VID_STEP	Select the VID step of the rail. 0: 5mV VID step 1: 10mV VID step
5:4	HPF_C_SET	Set the capacitance of the HPF in the compensation loop. CHPF = ([5:4] + 1)pF 00: 1pF 01: 2pF 10: 3pF 11: 4pF
3:0	HPF_R_SET	Set the resistance of the HPF in the compensation loop. RHPF = [3:0] x 100kΩ 0000: Disable HPF 0001: 100kΩ 0010: 200kΩ 0011: 300kΩ 1101: 1300kΩ 1110: 1400kΩ 1111: 1500kΩ

Table 53. LPF_RC_EXT_RC_SET

Page: 0x09 **Address: 0x0A**								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	LPF_TAU_SET			EXT_C_SET		EXT_R_SET	
Default	0	1	0	0	0	0	0	0
Type	R	RW			RW		RW	

Bit	Name	Description
7	Reserved	Reserved bit(s)
6:4	LPF_TAU_SET	Set the resistance of the LPF in the offset cancellation loop. RLPF = (8 – [6:4]) x 8us 000: Tau = 64us 001: Tau = 56us ..... 110: Tau = 16us 111: Tau = 8us
3:2	EXT_C_SET	Set the capacitance for the Mode 2 pole-zero extension. CEXT = [3:2] x 2pF 00: Mode 2 disabled (Mode 1 control) 01: 2pF 10: 4pF 11: 6pF
1:0	EXT_R_SET	Set the resistance for the Mode 2 pole-zero extension. REXT = 40kΩ + [1:2] x 40kΩ 00: 40kΩ 01: 80kΩ 10: 120kΩ 11: 160kΩ

Table 54. IMON_LPF_DEM_TON_TSEN_SOC_SEL

Page: 0x09 Address: 0x0B								
Bit	7	6	5	4	3	2	1	0
Field	IMON_LPF		DEM_SHRINK_TON			TSEN_SEL	SOC_TH_SEL	
Default	0	1	1	0	1	1	0	1
Type	RW		RW			RW	RW	

Bit	Name	Description
7:6	IMON_LPF	Set the low-pass filter time constant for the VIMON signal. 00: Disable 01: 320ns 10: 1.6μs 11: 3.2μs
5:3	DEM_SHRINK_TON	Control the PWM on-time during DEM ultra-low load operation (< 1A). 000: Disable t_{ON} shrink function 001: TON x 0.91 010: TON x 0.83 011: TON x 0.75 100: TON x 0.66 101: TON x 0.58 110: TON x 0.50 111: TON x 0.42
2	TSEN_SEL	Select the temperature sense input of the rail. 0: NTC thermistor 1: SPS TMON
1:0	SOC_TH_SEL	Select the sum overcurrent protection threshold for the rail. 00: SOC_TH = ICCMAX 01: SOC_TH = 1.3 x ICCMAX 10: SOC_TH = 1.6 x ICCMAX 11: SOC_TH = 2.0 x ICCMAX

Table 55. AR_AQR_TH

Page: 0x09 Address: 0x0C								
Bit	7	6	5	4	3	2	1	0
Field	Reserved			AR_TH		AQR_TH		
Default	0	0	1	0	0	1	1	1
Type	R			RW		RW		

Bit	Name	Description
7:5	Reserved	Reserved bit(s)
4:3	AR_TH	Set the trigger level of the adaptive ramp. 00: Disable 01: 20mV 10: 40mV 11: 80mV
2:0	AQR_TH	Set the trigger level of AQR for the rail. AQR_TH = ([2:0] + 1) * 40mV 000: 40mV 001: 80mV 010: 120mV 011: 160mV 100: 200mV 101: 240mV 110: 280mV 111: 320mV

Table 56. ANTIOVS_TH_DEM_RAMP_CLAMP

Page: 0x09 Address: 0x0D								
Bit	7	6	5	4	3	2	1	0
Field	ANTIOVS_TH			Reserved	DEM_RAMP_CLAMP			
Default	1	1	1	1	0	1	0	1
Type	RW			R	RW			

Bit	Name	Description
7:5	ANTIOVS_TH	Set the trigger level of ANTIOVS. ANTIOVS_TH = [7:5] x 20mV 000: Disable
4	Reserved	Reserved bit(s)
3:0	DEM_RAMP_CLAMP	Select the ramp clamping level during DEM operation. Ramp clamping level = 2.4V – [3:0] x 40mV 0000: 2400mV 0001: 2360mV 0010: 2320mV 1101: 1880mV 1110: 1840mV 1111: 1800mV

Table 57. EN_SPM_DVID_ENHANCE

Page: 0x09 Address: 0x0E								
Bit	7	6	5	4	3	2	1	0
Field	EN_SPM	DVID_UP_LIFT				DVID_DN_PULL		
Default	1	1	1	0	1	1	1	0
Type	RW	RW				RW		

Bit	Name	Description
7	EN_SPM	Enable/disable SPM of the rail. 0: Disable SPM 1: Enable SPM
6:3	DVID_UP_LIFT	Lift VSEN with a positive voltage offset during DVID up to compensate for the droop effect of the load-line. 0000: Disable 0001: 10mV 0010: 20mV 0011: 30mV 0100: 40mV 0101: 50mV 0110: 60mV 0111: 70mV 1000: 80mV 1001: 90mV 1010: 100mV 1011: 120mV 1100: 140mV 1101: 160mV 1110: 180mV 1111: 200mV
2:0	DVID_DN_PULL	Pull VSEN with a negative voltage offset during DVID down to compensate for the droop effect of the load-line. 000: Disable 001: DVID_DN_PULL = DVID_UP_LIFT x 0.25 010: DVID_DN_PULL = DVID_UP_LIFT x 0.50 011: DVID_DN_PULL = DVID_UP_LIFT x 0.75 100: DVID_DN_PULL = DVID_UP_LIFT x 1.00 101: DVID_DN_PULL = DVID_UP_LIFT x 1.25 110: DVID_DN_PULL = DVID_UP_LIFT x 1.50 111: DVID_DN_PULL = DVID_UP_LIFT x 1.75

Table 58. ZCD_SET_EN_VBOOT

Page: 0x09 Address: 0x0F								
Bit	7	6	5	4	3	2	1	0
Field	ZCD_TH_R_SET				ZCD_TH_I_SET			EN_VBOOT
Default	0	1	1	1	0	1	1	0
Type	RW				RW			RW

Bit	Name	Description
7:4	ZCD_TH_R_SET	Set the resistance for ZCD_TH. ZCD_TH = ZCD_TH_I_SET x ZCD_TH_R_SET / 36 ZCD_TH_R = [3:0] x 6kΩ 0000: Disable 0001: 6kΩ 0010: 12kΩ 0011: 18kΩ 1101: 78kΩ 1110: 84kΩ 1111: 90kΩ
3:1	ZCD_TH_I_SET	Set the current for ZCD_TH. ZCD_TH = ZCD_TH_I_SET x ZCD_TH_R_SET / 36 ZCD_TH_I = $(-1)^{[3]}$ x ([2:1] + 1) x 0.5μA 000: 0.5μA 001: 1.0μA 010: 1.5μA 011: 2.0μA 100: -0.5μA 101: -1.0μA 110: -1.5μA 111: -2.0μA
0	EN_VBOOT	0: Disable VBOOT 1: Enable VBOOT

Table 59. SVID_VBOOT

Page: 0x09 Address: 0x10								
Bit	7	6	5	4	3	2	1	0
Field	SVID_VBOOT							
Default	1	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	SVID_VBOOT	Set the VBOOT voltage of the rail.

Table 60. EN_SPS_OFS_LPF_INI_SET

Page: 0x09 Address: 0x11								
Bit	7	6	5	4	3	2	1	0
Field	EN_SPS	SPS_OFS			LPF_INI_SET			
Default	1	1	0	1	1	0	1	1
Type	RW	RW			RW			

Bit	Name	Description
7	EN_SPS	0: Disable SPS IMON current sensing (DCR current sensing). 1: Enable SPS IMON current sensing.
6:4	SPS_OFS	Set the per-phase current offset for SPS IMON. SPS_OFS = $(-1)^{[7]}$ x [6:5] x 0.0625mV 000: 0.0000mV 001: 0.0625mV 010: 0.1250mV 011: 0.1875mV 101: -0.0625mV 110: -0.1250mV 111: -0.1875mV
3:0	LPF_INI_SET	Set the initial value of the LPF in the offset cancellation loop. 0000: LPF_INI = 0mV 0001: LPF_INI = -5mV 0010: LPF_INI = -10mV 0011: LPF_INI = -20mV 0101: LPF_INI = 5mV 0110: LPF_INI = 10mV 0111: LPF_INI = 20mV 1001: LPF_INI = -35mV 1010: LPF_INI = -40mV 1011: LPF_INI = -50mV 1101: LPF_INI = 35mV 1110: LPF_INI = 40mV 1111: LPF_INI = 50mV All the other combinations are not defined.

Table 61. ZCD_HYS_ASYM_VID_HPF_GAIN_SET

Page: 0x09 Address: 0x12								
Bit	7	6	5	4	3	2	1	0
Field	ZCD_HYS		DVID_COMP_TAU	Reserved		HPF_GAIN_SET		
Default	1	1	0	0	0	0	0	1
Type	RW		RW	R		RW		

Bit	Name	Description
7:6	ZCD_HYS	Set the hysteresis for ZCD. 00: 0.278 mV 01: 0.556 mV 10: 1.111 mV 11: 2.222mV
5	DVID_COMP_TAU	Set the time constant for DVID enhancement. 0: 2μs 1: 4μs
4:3	Reserved	Reserved bit(s)
2:0	HPF_GAIN_SET	Set the DC gain for the HPF in the compensation loop. DC gain = 1.5 + [5:3] x 0.5 000: 1.5 001: 2.0 010: 2.5 011: 3.0 100: 3.5 101: 4.0 110: 4.5 111: 5.0

Table 62 to Table 82 provide bit field description of NVM registers for I²C settings. No specific key is required to access I²C settings. Make sure the PAGE register is properly set before changing the content of functional registers.

Table 62. NVM Table Summary for I²C Settings

Page	Address	Register Name	Default	Type	NVM
0x0D	0x00	SPM_TH5_TH4_A	0x69	RW	Y
0x0D	0x01	SPM_TH3_TH2_A	0xBD	RW	Y
0x0D	0x02	SPM_HYS_A	0xF8	RW	Y
0x0D	0x03	SPM_TH2_HYS_B	0x4D	RW	Y
0x0D	0x04	TSEN_VRHOT_ALERT_HYS	0x11	RW	Y
0x0D	0x05	TSEN_VRHOT_ALERT_TH	0xA9	RW	Y
0x0D	0x06	IBAL_GAIN_PH1_PH2_A	0x44	RW	Y
0x0D	0x07	IBAL_GAIN_PH3_PH4_A	0x44	RW	Y
0x0D	0x08	IBAL_GAIN_PH5_A_DISA_FVM	0x40	RW	Y
0x0D	0xA1	IOUT_RPT_A	0x00	R	N
0x0D	0xA2	IOUT_RPT_B	0x00	R	N
0x0D	0xA3	IOUT_RPT_C	0x00	R	N
0x0D	0xA4	IOUT_RPT_D	0x00	R	N
0x0D	0xA5	TEMPERATURE_RPT_A	0x00	R	N
0x0D	0xA6	TEMPERATURE_RPT_B	0x00	R	N
0x0D	0xA7	TEMPERATURE_RPT_C	0x00	R	N
0x0D	0xA8	TEMPERATURE_RPT_D	0x00	R	N
0x0D	0xA9	PSYS_RPT	0x00	R	N
0x0D	0xAA	VSYS_RPT	0x00	R	N
0x0D	0xAB	AUX_IMON_RPT	0x00	R	N

Table 63. SPM_TH5_TH4_A

Page: 0x0D Address: 0x00								
Bit	7	6	5	4	3	2	1	0
Field	SPM_TH5_A				SPM_TH4_A			
Default	0	1	1	0	1	0	0	1
Type	RW				RW			

Bit	Name	Description
7:4	SPM_TH5_A	Set the SPM 4-phase to 5-phase current threshold of rail A as a percentage of ICCMAX_A. 0000: 100% of ICCMAX_A 0001: 90% 0010: 80% 0011: 70% 0100: 60% 0101: 50% 0110: 45% 0111: 40% 1000: 35% 1001: 30% 1010: 25% 1011: 20% 1100: 15% 1101: 10% 1110: 5% 1111: 2.5%
3:0	SPM_TH4_A	Set the SPM 3-phase to 4-phase current threshold of rail A as a percentage of ICCMAX_A. 0000: 100% of ICCMAX_A 0001: 90% 0010: 80% 0011: 70% 0100: 60% 0101: 50% 0110: 45% 0111: 40% 1000: 35% 1001: 30% 1010: 25% 1011: 20% 1100: 15% 1101: 10% 1110: 5% 1111: 2.5%

Table 64. SPM_TH3_TH2_A

Page: 0x0D Address: 0x01								
Bit	7	6	5	4	3	2	1	0
Field	SPM_TH3_A				SPM_TH2_A			
Default	1	0	1	1	1	1	0	1
Type	RW				RW			

Bit	Name	Description
7:4	SPM_TH3_A	Set the SPM 2-phase to 3-phase current threshold of rail A as a percentage of ICCMAX_A. 0000: 100% of ICCMAX_A 0001: 90% 0010: 80% 0011: 70% 0100: 60% 0101: 50% 0110: 45% 0111: 40% 1000: 35% 1001: 30% 1010: 25% 1011: 20% 1100: 15% 1101: 10% 1110: 5% 1111: 2.5%
3:0	SPM_TH2_A	Set the SPM 1-phase to 2-phase current threshold of rail A as a percentage of ICCMAX_A. 0000: 100% of ICCMAX_A 0001: 90% 0010: 80% 0011: 70% 0100: 60% 0101: 50% 0110: 45% 0111: 40% 1000: 35% 1001: 30% 1010: 25% 1011: 20% 1100: 15% 1101: 10% 1110: 5% 1111: 2.5%

Table 65. SPM_HYS_A

Page: 0x0D Address: 0x02								
Bit	7	6	5	4	3	2	1	0
Field	RESERVED				SPM_HYS_A			
Default	1	1	1	1	1	0	0	0
Type	RW				RW			

Bit	Name	Description
7:4	RESERVED	Reserved bit(s)
3:0	SPM_HYS_A	Set the SPM hysteresis for rail A during SPM operation. SPM_HYS = 3mV x [3:0] / VICCMAX 0000: Disable 0001: 3mV/VICCMAX 0010: 6mV/VICCMAX 0011: 9mV/VICCMAX 0100: 12mV/VICCMAX 0101: 15mV/VICCMAX 0110: 18mV/VICCMAX 0111: 21mV/VICCMAX 1000: 24mV/VICCMAX 1001: 27mV/VICCMAX 1010: 30mV/VICCMAX 1011: 33mV/VICCMAX 1100: 36mV/VICCMAX 1101: 39mV/VICCMAX 1110: 42mV/VICCMAX 1111: 45mV/VICCMAX

Table 66. SPM_TH2_HYS_B

Page: 0x0D Address: 0x03								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	SPM_TH2_B			SPM_HYS_B			
Default	0	1	0	0	1	1	0	1
Type	R	RW			RW			

Bit	Name	Description
7	Reserved	Reserved bit(s)
6:4	SPM_TH2_B	Set the SPM 1-phase to 2-phase current threshold of rail B as a percentage of ICCMAX_B. 000: 35% 001: 30% 010: 25% 011: 20% 100: 15% 101: 10% 110: 5% 111: 2.5%
3:0	SPM_HYS_B	Set the SPM hysteresis for rail B. SPM_HYS = 3mV x [7:4] / VICCMAX 0000: Disable 0001: 3mV/VICCMAX 0010: 6mV/VICCMAX 0011: 9mV/VICCMAX 0100: 12mV/VICCMAX 0101: 15mV/VICCMAX 0110: 18mV/VICCMAX 0111: 21mV/VICCMAX 1000: 24mV/VICCMAX 1001: 27mV/VICCMAX 1010: 30mV/VICCMAX 1011: 33mV/VICCMAX 1100: 36mV/VICCMAX 1101: 39mV/VICCMAX 1110: 42mV/VICCMAX 1111: 45mV/VICCMAX

Table 67. TSEN_VRHOT_ALERT_HYS

Page: 0x0D Address: 0x04								
Bit	7	6	5	4	3	2	1	0
Field	TSEN_VRHOT_HYS				TSEN_ALERT_HYS			
Default	0	0	0	1	0	0	0	1
Type	RW				RW			

Bit	Name	Description
7:4	TSEN_VRHOT_HYS	Set the temperature hysteresis for VR_HOT# de-assertion. TSEN_HYS = [7:4] x 3°C 0000: Disable 0001: 3°C 0010: 6°C 0011: 9°C 0100: 12°C 0101: 15°C 0110: 18°C 0111: 21°C 1000: 24°C 1001: 27°C 1010: 30°C 1011: 33°C 1100: 36°C 1101: 39°C 1110: 42°C 1111: 45°C
3:0	TSEN_ALERT_HYS	Set the temperature hysteresis for SVID ThermAlert bit de-assertion. TSEN_HYS = [3:0] x 3°C 0000: Disable 0001: 3°C 0010: 6°C 0011: 9°C 0100: 12°C 0101: 15°C 0110: 18°C 0111: 21°C 1000: 24°C 1001: 27°C 1010: 30°C 1011: 33°C 1100: 36°C 1101: 39°C 1110: 42°C 1111: 45°C

Table 68. TSEN_VRHOT_ALERT_TH

Page: 0x0D Address: 0x05								
Bit	7	6	5	4	3	2	1	0
Field	TSEN_VRHOT_TH				TSEN_ALERT_TH			
Default	1	0	1	0	1	0	0	1
Type	RW				RW			

Bit	Name	Description
7:4	TSEN_VRHOT_TH	Set the temperature threshold for VR_HOT# assertion. 0000: 70°C 0001: 73°C 0010: 76°C 0011: 79°C 0100: 82°C 0101: 85°C 0110: 88°C 0111: 91°C 1000: 94°C 1001: 97°C 1010: 100°C 1011: 105°C 1100: 110°C 1101: 115°C 1110: 120°C 1111: 125°C
3:0	TSEN_ALERT_TH	Set the temperature threshold for SVID ThermAlert bit assertion. 0000: 70°C 0001: 73°C 0010: 76°C 0011: 79°C 0100: 82°C 0101: 85°C 0110: 88°C 0111: 91°C 1000: 94°C 1001: 97°C 1010: 100°C 1011: 105°C 1100: 110°C 1101: 115°C 1110: 120°C 1111: 125°C

Table 69. IBAL_GAIN_PH1_PH2_A

Page: 0x0D Address: 0x06								
Bit	7	6	5	4	3	2	1	0
Field	IBAL_GAIN_PH1_A				IBAL_GAIN_PH2_A			
Default	0	1	0	0	0	1	0	0
Type	RW				RW			

Bit	Name	Description
7:4	IBAL_GAIN_PH1_A	Set the current balance gain for phase 1 of rail A. IBAL_GAIN = $2^{[7]}$ x (60% + [6:4] x 10%) 0000: 60% 0001: 70% 0010: 80% 0011: 90% 0100: 100% 0101: 110% 0110: 120% 0111: 130% 1001: 140% 1010: 160% 1011: 180% 1100: 200% 1101: 220% 1110: 240% 1111: 260%
3:0	IBAL_GAIN_PH2_A	Set the current balance gain for phase 2 of rail A. IBAL_GAIN = $2^{[3]}$ x (60% + [2:0] x 10%) 0000: 60% 0001: 70% 0010: 80% 0011: 90% 0100: 100% 0101: 110% 0110: 120% 0111: 130% 1001: 140% 1010: 160% 1011: 180% 1100: 200% 1101: 220% 1110: 240% 1111: 260%

Table 70. IBAL_GAIN_PH3_PH4_A

Page: 0x0D Address: 0x07								
Bit	7	6	5	4	3	2	1	0
Field	IBAL_GAIN_PH3_A				IBAL_GAIN_PH4_A			
Default	0	1	0	0	0	1	0	0
Type	RW				RW			

Bit	Name	Description
7:4	IBAL_GAIN_PH3_A	Set the current balance gain for phase 3 of rail A. IBAL_GAIN = $2^{[7]}$ x (60% + [6:4] x 10%) 0000: 60% 0001: 70% 0010: 80% 0011: 90% 0100: 100% 0101: 110% 0110: 120% 0111: 130% 1001: 140% 1010: 160% 1011: 180% 1100: 200% 1101: 220% 1110: 240% 1111: 260%
3:0	IBAL_GAIN_PH4_A	Set the current balance gain for phase 4 of rail A. IBAL_GAIN = $2^{[3]}$ x (60% + [2:0] x 10%) 0000: 60% 0001: 70% 0010: 80% 0011: 90% 0100: 100% 0101: 110% 0110: 120% 0111: 130% 1001: 140% 1010: 160% 1011: 180% 1100: 200% 1101: 220% 1110: 240% 1111: 260%

Table 71. IBAL_GAIN_PH5_A_DISA_FVM

Page: 0x0D Address: 0x08								
Bit	7	6	5	4	3	2	1	0
Field	IBAL_GAIN_PH5_A				DISA_FVM_A	DISA_FVM_B	DISA_FVM_C	DISA_FVM_D
Default	0	1	0	0	0	0	0	0
Type	RW				RW	RW	RW	RW

Bit	Name	Description
7:4	IBAL_GAIN_PH5_A	Set the current balance gain for phase 5 of rail A. IBAL_GAIN = $2^{[7]}$ x (60% + [6:4] x 10%) 0000: 60% 0001: 70% 0010: 80% 0011: 90% 0100: 100% 0101: 110% 0110: 120% 0111: 130% 1001: 140% 1010: 160% 1011: 180% 1100: 200% 1101: 220% 1110: 240% 1111: 260%
3	DISA_FVM_A	Control the FVM behavior of rail A. 0: FVM follow SVID specification 1: Force disable FVM
2	DISA_FVM_B	Control the FVM behavior of rail B. 0: FVM follow SVID specification 1: Force disable FVM
1	DISA_FVM_C	Control the FVM behavior of rail C. 0: FVM follow SVID specification 1: Force disable FVM
0	DISA_FVM_D	Control the FVM behavior of rail D. 0: FVM follow SVID specification 1: Force disable FVM

Table 72. IOUT_RPT_A

Page: 0x0D Address: 0xA1								
Bit	7	6	5	4	3	2	1	0
Field	IOUT_RPT_A							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	IOUT_RPT_A	Rail A IOUT telemetry via the I^2C interface. The data format follows the SVID specification.

Table 73. IOUT_RPT_B

Page: 0x0D Address: 0xA2								
Bit	7	6	5	4	3	2	1	0
Field	IOUT_RPT_B							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	IOUT_RPT_B	Rail B IOUT telemetry via the I^2C interface. The data format follows the SVID specification.

Table 74. IOUT_RPT_C

Page: 0x0D Address: 0xA3								
Bit	7	6	5	4	3	2	1	0
Field	IOUT_RPT_C							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	IOUT_RPT_C	Rail C IOUT telemetry via the I^2C interface. The data format follows the SVID specification.

Table 75. IOUT_RPT_D

Page: 0x0D Address: 0xA4								
Bit	7	6	5	4	3	2	1	0
Field	IOUT_RPT_D							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	IOUT_RPT_D	Rail D IOUT telemetry via the I^2C interface. The data format follows the SVID specification.

Table 76. TEMPERATURE_RPT_A

Page: 0x0D Address: 0xA5								
Bit	7	6	5	4	3	2	1	0
Field	TEMPERATURE_RPT_A							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	TEMPERATURE_RPT_A	Rail A temperature reporting via the I^2C interface. The data format follows the SVID specification.

Table 77. TEMPERATURE_RPT_B

Page: 0x0D Address: 0xA6								
Bit	7	6	5	4	3	2	1	0
Field	TEMPERATURE_RPT_B							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	TEMPERATURE_RPT_B	Rail B temperature reporting via the I^2C interface. The data format follows the SVID specification.

Table 78. TEMPERATURE_RPT_C

Page: 0x0D Address: 0xA7								
Bit	7	6	5	4	3	2	1	0
Field	TEMPERATURE_RPT_C							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	TEMPERATURE_RPT_C	Rail C temperature reporting via the I^2C interface. The data format follows the SVID specification.

Table 79. TEMPERATURE_RPT_D

Page: 0x0D Address: 0xA8								
Bit	7	6	5	4	3	2	1	0
Field	TEMPERATURE_RPT_D							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	TEMPERATURE_RPT_D	Rail D temperature reporting via the I^2C interface. The data format follows the SVID specification.

Table 80. PSYS_RPT

Page: 0x0D Address: 0xA9								
Bit	7	6	5	4	3	2	1	0
Field	PSYS_RPT							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	PSYS_RPT	Input power monitoring via the I^2C interface. The data format follows the SVID specification.

Table 81. VSYS_RPT

Page: 0x0D Address: 0xAA								
Bit	7	6	5	4	3	2	1	0
Field	VSYS_RPT							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	VSYS_RPT	Input voltage monitoring via the I^2C interface. The data format follows the SVID specification.

Table 82. AUX_IMON_RPT

Page: 0x0D Address: 0xAB								
Bit	7	6	5	4	3	2	1	0
Field	AUX_IMON_RPT							
Default	0	0	0	0	0	0	0	0
Type	R							

Bit	Name	Description
7:0	AUX_IMON_RPT	IOUT telemetry for auxiliary VR via the I^2C interface. The data format follows the SVID specification.

Table 83 to Table 98 provide bit field description of NVM registers for extend function settings. A specific key is required to access extend function settings. Make sure the PAGE register is properly set before changing the content of functional registers.

Table 83. NVM Table Summary of Extend Function Settings

Page	Address	Register Name	Default	Type	NVM
0x0E	0x00	EN_ASYM_TON_PS1_PS2_SPM_A	0x00	RW	Y
0x0E	0x01	EN_PS1_SLOW_CCM_ASYM_TON_PS3_SPM_A	0x00	RW	Y
0x0E	0x02	FVM_CLAMP_TH_A	0x0C	RW	Y
0x0E	0x03	EN_ASYM_TON_PS1_PS2_SPM_B	0x00	RW	Y
0x0E	0x04	EN_PS1_SLOW_CCM_ASYM_TON_PS3_SPM_B	0x00	RW	Y
0x0E	0x05	FVM_CLAMP_TH_B	0x02	RW	Y
0x0E	0x06	EN_ASYM_TON_PS1_PS2_SPM_C	0x00	RW	Y
0x0E	0x07	EN_PS1_SLOW_CCM_ASYM_TON_PS3_SPM_C	0x00	RW	Y
0x0E	0x08	FVM_CLAMP_TH_C	0x04	RW	Y
0x0E	0x09	EN_ASYM_TON_PS1_PS2_SPM_D	0x00	RW	Y
0x0E	0x0A	EN_PS1_SLOW_DCM_ASYM_TON_PS3_SPM_D	0x00	RW	Y
0x0E	0x0B	FVM_CLAMP_TH_D	0x02	RW	Y
0x0E	0x0D	SSOC_TH_FVM_HYS_A_B	0xCC	RW	Y
0x0E	0x0E	SSOC_TH_FVM_HYS_C_D	0xCC	RW	Y
0x0E	0x0F	CRC2_CHECK	--	R	N

Table 84. EN_ASYM_TON_PS1_PS2_SPM_A

Page: 0x0E Address: 0x00								
Bit	7	6	5	4	3	2	1	0
Field	EN_ASYM_TON_A	EN_ASYM_TON_SPM_DEM_A	ASYM_TON_PS1_A			ASYM_TON_PS2_A		
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW			RW		

Bit	Name	Description
7	EN_ASYM_TON_A	0: Disable 1: Enable
6	EN_ASYM_TON_SPM_DEM_A	0: Disable the asymmetric t_{ON} mode in SPM DEM. 1: Enable the asymmetric t_{ON} mode in SPM DEM.
5:3	ASYM_TON_PS1_A	Set the PWM t_{ON} gain in PS1 when EN_ASYM_TON = 1 and EN_ASYM_TON_SPM_DEM = 0. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4
2:0	ASYM_TON_PS2_A	Set PWM t_{ON} gain in PS2 when EN_ASYM_TON = 1. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4

Table 85. EN_PS1_SLOW_CCM_ASYM_TON_PS3_SPM_A

Page: 0x0E Address: 0x01								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	EN_PS1_SLOW_CCM_A	ASYM_TON_PS3_A			ASYM_TON_SPM_DEM_A		
Default	0	0	0	0	0	0	0	0
Type	R	RW	RW			RW		

Bit	Name	Description
7	Reserved	Reserved bit(s)
6	EN_PS1_SLOW_CCM_A	0: PS1 PWM follows ASYM_TON_PS1. 1: PS1 PWM follows nominal tON.
5:3	ASYM_TON_PS3_A	Set the PWM tON gain in PS3 when EN_ASYM_TON = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4
2:0	ASYM_TON_SPM_DEM_A	Set the PWM tON gain in SPM DEM when EN_ASYM_TON = 1 and EN_ASYM_TON_SPM_DEM = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4

Table 86. FVM_CLAMP_TH_A

Page: 0x0E Address: 0x02								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FVM_CLAMP_TH_A			
Default	0	0	0	0	1	1	0	0
Type	R				RW			

Bit	Name	Description
7:4	Reserved	Reserved bit(s)
3:0	FVM_CLAMP_TH_A	Set the error amplifier clamping threshold in FVM for rail A. FVM_CLAMP_TH = (2.4 + RAMP_CTRL) – (RAMP_CTRL + 100mV) x (1 + [3:0]) / 16

Table 87. EN_ASYM_TON_PS1_PS2_SPM_B

Page: 0x0E Address: 0x03								
Bit	7	6	5	4	3	2	1	0
Field	EN_ASYM_TON_B	EN_ASYM_TON_SPM_DEM_B	ASYM_TON_PS1_B			ASYM_TON_PS2_B		
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW			RW		

Bit	Name	Description
7	EN_ASYM_TON_B	0: Disable 1: Enable
6	EN_ASYM_TON_SPM_DEM_B	0: Disable the asymmetric t_{ON} mode in SPM DEM. 1: Enable the asymmetric t_{ON} mode in SPM DEM.
5:3	ASYM_TON_PS1_B	Set the PWM t_{ON} gain in PS1 when EN_ASYM_TON = 1 and EN_BSYM_TON_SPM_DEM = 0. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4
2:0	ASYM_TON_PS2_B	Set PWM t_{ON} gain in PS2 when EN_ASYM_TON = 1. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4

Table 88. EN_PS1_SLOW_CCM_ASYM_TON_PS3_SPM_B

Page: 0x0E Address: 0x04								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	EN_PS1_SLOW_CCM_B	ASYM_TON_PS3_B			ASYM_TON_SPM_DEM_B		
Default	0	0	0	0	0	0	0	0
Type	R	RW	RW			RW		

Bit	Name	Description
7	Reserved	Reserved bit(s)
6	EN_PS1_SLOW_CCM_B	0: PS1 PWM follows ASYM_TON_PS1. 1: PS1 PWM follows nominal tON.
5:3	ASYM_TON_PS3_B	Set the PWM tON gain in PS3 when EN_ASYM_TON = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4
2:0	ASYM_TON_SPM_DEM_B	Set the PWM tON gain in SPM DEM when EN_ASYM_TON = 1 and EN_BSYM_TON_SPM_DEM = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4

Table 89. FVM_CLAMP_TH_B

Page: 0x0E Address: 0x05								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FVM_CLAMP_TH_B			
Default	0	0	0	0	0	0	1	0
Type	R				RW			

Bit	Name	Description
7:4	Reserved	Reserved bit(s)
3:0	FVM_CLAMP_TH_B	Set the error amplifier clamping threshold in FVM for rail B. FVM_CLAMP_TH = (2.4 + RAMP_CTRL) – (RAMP_CTRL + 100mV) x (1 + [3:0]) / 16

Table 90. EN_ASYM_TON_PS1_PS2_SPM_C

Page: 0x0E Address: 0x06								
Bit	7	6	5	4	3	2	1	0
Field	EN_ASYM_TON_C	EN_ASYM_TON_SPM_DEM_C	ASYM_TON_PS1_C			ASYM_TON_PS2_C		
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW			RW		

Bit	Name	Description
7	EN_ASYM_TON_C	0: Disable 1: Enable
6	EN_ASYM_TON_SPM_DEM_C	0: Disable the asymmetric t_{ON} mode in SPM DEM. 1: Enable the asymmetric t_{ON} mode in SPM DEM.
5:3	ASYM_TON_PS1_C	Set the PWM t_{ON} gain in PS1 when EN_ASYM_TON = 1 and EN_CSYM_TON_SPM_DEM = 0. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4
2:0	ASYM_TON_PS2_C	Set the PWM t_{ON} gain in PS2 when EN_ASYM_TON = 1. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4

Table 91. EN_PS1_SLOW_CCM_ASYM_TON_PS3_SPM_C

Page: 0x0E Address: 0x07								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	EN_PS1_SLOW_CCM_C	ASYM_TON_PS3_C			ASYM_TON_SPM_DEM_C		
Default	0	0	0	0	0	0	0	0
Type	R	RW	RW			RW		

Bit	Name	Description
7	Reserved	Reserved bit(s)
6	EN_PS1_SLOW_CCM_C	0: PS1 PWM follows ASYM_TON_PS1. 1: PS1 PWM follows nominal tON.
5:3	ASYM_TON_PS3_C	Set the PWM tON gain in PS3 when EN_ASYM_TON = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4
2:0	ASYM_TON_SPM_DEM_C	Set the PWM tON gain in SPM DEM when EN_ASYM_TON = 1 and EN_CSYM_TON_SPM_DEM = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4

Table 92. FVM_CLAMP_TH_C

Page: 0x0E Address: 0x08								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FVM_CLAMP_TH_C			
Default	0	0	0	0	0	1	0	0
Type	R				RW			

Bit	Name	Description
7:4	Reserved	Reserved bit(s)
3:0	FVM_CLAMP_TH_C	Set the error amplifier clamping threshold in FVM for rail C. FVM_CLAMP_TH = (2.4 + RAMP_CTRL) – (RAMP_CTRL + 100mV) x (1 + [3:0]) / 16

Table 93. EN_ASYM_TON_PS1_PS2_SPM_D

Page: 0x0E Address: 0x09								
Bit	7	6	5	4	3	2	1	0
Field	EN_ASYM_TON_D	EN_ASYM_TON_SPM_DEM_D	ASYM_TON_PS1_D			ASYM_TON_PS2_D		
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW			RW		

Bit	Name	Description
7	EN_ASYM_TON_D	0: Disable 1: Enable
6	EN_ASYM_TON_SPM_DEM_D	0: Disable the asymmetric t_{ON} mode in SPM DEM. 1: Enable the asymmetric t_{ON} mode in SPM DEM.
5:3	ASYM_TON_PS1_D	Set the PWM t_{ON} gain in PS1 when EN_ASYM_TON = 1 and EN_DSYM_TON_SPM_DEM = 0. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4
2:0	ASYM_TON_PS2_D	Set the PWM t_{ON} gain in PS2 when EN_ASYM_TON = 1. 000: Nominal t_{ON} x1 001: Nominal t_{ON} x1.2 010: Nominal t_{ON} x1.4 011: Nominal t_{ON} x1.6 100: Nominal t_{ON} x1.8 101: Nominal t_{ON} x2.0 110: Nominal t_{ON} x2.2 111: Nominal t_{ON} x2.4

Table 94. EN_PS1_SLOW_DCM_ASYM_TON_PS3_SPM_D

Page: 0x0E Address: 0x0A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	EN_PS1_SLOW_CCM_D	ASYM_TON_PS3_D			ASYM_TON_SPM_DEM_D		
Default	0	0	0	0	0	0	0	0
Type	R	RW	RW			RW		

Bit	Name	Description
7	Reserved	Reserved bit(s)
6	EN_PS1_SLOW_CCM_D	0: PS1 PWM follows ASYM_TON_PS1. 1: PS1 PWM follows nominal tON,
5:3	ASYM_TON_PS3_D	Set the PWM tON gain in PS3 when EN_ASYM_TON = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4
2:0	ASYM_TON_SPM_DEM_D	Set the PWM tON gain in SPM DEM when EN_ASYM_TON = 1 and EN_DSYM_TON_SPM_DEM = 1. 000: Nominal tON x1 001: Nominal tON x1.2 010: Nominal tON x1.4 011: Nominal tON x1.6 100: Nominal tON x1.8 101: Nominal tON x2.0 110: Nominal tON x2.2 111: Nominal tON x2.4

Table 95. FVM_CLAMP_TH_D

Page: 0x0E Address: 0x0B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FVM_CLAMP_TH_D			
Default	0	0	0	0	0	0	1	0
Type	R				RW			

Bit	Name	Description
7:4	Reserved	Reserved bit(s)
3:0	FVM_CLAMP_TH_D	Set the error amplifier clamping threshold in FVM for rail D. FVM_CLAMP_TH = (2.4 + RAMP_CTRL) – (RAMP_CTRL + 100mV) x (1 + [3:0]) / 16

Table 96. SSOC_TH_FVM_HYS_A_B

Page: 0x0E Address: 0x0D								
Bit	7	6	5	4	3	2	1	0
Field	SSOC_TH_SEL_A		FVM_HYS_A		SSOC_TH_SEL_B		FVM_HYS_B	
Default	1	1	0	0	1	1	0	0
Type	RW		RW		RW		RW	

Bit	Name	Description
7:6	SSOC_TH_SEL_A	Select the soft-startup OCP threshold for rail A. 00: 1.4 x ICCMAX 01: 1.6 x ICCMAX 10: 1.8 x ICCMAX 11: 2.0 x ICCMAX
5:4	FVM_HYS_A	Set the current hysteresis for the FVM of rail A. 00: FVM_HYS = 10% x ICCMAX 01: FVM_HYS = 15% x ICCMAX 10: FVM_HYS = 20% x ICCMAX 11: FVM_HYS = 25% x ICCMAX
3:2	SSOC_TH_SEL_B	Select the soft-startup OCP threshold for rail B. 00: 1.4 x ICCMAX 01: 1.6 x ICCMAX 10: 1.8 x ICCMAX 11: 2.0 x ICCMAX
1:0	FVM_HYS_B	Set the current hysteresis for the FVM of rail B. 00: FVM_HYS = 10% x ICCMAX 01: FVM_HYS = 15% x ICCMAX 10: FVM_HYS = 20% x ICCMAX 11: FVM_HYS = 25% x ICCMAX

Table 97. SSOC_TH_FVM_HYS_C_D

Page: 0x0E Address: 0x0E								
Bit	7	6	5	4	3	2	1	0
Field	SSOC_TH_SEL_C		FVM_HYS_C		SSOC_TH_SEL_D		FVM_HYS_D	
Default	1	1	0	0	1	1	0	0
Type	RW		RW		RW		RW	

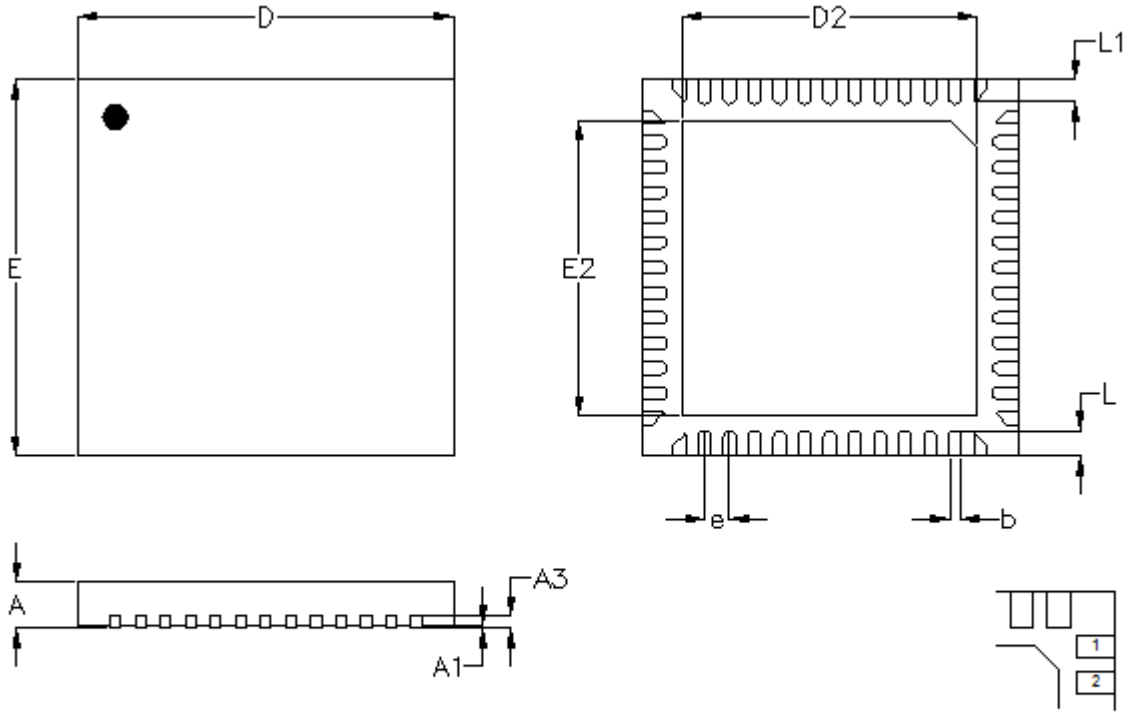
Bit	Name	Description
7:6	SSOC_TH_SEL_C	Select the soft-startup OCP threshold for rail C. 00: 1.4 x ICCMAX 01: 1.6 x ICCMAX 10: 1.8 x ICCMAX 11: 2.0 x ICCMAX
5:4	FVM_HYS_C	Set the current hysteresis for the FVM of rail C. 00: FVM_HYS = 10% x ICCMAX 01: FVM_HYS = 15% x ICCMAX 10: FVM_HYS = 20% x ICCMAX 11: FVM_HYS = 25% x ICCMAX
3:2	SSOC_TH_SEL_D	Select the soft-startup OCP threshold for rail D. 00: 1.4 x ICCMAX 01: 1.6 x ICCMAX 10: 1.8 x ICCMAX 11: 2.0 x ICCMAX
1:0	FVM_HYS_D	Set the current hysteresis for the FVM of rail D. 00: FVM_HYS = 10% x ICCMAX 01: FVM_HYS = 15% x ICCMAX 10: FVM_HYS = 20% x ICCMAX 11: FVM_HYS = 25% x ICCMAX

Table 98. CRC2_CHECK

Page: 0x0E Address: 0x0F								
Bit	7	6	5	4	3	2	1	0
Field	CRC2_CHECK							
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
7:6	CRC2_CHECK	The cyclic redundancy check (CRC) of the extend functional registers in PAGE 0x0E.

20 Outline Dimension



DETAIL A

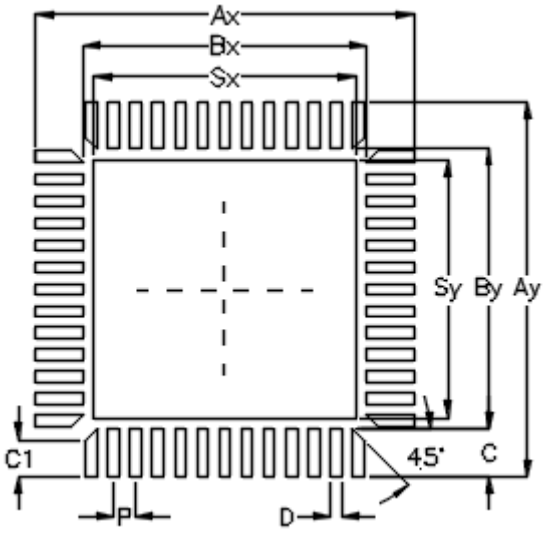
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

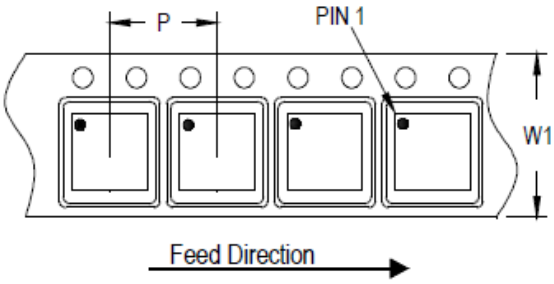
21 Footprint Information

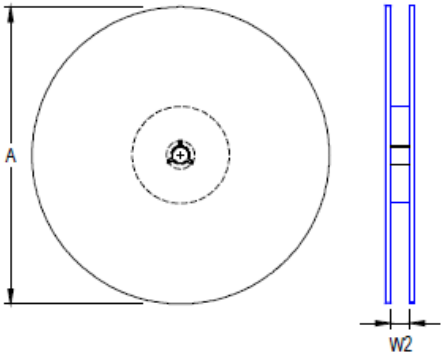


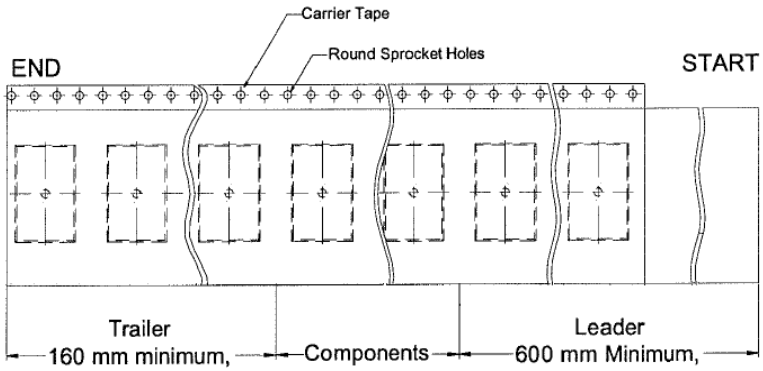
Package	Number of Pins	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*52	C1*8	D	Sx	Sy	
V/W/U/XQFN6*6-52	52	0.40	6.80	6.80	5.10	5.10	0.85	0.65	0.20	4.70	4.70	±0.05

22 Packing Information

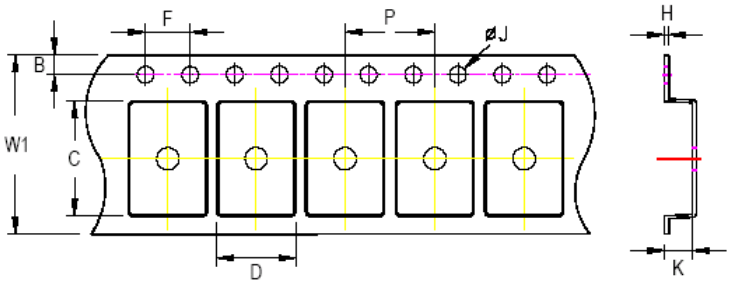
22.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 6x6	16	12	330	13	2,500	160	600	16.4/18.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W) QFN and DFN 6x6	13”	2,500	Box G	1	2,500	Carton A	6	15,000

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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23 Datasheet Revision History

Version	Date	Description
00	2025/10/30	First Edition
01	2025/12/2	General Description Features Functional Pin Description Functional Block Diagram Absolute Maximum Ratings Recommended Operating Conditions Electrical Characteristics Typical Operating Characteristics Operation Application Information
02	2026/2/11	Ordering Information