# Triple DC/DC Boost Converter for AMOLED

## General Description

RT4720A is a triple channels DC/DC converter which is designed to provide the power of AMOLED. It integrates step up DC/DC and an inverting converter to provide the positive and negative output voltage required by AMOLED.

For the portable application, board space and efficiency are always major concerns. The high switching frequency of RT4720A allows the use of low inductance inductor to save the board space. It provides dual positive output voltage, one is a fixed 5.8V or 7.7V output voltage by SEL pin and the other positive output is fixed 4.6V. For the negative output voltage, it can be programmed by external MCU through single wire (SWIRE pin). The output voltage range of negative output voltage is -1.4V to -5.4V. RT4720A has OTP, SCP, UVLO and over current protections. The RT4720A is available in a WQFN -16L 3x3 package to achieve saving PCB space.

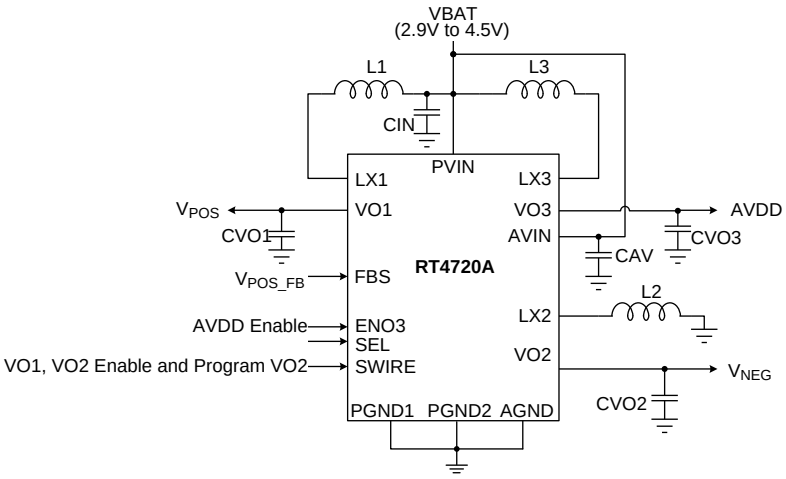
## Features

- **Boost Converter to Supply Positive AVDD Voltage Fixed 5.8V or 7.7V**
- **Boost Converter to Supply AMOLED Positive Voltage 4.6V**
- **Inverter Converter to Supply AMOLED Negative Voltage From -1.4V to -5.4V**
- **Maximum Output Current up to 300mA for AMOLED Positive & Negative Power Supply**
- **Maximum Output Current up to 50mA for Fixed 5.8V or 7.7V AVDD Output Voltage**
- **Typical Peak Efficiency : 90% (40mA to 150mA)**
- **PWM Mode @ 1.5MHz Switching Frequency**
- **High Output Voltage Accuracy**
- **Excellent Line and Load Transient**
- **Excellent Line and Load Regulation**
- **Programmable Negative Voltage by SWIRE Pin**
- **Fast Outputs Discharge Function**
- **Low Quiescent Current <1μA in Shutdown Mode**
- **Internal Soft Start to limit Inrush Current**
- **Over Temperature Protection (OTP)**
- **Over Current Protection (OCP)**
- **Short Circuit Protection (SCP)**

## Applications

- Cellular Phones
- Digital Cameras
- PDAs and Smart Phones
- Probable Instrument

## Simplified Application Circuit



## Ordering Information

RT4720A□□

Package Type
QW : WQFN-16L 3x3

Lead Plating System
G : Green (Halogen Free and Pb Free)

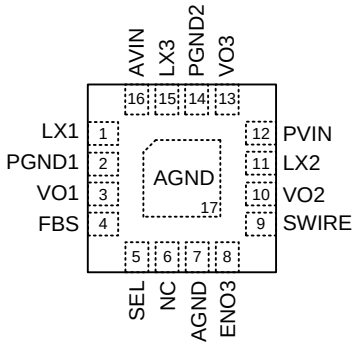
Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

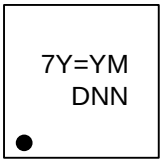
## Pin Configurations

(TOP VIEW)




WQFN-16L 3x3

## Marking Information

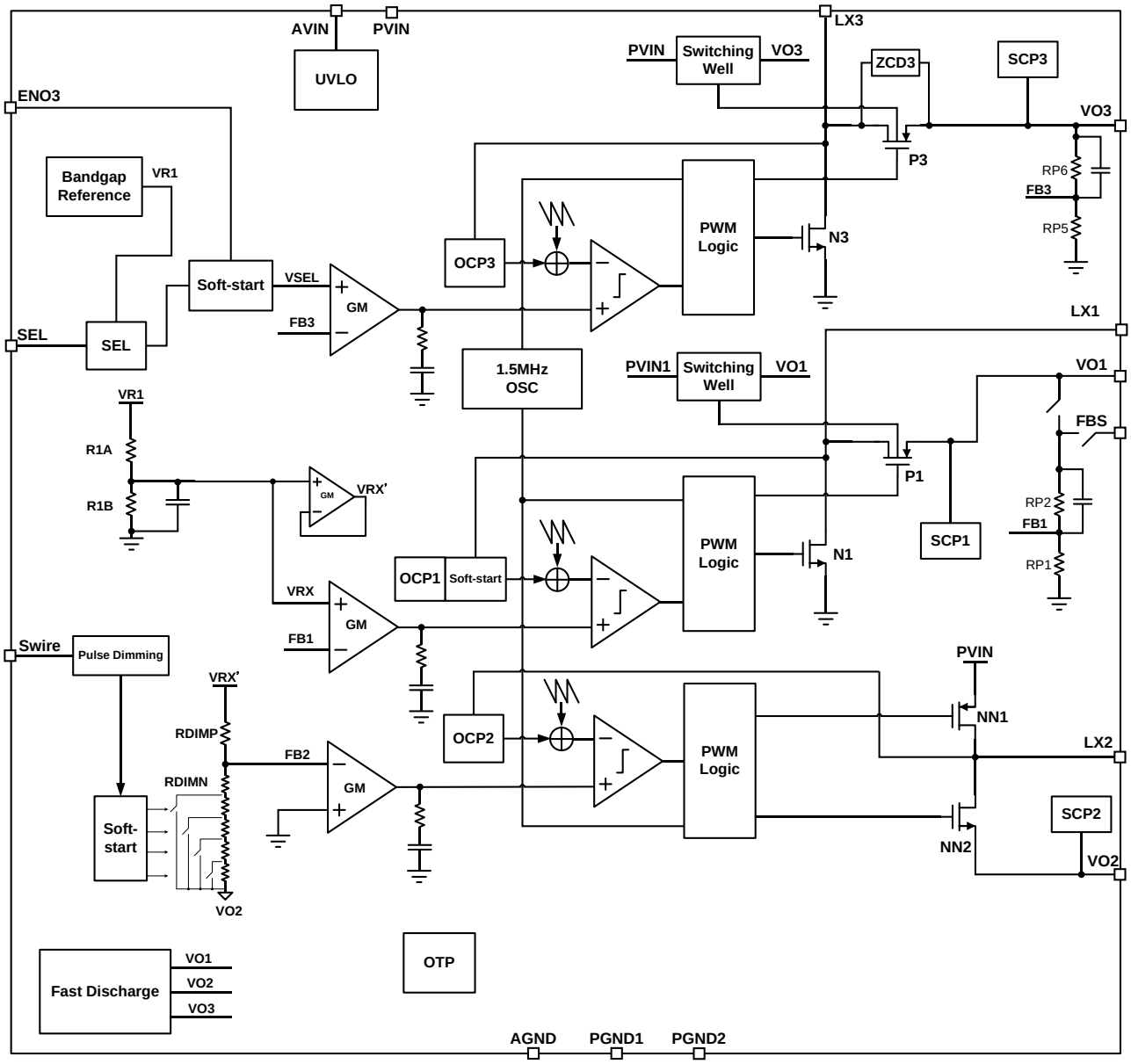



7Y= : Product Code
YMDNN : Date Code

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | LX1 | 1st Boost Converter Switching Node. |
| 2 | PGND1 | Power Ground. |
| 3 | VO1 | 1st Boost Converter Output. |
| 4 | FBS | 1st Boost Converter Output Feedback Sense. |
| 5 | SEL | 2nd Boost Converter Output Voltage Select Pin.<br>High = 5.8V, Low = 7.7V Output, Default Floating. |
| 6 | NC | No Connected. |
| 7,<br>17 (Exposed Pad) | AGND | Signal Ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation. |
| 8 | ENO3 | 2nd Boost Enable/Disable Pin. |
| 9 | SWIRE | $V_{POS}$, $V_{NEG}$ Control Pin (Enable/Disable Pin). |
| 10 | VO2 | Buck/Boost Converter Output (Negative Voltage). |
| 11 | LX2 | Buck/Boost Converter Switching Node. |
| 12 | PVIN | Power Input Voltage. |
| 13 | VO3 | 2nd Boost Converter Output. |
| 14 | PGND2 | Power Ground. |
| 15 | LX3 | 2nd Boost Converter Switching Node. |
| 16 | AVIN | Analog Input Voltage. |

## Functional Block Diagram




## Operation

The RT4720A is a triple channels DC/DC converter which is designed to provide the power of AMOLED that can support the input voltage range from 2.9V to 4.5V. The VO1&VO2 output current can be up to 300mA, and the VO3 output current can be up to 50mA. The RT4720A uses current mode architecture for the purpose of high efficiency and high transient response.

The VO1 positive output voltage is produced from the DC/DC Boost converter and is set at a typical value of 4.6V. When the SWIRE goes high, the positive output voltage will be enabled with an internal soft-start process. The VO2 negative output voltage is produced from the DC/DC Buck-Boost converter and the negative output voltage range is -1.4V to -5.4V. It can be programmed by external MCU through single wire (SWIRE pin). The VO3 positive output voltage is produced from the DC/DC Boost converter and is set at a fixed 7.7V or 5.8V by SEL pin. When SWIRE goes high and VO1 soft-start had finished already, negative output voltage VO2 will be enabled with an internal soft-start process.

**Table 1. SWIRE Command LUT for VO2**

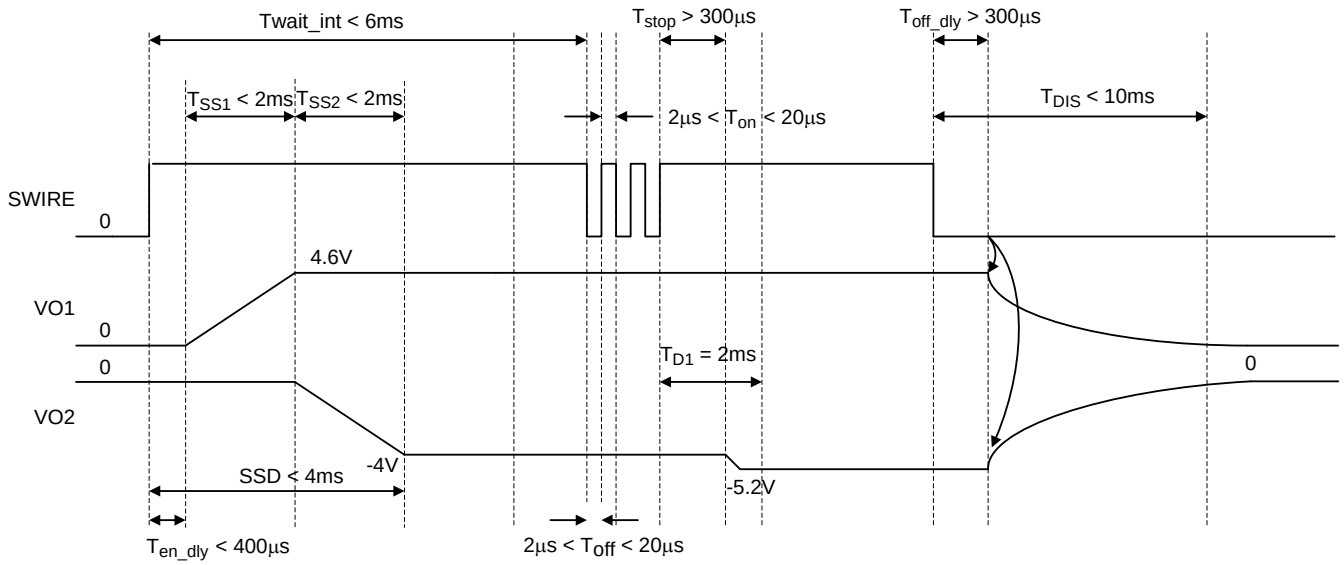
| Bit (Pulse) | VO2 (V) | Bit (Pulse) | VO2 (V) |
|---|---|---|---|
| 0 | –4.0 (Default) | 21 | –3.4 |
| 1 | –5.4 | 22 | –3.3 |
| 2 | –5.3 | 23 | –3.2 |
| 3 | –5.2 | 24 | –3.1 |
| 4 | –5.1 | 25 | –3 |
| 5 | –5 | 26 | –2.9 |
| 6 | –4.9 | 27 | –2.8 |
| 7 | –4.8 | 28 | –2.7 |
| 8 | –4.7 | 29 | –2.6 |
| 9 | –4.6 | 30 | –2.5 |
| 10 | –4.5 | 31 | –2.4 |
| 11 | –4.4 | 32 | –2.3 |
| 12 | –4.3 | 33 | –2.2 |
| 13 | –4.2 | 34 | –2.1 |
| 14 | –4.1 | 35 | –2 |
| 15 | –4 | 36 | –1.9 |
| 16 | –3.9 | 37 | –1.8 |
| 17 | –3.8 | 38 | –1.7 |
| 18 | –3.7 | 39 | –1.6 |
| 19 | –3.6 | 40 | –1.5 |
| 20 | –3.5 | 41 | –1.4 |

**Table 2. SWIRE Pin Characteristics**

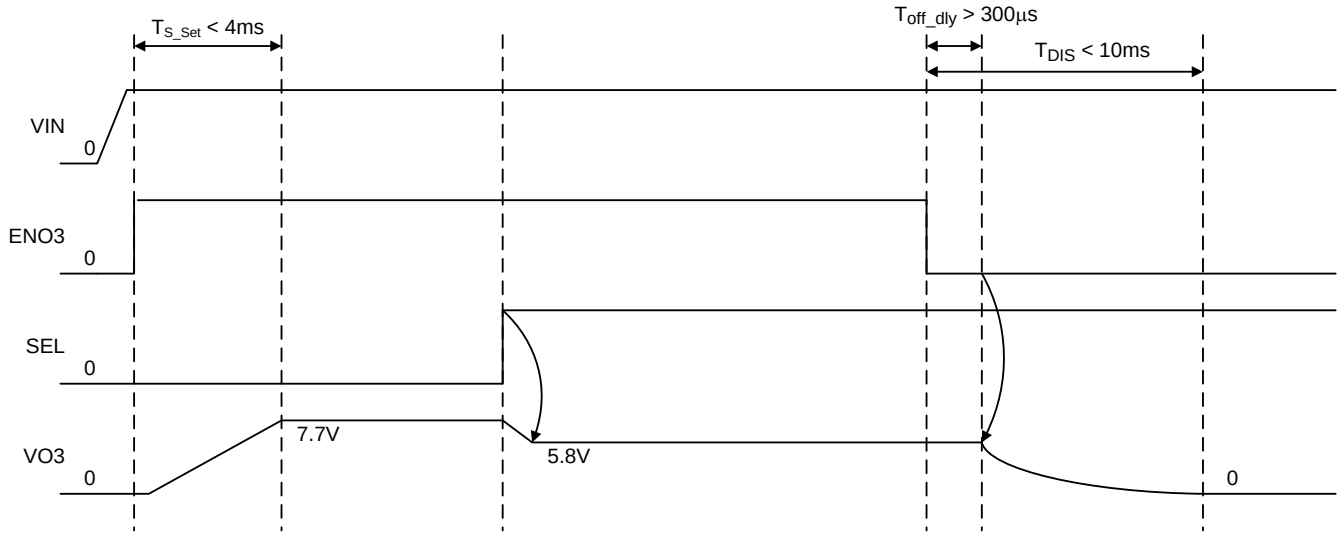
| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SWIRE High Delay Time | Ten_dly | -- | 300 | 400 | µs |
| SWIRE Turn-off Detection Time | Toff_dly | 300 | -- | -- | µs |
| SWIRE Signal Stop Indicate Time | Tstop | 300 | -- | -- | µs |
| Twait After Data | Twait_int | 6 | -- | -- | ms |
| Wake Up Delay | Twkp | -- | -- | 1 | µs |
| SWIRE Rising Time | Tr | -- | -- | 200 | ns |
| SWIRE Falling Time | Tf | -- | -- | 200 | ns |
| Clocked SWIRE High | Ton | 2 | 10 | 20 | µs |
| SWIRE Low | Toff | 2 | 10 | 20 | µs |
| Input SWIRE Frequency | Fswire | 25 | -- | 250 | kHz |

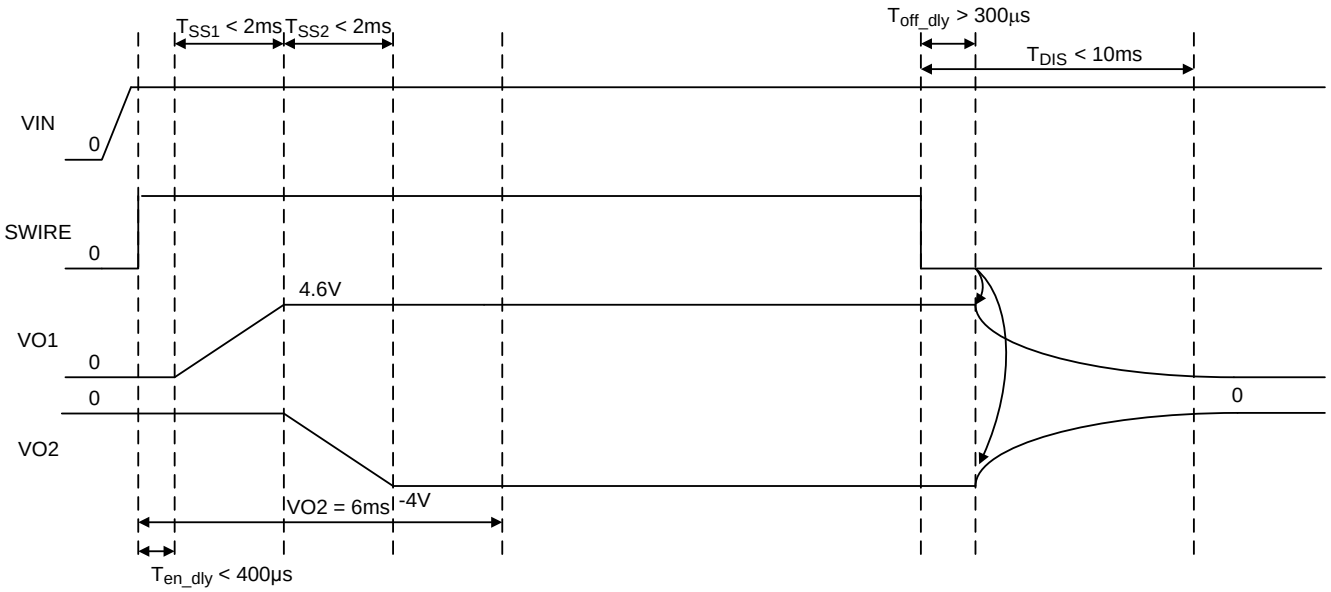
## Timing Diagram

SWIRE Command Timing Diagram




Power Sequence





## Absolute Maximum Ratings (Note 1)

- PVIN, AVIN, VO1, LX1, FBS, SEL, ENO3, SWIRE ---------- –0.3 to 6V
- VO3, LX3 ---------- –0.3 to 12V
- VO2 ---------- –6 to 0.3V
- LX2 ---------- –6 to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  WQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, $\theta_{JA}$ ---------- 30°C/W
  WQFN-16L 3x3, $\theta_{JC}$ ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.9V to 4.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

## Electrical Characteristics

($V_{IN}$ = 3.7V, $V_{O1}$ = 4.6V, $V_{O2}$ = –4V, $V_{O3}$ = 7.7V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 2.9 | 3.7 | 4.5 | V |
| Under Voltage Lockout High | UVLO_H | $V_{IN}$ Rising | 2.3 | 2.4 | 2.5 | V |
| Under Voltage Lockout Hysteresis | UVLO_Hys | $V_{IN}$ Hysteresis | -- | 0.2 | -- | V |
| VIN Shutdown Current | $I_{SHDN}$ | ENO3 = GND, SWIRE = GND | -- | -- | 1 | μA |
| ENO3 Input High Threshold | $V_{ENO3}$_H | $V_{IN}$ = 2.9V to 4.5V | 1.2 | -- | -- | V |
| ENO3 Input Low Threshold | $V_{ENO3}$_L | $V_{IN}$ = 2.9V to 4.5V | -- | -- | 0.4 | V |
| Pull Down Current | $I_{ENO3}$ | | -- | -- | 10 | μA |
| SWIRE Input High Threshold | $V_{SWIRE}$_H | $V_{IN}$ = 2.9V to 4.5V | 1.2 | -- | -- | V |
| SWIRE Input Low Threshold | $V_{SWIRE}$_L | $V_{IN}$ = 2.9V to 4.5V | -- | -- | 0.4 | V |
| Pull-down Resistor | $R_{SWIRE}$ | | -- | 150 | -- | kΩ |
| **Operation Section** | | | | | | |
| Switching Frequency | Freq | PWM Mode | 1.35 | 1.5 | 1.65 | MHz |
| VO1 Maximum Duty | $D_{MAX\_N1}$ | No Load | -- | 87 | -- | % |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VO2 Maximum Duty | $D_{MAX\_N}$ | No Load | -- | 87 | -- | % |
| VO3 Maximum Duty | $D_{MAX\_P2}$ | No Load | -- | 87 | -- | % |
| Over-Temperature Protection | OTP | | -- | 140 | -- | ℃ |
| Over-Temperature Protection Hysteresis | $OTP_{HYST}$ | | -- | 15 | -- | ℃ |
| **VO1 Positive Output** | | | | | | |
| Positive Output Range | VO1 | | -- | 4.6 | -- | V |
| Positive Output Voltage Variation | | PVIN = AVIN = 2.9V to 4.5V; $I_{O1}$ = 5mA to 300 mA, $I_{O2}$ no load | –2 | -- | 2 | % |
| Maximum Output Current | $IO1_{MAX}$ | $V_{IN}$ = 2.9V to 4.5V | -- | -- | 300 | mA |
| N1 N-MOSFET On-Resistance | $R_{DS(ON)1}$ | $I_{LX-N1}$ = 100mA | -- | 0.2 | -- | Ω |
| P1 P-MOSFET On-Resistance | | $I_{LX-P1}$ = 100mA | -- | 0.2 | -- | Ω |
| Current Limit | $I_{OCP1}$ | | -- | 0.8 | -- | A |
| Line Regulation | $VO1_{Line\_R}$ | $I_{O1}$ = 100mA | -- | 0.02 | -- | %/V |
| Load Regulation | $VO1_{Load\_R}$ | $I_{O1}$ = 5mA to 300mA | -- | 0.2 | -- | %/A |
| **VO2 Positive Output** | | | | | | |
| Adjustable Negative Output Voltage Range | VO2 | 41 different values set by SWIRE pin | –5.4 | –4 | –1.4 | V |
| Negative Output Voltage Variation | | VIN = 2.9V to 4.5V, $I_{O2}$ = 5mA to 300mA | –2 | -- | 2 | % |
| Maximum Output Current | $IO2_{MAX}$ | VINA, P = 2.9V to 4.5V | –300 | -- | -- | mA |
| $N_{N1}$ N-MOSFET On-Resistance | $R_{DS(ON)2}$ | $I_{LX-NN1}$ = 100mA | -- | 0.2 | -- | Ω |
| $N_{N2}$ P-MOSFET On-Resistance | | $I_{LX-NN2}$ = 100mA | -- | 0.2 | -- | Ω |
| Current Limit | $I_{OCP2}$ | | -- | 1.5 | -- | A |
| Line Regulation | $VO2_{Line\_R}$ | $I_{O2}$ = 100mA | -- | 0.02 | -- | %/V |
| Load Regulation | $VO2_{Load\_R}$ | | -- | 0.3 | -- | %/A |
| VO1 Discharge Resistor Value | $R_{DIS1}$ | | -- | 40 | -- | Ω |
| VO2 Discharge Resistor Value | $R_{DIS2}$ | | -- | 40 | -- | Ω |
| VO3 Discharge Resistor Value | $R_{DIS3}$ | | -- | 30 | -- | Ω |
| **VO3 AVDD Output** | | | | | | |
| Positive Output Voltage Range | VO3 | SEL = Low | -- | 7.7 | -- | V |
| | | SEL = High | -- | 5.8 | -- | |
| Output Voltage Total Variation | VO3_ACY | AVIN = PVIN = 2.9V to 4.5V; $I_{O3}$ = 0.1mA to 20mA | –2 | -- | 2 | % |
| Maximum Output Current | $IO3_{MAX}$ | $V_{IN}$ = 2.9V to 4.5V | -- | -- | 50 | mA |
| N3 N-MOSFET On-Resistance | $R_{DSON3}$ | $I_{LX-N3}$ = 20mA | -- | 0.4 | -- | Ω |
| P3 P-MOSFET On-Resistance | | $I_{LX-P3}$ = 20mA | -- | 1 | -- | |
| Current Limit | $I_{OCP3}$ | | -- | 0.35 | -- | A |
| Line Regulation | $VO3_{Line\_R}$ | $I_{O3}$ = 15mA | -- | 0.01 | -- | %/V |
| Load Regulation | $VO3_{Load\_R}$ | | -- | 0.4 | -- | %/A |

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

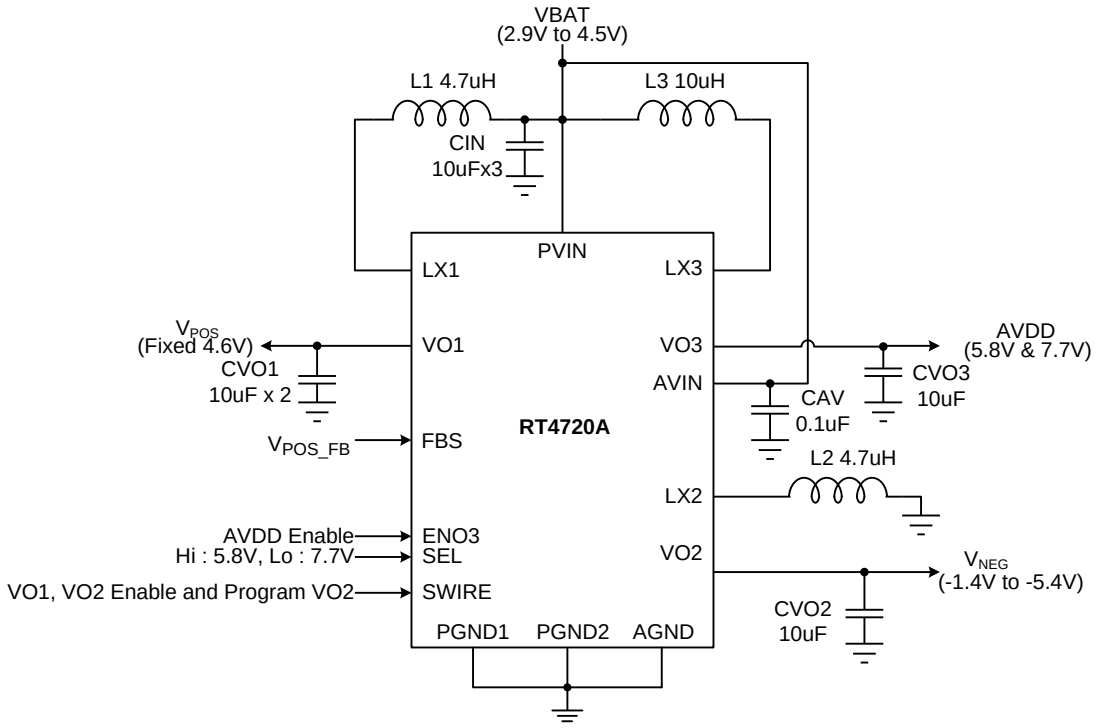
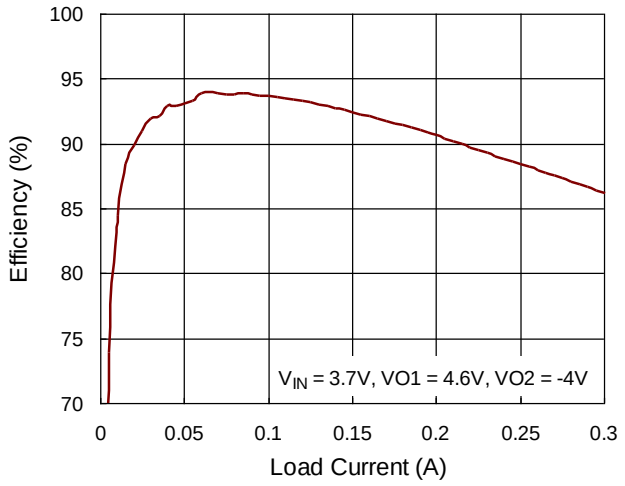



**Table 3. Typical BOM List**

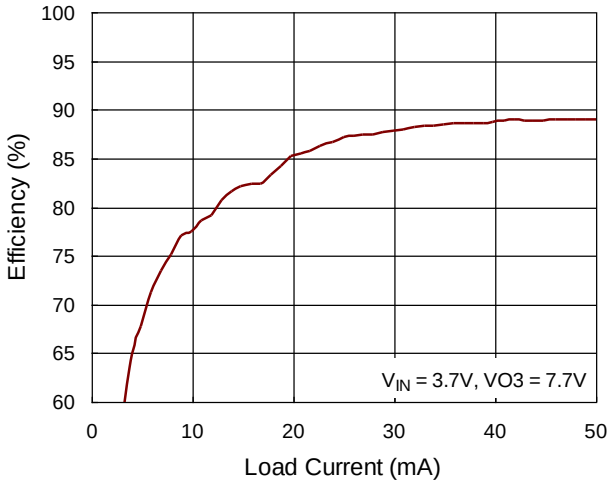
| Component | Value | Part Number | Manufacture |
|---|---|---|---|
| CIN | 10μFx3 | GRM21BR71A106KE51 | Murata |
| CVO1,CVO2,CVO3 | 10μF | GRM21BR71A106KE51 | Murata |
| L1,L2 | 4.7μH | DFE252012C-4R7N | TOKO |
| L3 | 10μH | DFE252012C-100M | TOKO |

## Typical Operating Characteristics

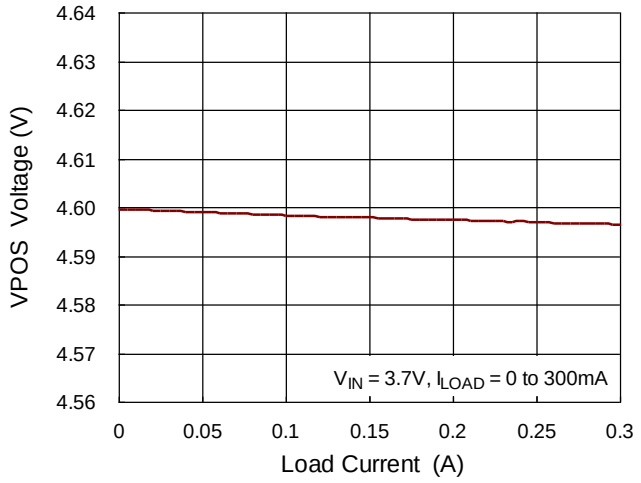
**VO1&VO2 Efficiency vs. Load Current**



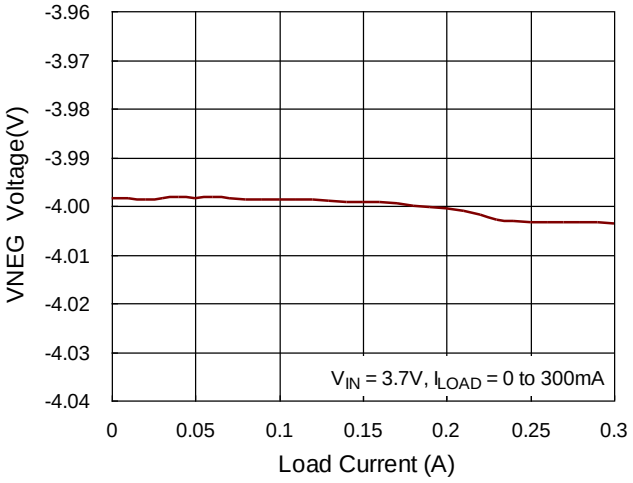

**VO3 Efficiency vs. Load Current**



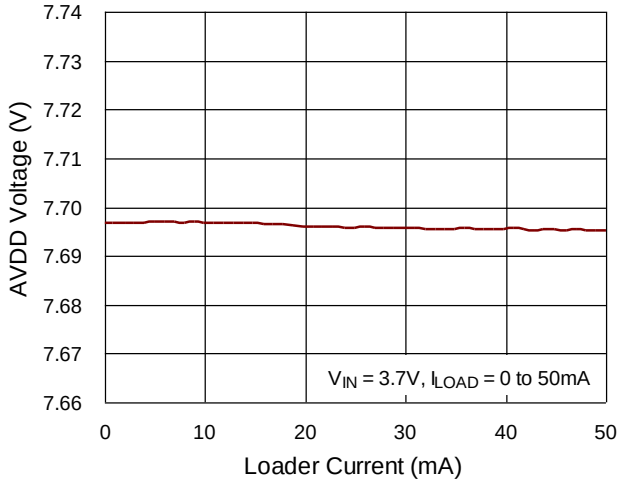

**VPOS Voltage vs. Load Current**



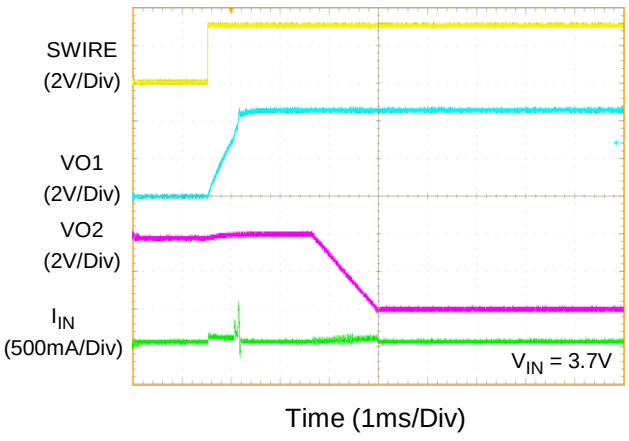

**VNEG Voltage vs. Load Current**



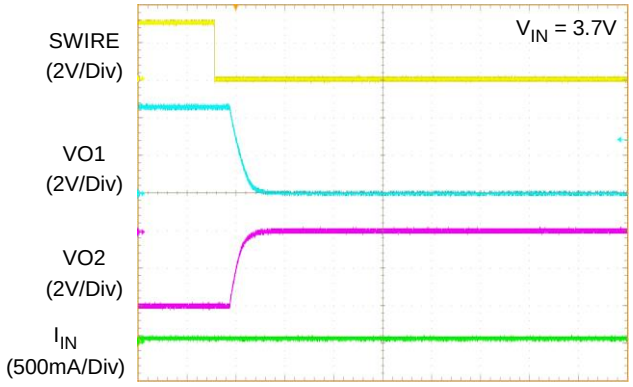

**AVDD Voltage vs. Load Current**



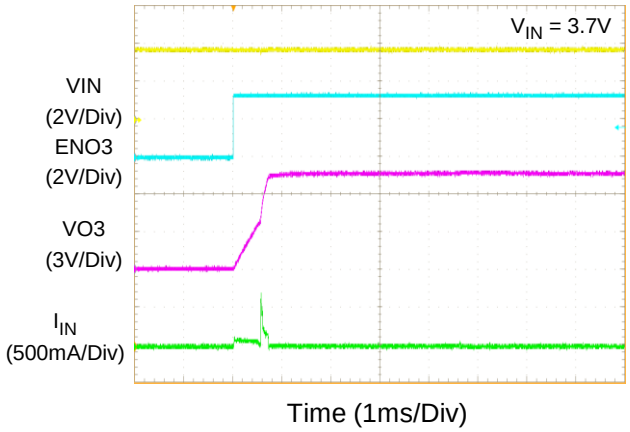

**VO1 & VO2 Power On**



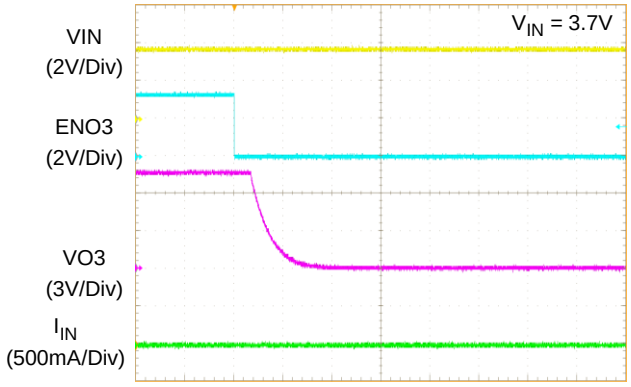
**VO1 & VO2 Power Off**




**VO3 Power On**




**VO3 Power Off**



## Application Information

The RT4720A is a triple channels DC/DC converter, which integrates dual step up converter and an inverting converter to provide the positive and negative output voltage required by AMOLED. RT4720A protection function includes Over Temperature Protection (OTP), Over Current Protection (OCP) and Short Circuit Protection (SCP), also it has Pulse Skipping Mode (PSM) to provide high efficiency during light load.

### Soft-Start

The RT4720A use an internal soft-start feature to avoid high inrush currents during step-up.

### Fast Discharge Function

All outputs voltage use an embedded discharge function to discharge the remaining output to 0V rapidly, preventing phenomena such as residual image on the display during shutdown.

### Over Temperature Protection (OTP)

The RT4720A includes an Over Temperature Protection (OTP) feature to prevent excessive power dissipation from overheating the device. The OTP will shut down switching operation when junction temperature exceeds 140°C. Once the junction temperature cools down by approximately 15°C, the converter resumes operation.

To maintain continuous operation, prevent the maximum junction temperature from rising above 125°C.

### Over Current Protection (OCP)

The RT4720A includes a current sensing circuitry which monitors the inductor current during each ON period. If the current value becomes greater than the current limit, the switch that pertains to inductor charging will turn off, forcing the inductor to leave charging stage and enter discharge stage.

### Short Circuit Protection (SCP)

The RT4720A has an advanced short circuit protection mechanism which prevents damage to the device from unexpected applications. When the output voltage becomes lower than about 90%, over 1ms the device enters shutdown mode. VO3 can only re-start normal operation after triggering the ENO3 pin and VO1, VO2 can only re-start normal operation after triggering the SWIRE pin.

### Under Voltage Lockout (UVLO)

To prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included, which shuts down the device at voltages lower than 2.2V. All functions will be turned off in this state.

### Input Capacitor Selection

Each channel input ceramic capacitors with 10μF capacitance are suggested for the RT4720A applications. However, to achieve best performance with the RT4720A, larger capacitance can be used. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types which are suitable because of their wider voltage and temperature ranges.

### Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$\Delta I_L = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the converter, $I_{IN(MAX)}$ is the maximum input current, and $\Delta I_L$ is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$I_{PEAK} = 1.2 \times I_{IN(MAX)}$

Note that the saturated current of the inductor must be greater than $I_{PEAK}$.

The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where $f_{OSC}$ is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

### Boost Output Capacitor Selection

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of the inductor peak current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1, $\Delta V_{OUT1}$ can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[ \left( I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left( I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times V_{OUT1}$$

where $f_{OSC}$ is the switching frequency and $\Delta I_L$ is the inductor ripple current. Bring $C_{OUT}$ to the left side to estimate the value of $\Delta V_{OUT1}$ according to the following equation :

$$\Delta V_{OUT1} = \Delta V_{ESR} + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

where $\Delta V_{ESR} = \Delta I_C \times R_{C\_ESR} = I_{PEAK} \times R_{C\_ESR}$

The output capacitor, $C_{OUT}$, should be selected accordingly.

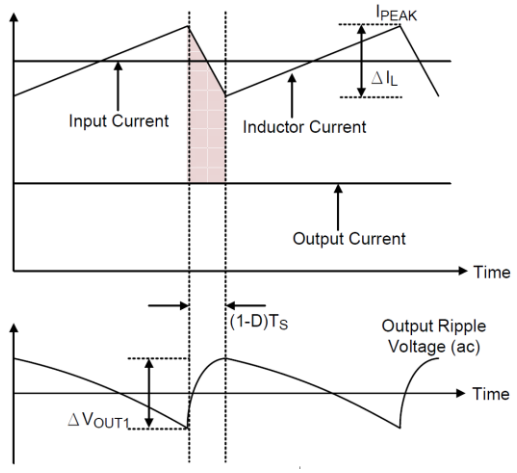



Figure 1. The Output Ripple Voltage without the Contribution of ESR

### AVDD Output Voltage Setting

The AVDD boost output voltage VO3 is fixed 7.7V or 5.8V output voltage by SEL pin. When SEL pin is set to high, the output voltage is 5.8V or otherwise SEL pin is set to low, the output voltage is changed to 7.7V.

### Buck-boost Converter Inductor Selection

The first step in the design procedure is to verify whether the maximum possible output current of the buck-boost converter supports the specific application requirements. To simply the calculation, the fastest approach is to estimate converter efficiency by taking the efficiency numbers from provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 80%. The calculation must be performed for the minimum assumed input voltage where the peak switch current is the highest. The inductor has an internal switch to be able to handle this current.

- Converter Duty Cycle :

$$D = \frac{-V_{OUT}}{V_{IN} \times \eta - V_{OUT}}$$

- Maximum output current :

$$I_{OUT} = \left( I_{PEAK} - \frac{V_{IN} \times D}{2 \times f_{OSC} \times L} \right) \times (1-D)$$

- Inductor peak current :

$$I_{PEAK} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times f_{OSC} \times L}$$

As for inductance, we are going to derive the transition point, where the converter toggles from CCM to DCM. We need to define the point at which the inductor current ripple touches zero, and as the power switch SW is immediately reactivated, the current ramps up again. Figure 2 portrays the input current activity of the buck-boost converter.

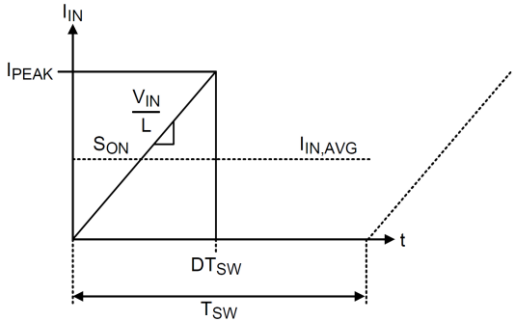



Figure 2. The Buck-Boost Input Signature in BCM

The inductance can eventually be determined according to the following equation :

$$L_{critical} = \frac{|V_{OUT}| \times \eta}{2 \times f_{OSC} \times I_{OUT}} \times \left( \frac{V_{IN}}{V_{IN} + |V_{OUT}|} \right)^2$$

### Buck-Boost Converter Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. One 10µF output capacitors with sufficient voltage ratings in parallel are adequate for most applications. Additional capacitors can be added to improve load transient response.

To calculate the output voltage ripple, the following equations can be used :

$$\Delta V = \frac{D \times |V_{OUT}|}{f_{OSC} \times R_{LOAD} \times C_{OUT}} + \Delta V_{ESR}$$

where $\Delta V_{ESR} = \Delta I_C \times R_{C\_ESR} = I_{PEAK} \times R_{C\_ESR}$

$\Delta V_{ESR}$ can be neglected in many cases since ceramic capacitors provides very low ESR.

### Negative Output Voltage Setting

Buck-boost converter is implementing a pulse dimming method to control the output voltage (VO2) and its value is from –1.4V to –5.4V in 0.1V increments. User can control VO2 by SWIRE command. See SWIRE command section for details on how to adjust the output voltage.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For WQFN-16L 3x3 package, the thermal resistance, $\theta_{JA}$, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

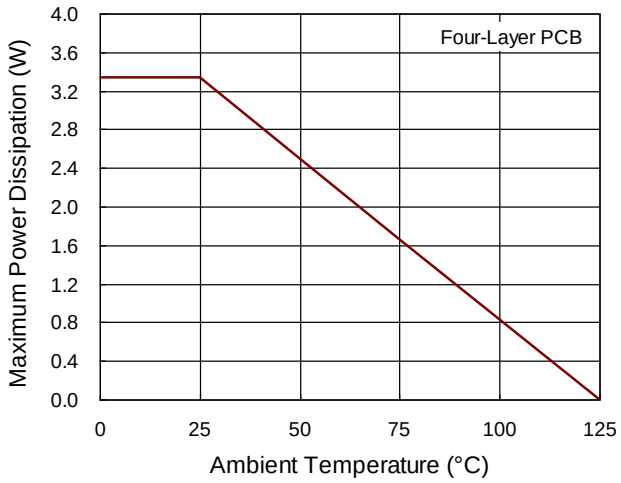



Figure 3. Derating Curve of Maximum Power Dissipation

### Layout Consideration

For the best performance of RT4720A, the following PCB layout guidelines should be strictly followed.

- For good regulation, place the power components as close to the IC as possible. The traces should be wide and short, especially for the high current output loop.
- The input and output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
- Minimize the size of the LX1, LX2, LX3 nodes and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near LX or high-current traces.
- Separate power ground (PGND) and analog ground (AGND). Connect the AGND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes.
- Connect the exposed pad to a strong ground plane for maximum thermal dissipation.

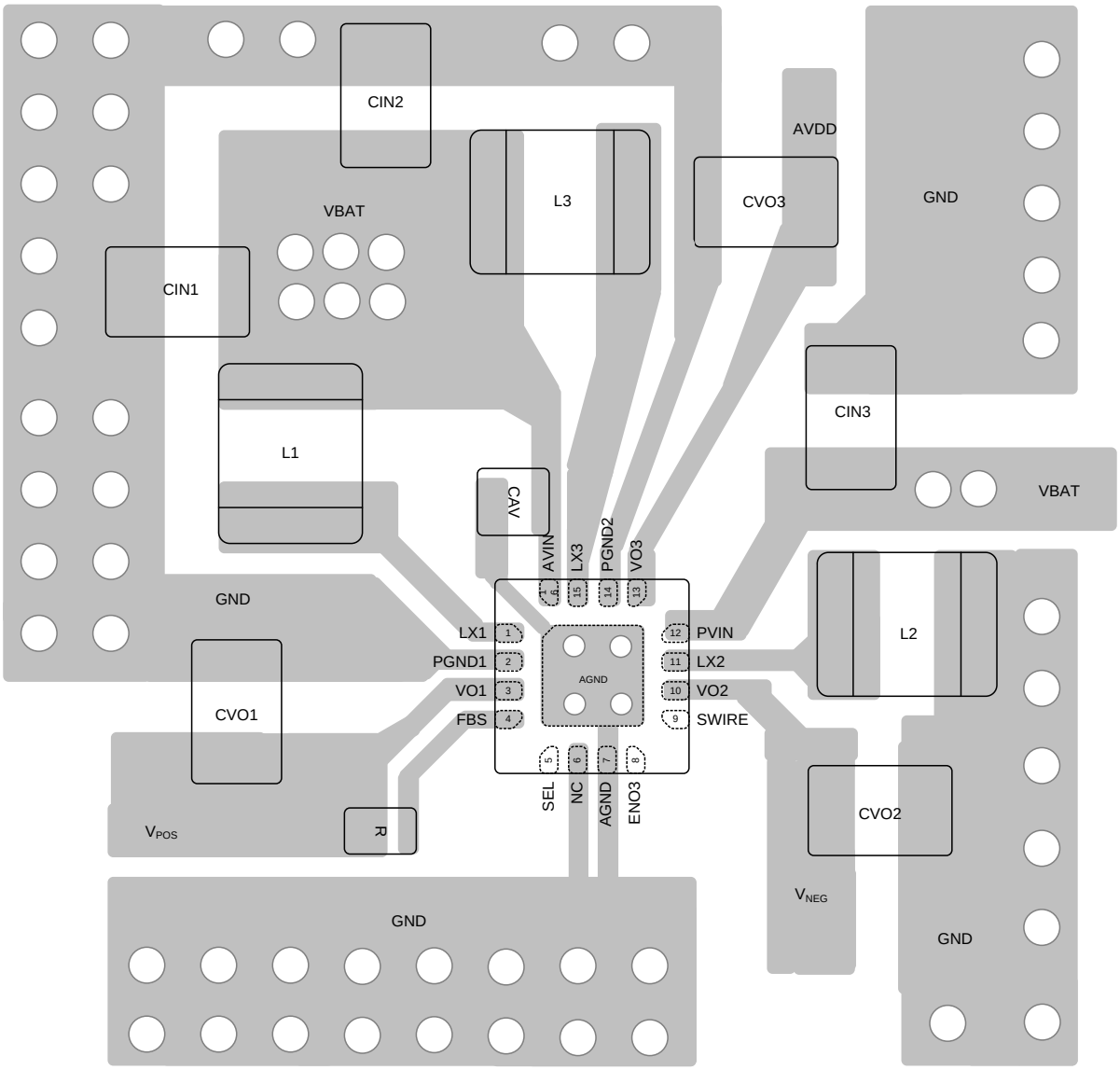
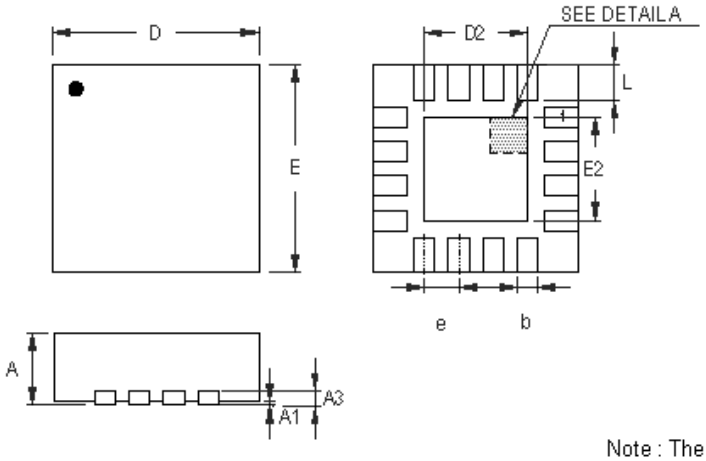
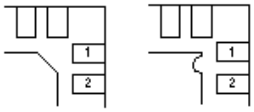



Figure 4. PCB Layout Guide

## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| D | 2.950 | 3.050 | 0.116 | 0.120 |
| D2 | 1.300 | 1.750 | 0.051 | 0.069 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| E2 | 1.300 | 1.750 | 0.051 | 0.069 |
| e | 0.500 | | 0.020 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

**W-Type 16L QFN 3x3 Package**

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