

7 + 1 Channel DC/DC PMU with Li-Ion Battery Charger for DSC

General Description

The RT5002C is a complete power supply solution for digital still cameras and other handheld devices. It includes a 7+1 channel DC/DC power converter unit, a single-cell Li-ion battery charger, and an I²C control interface.

The power converter unit includes one synchronous step-up converter and three synchronous step-down converters for DSP core, I/O, Motor, and memory power supply, one synchronous high voltage step-up converter and one asynchronous inverting converter for CCD± bias, one WLED driver in either synchronous high voltage step-up or current source operation, and one low quiescent LDO for RTC application. All converters are internally frequency compensated and integrate power MOSFETs. The power converter unit provides complete protection functions: over current, thermal shutdown, over voltage, over-load, and under voltage protection.

The battery charger includes Auto Power Path Management (APPM). No external MOSFETs are required. The charger enters sleep mode when power is removed. Charging tasks are optimized by using a control algorithm to vary the charge rate, including pre-charge mode, fast charge mode and constant voltage mode. The charge current can also be programmed with an external resistor and modified via the I²C control interface. The scope that the battery regulation voltage can be modified via the I²C

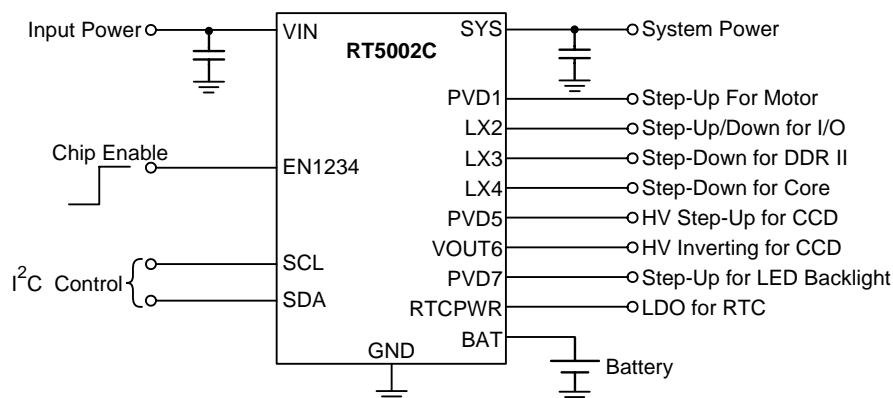
interface depends on the battery temperature. The internal thermal feedback circuitry regulates the die temperature to optimize the charge rate for all ambient temperatures. The charging task will always be terminated in constant voltage mode when the charging current reduces to the termination current of 10% x I_{CHG_FAST}. The charger includes under voltage and over-voltage protection for the supply input voltage, V_{IN}.

Features

Power Converter Unit :

- **One Channel LV Sync Step-Up and Three Channel LV Sync Step-Down**
 - ▶ **Up to 95% Efficiency**
- **One Sync Step-Up and One Async Inverting for CCD± bias**
- **One WLED Driver in either Sync Step-Up or Current Source Operation**
 - ▶ **WLED Driver with Dimming Control**
 - ▶ **Step-Up Mode with LED Open Protection (OVP7)**
- **One Low Quiescent LDO with Reverse Leakage Prevention for RTC Power Supply**
- **Preset On/Off Sequence of CH1, CH2, CH3, CH4 (1→3→4→2)**
- **Three Preset On/Off Sequences of CH5, CH6 (5→6, 6→5, and 5/6 at the same time)**

Simplified Application Circuit



- All Power Switches Integrated with Internal Compensation
- All Step-Up Converters with Load Disconnect
- Wake Up Impulse to Monitor BAT and VIN Plug-In Charger Unit :
- 28V Maximum Rating for VIN Power
- Selectable Power Current Limit (0.1A / 0.5A / 1.5A)
- Auto Power Path Management (APPM) and Integrated Power MOSFETs
- Battery Charging Current Control
- Battery Regulation Voltage Control
- Programmable Charging Current and Safe Charge Timer
- Under Voltage and Over Voltage Protection
- Charge Status Indicator
- Optimized Charge Rate via Thermal Feedback
- Interrupt Indicator to Fault/Status Events
- I²C Control Interface : Support Fast Mode up to 400kb/s
- Small 40-Lead WQFN Package
- RoHS Compliant and Halogen Free

Ordering Information

RT5002C□□

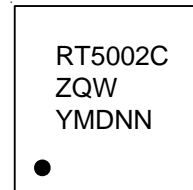
- Package Type
QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

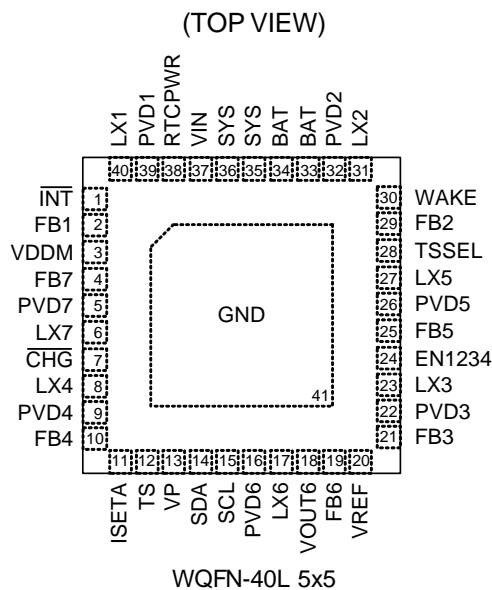


RT5002CZQW : Product Number
YMDNN : Date Code

Applications

- DSC

Pin Configurations

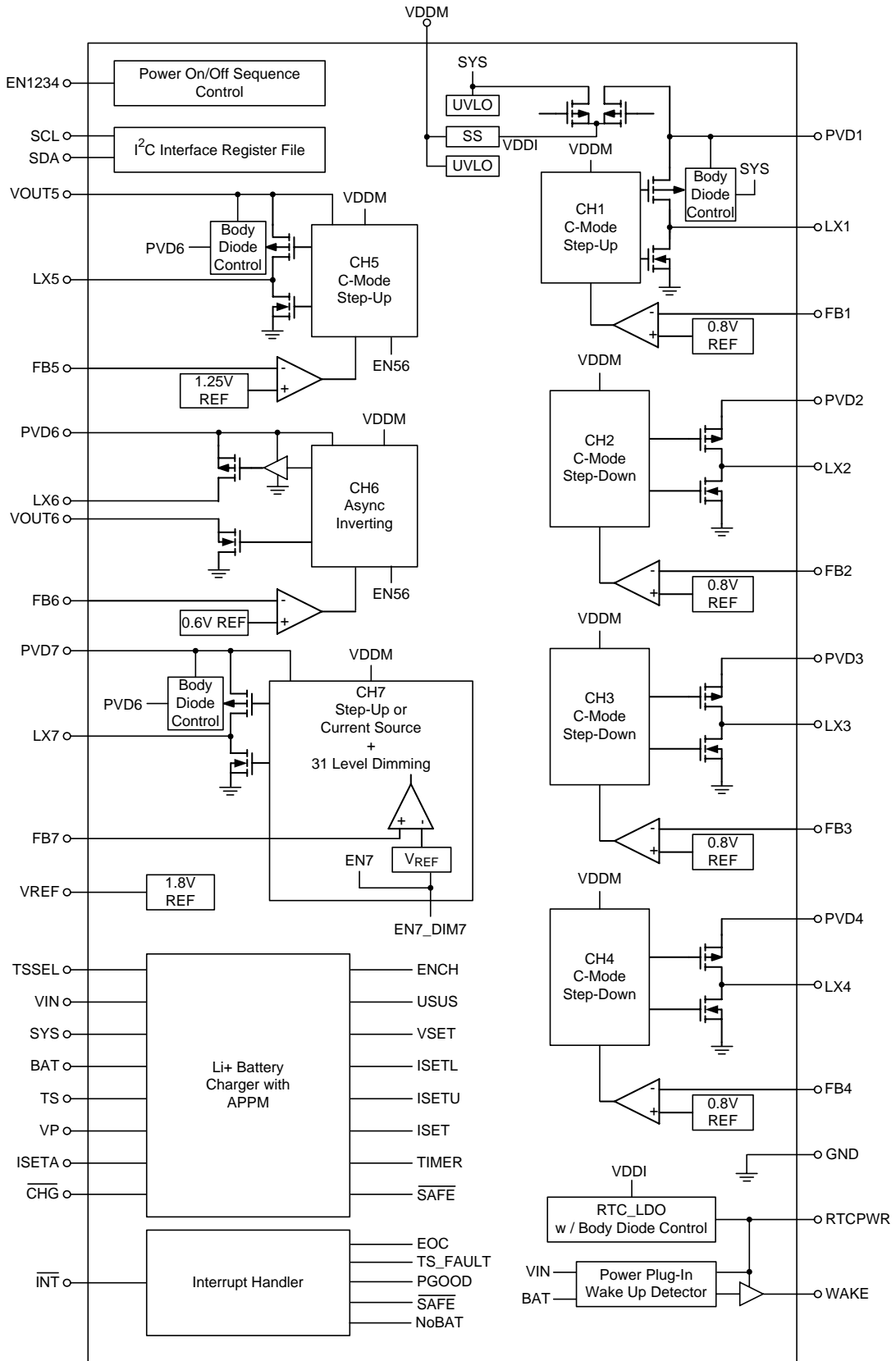


Functional Pin Description

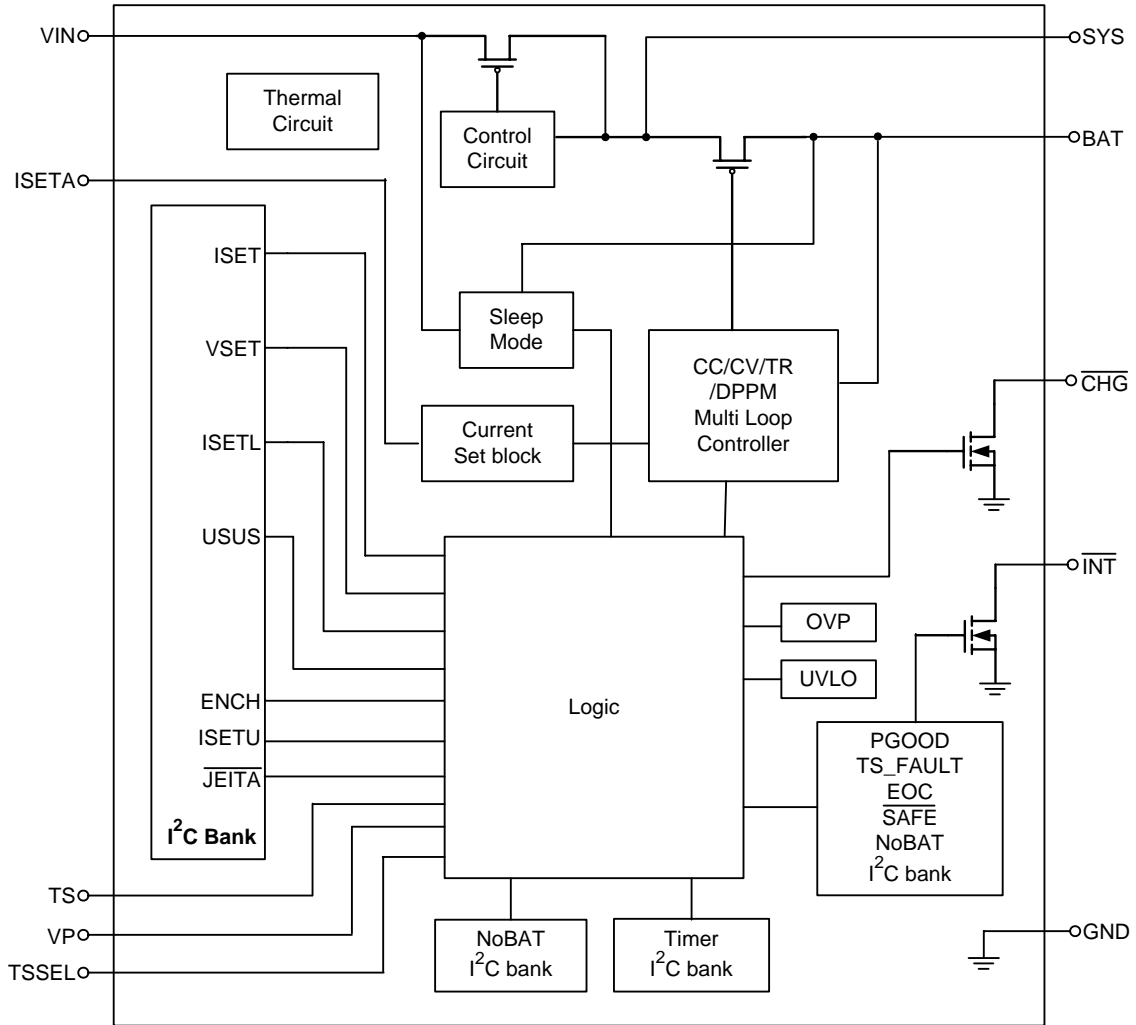
Pin No.	Pin Name	Pin Function
1	INT	Interrupt Indicator Open Drain Output. If any toggle events of TS_FAULT, PGOOD, EOC, NoBAT, or SAFE happen, the output INT goes low. After I ² C register bank address 0x2 is read or power on reset, INT goes high.
2	FB1	Feedback Input of CH1.
3	VDDM	IC Analog Power Pin.
4	FB7	Feedback Input of CH7 in Step-Up Mode or Current Sink Pin of CH7 in Current Source Mode.
5	PVD7	Power Output of CH7.
6	LX7	Switch Node of CH7 in Step-Up Mode.
7	CHG	Charger Status Output. Open-drain output.
8	LX4	Switch Node of CH4.
9	PVD4	Power Input of CH4.
10	FB4	Feedback Input of CH4.
11	ISETA	Charge Current Set Input. Connect a resistor (R _{ISETA}) between ISETA and GND.
12	TS	Temperature Sense Input. The TS pin connects to a battery's thermistor to determine whether the battery is too hot or too cold to be charged. If the battery's temperature is out of range, charging is paused until it re-enters the valid range. TS also detects whether the battery (with NTC) is present or not.
13	VP	Power Output of 3.3V Buffer for Battery Temperature Sensing.
14	SDA	Data Signal Pin of I ² C Interface.
15	SCL	Clock Signal Pin of I ² C Interface.
16	PVD6	Power Input of CH6.
17	LX6	Switch Node of CH6.
18	VOUT6	Sense Input of CH6 Inverting Output Node.
19	FB6	Feedback Input of CH6.
20	VREF	1.8V Reference Output.
21	FB3	Feedback Input of CH3.
22	PVD3	Power Input of CH3.
23	LX3	Switch Node of CH3.
24	EN1234	Enable Pin of CH1, CH2, CH3, and CH4.
25	FB5	Feedback Input of CH5.
26	PVD5	Power Output of CH5.
27	LX5	Switch Node of CH5.
28	TSSEL	Input Pin to Select Temperature Sensing Thresholds. Thresholds of TSSEL = H are 60% and 38% of VP voltage. Thresholds of TSSEL = L are 74% and 28% of VP voltage.
29	FB2	Feedback Input of CH2.
30	WAKE	Wake-Up Impulse Push-Pull Output. If VIN or BAT plugs in, WAKE pin generates one 90ms width high pulse to notify micro processor.
31	LX2	Switch Node of CH2.
32	PVD2	Power Input of CH2.

Pin No.	Pin Name	Pin Function
33, 34	BAT	Battery Charge Current Output.
35, 36	SYS	System Connect. Connect this pin to system with a minimum 10 μ F ceramic capacitor to GND.
37	VIN	Supply Voltage Input.
38	RTCPWR	RTC Power Output.
39	PVD1	Power Output of CH1.
40	LX1	Switch Node of CH1.
41 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.

Function Block Diagram



Charge Function Block Diagram



Operation

The RT5002C is an integrated power system for digital still cameras and other small handheld devices. It includes six DC/DC converters as well as one WLED driver, one RTC LDO, and a fully integrated single-cell Li-ion battery charger ideal for portable applications.

CH1 : Step-up synchronous current mode DC/DC converter with internal power MOSFETs and compensation network.

The P-MOSFET body can be controlled to disconnect the load. It is suitable for providing power to the motor.

CH2 to CH4 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs and compensation network.

CH5 : High voltage step-up synchronous current mode DC/DC converter with internal power MOSFET and compensation network. The P-MOSFET body can be controlled to disconnect the load.

CH6 : Asynchronous inverting current mode DC/DC converter with internal power MOSFET and compensation network. An external Schottky diode is required. This channel supplies the CCD– bias.

CH7 : WLED driver operating in either current source mode or synchronous step-up mode with internal power MOSFET and compensation network. The operation mode is determined via the I2C interface.

RTC_LDO : 3.05V output LDO with low quiescent current and reverse leakage prevention from output node.

Charger Unit

The RT5002C includes a Li-ion battery charger with Automatic Power Path Management. The charger is designed to operate in below modes.

Pre-charge Mode

When the output voltage is lower than 2.8V, the charging current will be reduced to a fast-charge current ratio set by RISETA to protect the battery life-time.

Fast-charge Mode

When the output voltage is higher than 3V, the charging current will be equal to the fast-charge current set by RISETA.

Constant Voltage Mode

When the output voltage is near 4.2V and the charging current falls below the termination current, after a deglitch time check of 25ms, the charger will become disabled and $\overline{\text{CHG}}$ will go from L to H.

Re-charge Mode

When the chip is in charge termination mode, the charging current gradually goes down to zero. However, once the voltage of the battery drops to below 4.1V, there will be a deglitch time of 100ms and then the charging current will resume again.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, BAT ----- -0.3V to 6V
- Supply Voltage, VDDM ----- -0.3V to 6V
- Supply Input Voltage, VIN ----- -0.3V to 28V
- $\overline{\text{CHG}}$, $\overline{\text{INT}}$ ----- -0.3V to 28V
- Other Pins ----- -0.3V to 6V
- Power Switch (DC) :
 - VOUT6 ----- -10V to 0.3V
 - LX1, LX2, LX3, LX4 ----- -0.3V to 6V
 - PVD5, LX5 ----- -0.3V to 24V
 - PVD7, LX7 ----- -0.3V to 17V
 - LX6 ----- (PVD6 – 16V) to (PVD6 + 0.3V)
- $\overline{\text{CHG}}$, $\overline{\text{INT}}$ Continuous Current ----- 20mA
- BAT Continuous Current (total in two pins) (Note 2) ----- 2.5A
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 - WQFN-40L 5x5 ----- 3.64W
- Package Thermal Resistance (Note 3)
 - WQFN-40L 5x5, θ_{JA} ----- 27.5°C/W
 - WQFN-40L 5x5, θ_{JC} ----- 6°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 125°C
- ESD Susceptibility (Note 4)
 - HBM (Human Body Model) ----- 2kV
 - MM (Machine Model) ----- 200V

Recommended Operating Conditions (Note 5)

- Supply Voltage, VDDM ----- 2.7V to 5.5V
- Supply Input Voltage, VIN (ISETL = 1) ----- 4.4V to 6V
- Supply Input Voltage, VIN (ISETL = 0) ----- 4.5V to 6V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

Power Converter Unit : ($V_{DDM} = 4.2V$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
SYS Startup Voltage for PMU	V_{ST}		2.4	--	--	V
SYS UVLO (Hysteresis Low)			--	1.5	--	V
SYS UVLO Hysteresis (Gap)			--	0.2	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDM Over Voltage Protection (OVP) (Hysteresis High)			5.82	6.0	6.18	V
VDDM OVP Hysteresis (Gap)			--	-0.25	--	V
VDDM UVLO (Hysteresis High)			2.2	2.4	2.6	V
VDDM UVLO Hysteresis (Gap)			--	0.3	--	V
Supply Current						
Shutdown Supply Current	I _{OFF}	All Channels are Off, V _{EN1234} = 0V, V _{BAT} = 4.2V	--	10	20	μA
CH1 (Sync-Step-Up) Supply Current into VDDM	I _{Q1}	No Switching, V _{EN1234} = 3.3V	--	--	800	μA
CH2 (Syn-Step-Down) Supply Current into VDDM	I _{Q2}	No Switching, V _{EN1234} = 3.3V	--	--	800	μA
CH3 (Syn-Step-Down) Supply Current into VDDM	I _{Q3}	No Switching, V _{EN1234} = 3.3V	--	--	800	μA
CH4 (Syn-Step-Down) Supply Current into VDDM	I _{Q4}	No Switching, V _{EN1234} = 3.3V	--	--	800	μA
CH5 (Syn-Step-Up) Supply Current into VDDM	I _{Q5}	Non Switching, EN56 = 1	--	--	800	μA
CH6 (Inverting) Supply Current into VDDM	I _{Q6}	No Switching, EN56 = 1	--	--	800	μA
CH7 (WLED) in Step-Up Mode Supply Current into VDDM	I _{Q7b}	No Switching, EN7_DIM7 [4:0] = 31	--	--	800	μA
CH7 (WLED) in Current Source mode Supply Current into VDDM	I _{Q7c}	EN7_DIM7 [4:0] = 31	--	--	800	μA
Oscillator						
CH1, 2, 3, 4 Operation Frequency	f _{OSC}		1800	2000	2200	kHz
CH5, 6, 7 Operation Frequency	f _{OSC2}	CH7 in Step-Up Mode	900	1000	1100	kHz
CH1 Maximum Duty Cycle (Step-Up)		V _{FB1} = 0.75V	80	83	86	%
CH2 Maximum Duty Cycle (Step-Down)		V _{FB2} = 0.75V	--	--	100	%
CH3 Maximum Duty Cycle (Step-Down)		V _{FB3} = 0.75V	--	--	100	%
CH4 Maximum Duty Cycle (Step-Down)		V _{FB4} = 0.75V	--	--	100	%
CH5 Maximum Duty Cycle (Step-Up)		V _{FB5} = 1.15V	91	93	97	%
CH6 Maximum Duty Cycle (Inverting)		V _{FB6} = 0.7V	91	93	97	%
CH7 Maximum Duty Cycle (Step-Up)		V _{FB7} = 0.15V	91	93	97	%
Feedback, Output Regulation Voltage, and Output Regulation Current						
Feedback Regulation Voltage @ FB1, FB2, FB3, FB4			0.788	0.8	0.812	V
Feedback Regulation Voltage @ FB5			1.237	1.25	1.263	V
Feedback Regulation Voltage @ FB6 (Inverting)			0.58	0.6	0.62	V
Feedback Regulation Voltage @ FB7 (Step-Up mode and current source mode)		EN7_DIM7 [4:0] = 31	0.237	0.25	0.263	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference						
VREF Output Voltage	V _{REF}		1.77	1.8	1.83	V
(VREF-FB6) Regulation Voltage			1.182	1.2	1.218	V
VREF Load Regulation		0μA < IREF < 200μA	--	--	10	mV
Power Switch						
CH1 On Resistance of MOSFET		P-MOSFET, V _{PVD1} = 3.3V	--	200	300	mΩ
		N-MOSFET, V _{PVD1} = 3.3V	--	150	250	
CH1 Current Limitation (Step-Up)			2.2	3	4	A
CH2 On Resistance of MOSFET		P-MOSFET, V _{PVD2} = 3.3V	--	200	300	mΩ
		N-MOSFET, V _{PVD2} = 3.3V	--	150	250	
CH2 Current Limitation (Step-Down)			1.4	1.8	2.2	A
CH3 On Resistance of MOSFET		P-MOSFET, V _{PVD3} = 3.3V	--	300	400	mΩ
		N-MOSFET, V _{PVD3} = 3.3V	--	300	400	
CH3 Current Limitation (Step-Down)			1.2	1.6	2	A
CH4 On Resistance of MOSFET		P-MOSFET, V _{PVD4} = 3.3V	--	300	400	mΩ
		N-MOSFET, V _{PVD4} = 3.3V	--	300	400	
CH4 Current Limitation (Step-Down)			1.2	1.6	2	A
CH5 On Resistance of P-MOSFET		V _{PVD5} = 16V	--	1.1	1.5	Ω
CH5 On Resistance of N-MOSFET		V _{DDM} = 3.3V	--	0.6	0.8	Ω
CH5 Current Limitation (Step-Up)		N-MOSFET	0.9	1.2	1.6	A
CH6 On Resistance of MOSFET		P-MOSFET, V _{PVD6} = 3.3V	--	0.5	0.7	Ω
CH6 Current Limitation (Inverting)		P-MOSFET	1	1.5	2	A
CH7 On Resistance of P-MOSFET		V _{PVD7} = 10V	--	2.0	3.0	Ω
CH7 On Resistance of N-MOSFET		V _{DDM} = 3.3V	--	0.9	1.1	Ω
CH7 Current Limitation (Step-Up)		N-MOSFET	0.6	0.8	1	A
Protection						
Over Voltage Protection of PVD1			5.82	6.0	6.18	V
Over Voltage Protection of PVD5			20	22	24	V
Over Voltage Protection of VOUT6			--	-13	--	V
Over Voltage Protection of PVD7 (Step-Up mode)			14.2	15	16	V
CH1 Step-Up Under Voltage Protection of PVD1			--	V _{sys} - 0.8V	--	V
CH1/2/3/4 Under Voltage Protection		At V _{FBx} < 0.4V after soft-start ends	0.35	0.4	0.45	V
CH5 Under Voltage Protection		At V _{FB5} < 0.6V after soft-start ends	0.5	0.6	0.7	V
CH6 Under Voltage Protection		At V _{FB6} > 1.2V after soft-start end	1.1	1.2	1.3	V
CH1/2/3/4 Overload Protection		At V _{FBx} < 0.72V after fault delay (100ms)	0.65	0.7	0.75	V
CH5 Overload Protection		At V _{FB5} < 1.1V after fault delay (100ms)	1.05	1.1	1.15	V
CH6 Overload Protection		At V _{FB6} > 0.74V after fault delay (100ms)	0.69	0.74	0.79	V
Protection Fault Delay			--	100	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Control						
EN1234, TSSEL Input Voltage Threshold	Logic-High		1.3	--	--	V
	Logic-Low		--	--	0.4	
EN1234, TSSEL Sink Current			--	1	6	μA
Thermal Protection						
Thermal Shutdown	T _{SD}		--	155	--	°C
Thermal Shutdown Hysteresis	ΔT _{SD}		--	20	--	°C
RTC LDO						
Standby Current		V _{DDM} = 4.2V	--	3	6	μA
V _{OUT} (RTCPWR)		I _{OUT} = 0mA, V _{DDM} = 4.2V	3	3.05	3.1	V
Max Output Current (Current Limit)		V _{DDM} = 4.2V	60	130	200	mA
Dropout Voltage		I _{OUT} = 50mA	--	--	1000	mV
		I _{OUT} = 10mA	--	--	150	
		I _{OUT} = 3mA	--	--	60	
WAKE Up Detector						
WAKE Impulse High Duration	t _{WAKEUP}	V _{IN} or BAT plug in, RTCPWR = 3.05V	--	90	--	ms
WAKE Output	High Level	V _{WAKE_H} Source Current 0.5mA, RTCPWR = 3.05V	--	RTCPWR - 0.3	RTCPWR	V
	Low Level	V _{WAKE_L} Sink Current -0.5mA, RTCPWR = 3.05V	0	0.3	--	
V _{IN} Threshold to Wake Up		RTCPWR = 3.05V	3.6	3.8	4	V
BAT Threshold to Wake Up			--	3	--	V
BAT Threshold Hysteresis to Wake Up			--	200	--	mV

Charger Unit : (V_{IN} = 5V, V_{BAT} = 4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
V _{IN} Under Voltage Lockout Threshold	V _{UVLO}	V _{IN} = 0V to 5V	3.6	3.8	4	V
V _{IN} Under Voltage Lockout Hysteresis	ΔV _{UVLO}	V _{IN} = 5V to 0V	--	240	--	mV
V _{IN} Supply Current	I _{SUPPLY}	I _{SYS} = I _{BAT} = 0mA, ENCH = 1 (V _{BAT} > V _{REGx})	--	1	2	mA
		I _{SYS} = I _{BAT} = 0mA, ENCH = 0 (V _{BAT} > V _{REGx})	--	0.8	1.5	
V _{IN} Suspend Current	I _{USUS}	V _{IN} = 5V, USUS = 1	--	195	300	μA
V _{IN} - BAT VOS Rising	V _{OS_H}		--	200	300	mV
V _{IN} - BAT VOS Falling	V _{OS_L}		10	50	--	mV
Voltage Regulation						
System Regulation Voltage	V _{SYS}	I _{SYS} = 800mA	4.4	4.5	4.6	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Regulation Voltage	V _{REG1}	0 to 85°C, Loading = 20mA, when V _{SET} = 1	4.16	4.2	4.23	V
Battery Regulation Voltage	V _{REG2}	0 to 85°C, Loading = 20mA, when V _{SET} = 0	4.01	4.05	4.08	V
APPM Regulation Voltage	ΔV _{APPM}	V _{SYS} – V _{APPM}	120	200	280	mV
DPM Regulation Voltage	V _{DPM}	I _{SETL} = 0	4.3	4.4	4.5	V
VIN to SYS MOSFET On-Resistance		I _{VIN} = 1000mA	--	0.2	0.35	Ω
BAT to SYS MOSFET On-Resistance		V _{BAT} = 4.2V, I _{SYS} = 1A	--	0.05	0.1	Ω
Re-Charge Threshold	ΔV _{REGCHG}	Battery Regulation – Recharge Level	60	100	140	mV
Current Regulation						
ISETA Set Voltage (Fast Charge Phase)	V _{ISETA}	V _{BAT} = 4V, R _{ISETA} = 1kΩ	--	2	--	V
Charge Current Setting Range	I _{CHG}		100	--	1200	mA
Charge Current Accuracy1	I _{CHG1}	V _{BAT} = 4V, R _{ISETA} = 1kΩ I _{SET} = 1	570	600	630	mA
Charge Current Accuracy2	I _{CHG2}	V _{BAT} = 3.8V, R _{ISETA} = 1kΩ, I _{SET} = 0	285	300	315	mA
VIN Current Limit	I _{VIN}	I _{SETL} = 1 (1.5A Mode)	1.2	1.5	1.8	A
		I _{SETL} = 0, I _{SETU} = 1 (500mA Mode)	450	475	500	mA
		I _{SETL} = 0, I _{SETU} = 0 (100mA Mode)	90	95	100	
Pre-Charge						
BAT Pre-Charge Threshold	V _{PRECH}	BAT Falling	2.7	2.8	2.9	V
BAT Pre-Charge Threshold Hysteresis	ΔV _{PRECH}		--	200	--	mV
Pre-Charge Current	I _{CHG_PRE}	V _{BAT} = 2V	5	10	15	%
Charge Termination Detection						
Termination Current Ratio to Fast Charge (Except USB 100 Mode)	I _{TERM}	I _{SETL} = 0, I _{SETU} = 1 I _{SETL} = 1, I _{SETU} = X	5	10	15	%
Termination Current Ratio to Fast Charge (USB100 Mode)	I _{TERM2}	I _{SETL} = 0, I _{SETU} = 0	--	3.3	--	%
Login Input/Output						
CHG Pull Down Voltage	V _{CHG}	I _{CHG} = 5mA	--	200	--	mV
INT Pull Down Voltage	V _{INT}	I _{INT} = 5mA	--	200	--	mV
Protection						
Thermal Regulation	T _{REG}		--	125	--	°C
Thermal Shutdown Temperature	T _{SD}		--	155	--	°C
Thermal Shutdown Hysteresis	ΔT _{SD}		--	20	--	°C
Over Voltage Protection	V _{OVP}	V _{VIN} Rising	6.25	6.5	6.75	V
Over Voltage Protection Hysteresis	ΔV _{OVP}	V _{VIN} = 7V to 5V, V _{OVP} – ΔV _{OVP}	--	100	--	mV
Output Short Circuit Detection Threshold	V _{SHORT}	V _{BAT} – V _{SYS}	--	300	--	mV
Battery Installation Detection Threshold at TS		EN1234 = H	--	90	--	% of VP

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time						
Pre-Charge Fault Time	t _{PCHG}	TIMER [3:0] = 0100, (1/8 x t _{FCHG})	1800	2250	2700	s
Fast charge Fault Time	t _{FCHG}	TIMER [3:0] = 0100	14400	18000	21600	s
PGOOD Deglitch Time	t _{PGOOD}	Time measured from VIN : 0 to 5V 1μs rise-time to PGOOD = 1 in I ² C Register	--	1	--	s
Input Over Voltage Blanking Time	t _{OVP}		--	50	--	μs
Pre-Charge to Fast-Charge Deglitch Time	t _{PF}		--	25	--	ms
Fast-Charge to Pre-Charge Deglitch Time	t _{FP}		--	25	--	ms
Termination Deglitch Time	t _{TERMI}		--	25	--	ms
Recharge Deglitch Time	t _{RECHG}		--	100	--	ms
Input Power Loss to SYS LDO Turn-Off Delay Time	t _{NO_IN}		--	25	--	ms
Pack Temperature Fault Detection Deglitch Time	t _{TS}		--	25	--	ms
Short Circuit Deglitch Time	t _{SHORT}		--	250	--	μs
Short Circuit Recovery Time	t _{SHORT-R}		--	64	--	ms
Other						
VP Regulation Voltage	V _{VP}	V _{DDM} = 4.2V	3.234	3.3	3.366	V
VP Load Regulation	V _{VP}	VP Source Out 2mA	--	--	-0.1	V
VP Under Voltage Lockout Threshold		Falling Threshold	--	0.8	--	V
TS Battery Detect Threshold	V _{TS}		2.75	2.85	2.95	V
NTC						
Low Temperature Trip Point (0°C)	V _{COLD}	Rising Threshold when TSSEL = L (100k NTC)	73	74	75	% of VP
		Rising Threshold when TSSEL = H (10k NTC)	59	60	61	
Low Temperature Trip Point Hysteresis (near 0°C)	ΔV _{COLD}		--	1	--	% of VP
High Temperature Trip Point (60°C)	V _{HOT}	Falling Threshold when TSSEL = L	27	28	29	% of VP
		Falling Threshold when TSSEL = H	37	38	39	
High Temperature Trip Point Hysteresis (near 60°C)	ΔV _{HOT}		--	1	--	% of VP
Low Temperature Trip Point (10°C) for JEITA		Rising Threshold when TSSEL = L (100k NTC)	63	64	65	% of VP
		Rising Threshold when TSSEL = H (10k NTC)	53	54	55	
Low Temperature Trip Point Hysteresis (near 10°C) for JEITA			--	1	--	% of VP
High Temperature Trip Point (45°C) for JEITA		Falling Threshold when TSSEL = L	34	35	36	% of VP
		Falling Threshold when TSSEL = H	39	40	41	
High Temperature Trip Point Hysteresis (near 45°C) for JEITA			--	1	--	% of VP

(V_{DDM} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Inputs (SDA SCL)							
SDA, SCL Input Threshold Voltage	Logic-High			2.0	--	--	V
	Logic-Low			--	--	0.8	
I²C Timing Characteristics							
SCL Clock Rate	f _{SCL}	V _{DDM} = 3.3V		--	--	400	kHz
Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated	t _{HD;STA}			0.6	--	--	μs
LOW Period of SCL Clock	t _{LOW}			1.3	--	--	μs
HIGH Period of SCL Clock	t _{HIGH}			0.6	--	--	μs
Set-up Time for Repeated START Condition	t _{SU;STA}			0.6	--	--	μs
Data Hold Time	t _{HD;DAT}			0	--	0.9	μs
Data Set-up Time	t _{SU;DAT}			100	--	--	ns
Set-up Time for STOP Condition	t _{SU;STO}			0.6	--	--	μs
Bus Free Time between a STOP and START Condition	t _{BUF}			1.3	--	--	μs
Rise Time of both SDA and SCL Signals	t _R			20	--	300	ns
Fall Time of both SDA and SCL Signals	t _F			20	--	300	ns
SDA and SCL Output Low Sink Current	I _{OL}	SDA or SCL Voltage = 0.4V		2	--	--	mA

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

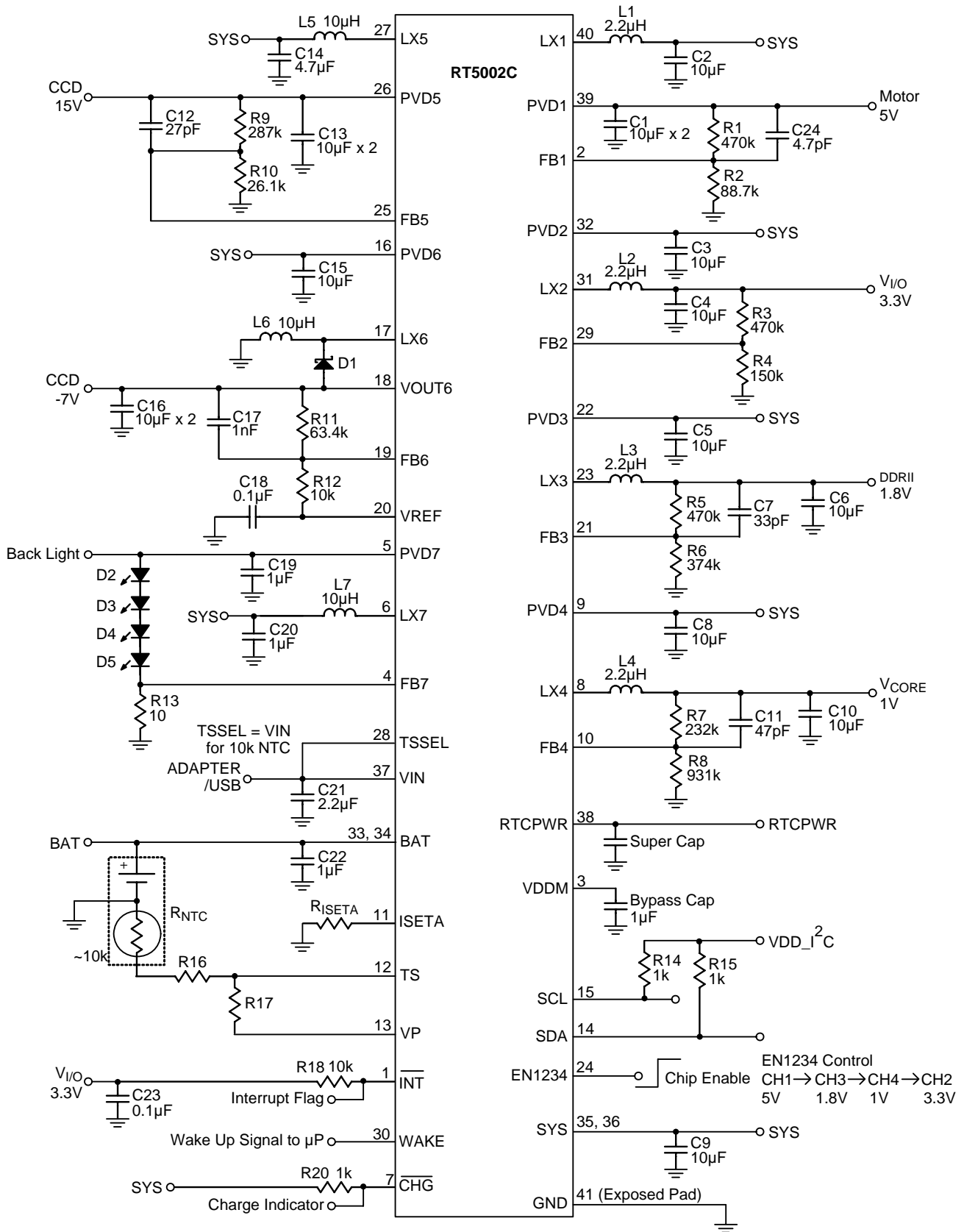
Note 2. Guaranteed by design.

Note 3. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

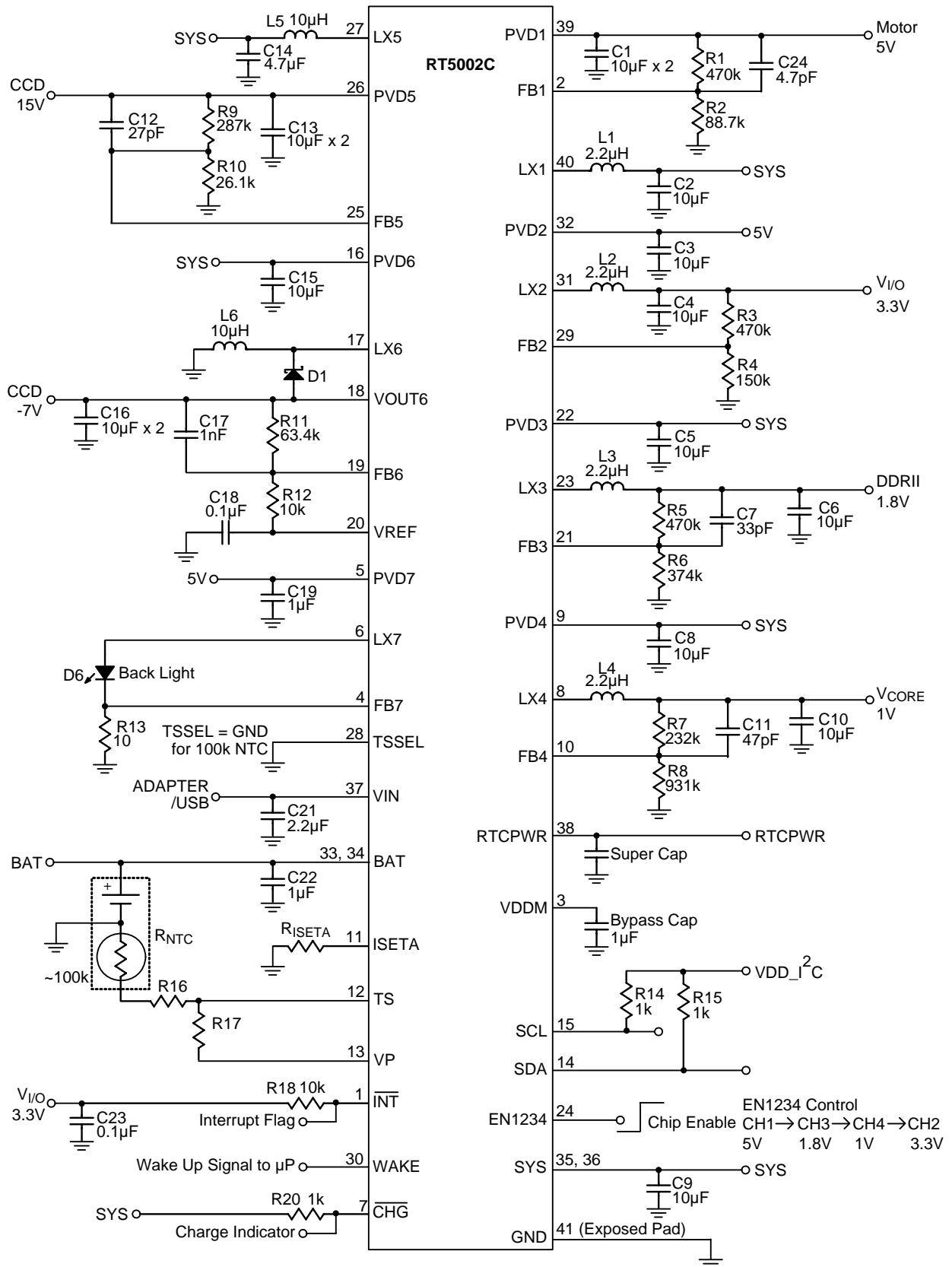
Note 4. Devices are ESD sensitive. Handling precaution is recommended.

Note 5. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit
For 4-LED Application

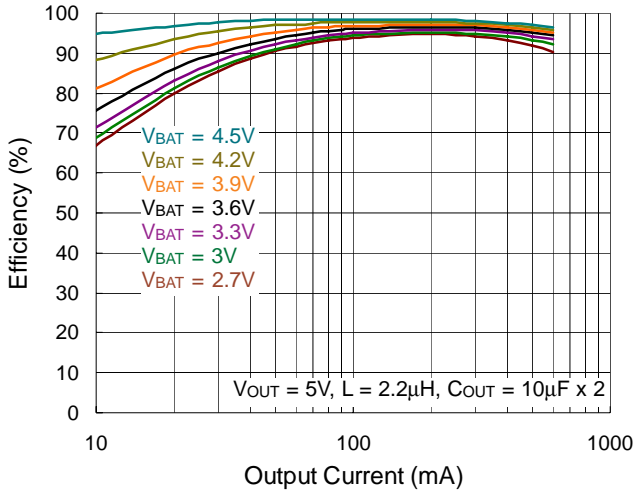


For 1-LED Application

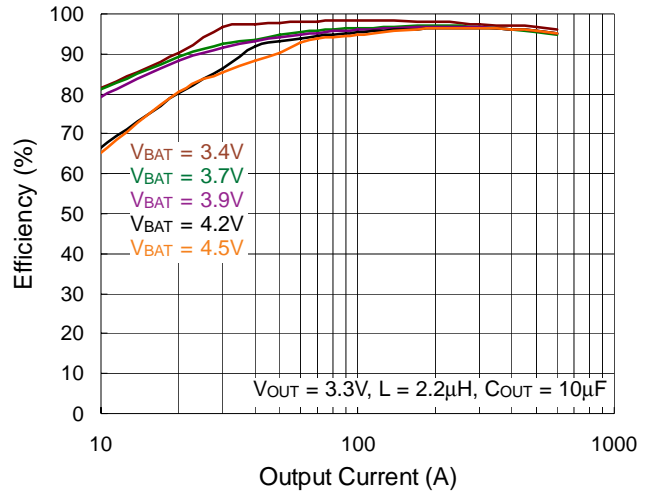


Typical Operating Characteristics

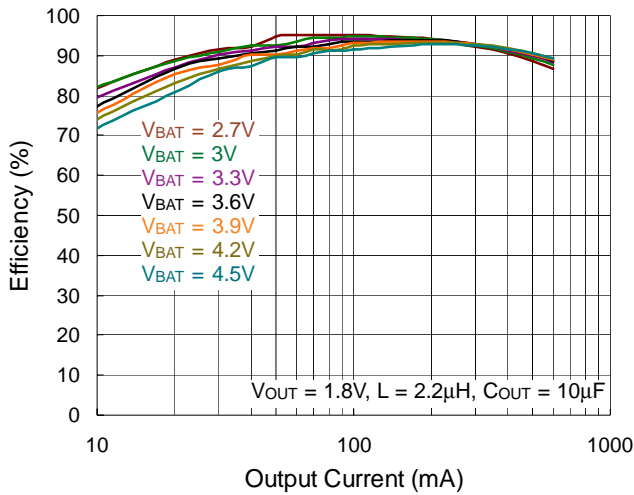
CH1 Step-Up Efficiency vs. Output Current



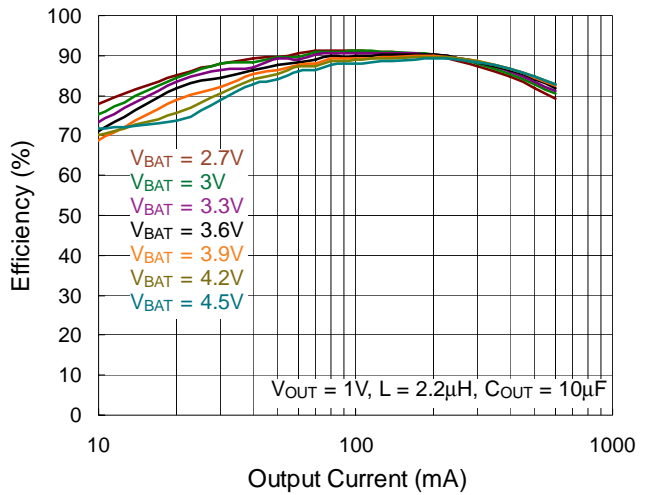
CH2 Step-Down Efficiency vs. Output Current



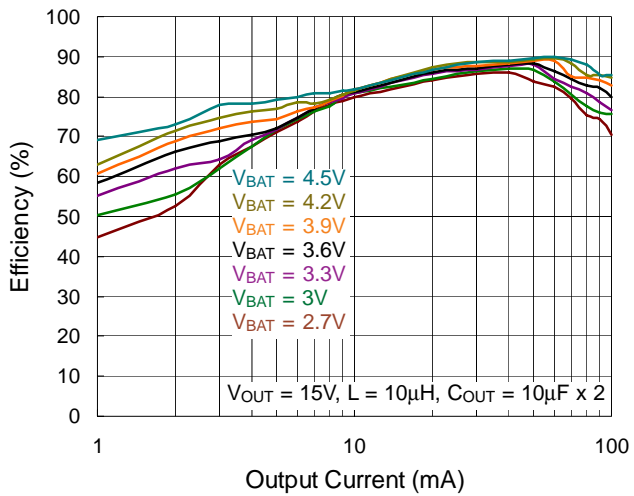
CH3 Step-Down Efficiency vs. Output Current



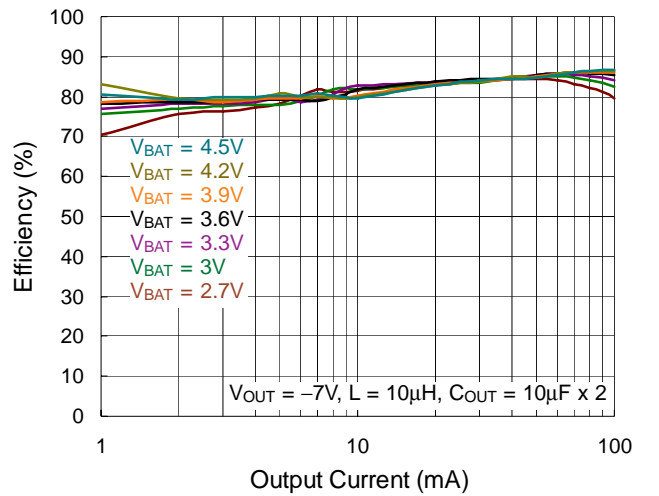
CH4 Step-Down Efficiency vs. Output Current



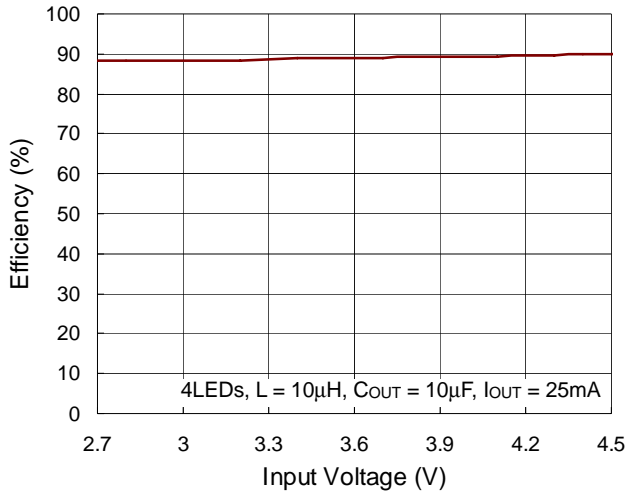
CH5 Step-Up Efficiency vs. Output Current



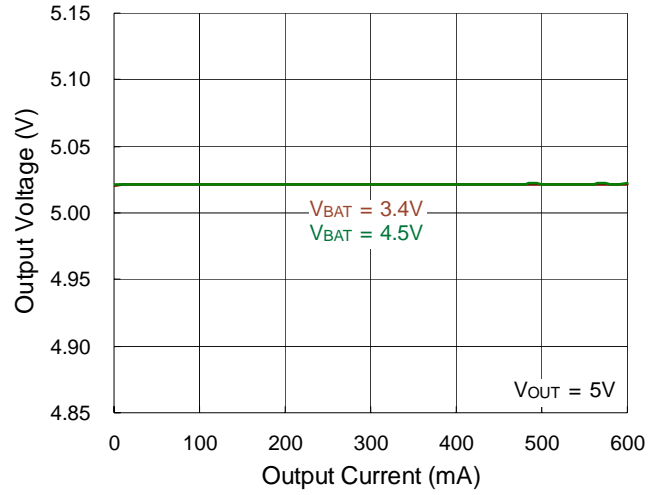
CH6 Inverting Efficiency vs. Output Current



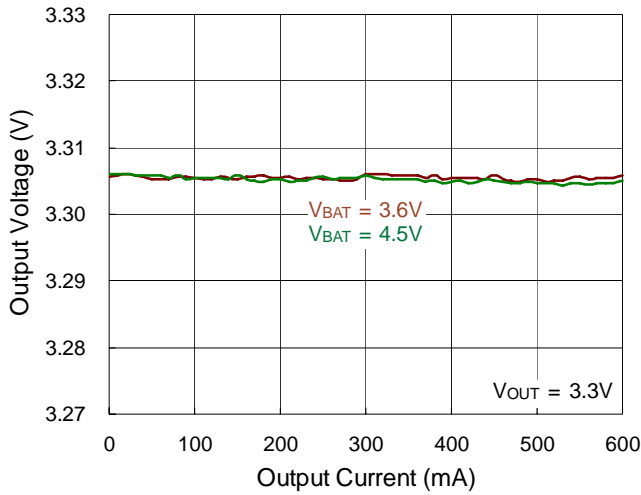
CH7 Efficiency vs. Input Voltage



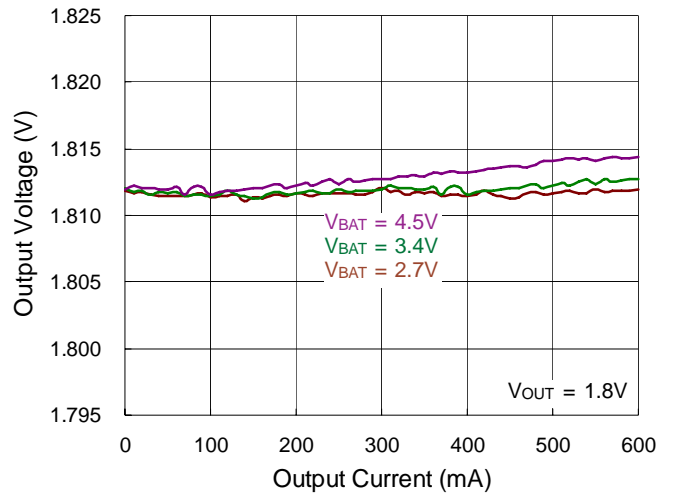
CH1 Step-Up Output Voltage vs. Output Current



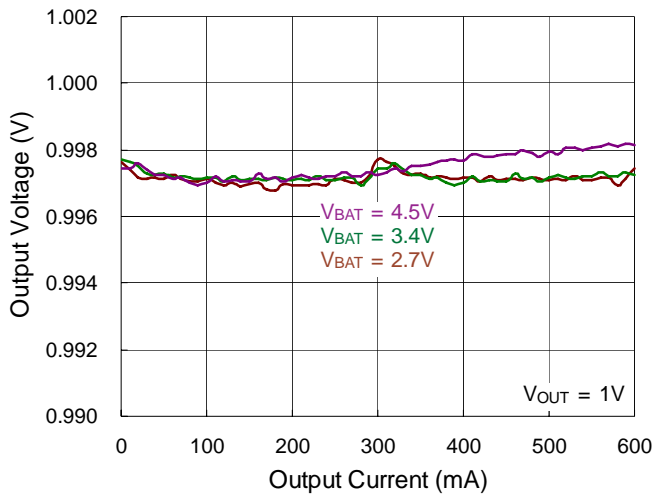
CH2 Step-Down Output Voltage vs. Output Current



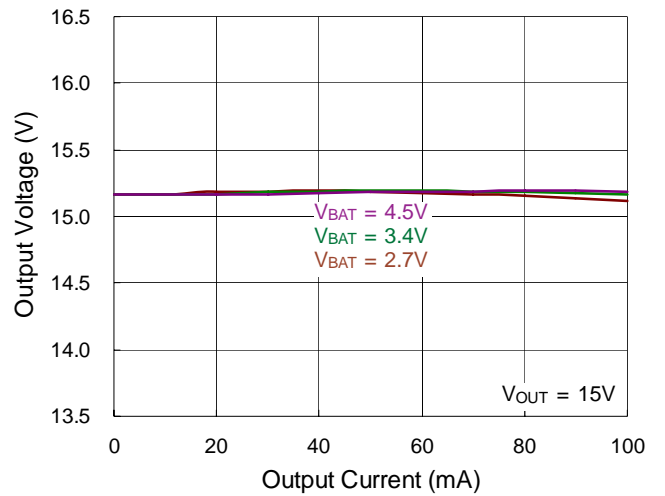
CH3 Step-Down Output Voltage vs. Output Current



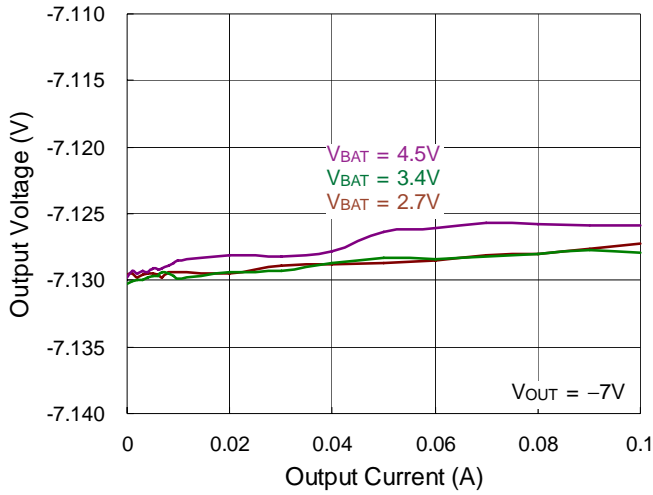
CH4 Step-Down Output Voltage vs. Output Current



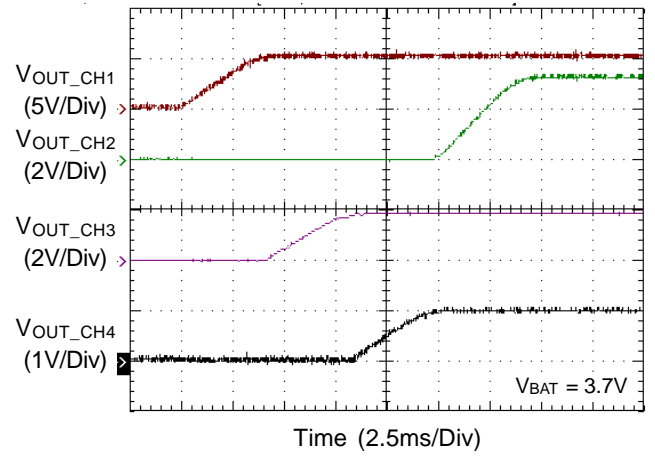
CH5 Step-Up Output Voltage vs. Output Current



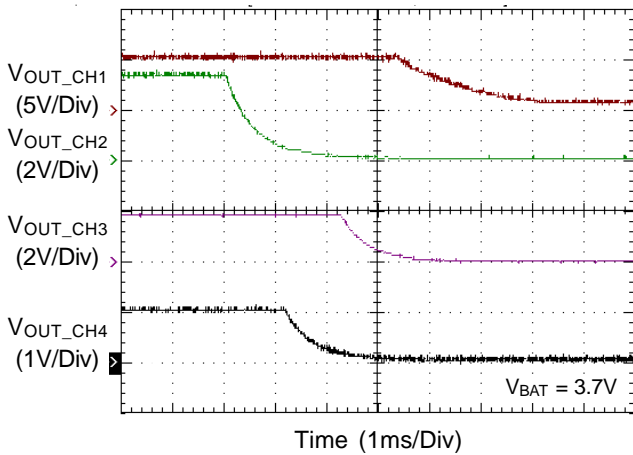
CH6 Inverting Output Voltage vs. Output Current



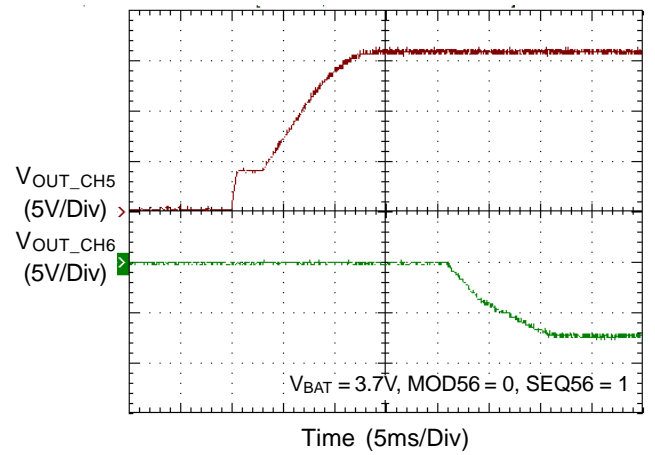
Power On Sequence



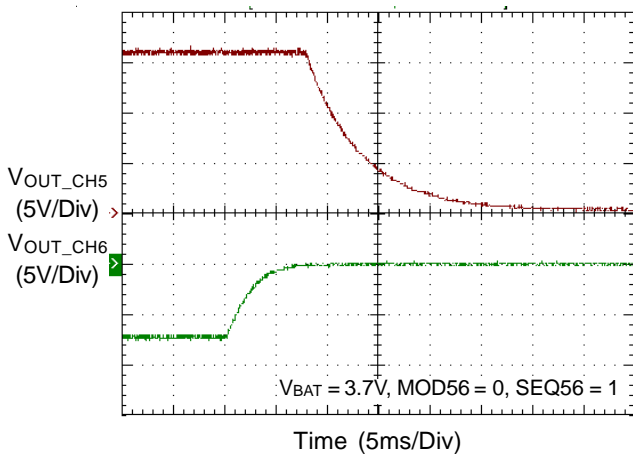
Power Off Sequence



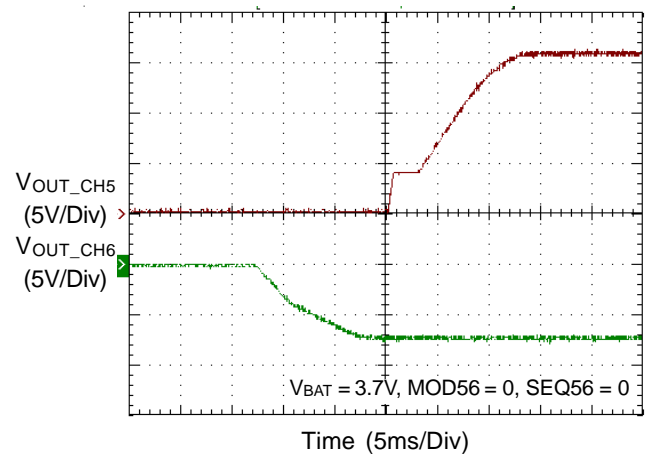
Power On Sequence



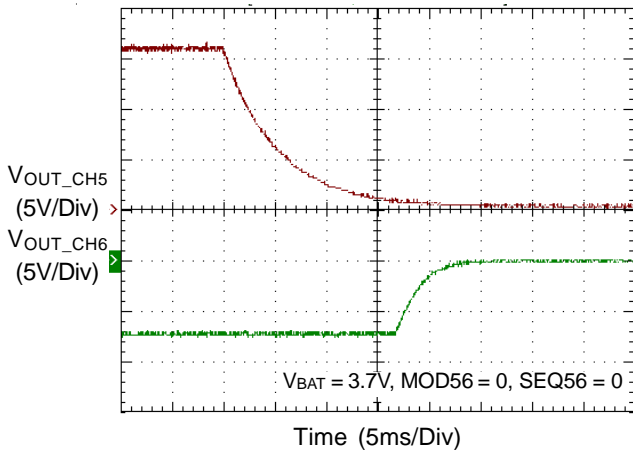
Power Off Sequence



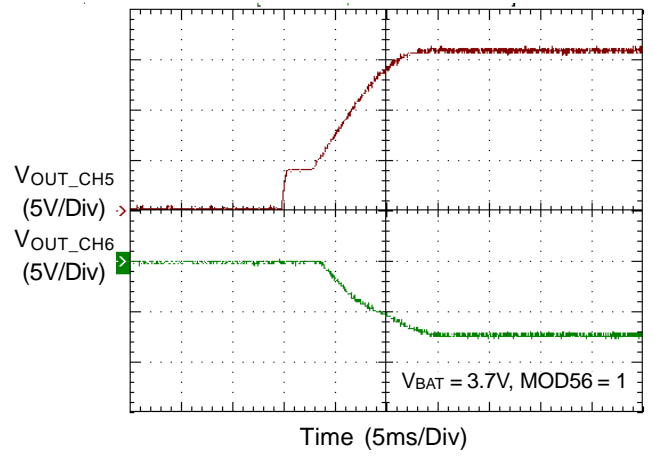
Power On Sequence



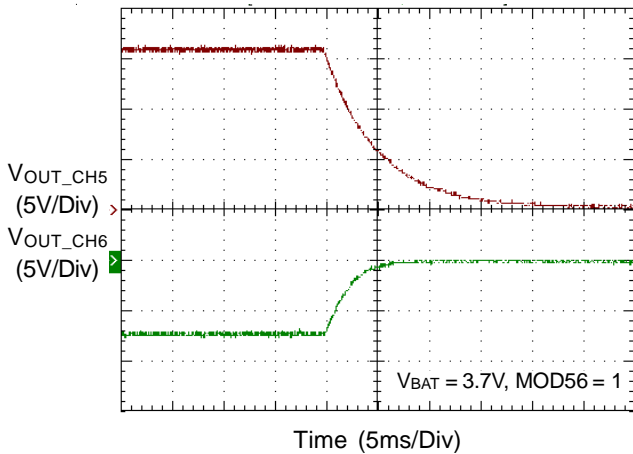
Power Off Sequence



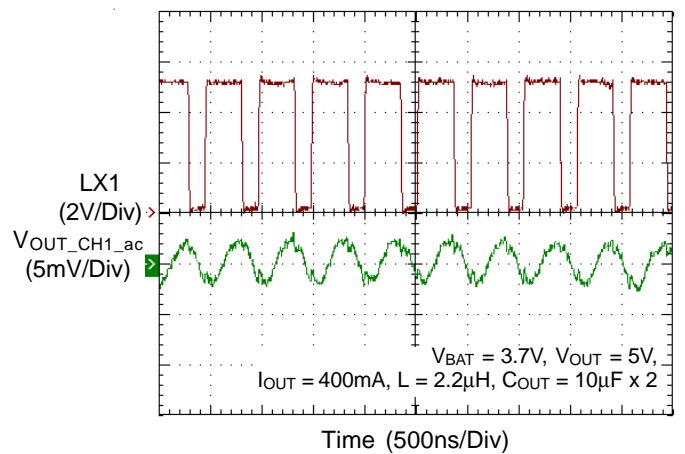
Power On Sequence



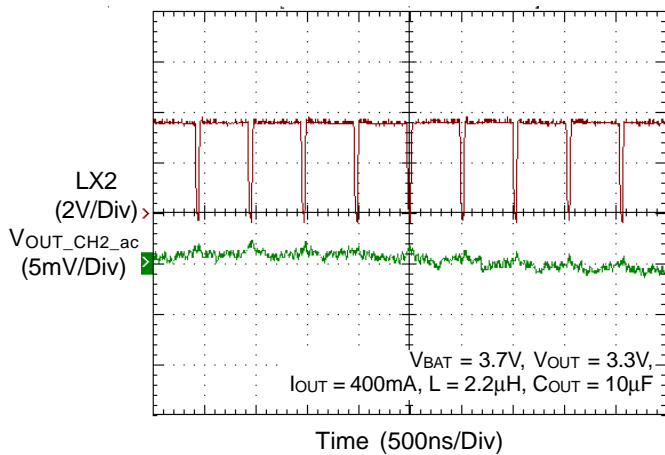
Power Off Sequence



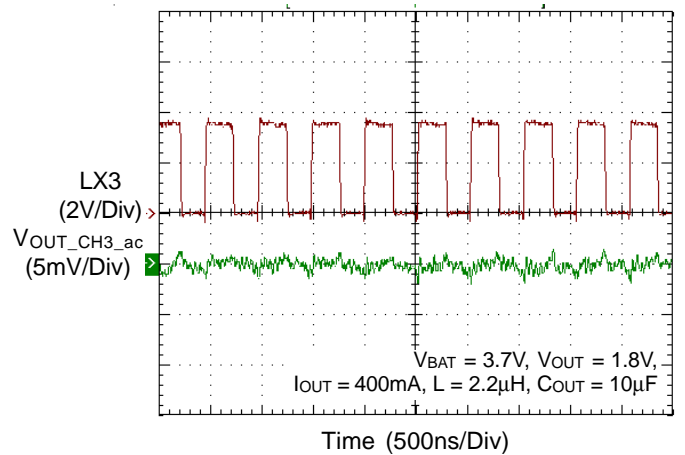
CH1 Output Voltage Ripple



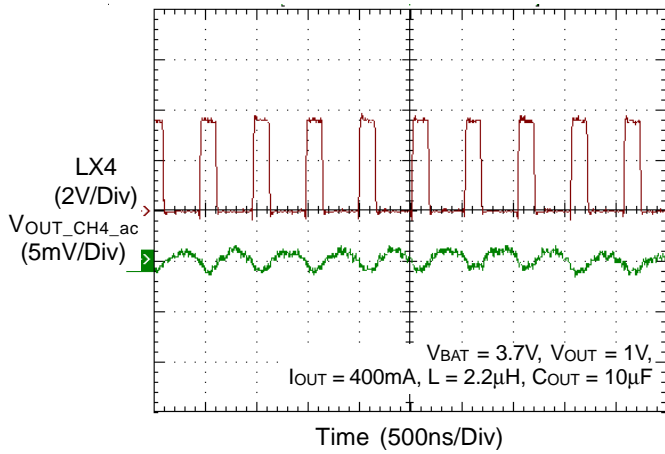
CH2 Output Voltage Ripple



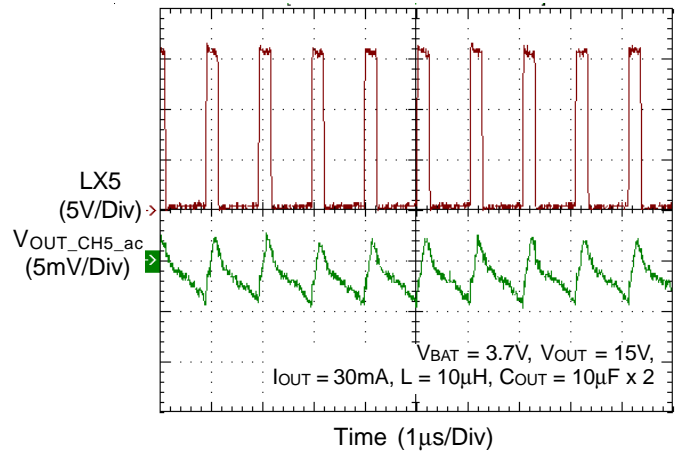
CH3 Output Voltage Ripple



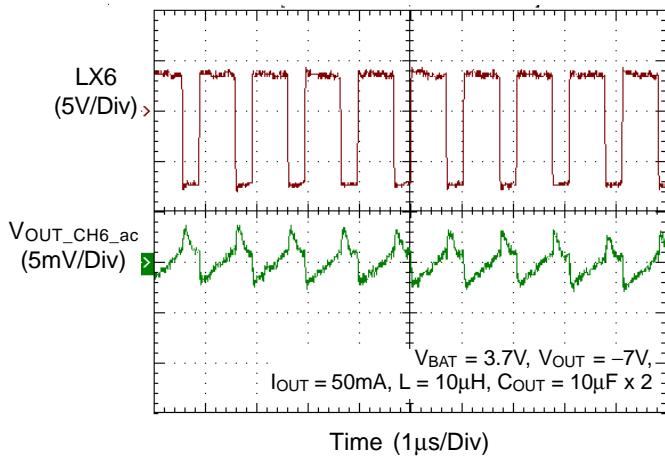
CH4 Output Voltage Ripple



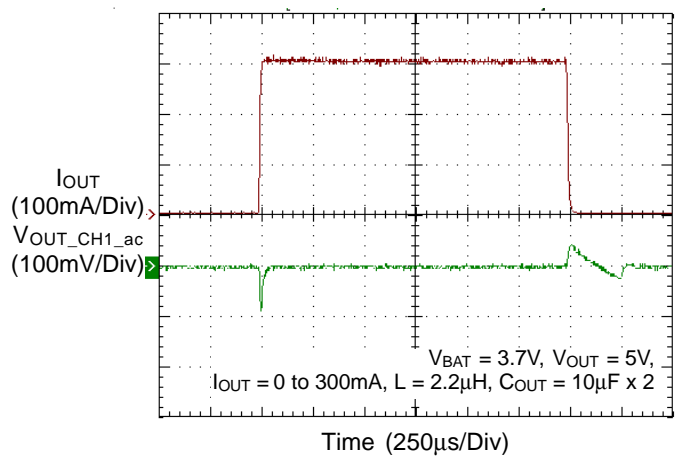
CH5 Output Voltage Ripple



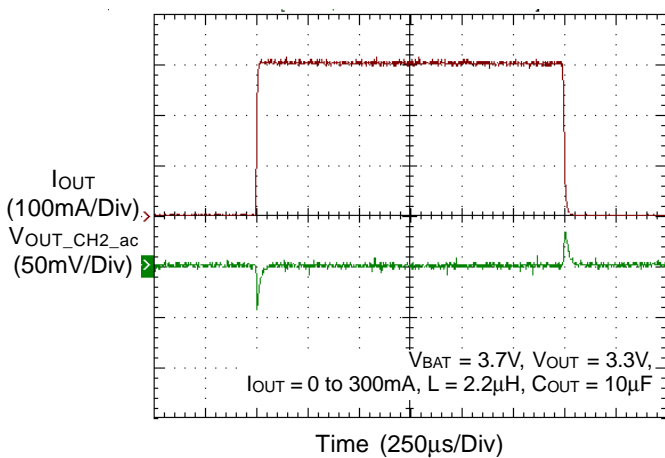
CH6 Output Voltage Ripple



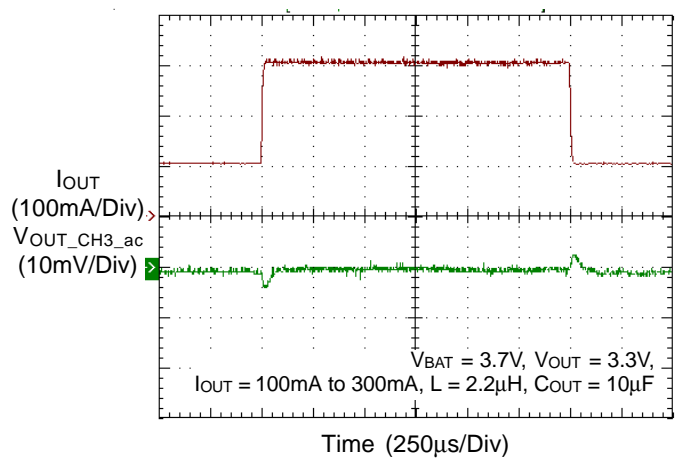
CH1 Load Transient Response



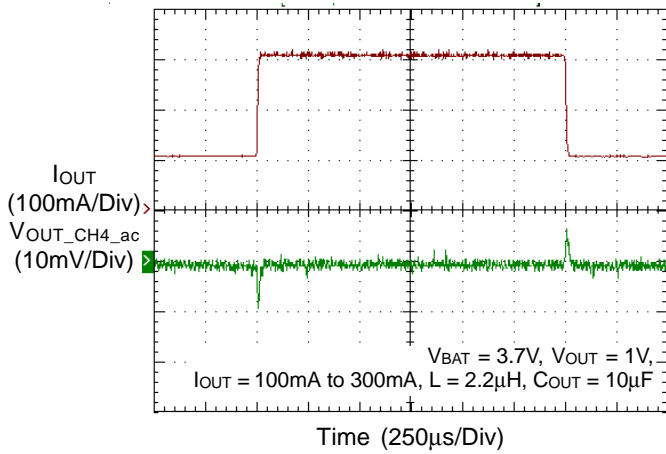
CH2 Load Transient Response



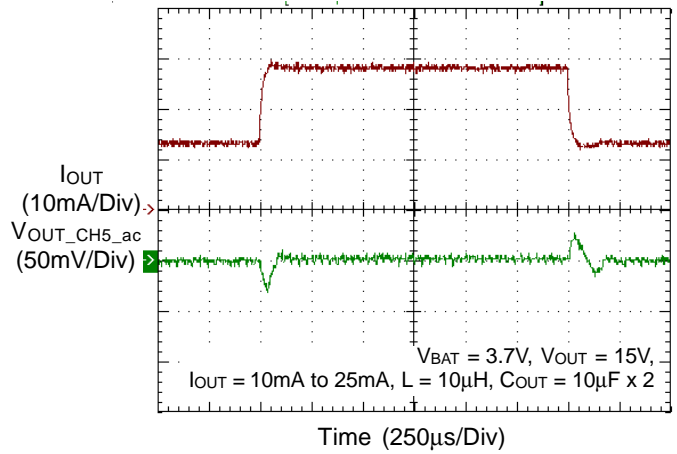
CH3 Load Transient Response



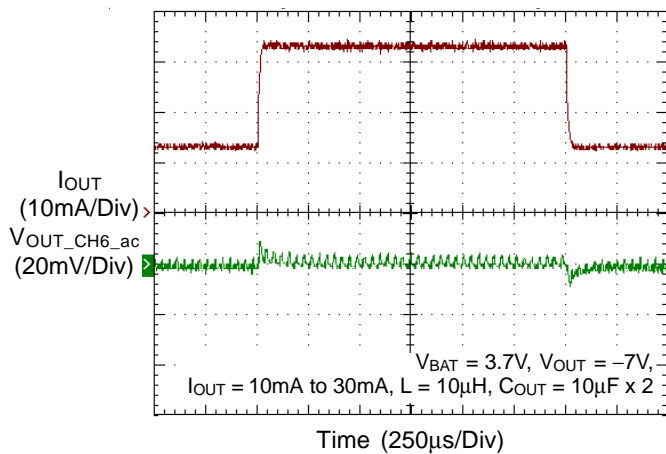
CH4 Load Transient Response



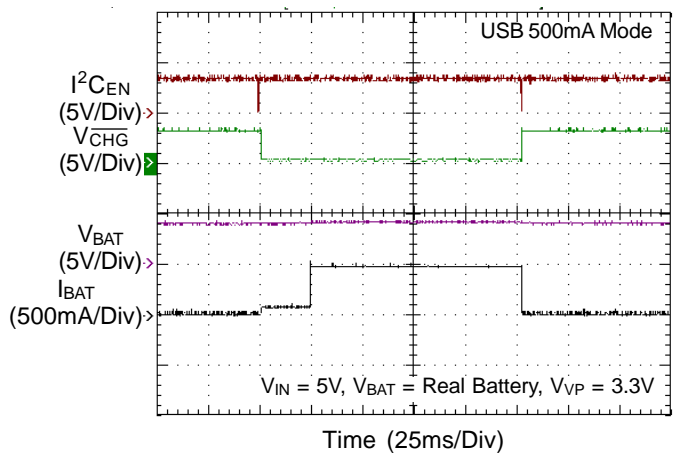
CH5 Load Transient Response



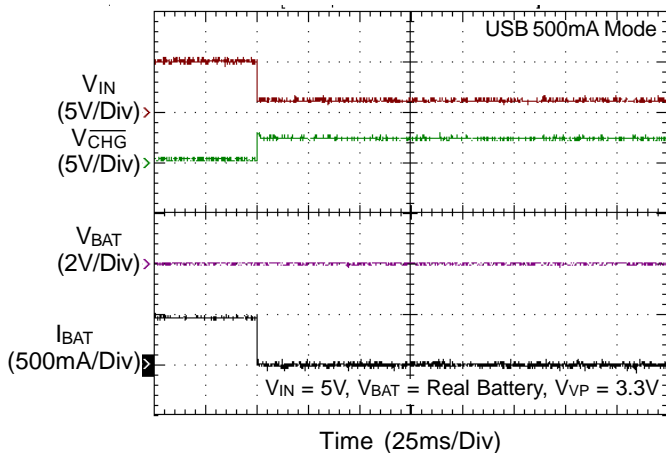
CH6 Load Transient Response



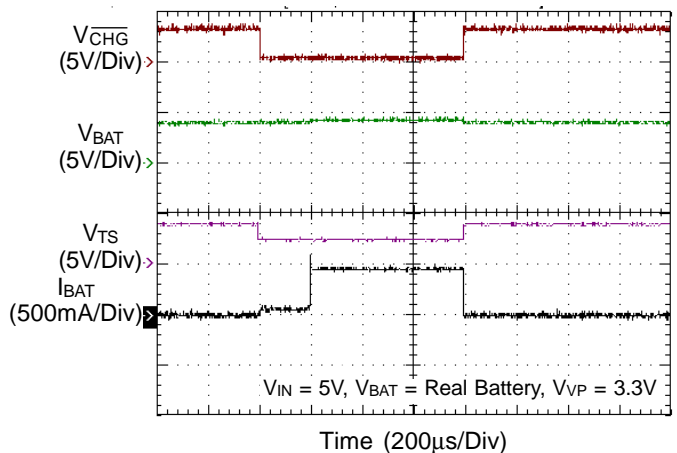
Charge On/Off Control from EN



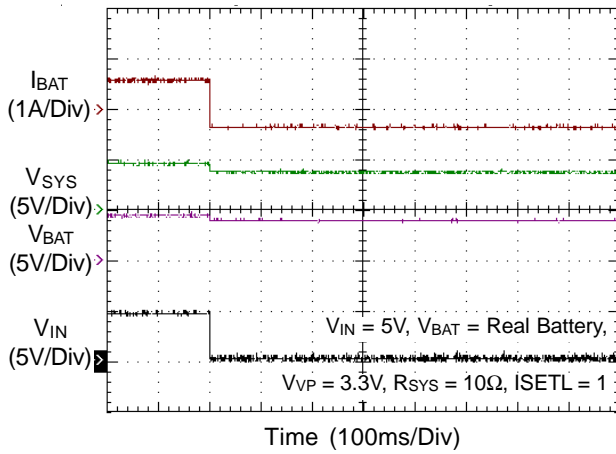
Charge On/Off Control from VIN



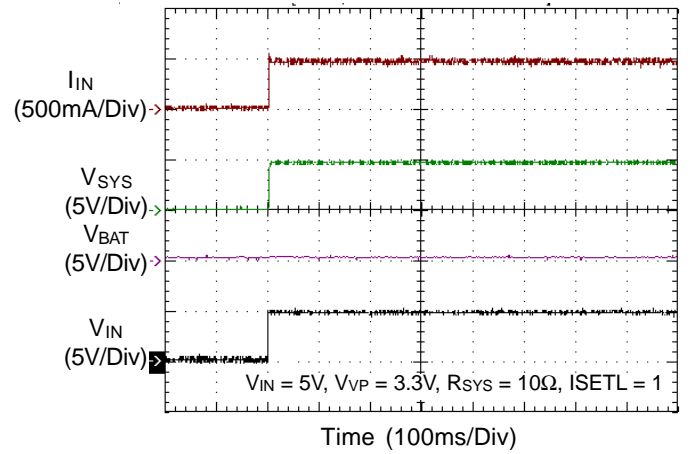
TS Inserted/Removed



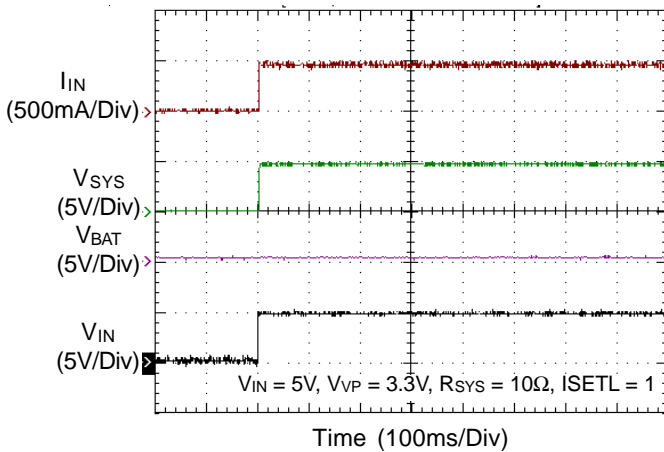
V_{IN} Removal



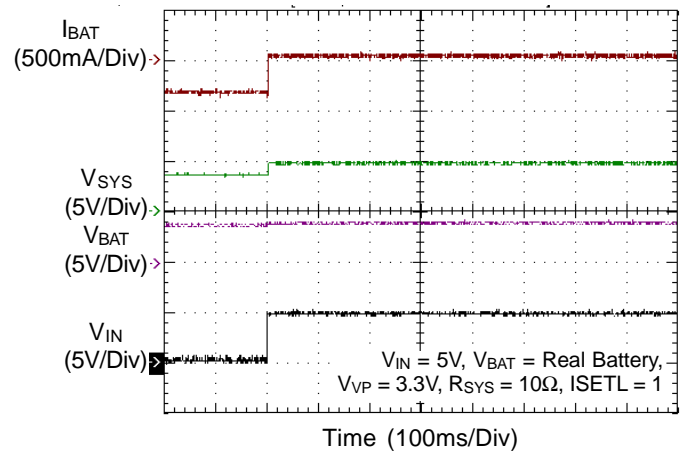
V_{IN} Hot-Plug with NTC/without Battery



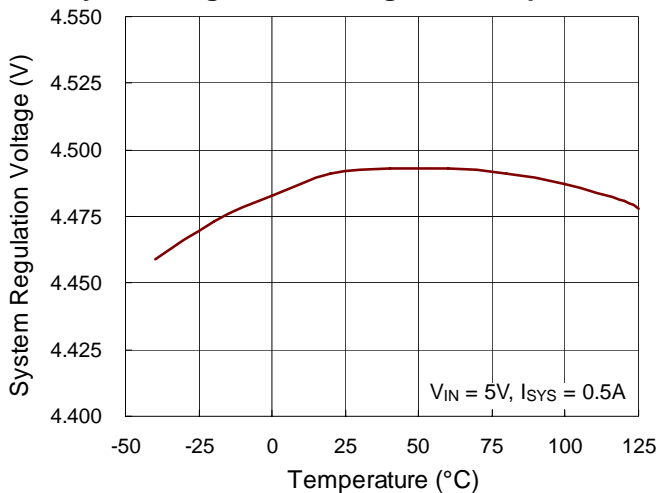
V_{IN} Hot-Plug without NTC/Battery



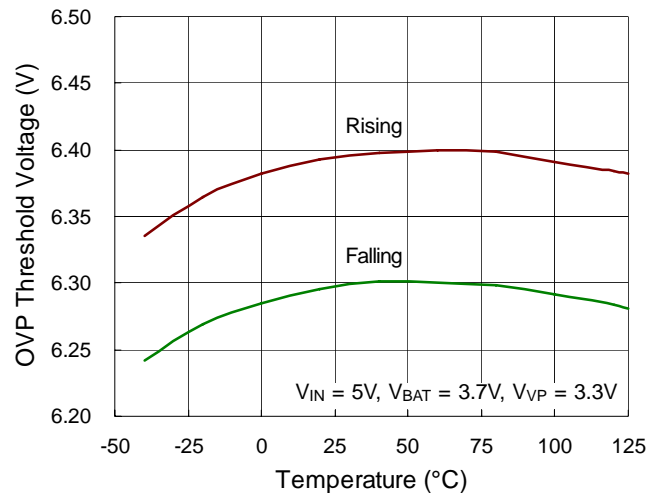
V_{IN} Hot-Plug with Battery



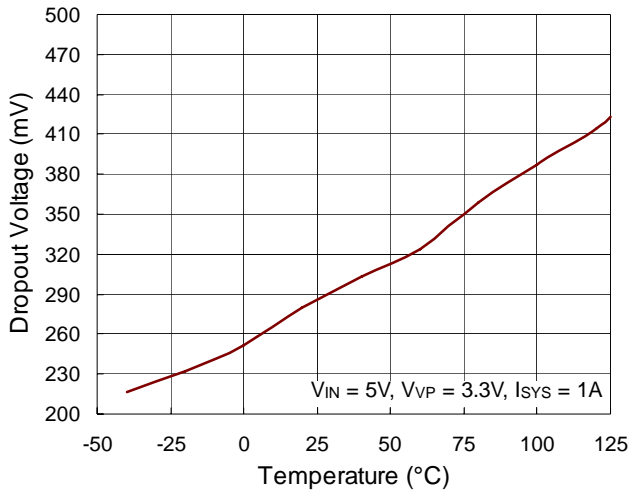
System Regulation Voltage vs. Temperature



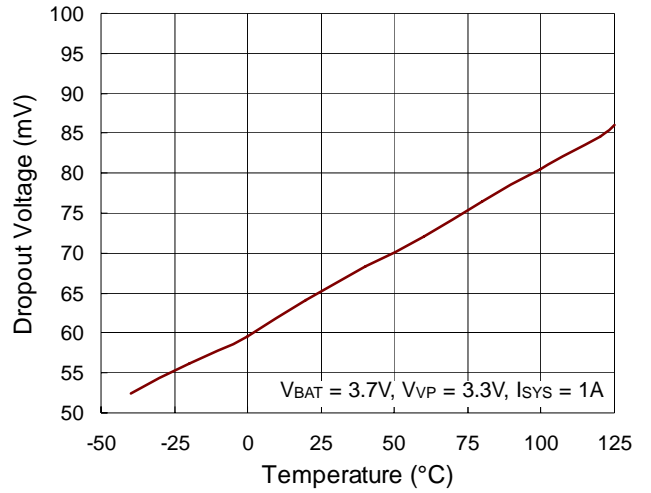
OVP Threshold Voltage vs. Temperature



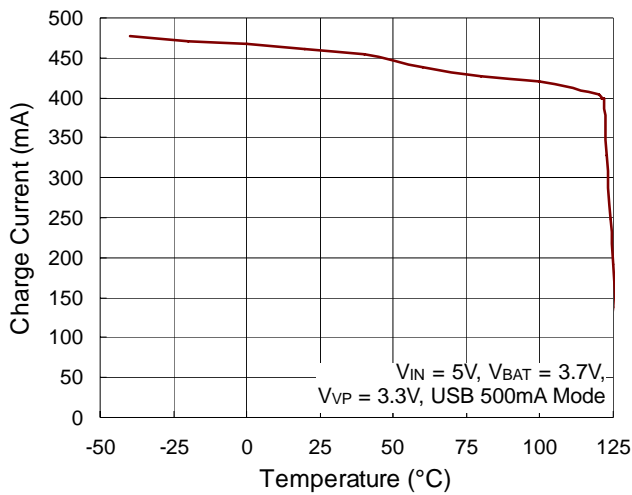
$V_{IN} - V_{SYS}$ Dropout Voltage vs. Temperature



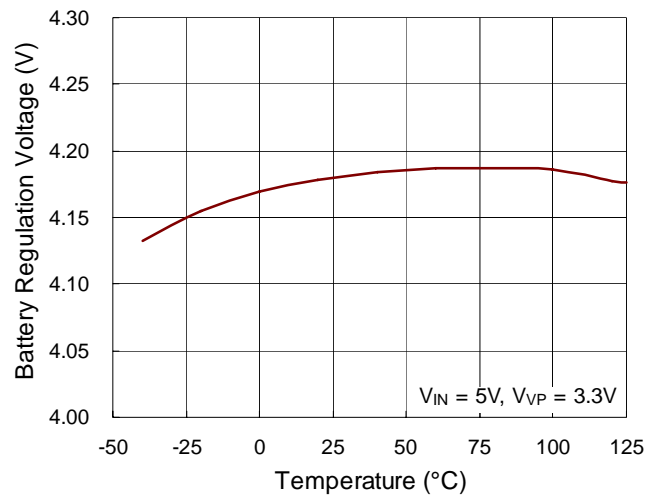
$V_{BAT} - V_{SYS}$ Dropout Voltage vs. Temperature



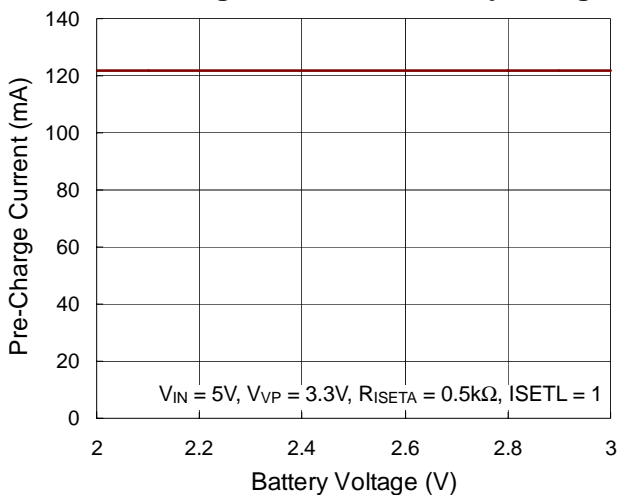
I_{CHG} Thermal Regulation vs. Temperature



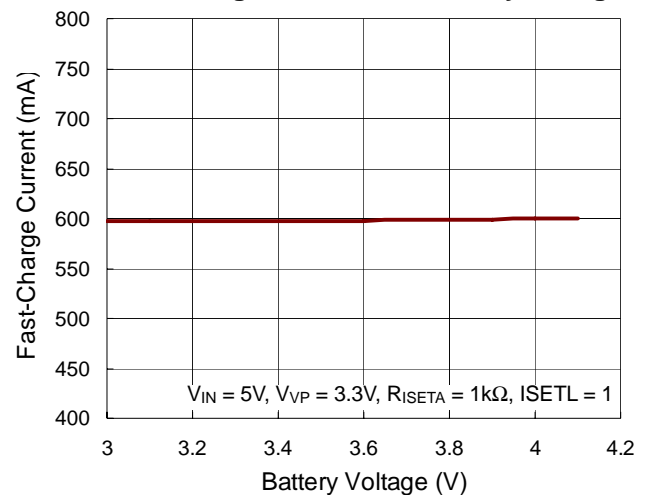
Battery Regulation Voltage vs. Temperature



Pre-Charge Current vs. Battery Voltage



Fast-Charge Current vs. Battery Voltage



Application Information

Power Converter Unit

The RT5002C is an integrated power system for digital still cameras and other small handheld devices. It includes six DC/DC converters as well as one WLED driver, one RTC LDO, and a fully integrated single-cell Li-ion battery charger ideal for portable applications.

CH1 : Step-up synchronous current mode DC/DC converter with internal power MOSFETs and compensation network. The P-MOSFET body can be controlled to disconnect the load. It is suitable for providing power to the motor.

CH2 to CH4 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs and compensation network. These channels supply the power for I/O, DRAM, and core. They can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple.

CH5 : High voltage step-up synchronous current mode DC/DC converter with internal power MOSFET and compensation network. The P-MOSFET body can be controlled to disconnect the load. This channel supplies the CCD+ bias.

CH6 : Asynchronous inverting current mode DC/DC converter with internal power MOSFET and compensation network. An external Schottky diode is required. This channel supplies the CCD- bias.

CH7 : WLED driver operating in either current source mode or synchronous step-up mode with internal power MOSFET and compensation network. The operation mode is determined via LX7 detection. The P-MOSFET body in step-up mode can be controlled to disconnect the load.

CH1 to CH4 operate in PWM mode with 2MHz, while CH5 to CH7 operate in PWM mode with 1MHz switching frequency.

RTC_LDO : 3.05V output LDO with low quiescent current and reverse leakage prevention from output node.

Output Voltage Design Equation of CH1 to CH4 :

The output voltage can be set by the following equation :

$$V_{OUT} = (1 + R_H / R_L) \times V_{FB}$$

where VFB is 0.8V typically, R_H is R1, R3, R5, and R7 respectively for CH1 to 4, and R_L is R2, R4, R6, and R8 respectively for CH1 to 4.

Output Voltage Design Equation of CH5 :

The output voltage can be set by the following equation:

$$V_{OUT_CH5} = (1 + R9 / R10) \times V_{FB5}$$

where V_{FB5} is 1.25V typically.

Output Voltage Design Equation of CH6 :

The output voltage can be set by the following equation :

$$V_{OUT_CH6} = -(R11 / R12) \times (1.2V) + 0.6V$$

where R11 and R12 are the feedback resistors connected to FB6, 1.2V equals to (V_{REF} – V_{FB6}), and 0.6V is the typical value of V_{FB6}.

Reference Voltage

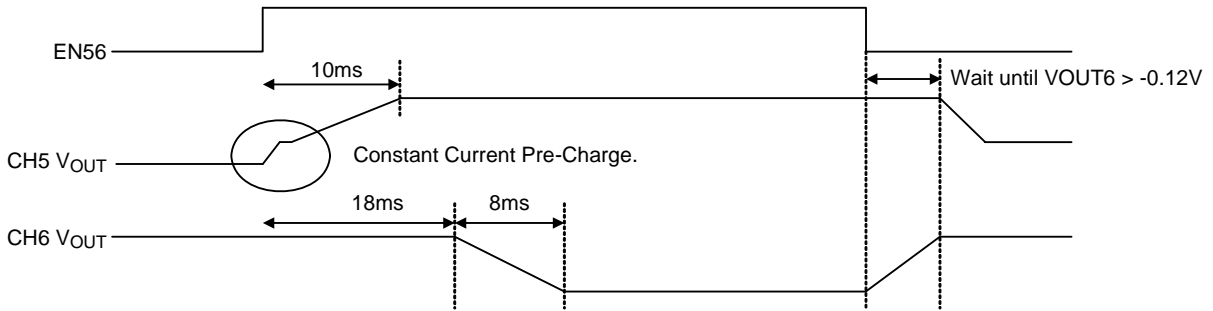
The RT5002C provides a precise 1.8V reference voltage, V_{REF}, with sourcing capability of 100µA. Connect a 0.1µF ceramic capacitor from the V_{REF} pin to GND. Reference voltage is enabled by I²C register bit EN56 = 1. Furthermore, this reference voltage is internally pulled to GND at shutdown.

CH5 and CH6 Power Sequence :

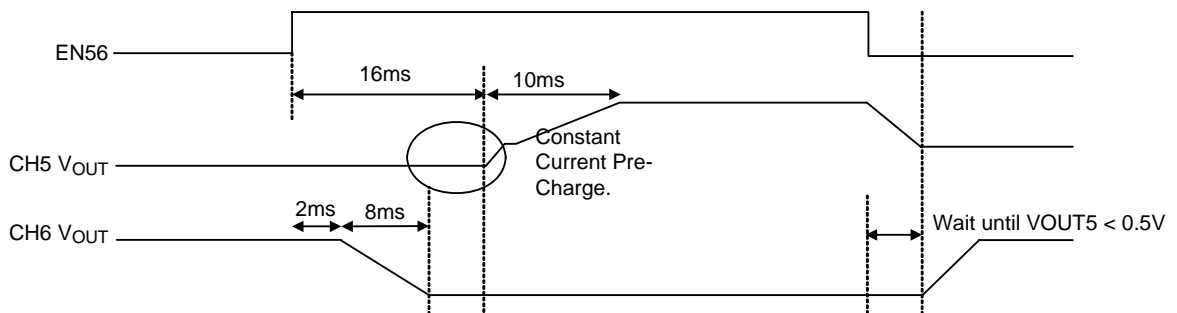
CH5 and CH6 are enabled together via I²C interface and their power on sequence can be chosen via I²C register setting as following table.

MOD56	SEQ56	Power On	Power Off
0	0	CH6 → CH5	CH5 → CH6
0	1	CH5 → CH6	CH6 → CH5
1	X	Same Time	Same Time

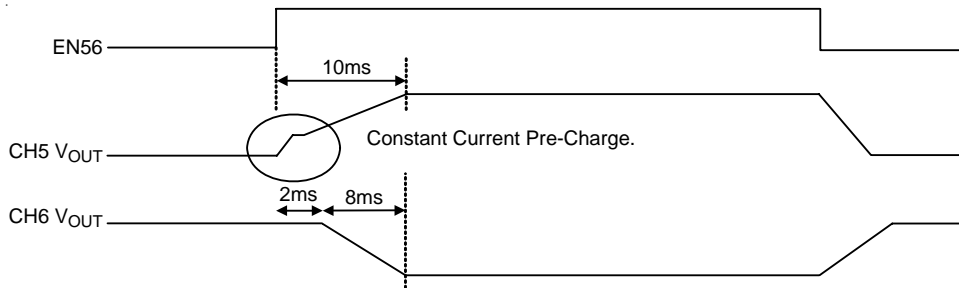
EN56 (MOD56 = 0, SEQ56 = 1)



EN56 (MOD56 = 0, SEQ56 = 0)



EN56 (MOD56 = 1, SEQ56 = X)



CH7 : WLED Driver

CH7 is a WLED driver that can operate in either current source mode or synchronous step-up mode, as determined by LX7 detection. When CH7 works in current source mode, it sources an LED current out of LX7 pin and regulates the current by FB7 voltage. The LED current is defined by the FB7 voltage as well as the external resistor between FB7 and GND. The FB7 regulation voltage can

be set in 31 steps from 8mV to 250mV, typically, via I²C interface. If CH7 works in synchronous step-up mode, it integrates synchronous step-up mode with an internal MOSFET and internal compensation to output a voltage up to 15V. The LED current is also set via an external resistor and FB7 regulation voltage.

Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x0	Meaning	MOD56	SEQ56	EN56	EN7_DIM7 [4:0]				
	Default	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MOD56	1	CH5/6 power on/off sequence at the same time
	0	CH5/6 power sequence is determined by SEQ56

SEQ56	1	CH5/6 power on sequence is CH5 → CH6, power off sequence is CH6 → CH5
	0	CH5/6 power on sequence is CH6 → CH5, power off sequence is CH5 → CH6

EN56	1	Enable (turn on) CH5 and CH6 by preset sequence
	0	Disable (turn off) CH5 and CH6 by preset

Enable CH7 and define FB7 regulation voltage

EN7_DIM7 [4:0]	00000	Ch7 turn off
	00001 to 11111	Ch7 turn on and dimming ratio : $V_{FB7} = EN7_DIM7 [4:0] / 31 \times 0.25V$

CH7 WLED Current Dimming Control

If CH7 is in synchronous step-up mode or current source mode, the WLED current is set by an external resistor. Regardless of the mode, dimming is always controlled by the I²C interface.

The WLED current can be set by the following equations :

$$I_{LED} \text{ (mA)} = [250\text{mV} / R \text{ (}\Omega\text{)}] \times EN7_DIM7 [4:0] / 31$$

where R is the current sense resistor from FB7 to GND and EN7_DIM7 [4:0] / 31 ratio refers to the I²C control register file. It is recommended that CH7 input power connects to the node SYS in order to prevent abnormal CH7 start-up.

VDDM Bootstrap

To support bootstrap function, the RT5002C includes a power selection circuit which selects between SYS and PVD1 to create the internal node voltage VDDI and VDDM.

VDDM is the power of the RT5002C PMU control circuits which must be connected to an external decoupling capacitor by way of the VDDM pin. VDDI is the power input of the RTC LDO. The output PVD1 of CH1 can bootstrap VDDM and VDDI. The RT5002C includes UVLO circuits to monitor VDDM and SYS voltage status.

RTC LDO

The RT5002C provides a 3.05V output LDO for real-time clock. The LDO features low quiescent current (3μA) and high output voltage accuracy. This LDO is always on, even when the system is shut down. For better stability, it is recommended to connect a 0.1μF capacitor to the RTCPWR pin. The RTC LDO includes pass transistor body diode control to avoid the RTCPWR node from back-charging into the input node VDDI.

Power On/Off Sequence for CH1 to CH4

EN1234 will turn on/off CH1 to CH4 in preset sequence.

CH1 to CH4 Power on Sequence is :

When EN1234 goes high, CH1 will turn on first. 3.5ms after CH1 is turned on, CH3 will turn on. 3.5ms after CH3 is turned on, CH4 will turn on. 3.5ms after CH4 is turned on, CH2 will turn on.

CH1 to CH4 Power off Sequence is :

When EN1234 goes low, CH2 will turn off first and internally discharge output. When $FB2 < 0.1V$, CH4 will turn off and also internally discharge output via the LX4 pin. When $FB4 < 0.1V$, CH3 will turn off and internally discharge output via the LX3 pin. Likewise, when $FB3 < 0.1V$, CH1 will turn off and discharge output. After $FB1 < 0.1V$, CH1 to 4 shutdown sequence will be completed.

Charger Unit

The RT5002C includes a Li-ion battery charger with Automatic Power Path Management. The charger is designed to operate in below modes :

Pre-charge Mode

When the output voltage is lower than 2.8V, the charging current will be reduced to a fast-charge current ratio set by R_{ISETA} to protect the battery life-time.

Fast-charge Mode

When the output voltage is higher than 3V, the charging current will be equal to the fast-charge current set by R_{ISETA}.

Constant Voltage Mode

When the output voltage is near 4.2V and the charging current falls below the termination current, after a deglitch time check of 25ms, the charger will become disabled and $\overline{\text{CHG}}$ will go from L to H.

Re-charge Mode

When the chip is in charge termination mode, the charging current gradually goes down to zero. However, once the voltage of the battery drops to below 4.1V, there will be a deglitch time of 100ms and then the charging current will resume again.

I²C Register for Charging Status Setting

Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x2	Meaning	ISETU	ISETL	USUS	NoBAT	EOC	PGOOD	TS_FAULT	$\overline{\text{SAFE}}$
	Default	1	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R	R	R	R	R

ISETU and ISETL : Set VIN Input Current Limit

ISETU	ISETL	VIN Input Current Limit
0	0	95mA
1	0	475mA
X	1	1.5A

USUS : VIN Suspend Control Input

USUS	1	Suspend
	0	No Suspend

Battery Installation Detection

NoBAT	1	No Battery Installed (TS > 90% of VP)
	0	BAT Installed (TS < 90% of VP)

End_Of_Charge Status

EOC	1	Charging Done or Recharging after Termination
	0	During Charging

VIN Power Good Status

PGOOD	0	$V_{IN} < V_{UVLO}$
	0	$V_{UVLO} < V_{IN} < V_{BAT} + V_{OS_H}$
	1	$V_{BAT} + V_{OS_H} < V_{IN} < V_{OVP}$
	0	$V_{IN} > V_{OVP}$

Temperature Sensing Status

TS_FAULT	1	TS is at fault (too cold, too hot) or VP triggers UVLO.
	0	TS and VP are normal.

Charger Safety Timer Status

$\overline{\text{SAFE}}$	1	Safety timer expired.
	0	Otherwise

Interrupt Indicator

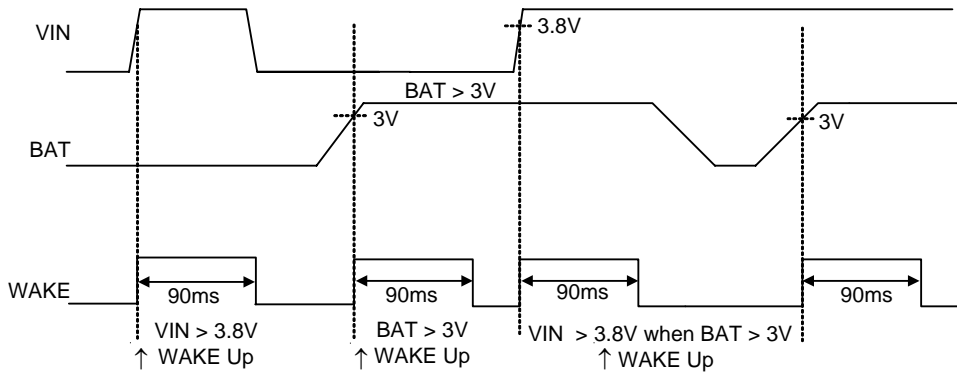
The RT5002C provides the interrupt indicator output pin ($\overline{\text{INT}}$). $\overline{\text{INT}}$ is an open drain pin.

When the status bits (PGOOD, TS_FAULT, EOC, $\overline{\text{SAFE}}$, NoBAT) of I²C register address 0x2 toggle, the $\overline{\text{INT}}$ is set to be low. After Reg 0x2 is read or PMU is turned off, $\overline{\text{INT}}$ goes high.

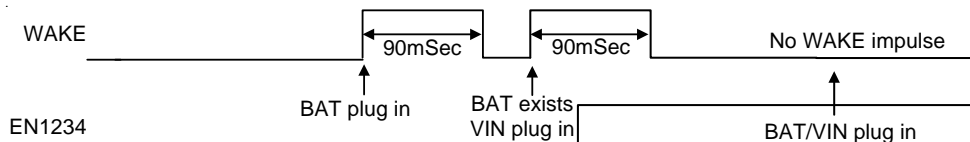
Wake-Up Detector

Wake-Up Detector detects VIN or BAT plug-in events. Once BAT plugs in or VIN plugs in when BAT exist, WAKE pin asserts one 90ms width high pulse. The timing diagram is shown below.

WAKE Timing Diagram



When PMU is enabled, WAKEUP impulse would be masked off. WAKE impulse width 90ms can not be cut by EN1234 = H.



Battery Installation Detection

RT5002C also detect TS voltage to judge the battery installation status. If PMU is enabled but TS voltage > 90% of VP node voltage, RT5002C would set the bit NoBAT = 1 in I²C register bank 0x2.

End_Of_Charge (EOC) Status

The bit EOC in I²C register bank 0x2 can show the EOC status. If EOC = 1, the Charger is in EOC State.

Suspend Mode

Set USUS = 1, and the charge will enter Suspend Mode. In Suspend Mode, $\overline{\text{CHG}}$ is in high impedance and $I_{\text{USUS(MAX)}} < 300\mu\text{A}$.

Charge State Indicator $\overline{\text{CHG}}$

Charger State	$\overline{\text{CHG}}$ Output	Bit EOC	Bit PGOOD	Bit $\overline{\text{SAFE}}$
Charging	Low (for first charge cycle)	0	1	0
Charging Suspended by Thermal Loop		0	1	0
Safety Timers Expired	2Hz Flash	0	1	1
Charging Done	High Impedance	1	1	0
Recharging after Termination		1	1	0
IC Disabled or no Valid Input Power		0	0	0

Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x1	Meaning	TIMER [3:0]				ENCH	$\overline{\text{JEITA}}$	ISET	VSET
	Default	0	1	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

VIN Power Good Status

TIMER [3:0]	0000 to 1111	Fast Charge timeout time: $t_{\text{FCHG}} = (\text{TIMER [3:0]} + 1)$ hours. (ISET = 1) Pre-Charge timeout time : $t_{\text{PCHG}} = t_{\text{FCHG}} / 8$
-------------	--------------	---

ENCH	1	Enable charger
	0	Disable charger

$\overline{\text{JEITA}}$	1	Charger operation controlled by I ² C bits VSET and ISET
	0	Charger operation automatically in JEITA temperature standard

Half Charge Current Set Input

ISET	1	For I _{CHG1} : time = t_{FCHG}
	0	For I _{CHG2} : time = $2 \times t_{\text{FCHG}}$, I _{CHG2} = I _{CHG1} / 2

Battery Regulation Set Input

VSET	1	Battery regulation voltage is 4.2V
	0	Battery regulation voltage is 4.05V

Charging Current Decision

The charge current can be set according to the following equations :

If ISET = 1 (for ICHG1)

$$I_{CHG_FAST} = \frac{V_{ISETA}}{R_{ISETA}} \times 300$$

If ISET = 0 (for ICHG2)

$$I_{CHG_FAST} = \frac{V_{ISETA}}{R_{ISETA}} \times 150$$

$$I_{CHG_PRE} = 10\% \times I_{CHG_FAST}$$

Time Fault

During the fast charge phase, several events may increase the charging time.

For example, the system load current may have activated the APPM loop which reduces the available charging current or the device has entered thermal regulation because the IC junction temperature has exceeded T_{REG}.

However, once the duration exceeds the fault time, the CHG output pin will flash at approximately 2Hz to indicate a fault condition and the charge current will be reduced to about 1mA.

Time fault release methods :

- (1) Re-plug power
- (2) Toggle EN
- (3) Enter/exit suspend mode
- (4) Remove Battery
- (5) OVP

If ISET = 1 (for ICHG1)

$$\text{time} = t_{FCHG}$$

If ISET = 0 (for ICHG2)

$$\text{time} = 2 \times t_{FCHG}$$

JEITA Battery Temperature Standard

CV regulation voltage will change at the following battery temperature ranges : 0°C to 10°C and 45°C to 60°C.

CC regulation current will change at the following battery temperature ranges : 0°C to 10°C and 45°C to 60°C.

Battery Pack Temperature Monitoring

The battery pack temperature monitoring function can be realized by connecting the TS pin to an external Negative Temperature Coefficient (NTC) thermistor to prevent over temperature condition. Charging is suspended when the voltage at the TS pin is out of normal operating range. The internal timer is then paused, but the value is maintained.

When the TS pin voltage returns to normal operating range, charging will resume and the safe charge timer will continue to count down from the point where it was suspended. Note that although charging is suspended due to the battery pack temperature fault, the CHG pin will remain low and indicate charging.

The 3.3V at VP pin is buffered by the RT5002C once it is in charging state or its PMU part is enabled.

For 100kΩ NTC thermistor, the input pin, TSSEL, should be connected to GND. For 10kΩ NTC thermistor, the input pin, TSSEL, should be connected to VIN. TSSEL determines the TS threshold levels for 0°C and 60°C. It also defines the TS threshold levels used in JEITA operation. The choosing method of R1 and R2 to meet battery temperature monitoring is shown below :

Case 1 : TSSEL = L (For 100kΩ NTC) :

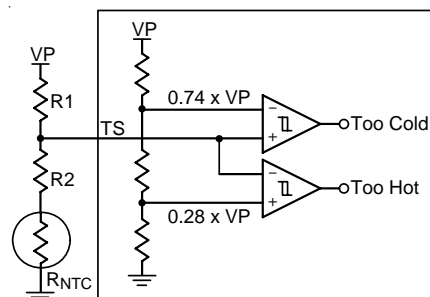


Figure 1

Too Cold Temperature

$$R_{COLD} = R_{NTC}$$

Too Hot Temperature

$$R_{HOT} = R_{NTC}$$

$$\frac{R2 + R_{COLD}}{R_{COLD} + R1 + R2} = 0.74 \tag{1}$$

$$\frac{R2 + R_{HOT}}{R_{HOT} + R1 + R2} = 0.28 \tag{2}$$

Form (1), (2)

$$R1 = \frac{R_{COLD} - R_{HOT}}{2.457}$$

$$R2 = 0.389 \times R1 - R_{HOT}$$

If $R2 < 0$

$$\frac{R_{COLD}}{R_{COLD} + R1} = 0.74 \tag{3}$$

Form (3)

$$R1 = \frac{R_{COLD}}{0.74} - R_{COLD}$$

Case 2 : TSSEL = H (For 10kΩ NTC) :

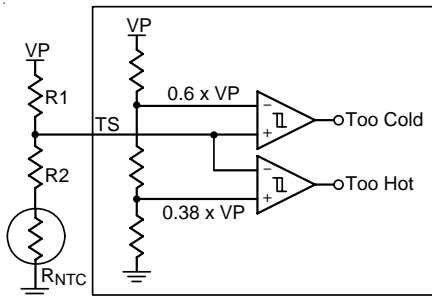


Figure 2

Too Cold Temperature

$$R_{COLD} = R_{NTC}$$

Too Hot Temperature

$$R_{HOT} = R_{NTC}$$

$$\frac{R2 + R_{COLD}}{R_{COLD} + R1 + R2} = 0.6 \tag{1}$$

$$\frac{R2 + R_{HOT}}{R_{HOT} + R1 + R2} = 0.38 \tag{2}$$

Form (1), (2)

$$R1 = \frac{R_{COLD} - R_{HOT}}{0.9}$$

$$R2 = 0.6 \times R1 - R_{HOT}$$

If $R2 < 0$

$$\frac{R_{COLD}}{R_{COLD} + R1} = 0.6 \tag{3}$$

Form (3)

$$R1 = \frac{R_{COLD}}{0.6} - R_{COLD}$$

The Control Temperature Used in JEITA Operation :

The above calculation gives R1 and R2. JEITA control thresholds for full charging current and 4.2V regulation voltage are at TS/VP ratio = 40% and 54% (for TSSEL = H), 35% and 64% (for TSSEL = L). With the ratio, the corresponding NTC thermistor resistances from the resistors in the voltage divider circuit can be obtained. According to the NTC resistances, the corresponding temperatures can be found. The two temperatures are the control temperatures used in JEITA operation.

Power Switch

For the charger, there are three power scenarios:

(1) When a battery and an external power supply (USB or adapter) are connected simultaneously :

If the system load requirements exceed that of the input current limit, the battery will be used to supplement the current to the load. However, if the system load requirements are less than that of the input current limit, the excess power from the external power supply will be used to charge the battery.

(2) When only the battery is connected to the system :

The battery provides the power to the system.

(3) When only an external power supply is connected to the system :

The external power supply provides the power to the system.

Input DPM Mode

For the charger, the input voltage is monitored when USB100 or USB500 is selected. If the input voltage is lower than VDPM, the input current limit will be reduced to stop the input voltage from dropping any further. This can prevent the IC from damaging improperly configured or inadequately designed USB sources.

APPM Mode

Once the sum of the charging and system load currents becomes higher than the maximum input current limit, the SYS pin voltage will be reduced. When the SYS pin voltage is reduced to VAPPM, the RT5002C will automatically operate in APPM mode. In this mode, the

charging current is reduced while the SYS current is increased to maintain system output. In APPM mode, the battery termination function is disabled.

Battery Supplement Mode Short Circuit Protect

In APPM mode, the SYS voltage will continue to drop if the charge current is zero and the system load increases beyond the input current limit. When the SYS voltage decreases below the battery voltage, the battery will kick in to supplement the system load until the SYS voltage rises above the battery voltage.

While in supplement mode, there is no battery supplement current regulation. However, a built-in short circuit protection feature is available to prevent any abnormal current situations. While the battery is supplementing the load, if the difference between the battery and SYS voltage becomes more than the short circuit threshold voltage, SYS will be disabled. After a short circuit recovery time, t_{SHORT_R} , the counter will be restarted. In supplement mode, the battery termination function is disabled. Note that for the battery supply mode exit condition, $V_{BAT} - V_{SYS} < 0V$.

Thermal Regulation and Thermal Shutdown

The charger provides a thermal regulation loop function to monitor the device temperature. If the die temperature rises above the regulation temperature, TREG, the charge current will automatically be reduced to lower the die temperature. However, in certain circumstances (such as high VIN, heavy system load, etc.) even with the thermal loop in place, the die temperature may still continue to increase. In this case, if the temperature rises above the thermal shutdown threshold, TSD, the internal switch between VIN and SYS will be turned off. The switch between the battery and SYS will remain on, however, to allow continuous battery power to the load. Once the die temperature decreases by ΔTSD , the internal switch between VIN and SYS will be turned on again and the device returns to normal thermal regulation.

The internal thermal feedback circuitry regulates the die temperature to optimize the charge rate for all ambient temperatures.

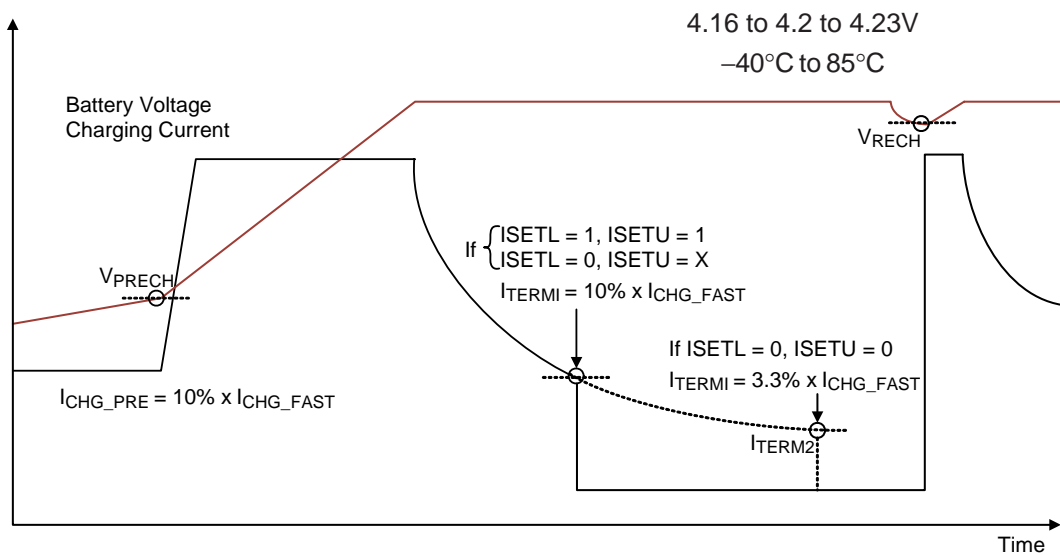
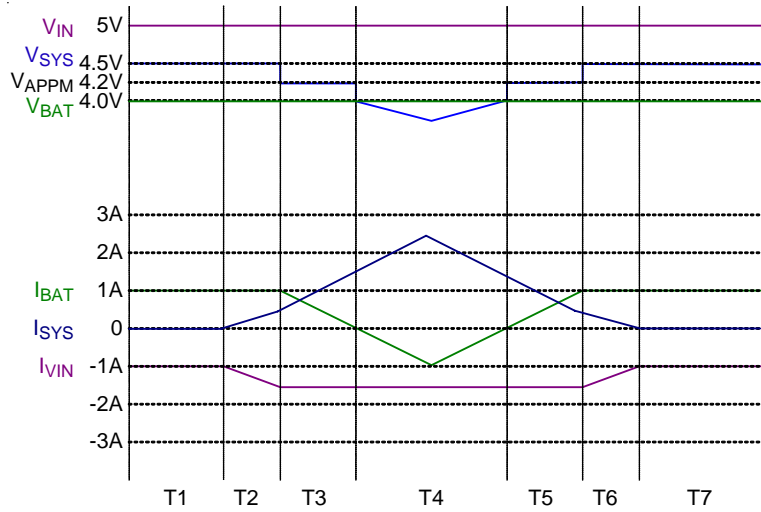


Figure 3

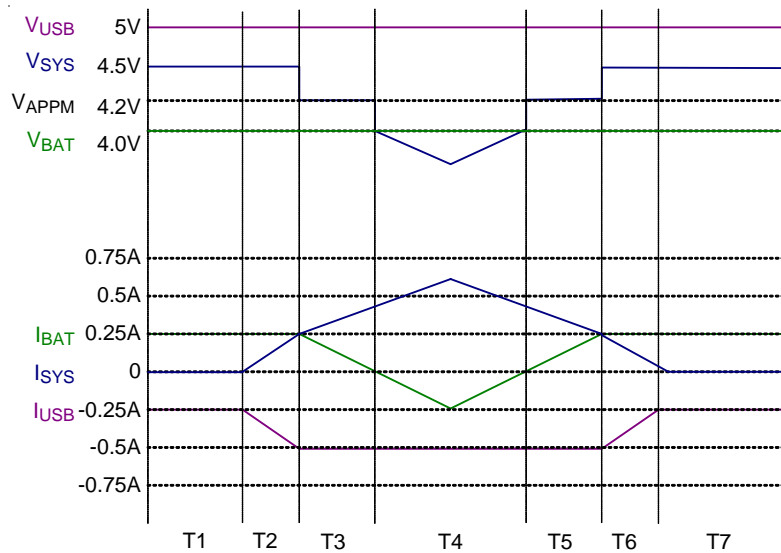
APPM Profile

1.5A Mode :



	I_{SYS}	V_{SYS}	I_{VIN}	I_{BAT}
T1, T7	0	SYS Regulation Voltage	CHG_MAX	CHG_MAX
T2, T6	$< I_{VIN_OC} - CHG_MAX$	SYS Regulation Voltage	$I_{SYS} + CHG_MAX$	CHG_MAX
T3, T5	$> I_{VIN_OC} - CHG_MAX < I_{VIN_OC}$	Auto Charge Voltage Threshold	V_{IN_OC}	$V_{IN_OC} - I_{SYS}$
T4	$> I_{VIN_OC}$	$V_{BAT} - I_{BAT} \times R_{DS(ON)}$	V_{IN_OC}	$I_{SYS} - I_{VIN_OC}$

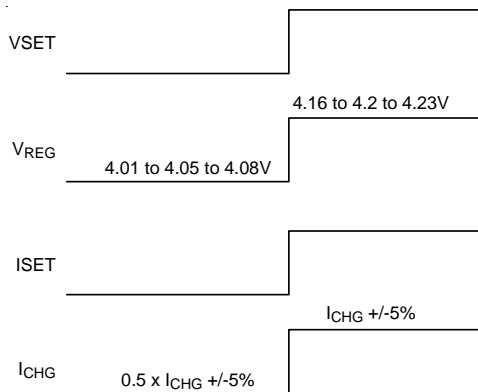
USB 500mA Mode :



	I_{SYS}	V_{SYS}	I_{USB}	I_{BAT}
T1, T7	0	SYS Regulation Voltage	CHG_MAX	CHG_MAX
T2, T6	$< I_{VIN_OC} (USB) - CHG_MAX$	SYS Regulation Voltage	$I_{SYS} + CHG_MAX$	CHG_MAX
T3, T5	$> I_{VIN_OC} (USB) - CHG_MAX < I_{VIN_OC} (USB)$	Auto Charge Voltage Threshold	$I_{VIN_OC} (USB)$	$I_{VIN_OC} (USB) - I_{SYS}$
T4	$> I_{VIN_OC} (USB)$	$V_{BAT} - I_{BAT} \times R_{DS(ON)}$	$I_{VIN_OC} (USB)$	$I_{SYS} - I_{VIN_OC} (USB)$

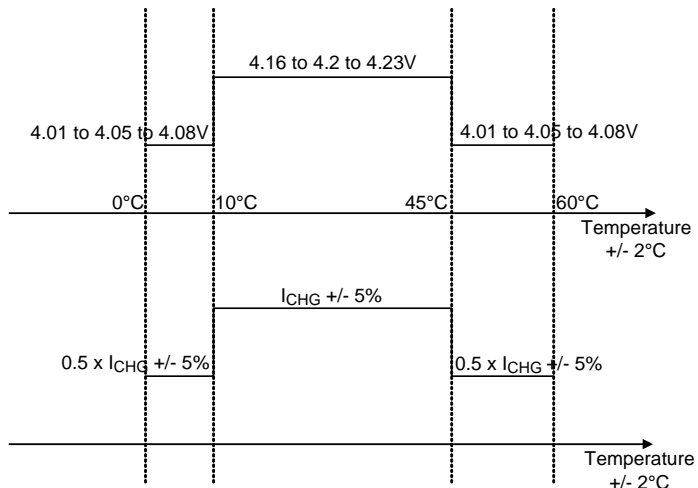
VSET vs. V_{REG} , ISET vs. I_{CHG}

When $\overline{JEITA} = 1$, V_{REG} and I_{CHG} are set by the bits VSET and ISET, respectively.

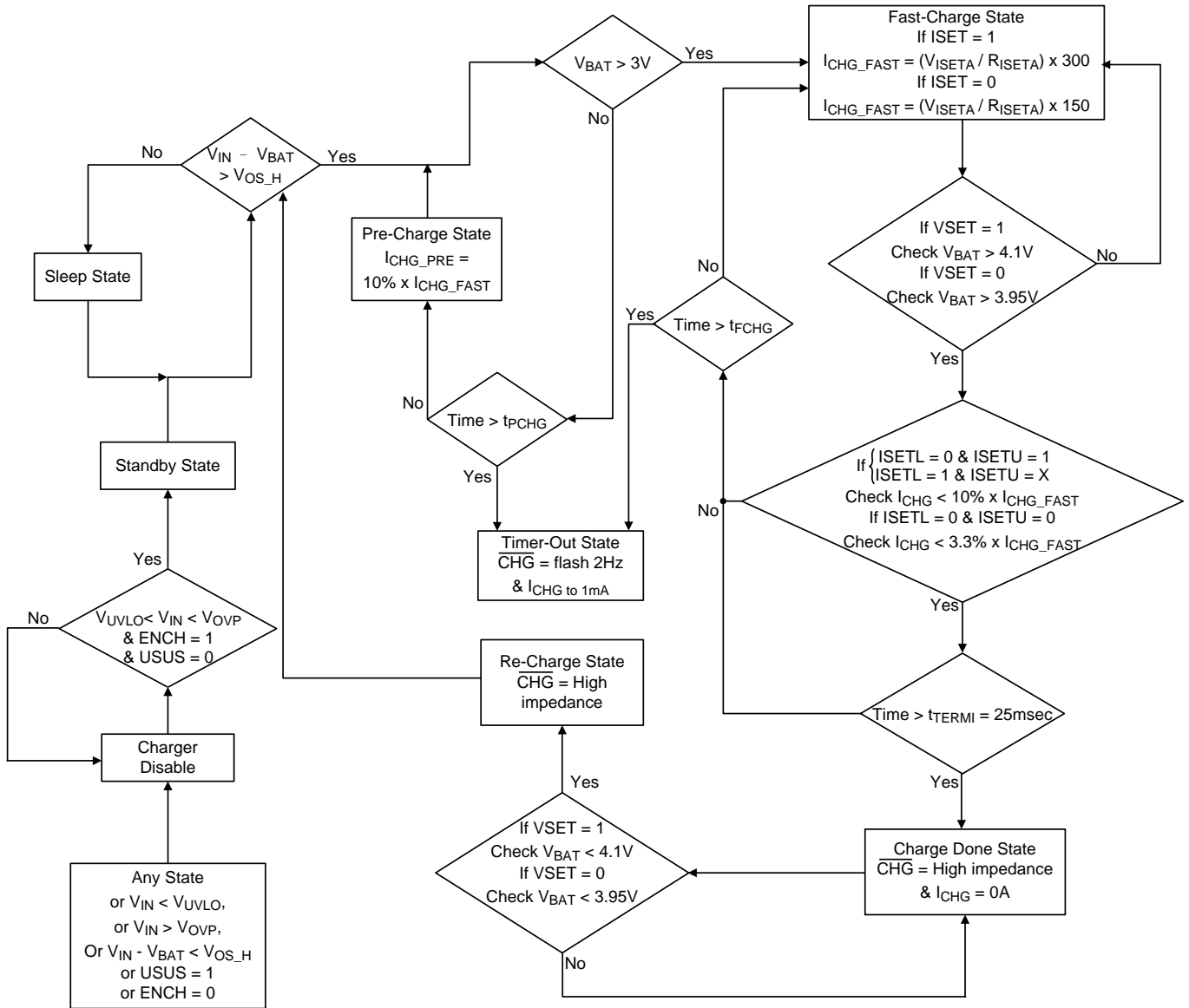


When $\overline{JEITA} = 0$, V_{REG} and I_{CHG} follows JEITA temperature standard.

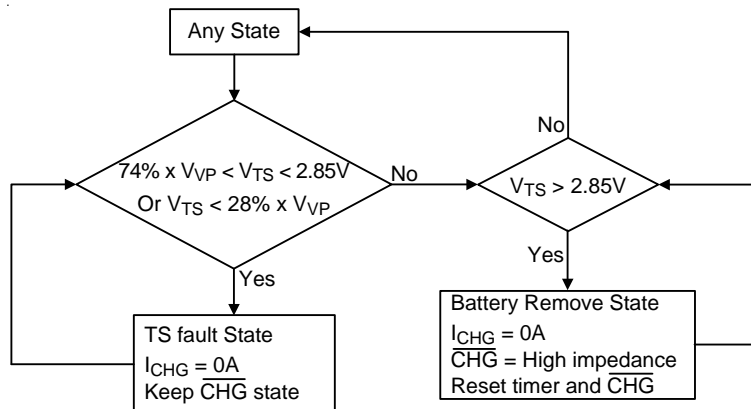
For JEITA Battery Temperature Standard :
 CV regulation voltage will change at the following battery Temp ranges
 0°C to 10°C and 45°C to 60°C
 CC regulation current will change at the following battery Temp ranges
 0°C to 10°C and 45°C to 60°C



RT5002C Operation State Diagram for Charging



Operation State Diagram for TS Pin (TSSEL = L)

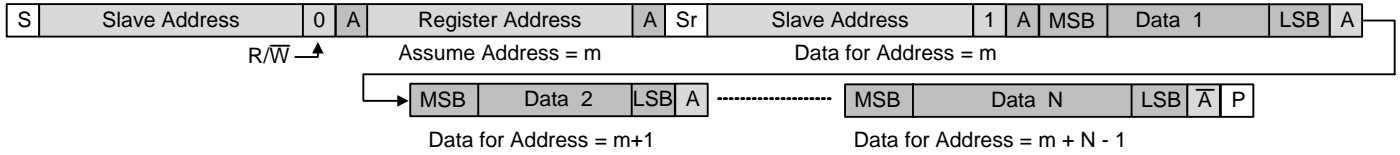


I²C Interface

The RT5002C I²C slave address is by default = 0011000 (7bits), but if customers request, the slave address can

be changed to 0011010 (7bits). The I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :

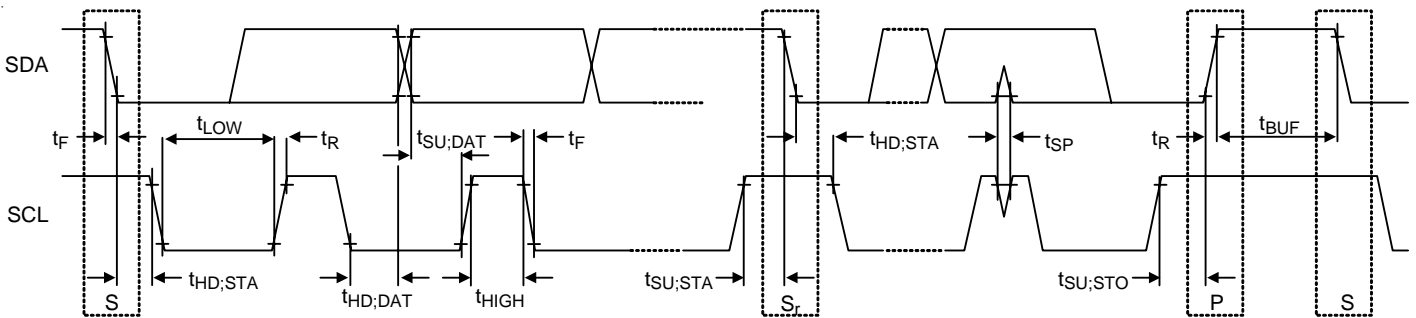
Read N bytes



Write N bytes



Legend: Driven by Master, Driven by Slave (RT5002C), P Stop, S Start, Sr Repeat Start



I²C Register File

Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x0	Meaning	MOD56	SEQ56	EN56	EN7_DIM7 [4:0]				
	Default	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x1	Meaning	TIMER [3:0]				ENCH	JEITA	ISET	VSET
	Default	0	1	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x2	Meaning	ISETU	ISETL	USUS	NoBAT	EOC	PGOOD	TS_FAULT	SAFE
	Default	1	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R	R	R	R	R

Reset after EN1234 = L and PMU shutdown completely for register 0x0.

Reset after PGOOD = 0 and EN1234 = L then PMU shutdown completely for register 0x1 and 0x2.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For WQFN-40L 5x5 package, the thermal resistance, θ_{JA} , is 27.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (27.5^\circ\text{C}/\text{W}) = 3.64\text{W for WQFN-40L 5x5 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . The derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

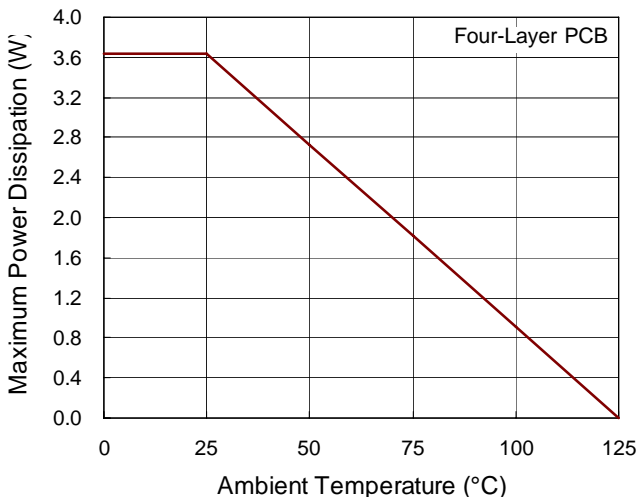
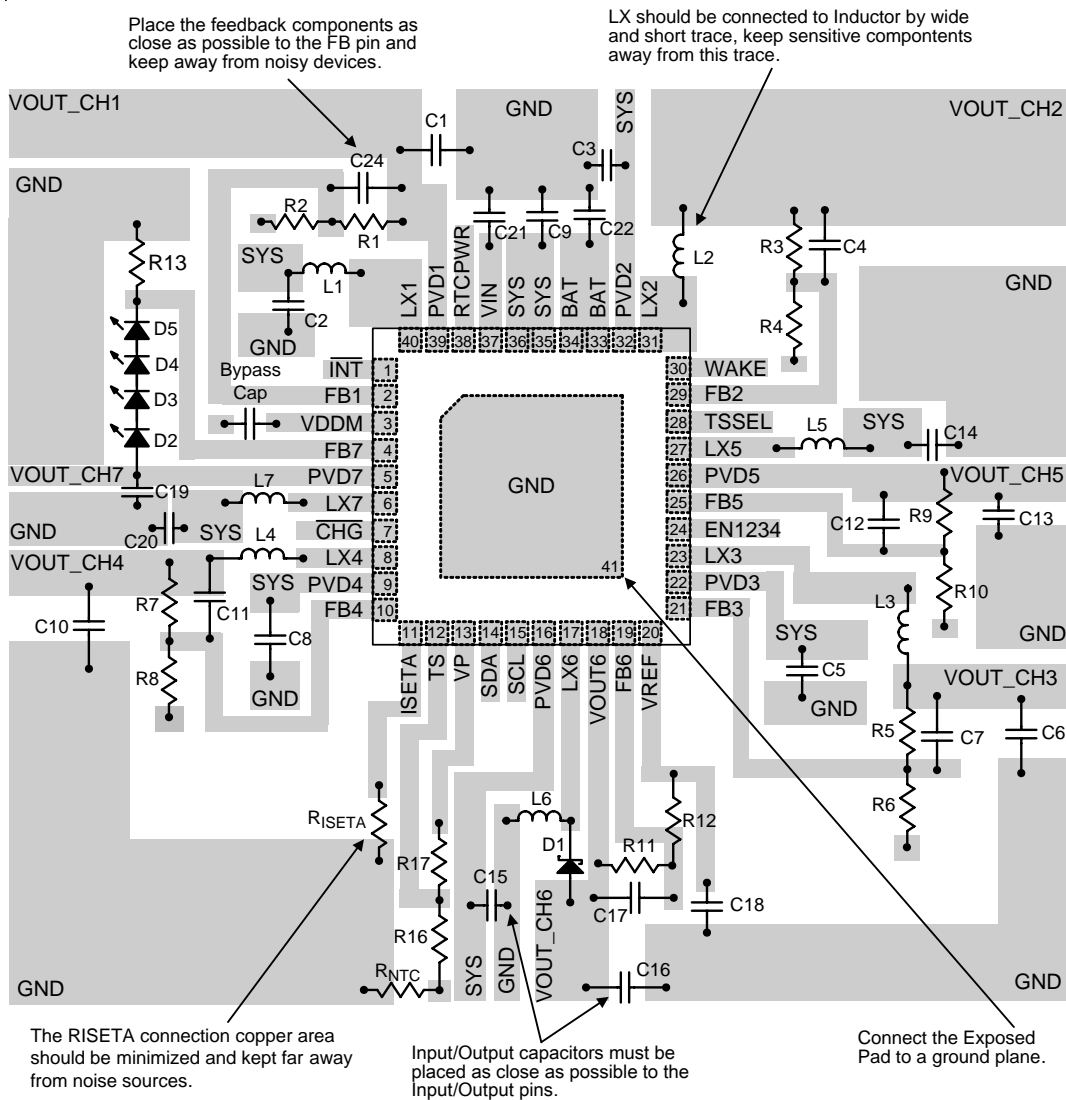


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT5002C, the following PCB layout guidelines must be strictly followed.

- ▶ Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- ▶ Keep the main power traces as wide and short as possible.
- ▶ The switching node area connected to LX and inductor should be minimized for lower EMI.
- ▶ Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- ▶ Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- ▶ The connection of RISETA should be isolated from other noisy traces. A short wire is recommended to prevent EMI and noise coupling.

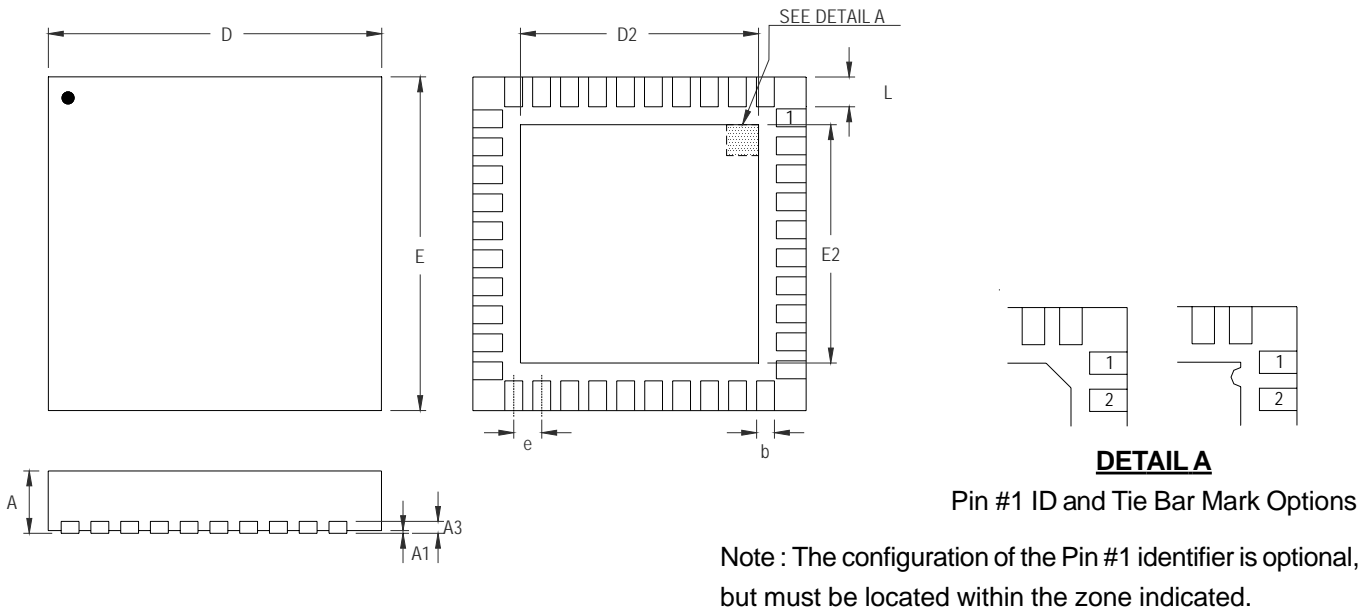


	Protection Type	Threshold (Typical) Refer to Electrical Spec.	Protection Methods	PMU Shutdown Delay Time	Reset Method
SYS	UVLO	$SYS < 1.5V$	PMU Shutdown.	No-delay	VDDM power reset or EN1234 pin set to low
VDDM	OVP	$VDDM > 6V$	Automatic reset at $VDDM < 5.75V$	100ms	VDDM power reset or EN1234 pin set to low
	UVLO	$VDDM < 2.4V$	PMU Shutdown.	No-delay	VDDM power reset or EN1234 pin set to low
CH1 Step-Up	Current limit	N-MOSFET current $> 3A$	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDM power reset or EN1234 pin set to low
	PVDD1 OVP	$PVDD1 > 6V$	N-MOSFET off, P-MOSFET off.	No-delay	VDDM power reset or EN1234 pin set to low
	PVDD1 UVP	$PVDD1 < (V_{SYS} - 0.8V)$ or $PVDD1 < 1.28V$ after soft-start end.	N-MOSFET off, P-MOSFET off.	100ms	VDDM power reset or EN1234 pin set to low
	FB1 UVP	$FB1 < 0.4V$ after precharge	N-MOSFET off, P-MOSFET off	No-delay	VDDM power reset or EN1234 pin set to low
	FB1 Over Load (OL)	$FB1 < 0.7V$	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDM power reset or EN1234 pin set to low
CH2 Step-Down	Current limit	P-MOSFET current $> 1.8A$	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDM power reset or EN1234 pin set to low
	FB2 UVP	$FB2 < 0.4V$ after soft-start end.	N-MOSFET off, P-MOSFET off.	100ms	VDDM power reset or EN1234 pin set to low
	FB2 Over Load	$FB2 < 0.7V$	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDM power reset or EN1234 pin set to low
CH3 Step-Down	Current limit	P-MOSFET current $> 1.6A$	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDM power reset or EN1234 pin set to low
	FB3 UVP	$FB3 < 0.4V$ after soft-start end.	N-MOSFET off, P-MOSFET off.	100ms	VDDM power reset or EN1234 pin set to low
	FB3 Over Load	$FB3 < 0.7V$	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDM power reset or EN1234 pin set to low
CH4 Step-Down	Current limit	P-MOSFET current $> 1.6A$	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDM power reset or EN1234 pin set to low
	FB4 UVP	$FB4 < 0.4V$ after soft-start end.	N-MOSFET off, P-MOSFET off.	100ms	VDDM power reset or EN1234 pin set to low
	FB4 Over Load	$FB4 < 0.7V$	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDM power reset or EN1234 pin set to low

	Protection Type	Threshold (Typical) Refer to Electrical spec.	Protection Methods	PMU Shutdown Delay Time	Reset Method
CH5 Step-Up	Current limit	N-MOSFET current > 1.2A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDM power reset or EN1234 pin set to low
	PVDD5 OVP	PVDD5 > 22V	N-MOSFET off, P-MOSFET off.	No-delay	VDDM power reset or EN1234 pin set to low
	FB5 UVP	FB5 < 0.6V after soft-start end.	N-MOSFET off, P-MOSFET off.	100ms	VDDM power reset or EN1234 pin set to low
	FB5 Over Load	FB5 < 1.1V	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDM power reset or EN1234 pin set to low
CH6 Async Inverting	Current limit	P-MOSFET current > 1.5A	P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDM power reset or EN1234 pin set to low
	PVDD6 OVP	PVDD6 < -13V	P-MOSFET off.	No-delay	VDDM power reset or EN1234 pin set to low
	FB6 UVP	FB6 > 1.2V	P-MOSFET off.	100ms	VDDM power reset or EN1234 pin set to low
	FB6 Over Load	FB6 > 0.74V	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDM power reset or EN1234 pin set to low
CH7 WLED	Current limit	N-MOSFET current > 0.8A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDM power reset or EN1234 pin set to low
	PVDD7 OVP	PVDD7 > 15V	N-MOSFET off, P-MOSFET off. Shutdown CH7 by self	No-delay	VDDM power reset and Reg0x00[4 to 0] = 00000 reset or EN1234 pin set to low
Thermal	Thermal shutdown	Temperature > 155°C	All channels stop switching	No-delay	VDDM power reset or EN1234 pin set to low

	Protection Type	Threshold (Typical) Refer to Electrical Spec.	Protection Methods	Charger Shutdown Delay Time	Reset Method
VIN	VIN UVLO	VIN < 3.3V	No-charge	No-delay	No latch
	VIN OVP	VIN > 6.5V	No-charge	No-delay	No latch

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

Richtek Technology Corporation

5F, No. 20, Taiyuen Street, Chupei City
 Hsinchu, Taiwan, R.O.C.
 Tel: (8863)5526789

Richtek products are sold by description only. Richtek reserves the right to change the circuitry and/or specifications without notice at any time. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.