Single Output LNB Power Supply Controller with I²C Interface

General Description

The RT5007 is a highly integrated voltage regulator and interface IC, specifically designed for supplying power and control signals from advanced satellite Set-Top Box (STB) modules to the Low Noise Block (LNB) down converter in the antenna dish or to the multi-switch box.

The device consists of an independent current-mode Boost controller and low a dropout linear regulator and the circuitry required for 22kHz tone generation to support one-way DiSEqC™ communications.

All the functions and the LNB output voltages (8 programmable levels) can be controlled via the I²C bus. The RT5007 has fault signal to serve as an interrupt for the processor when any condition turns off the LNB controller (over current, over temperature and under voltage lockout). The states of these flags to the faults can be thoroughly examined through the I²C registers.

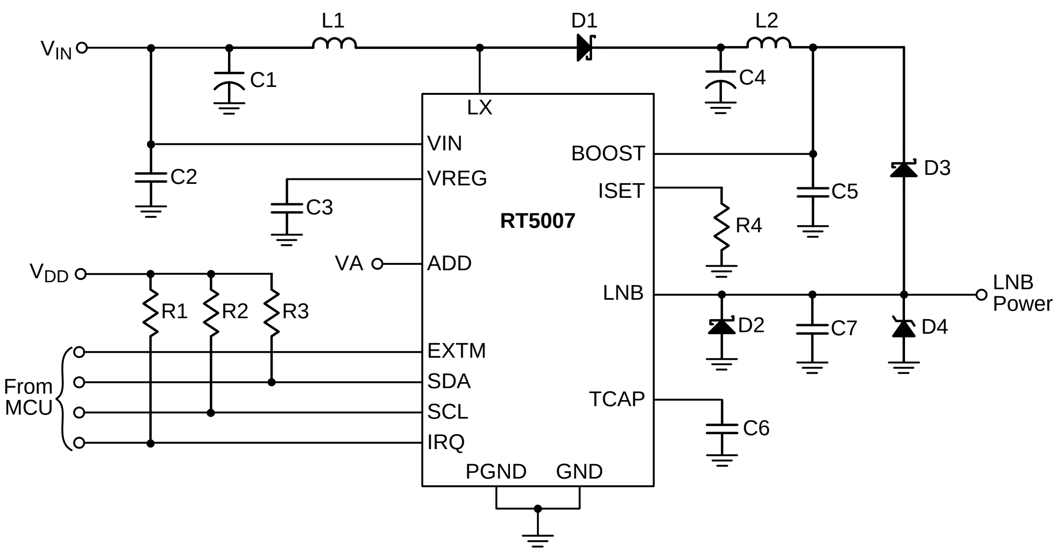
Features

- **Wide Input Supply Voltage Range : 8V to 16V**
- **Wide Output Supply Current Range : 0mA to 500mA**
- **Adjustable Output Current Limit Up to 500mA with 5ms Timer**
- **LNB Voltages (8 Programmable Levels)**
- **±4.5% High Accuracy of LNB Voltage for 0mA to 500mA Current Output**
- **Fault Latch for OTP, OCP, UVLO**
- **Built-in 22kHz Tone Generator One-Way DiSEqC™ Communication**
- **Adjustable Rising/Falling Time via External Capacitor**
- **2-Wire Serial I²C Compatible Interface**
- **RoHS Compliant and Halogen Free**

Applications

- LNB Power Supply and Control for Satellite Set-Top Box
- Analog and Digital Satellite Receivers/ Satellite TV, Satellite PC cards

Simplified Application Circuit



Ordering Information

RT5007 □□

- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

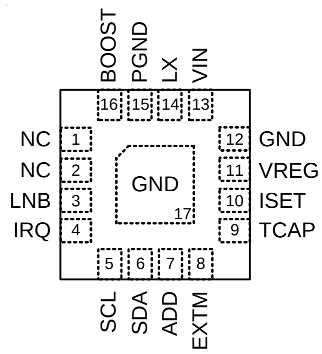
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

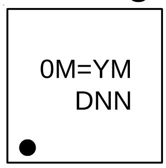
Pin Configurations

(TOP VIEW)



WQFN-16L 3x3

Marking Information



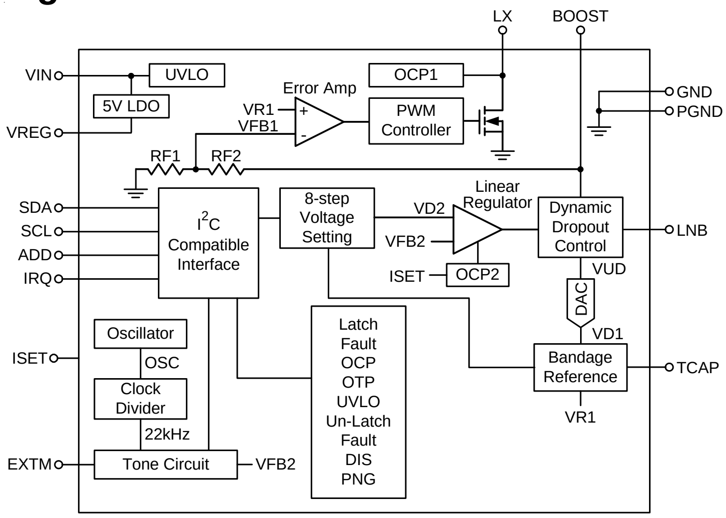
0M= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	NC	No Internal Connection.
3	LNB	Linear Regulator Output Provides the LNB Power. It can supply a 13V to 18V, 500mA and transmit a 600mVpp Tone signal to LNB. It can diagnose the OCP, PNG, CAD and DIS status by I^2C.
4	IRQ	Interrupt Request (Active High). IRQ is an open drain output that connects to VDD (typ. 3.3V to 5V) via a pull high resistor (typ. 4.7kΩ). The voltage level would be pulled low and latched when the faults (UVLO, OCP, TSD) occur. The release condition is fault removing, as I^2C enables reading the status register.
5	SCL	Serial Interface Clock Input. Connect to VDD (typ. 3.3V to 5V) via a pull high resistor (typ. 4.7kΩ). Connect to MCU for I^2C communication. Support I^2C fast mode (typ. 400kHz) communication.
6	SDA	Serial Interface Data Input/Output. Connect to VDD (typ. 3.3V to 5V) via a pull high resistor (typ. 4.7kΩ). Connect to MCU for I^2C communication. Support I^2C fast mode (typ. 400kHz) communication.
7	ADD	Address Select. Supply by VA for different slave address selection. Several devices can connect to the same I^2C bus by different V_A and slave address. Slave address is 0x10 for V_A = 0 to 0.7V, Slave address is 0x12 for V_A = 1.3V to 1.7V, 0x14 for V_A = 2.3V to 2.7V, 0x16 for V_A = 3.3V to 5V.
8	EXTM	External Modulation Input. Used for Tone generation control. Supply (by MCU) high level to apply a DiSEqC™ modulation envelope that modulates an internal tone and then transfers it symmetrically.
9	TCAP	Capacitor (typ. 39nF) for Setting the Rise and Fall Time of the LNB Output. The capacitor should not be too small to avoid inrush current.
10	ISET	Output Current Limit set Via External Resister. Minimum is 50kΩ for the 500mA OCP setting.
11	VREG	Internal Reference Output Typically. Connecting a capacitor (typ. 0.22μF) from this pin to GND.
12, 17 (Exposed Pad)	GND	Analog Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
13	VIN	Power Supply Input. A capacitor (typ. 0.1μF) should be connected to this pin. The operating voltage is 8V to 16V. Under Voltage Lockout (UVLO) is 7.35V.
14	LX	Switch Node. Connect an inductor (typ. 33μH) to input and a schottky diode to output. A RC snubber should be connected to this pin to reduce the voltage spike.
15	PGND	Power Ground.
16	BOOST	Track Supply Voltage to Linear Regulator. Connect to the converter output. Use a low ESR capacitor to ensure low voltage ripple.

Function Block Diagram



Operation

The RT5007 integrates the functions of a current mode Boost converter and a linear regulator. Use the I^2C to control the LNB voltage and the Boost converter is at least 800mV greater than LNB voltage. The Boost converter is the high efficiency PWM architecture with 352kHz operation frequency. The linear regulator has the capability to source current up to 500mA during continuous operation. All the loop compensation, current sensing, and slope compensation functions are provided internally.

OCP

Both the Boost converter and the linear regulator have independent current limit. In the Boost converter (OCP1), this is achieved through cycle-by-cycle internal current limit (typ. 3.8A). In the linear regulator (OCP2), when the linear regulator exceeds OCP more than 5ms, the LNB output will be disabled and the OCP bit of the status register will be set to high.

I^2C

User can communicate with RT5007 by microcontroller via the two wires I^2C. The two lines SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-high resistor (typically 4.7kΩ).

Fault

The IRQ output becomes logic low when the RT5007 recognizes a latch fault condition. Latch fault conditions are indicated by the TSD, UVLO and OCP, and are latched in the status register. The RT5007 latches all conditions in the status register until the completion of the data read.

Bandage Reference

The RT5007 provides the slew rate control during either start-up, or output voltage is transitioning. The rising and falling times of the output voltage can be set by the external capacitor connected from TCAP pin to GND.

Tone Circuit

This circuit is used for tone generation. Use the EXTM pin to control internal 22kHz oscillator output from LNB.

OTP

When the junction temperature reaches the critical temperature (typically 150°C), the Boost converter and the linear regulator are immediately disabled.

UVLO

The UVLO circuit compares the VIN with the UVLO threshold (7.7V rising typically) to ensure that the input voltage is high enough for reliable operation. The 350mV (typ.) hysteresis prevents supply transients from causing a shutdown.

PWM Controller

The loop compensation, current sensing, and slope compensation functions are provided internally.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 28V
- Output Voltage LNB, LX, BOOST ---------- –0.3V to 28V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage (Note 5) ---------- 8V to 16V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{LOAD}, I_{LOAD} is the output of LNB power, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LNB Output Accuracy, Load and Line Regulation	E_{RR}	Relative to selected V_{LNB} target level, I_{LOAD} = 0 to 500mA	–4.5	--	4.5	%
Supply Current	I_{IN_OFF}	ENB bit = 0, LNB output disabled	--	--	10	mA
	I_{IN_ON}	ENB bit = 1, LNB output enabled, I_{LOAD} = 0mA	--	--	19	
Boost Switch On Resistance	R_{DSON}		--	300	600	mΩ
Switching Frequency	f_{SW}		320	352	384	kHz
Switch Current Limit	I_{LIMSW}	V_{IN} = 10V, V_{BOOST} = 19.84V	--	3.8	--	A
Linear Regulator Voltage Drop	V_{DROP}	V_{BOOST} – V_{LNB}, no tone signal, I_{LOAD} = 500mA	600	800	1000	mV
VREG output	V_{REG}		--	5	--	V
TCAP Pin Current	I_{CHG}	V_{TCAP} = 0V	–12.5	–10	–7.5	μA
	I_{DISCHG}	V_{TCAP} = 4V	7.5	10	12.5	
Ripple and Noise on LNB Output	V_{RIP_PP}	20MHz Bandwidth Limit	--	30	--	mV_{PP}
Load Regulation	V_{OUT_LOAD}	V_{LNB} = 13.667V, I_{LNB} = 50mA to 450mA	--	38	76	mV
		V_{LNB} = 19.667V, I_{LNB} = 50mA to 450mA	--	45	90	
ISET Voltage	V_{ISET}		--	1	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	V_{OUT_LINE}	V_{IN} = 10V to 16V, V_{LNB} = 13.667V, I_{LNB} = 50mA	−10	--	10	mV
		V_{IN} = 10V to 16V, V_{LNB} = 19.667V, I_{LNB} = 50mA	−10	--	10	
Protection						
Output Over Current Limit	I_{LIM_LNB}	R_{ISET} = 50kΩ	450	550	650	mA
Output Over Current Disable Time	t_{DIS}		--	5	--	ms
VIN Turn On Threshold	V_{IN_TH}	V_{IN} Rising	7.4	7.7	8	V
VIN Under Voltage Lockout Hysteresis	V_{UVLO_HYS}		--	350	--	mV
OTP Threshold	T_{OTP}		--	150	--	°C
OTP Hysteresis	T_{OTPHYS}		--	30	--	°C
Power Not Good (Low)	PNG_{LOSET}	With respect to V_{LNB} setting; V_{LNB} low, PNG set to 1	88	91	94	%
Power Not Good (Low) Hysteresis	PNG_{LO_HYS}	With respect to V_{LNB} setting	--	4	--	%
Power Not Good (High)	PNG_{HISET}	With respect to V_{LNB} setting; V_{LNB} high, PNG set to 1	106	109	112	%
Power Not Good (High) Hysteresis	PNG_{HIHYS}	With respect to V_{LNB} setting	--	4	--	%
Tone						
Tone Frequency	f_{TONE}		20	22	24	kHz
Tone Amplitude, Peak to Peak	V_{TONE_PP}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 750nF	550	720	900	mV
Tone Duty Cycle	DC_{TONE}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 750nF	40	50	60	%
Tone Rise Time	t_{RTONE}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 750nF	5	10	15	μs
Tone Fall Time	t_{FTONE}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 750nF	5	10	15	μs
EXTM Logic Input	V_{EXTM_H}		2	--	--	V
	V_{EXTM_L}		--	--	0.6	
EXTM Input Leakage	$I_{EXTMLKG}$		--	--	5	μA
I^2C Compatible Interface						
Logic Input (SDA, SCL) — High Level	V_{SCL_H}		2	--	--	V
Logic Input (SDA, SCL) — Low Level	V_{SCL_L}		--	--	0.6	
Logic Input Hysteresis	$V_{I2CIHYS}$		--	150	--	mV
Logic Input Current	I_{I2CI}		−10	<±1	10	μA
Logic Output Voltage SDA and IRQ	V_{T2COUT_L}		--	--	0.4	V
Logic Output Leakage SDA and IRQ	I_{T2CLKG}		--	--	10	μA
SCL Clock Frequency	f_{CLK}		--	--	400	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Fall Time	$t_{FL2COUT}$		--	--	250	ns
Bus Free Time Between Stop/Start	t_{BUF}		1.3	--	--	μs
Hold Time Start Condition	t_{HD_STA}		0.6	--	--	μs
Setup Time for Start Condition	t_{SU_STA}		0.6	--	--	μs
SCL Low Time	t_{LOW}		1.3	--	--	μs
SCL High Time	t_{HIGH}		0.6	--	--	μs
Data Setup Time	t_{SU_DAT}		100	--	--	ns
Data Hold Time	t_{HD_DAT}		0	--	900	ns
Setup Time for Stop Condition	t_{SU_STO}		0.6	--	--	μs
I^2C Address Setting						
ADD Voltage for Address 0001, 000	Address1		0	--	0.7	V
ADD Voltage for Address 0001, 001	Address2		1.3	--	1.7	V
ADD Voltage for Address 0001, 010	Address3		2.3	--	2.7	V
ADD Voltage for Address 0001, 011	Address4		3.3	--	5	V

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

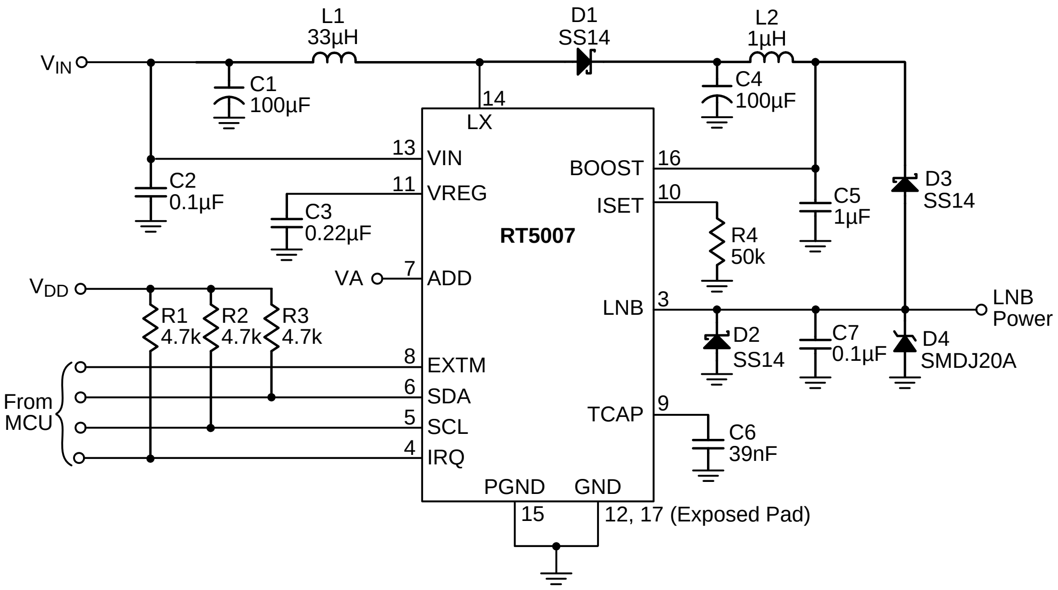
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Operation at V_{IN} = 16V may be limited by power loss in the linear regulator.

Typical Application Circuit



Note :

(1) C5 and L2 are used for filter to reduce the voltage ripple into BOOST pin.

(2) D2, D3, D4, are used for surge protection. The clamping voltage of D4 is 30V, the break down voltage must higher be than 24V as recommended.

(3) IRQ, SDA and SCL are connected to VDD via a pull high resistor (typ. 4.7kΩ).

(4) EXTM, SDA, SCL and IRQ are connected to microcontroller directly.

(5) Use a low ESR capacitor for C4 (typ. 100μF) to reduce the voltage ripple.

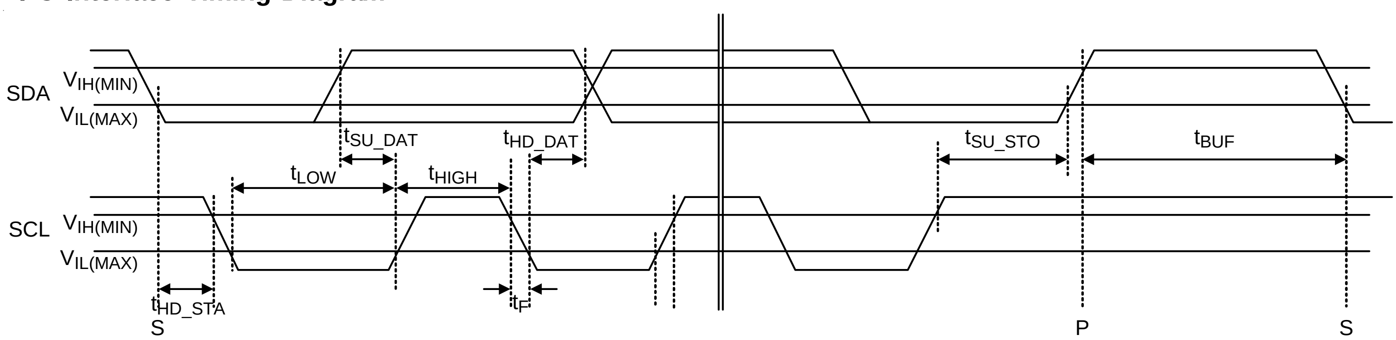
(6) The capacitor C6 of TCAP should not be less than 39nF to avoid inrush current.

(7) The capacitor C3 should not be less than 0.1μF for the power stability.

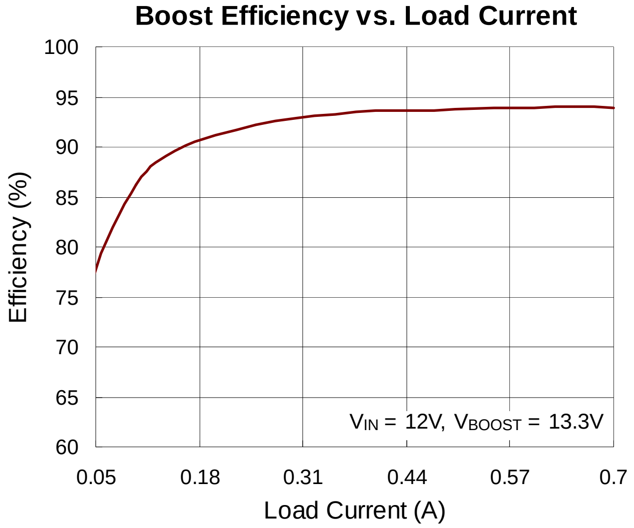
(8) The Over Current Protection Resister R4 shouldn't be less than 50kΩ.

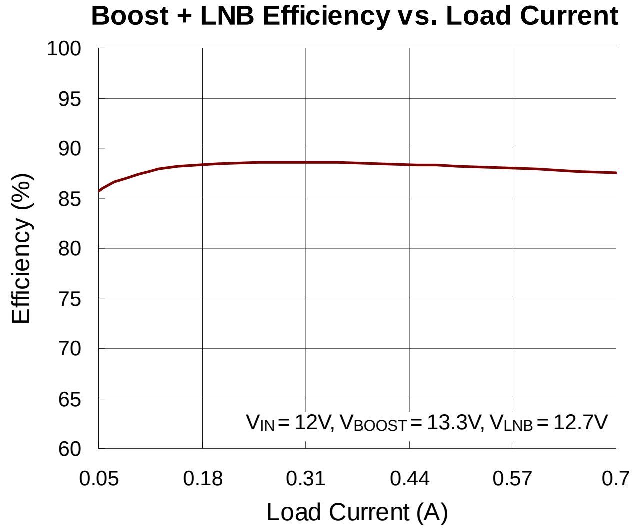
Timing Diagram

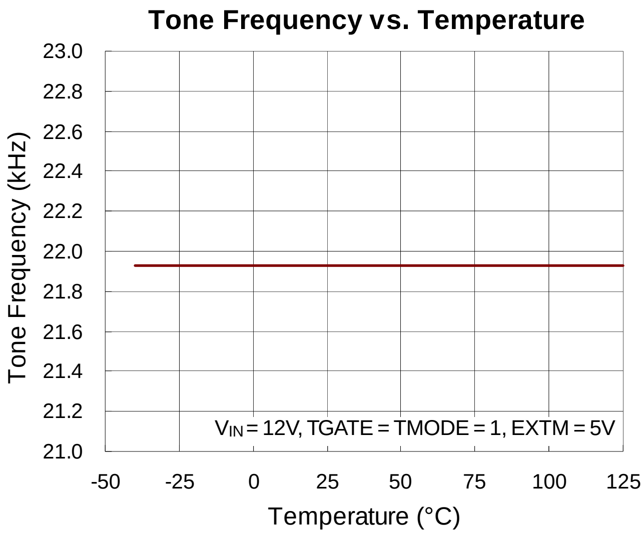
I²C Interface Timing Diagram

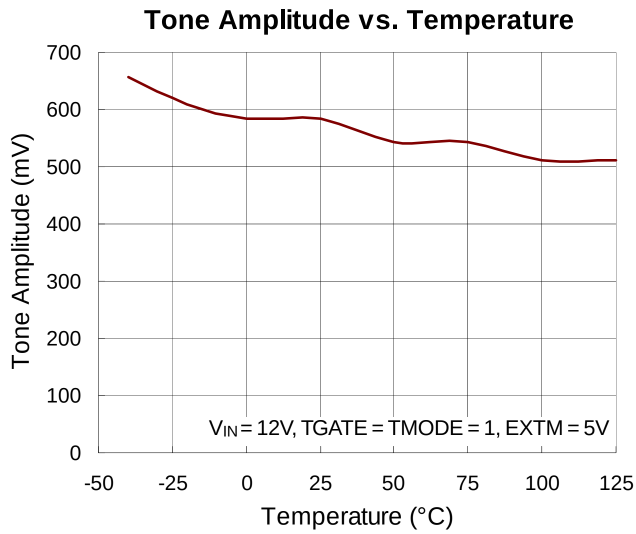


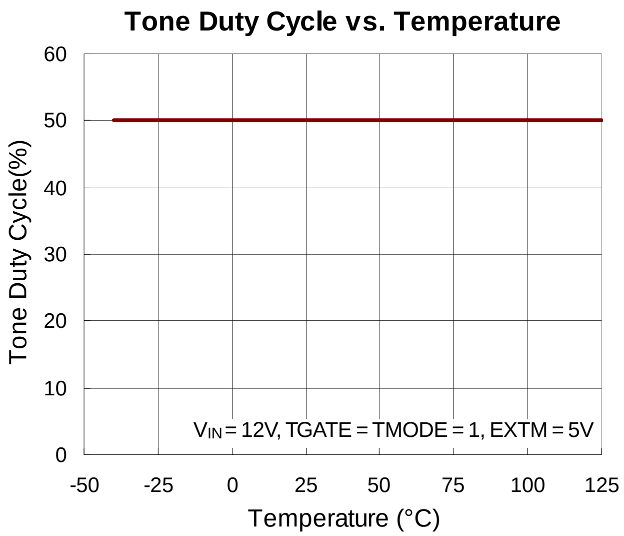
Typical Operating Characteristics

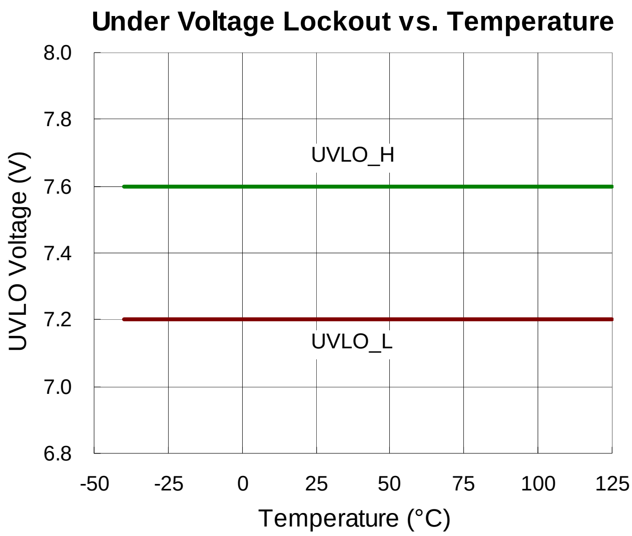




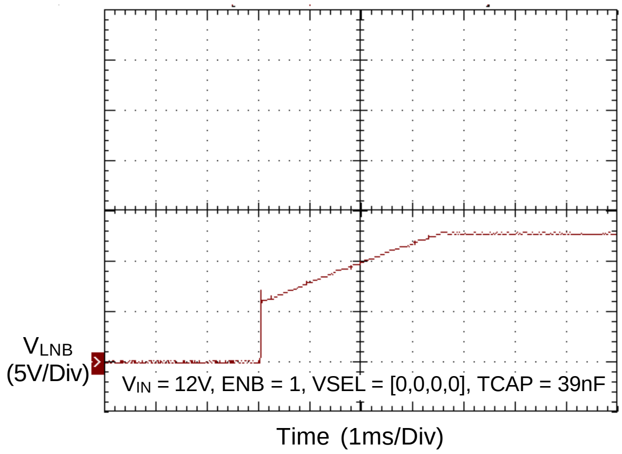




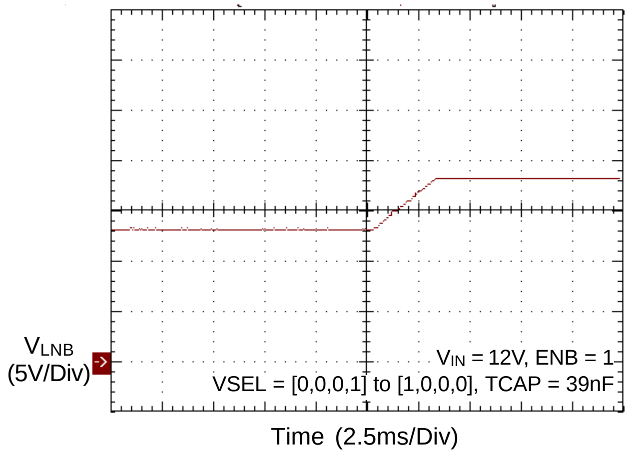




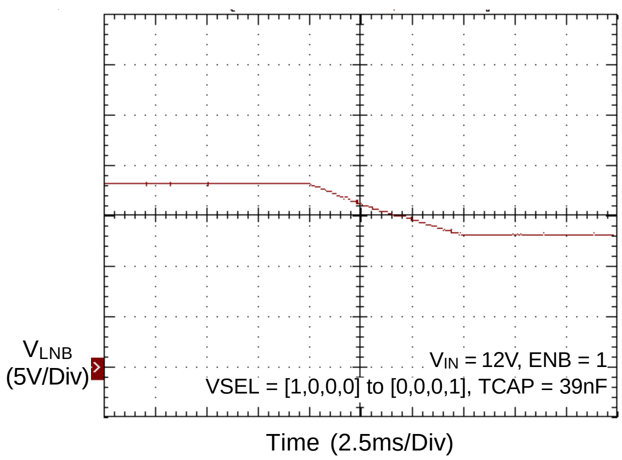
LNB Rising Time



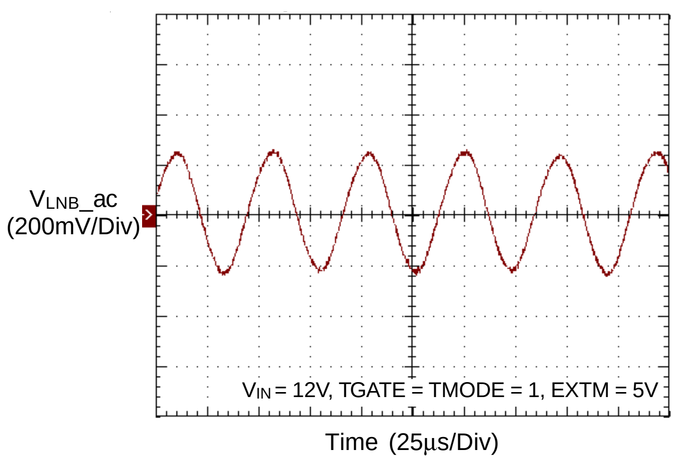
VLNB Transition from 13V to 18V



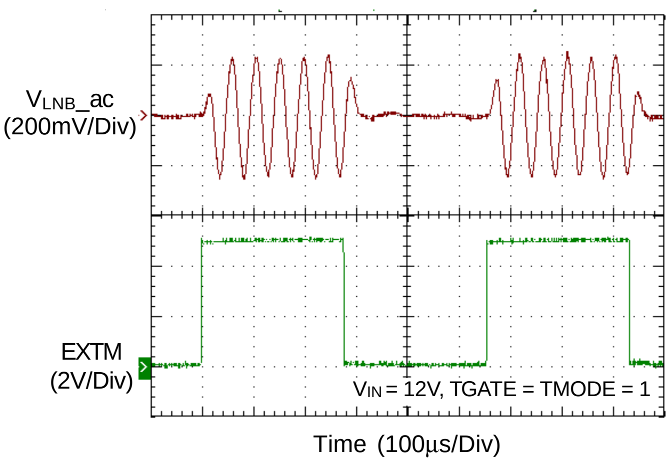
VLNB Transition from 18V to 13V



22kHz Tone



Tone Control by EXTM



Application Information

Boost Converter/Linear Regulator

The RT5007 integrates a current mode Boost converter and linear regulator. Use the I^2C to control the LNB voltage and the Boost converter track is at least greater 800mV than LNB voltage. The Boost converter is the high efficiency PWM architecture with 352kHz operation frequency. The linear regulator has the capability to source current up to 500mA during continuous operation. All the loop compensation, current sensing, and slope compensation functions are provided internally.

The RT5007 has current limiting on the Boost converter and the LNB output to protect the IC against short circuits. The internal MOSFET will turn off when the LX current is higher than 3.8A cycle-by-cycle. If the LNB output in heavy load, output current is limited to typically 500mA, IRQ latch to low and the LNB output will be disabled if the over current condition is more than 5ms. The RT5007 must be enabled by reading the status register to release the IRQ.

Input Capacitor Selection

The input capacitor reduces voltage spikes from the input supply and minimizes noise injection to the converter. A 100μF capacitance is sufficient for most applications. Nevertheless, a higher or lower value may be used depending on the noise level from the input supply and the input current to the converter. Note that the voltage rating of the input capacitor must be greater than the maximum input voltage.

Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the converter, $I_{IN(MAX)}$ is the maximum input current, and I_{RIPPLE} is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of the inductor must be greater than I_{PEAK}. The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Output Capacitor Selection

The RT5007 Boost regulator is internally compensated and relies on the inductor and output capacitor value for overall loop stability. The output capacitor is in the 50μF to 200μF range with a low ESR, as strongly recommended. The voltage rating on this capacitor should be in the 25V to 35V range since it is connected to the Boost V_{OUT} rail.

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of the inductor current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT}\right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{OUT}\right)\right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. Bring C_{OUT} to the left side to estimate the value of ΔV_{OUT1} according to the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

where D is the duty cycle and η is the Boost converter efficiency. Finally, take ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT1} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

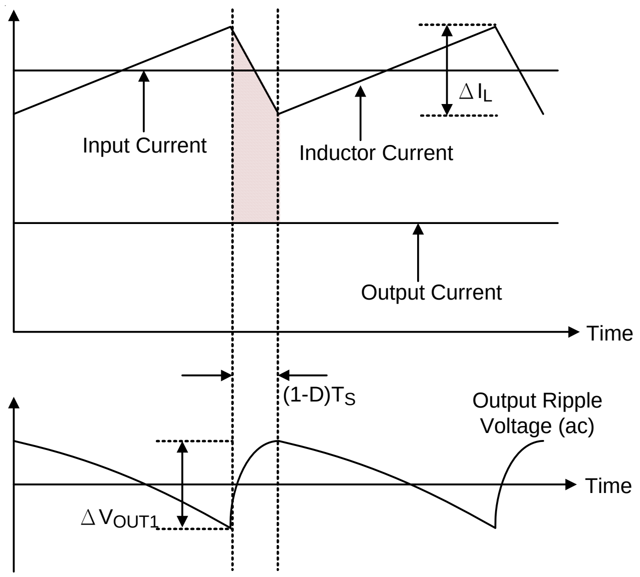


Figure 1. The Output Ripple Voltage without the Contribution of ESR

Schottky Diode Selection

Schottky diodes are chosen for their low forward voltage drop and fast switching speed. However, when making a selection, important parameters such as power dissipation, reverse voltage rating, and pulsating peak current should all be taken into consideration. A suitable Schottky diode's reverse voltage rating must be greater than the maximum output voltage and its average current rating must exceed the average output current. The chosen diode should also have a sufficiently low leakage current level, since it increases with temperature.

Under Voltage Lockout (UVLO)

The UVLO circuit compares the input voltage at VIN with the UVLO threshold (7.7V Rising typ.) to ensure that the input voltage is high enough for reliable operation. The 350mV (typ.) hysteresis prevents supply transients from causing a shutdown. Once the input voltage exceeds the UVLO rising threshold, start-up begins. When the input voltage falls below the UVLO falling threshold, all IC internal functions will be turned off by the controller.

Over Current Protection

The RT5007 features an over-current protection function to prevent chip damage from high peak currents. Both the Boost converter and the LNB output have independent current limit. In the Boost converter, this is achieved through cycle-by-cycle internal current limit. During the ON-period, the chip senses the inductor current that is flowing into the LX pin. The internal N-MOSFET will be turned off if the peak inductor current reaches the current limit value of 3.8A(typ.). The LNB output current limit can be set by the resistor from the ISET pin. This current can be set from 300mA to 500mA by setting the resistor from 75kΩ to 50kΩ. The typical LNB output current limit can be set by the following equation:

I_{OCP} (mA) = 23000 / R_{ISET} (kΩ)

When the output current exceeds the current limit for 5ms, the LNB output will be disabled and the OCP bit of the status register will be set to high. The minimum value of the R_{ISET} is 50kΩ. Be aware that the ISET pin can not be inadvertently grounded.

Short Circuit Protection

If the LNB output is shorted to ground, and more than 5ms, the RT5007 will be disabled.

Slew Rate Control

The RT5007 provides the slew rate control during either start-up, or output voltage is transitioning. The output voltage rise and fall times can be set by the capacitor connected from TCAP pin to GND. The value of C_{TCAP} can be calculated using the following formula :

$$C_{TCAP} = 6\left(I_{TCAP} / SR\right)$$

$$SR = \Delta V_{LNB} / \Delta t$$

Where C_{TCAP} is the TCAP value in nF, I_{TCAP} is the TCAP pin charge/discharge current (typ. 10μA), SR is the LNB output voltage slew rate, ΔV_{LNB} is the differential transition voltage and the Δt is the required transition time in ms.

The typical value of C_{TCAP} is 39nF for most applications. However, it is necessary to increase the value of C_{TCAP} to avoid inrush current of the LNB output but too large value will probably cause the voltage transition specifications to be exceeded. The output linear regulator provides approximately 40mA of pull-down capability to ensure that the output volts are ramped from 20V to 13V in a reasonable amount of time.

Over Temperature Protection

When the junction temperature reaches the critical temperature (typ. 150°C), the Boost converter and the linear regulator are immediately disabled, the TSD bit set to high and the IRQ voltage goes low. When the junction temperature cools down to a lower temperature threshold specified, this bit will be cleared and the RT5007 will be allowed to restart by normal start operation.

I^{2}C Write/Read

Writing and reading to the RT5007 register is shown in Figure 2. The slave address is controlled by ADD voltage, please refer to the Table 1. In writing mode, the slave address is proportional to ADD voltage. It requires transmission of total three bytes, slave address, control register address and control data. Address of RT5007 is 0x00. In reading mode, the R/W bit of the slave address is 1, RT5007 outputs data after receiving the right slave address and status register address (0x00). The master (microcontroller) should make an ACK to slave for continuous transmission. The RT5007 stops the data outputs if the master feedbacks a NACK before stop condition.

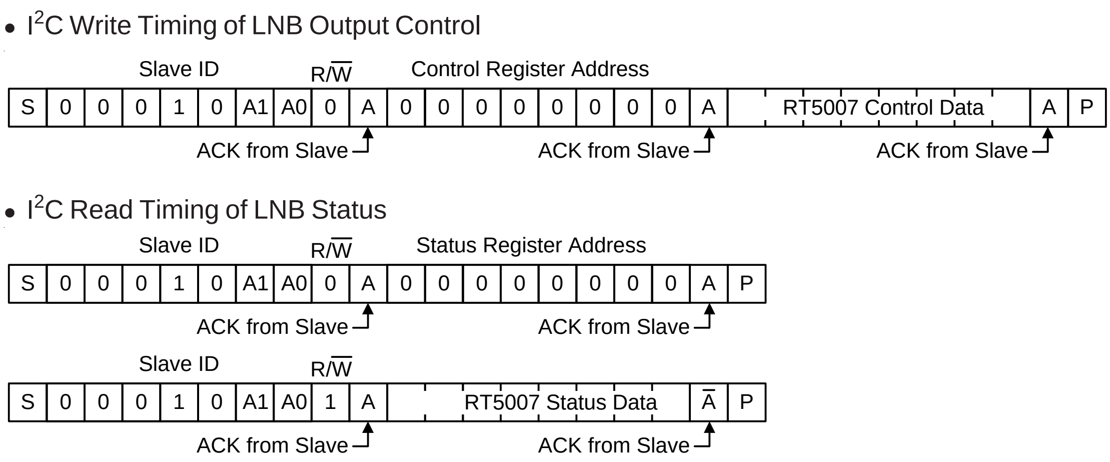


Figure 2. I^{2}C Write and Read Timing Control

Table 1. RT5007 ADD Voltage and Slave Address

RT5007 Slave Address		Write	Read	Min	Typ	Max
Address1	[A1,A0] = [0,0]	0x10	0x11	0	--	0.7
Address2	[A1,A0] = [0,1]	0x12	0x13	1.3	--	1.7
Address3	[A1,A0] = [1,0]	0x14	0x15	2.3	--	2.7
Address4	[A1,A0] = [1,1]	0x16	0x17	3.3	--	5

Interrupt Request (IRQ)

The RT5007 provides an interrupt pin (IRQ), which is an open-drain, active high output. This output may be connected to a common IRQ line with a suitable external pull-up resistor and can be used with other I^2C compatible devices to request attention from the master controller.

The IRQ output becomes logic low when the RT5007 recognizes a fault condition, or at power on, when the main supply, V_{IN}, and the internal logic supply, VREG, reach the correct operating conditions. It is only reset to inactive when the I^2C master addresses the RT5007 with the read/write bit set (reading mode enabled), shown as below. Fault conditions are indicated by the TSD, UVLO and OCP bits, and are latched in the status register (see the Table 2).

The DIS, PNG status bits do not cause an interrupt. All these bits are continually updated, apart from the DIS bit, which changes when the LNB is either disabled, intentionally or due to a fault, or is enabled. When the master recognizes an interrupt, reference the Figure3, it addresses all slaves connected to the interrupt line in sequence, and then reads the status register to determine which device is requesting attention. The RT5007 latches all conditions in the status register until the completion of the data read.

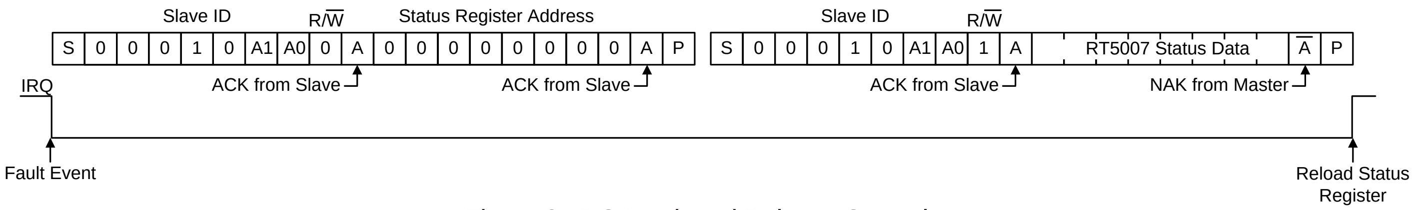


Figure 3. IRQ Latch and Release Control

Table 2. Fault Detect Function and IRQ Status

Bit	Bit Name	Description	Latched or Not	Reset Condition	IRQ Status
0	DIS	LNB output disable	No	LNB enabled and no latched faults	None
1		Not used			None
2	OCP	Over current	Yes	LNB output current less than OCP current and I^2C Read the status register.	IRQ set low
3		Not used			None
4	PNG	Power not good	No	LNB Voltage within setting range	None
5		Not used			None
6	TSD	Thermal shutdown	Yes	Junction temperature less than TSD limit and I^2C read the status register.	IRQ set low
7	UVLO	VIN under voltage	Yes	VIN voltage higher than the UVLO voltage and I^2C read the status register.	IRQ set low

LNB Output Voltage and Control Registers

The RT5007 control register 1 is shown in Table 3. VSEL [2:0] provides voltage control on the LNB output. This function provides the necessary levels for all the common standards. The function of line-adding compensation is enabled if the cable line has voltage drop. The voltage levels are defined in Table 4. Bit 3 VSEL2 switches between the low level and high level output voltages on the LNB output. The low level, set to 0, is 13.333V nominal and the high level, set to 1, is 18.667V nominal. ENB bit controls the LNB output. When set to 1, the LNB output is switched on. When set to 0, the LNB output is disabled.

Table 3. RT5007 Control Register 1

RT5007 Control Register				
Bit	Bit Name	Default	Access	Description
2 : 0	VSEL <2 : 0>	000	W	8 steps output voltage selection
3	ENB	0	W	Enables or disables the LNB output 0 : Disable LNB output 1 : Enable LNB output
7 : 4		0000	W	Not used

Table 4. Output Voltage Amplitude Selection

VSEL2	VSEL1	VSEL0	LNB (V)
0	0	0	13.333
0	0	1	13.667
0	1	0	14.000
0	1	1	14.333
1	0	0	18.667
1	0	1	19.000
1	1	0	19.667
1	1	1	20.000

RT5007 control signal :

Bit 0 to 3, VSEL<2:0> : These four bits provide 8-level LNB output voltage.

Bit 3, ENB : Enable the LNB output. When set to 1 the LNB output is switched on. When set to 0, the LNB output is disabled.

Bit 4 to 7, set to 0 (unused).

Tone Generation

The RT5007 only provides one tone generation function. By external EXTM pin. When EXTM pin set to high control the tone generation on the LNB output by the internal 22kHz oscillator.

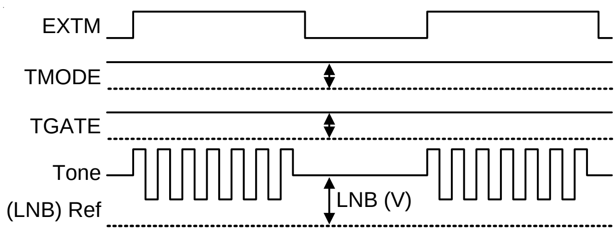


Figure 4. Tone Generation

Status Registers

The RT5007 status register table is shown in Table 6 and Table 7. The status register is used for diagnosing the main fault conditions : Over Current Protection (OCP), Under Voltage Lockout (UVLO) and Thermal Shutdown (TSD). When these three faults occur, the LNB output is disabled and the bit is latch to 1 until the RT5007 is read by the master, assuming the fault has been resolved. The status register is updated on the rising edge of the 9th clock pulse in the data read sequence.

The Disable bit (DIS) is used to indicate the current condition of the LNB output. It is set when either a fault occurs or if the LNB is disabled intentionally by the I^2C^{TM} master. This bit isn't latched if the LNB is commanded on again.

The OCP bit is set to 1 if the LNB output detects an over current condition (typ. 500mA) over than 5ms. Where the OCP bit is reset in all cases, allowing the master to enable the LNB output. If this bit has been set, please check that the output loading is short or too heavy before re-enable again.

The Power Not Good (PNG) is used for over voltage (typ. 109%) or under voltage (typ. 91%) detection of the LNB output voltage. If the LNB disabled or the output voltage is abnormal, PNG reports a logic 1 until the LNB output is enabled.

The TSD bit indicates 1 when the RT5007 has detected the over-temperature condition. The disable bit, DIS, will also be set. If the condition is no longer present, then the TSD bit will be reset, allowing the master to enable the LNB output if required. If the condition is still present, then the TSD bit will remain at 1.

The UVLO bit, 1 is indicated that the RT5007 has detected that the input supply is below the minimum level. The disable bit, DIS, will also be set and the RT5007 will not re-enable the output until the condition is no longer present, then the UVLO bit will be reset allowing the master to re-enable the LNB output if required. If the condition is still present, then the UVLO bit will remain at 1.

The DIS, PNG bits are reset without an I^2C^{TM} read sequence. The power on sequence of the master in a fault condition is to check the fault status by reading the Status registers then removing the fault condition until the status bit is reset. The fault may be detected either by continuously polling status registers or by responding to an interrupt request (IRQ).

Table 6. RT5007 Status Register 1

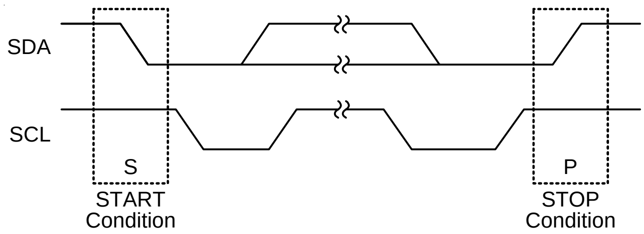
Status Address		RT5007 Status Register 1		
Bit	Bit Name	Default	Access	Description
0	DIS	0	R	LNB output disable
1		0	R	Not used
2	OCP	0	R	Over current
3		0	R	Not used
4	PNG	0	R	Power not good
5		0	R	Not used
6	TSD	0	R	Thermal shutdown
7	UVLO	0	R	VIN under voltage

I^2C Interface

User can communicate with RT5007 by microcontroller via the two wires I^2C. The two lines SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-high resistor (typ. 4.7kΩ). The level of logic "0" and logic "1" is defined in the "Electrical Specifications" table. The output stages of RT5007 will have an open drain/ open collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred up to 100kbps in the standard mode or up to 400kbps in the fast mode. One clock pulse is generated for each data bit transferred.

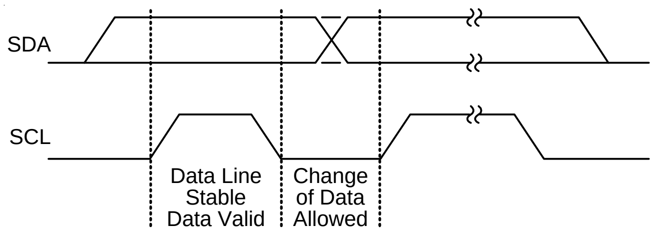
START and STOP Conditions

START condition is the SDA line level transition from high to low while SCL is high level. The STOP is the SDA line level transition from low to high while SCL is high level. Each command has to begin with a START condition and finish by a STOP condition.



Data Validity

The high or low level of the data line can only change when the SCL is low level. The data on the SDA line must be stable during the high period of the clock.

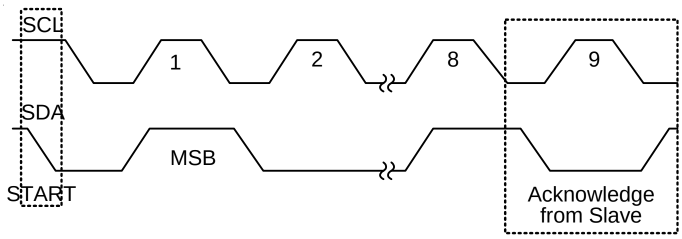


Byte Format

Every part the SDA and SCL line must be 9 bits long. There are 8 bits for a data byte and the 9th is the acknowledged bit. The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transferred with the most significant bit first (MSB).

Acknowledge

The master puts a resistive high level on the SDA line during the acknowledge clock pulse. The slave has to pull-low the SDA line during the acknowledge clock pulse. This behavior is called acknowledge, ACK. If the slave doesn't pull the SDA low, that is NACK (Not-Acknowledged) behavior. The RT5007 will not generate the ACK if the input voltage is under UVLO.



Transmitted Data (I^2C Bus Write Mode)

In writing mode, the master (microcontroller) transmits the 8 bits data (MSB transmitted first) after START condition. Then the slave (RT5007) has to feedback an ACK condition during the acknowledge clock pulse if the data receiving is OK. The master transmitter can generate the STOP condition to end the transfer.

Received Data (I^2C Bus Read Mode)

In reading mode, after the user transmits the slave address and data address, the master changes to RT5007 and the slave becomes the microcontroller. As for the following master generated clock bits, the RT5007 issues a byte on the SDA data bus line (MSB transmitted first) and the ACK condition is generated by microcontroller. After receiving the last data, the microcontroller enables a NACK condition to issue the data from master and the STOP condition to end the transfer.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for

WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

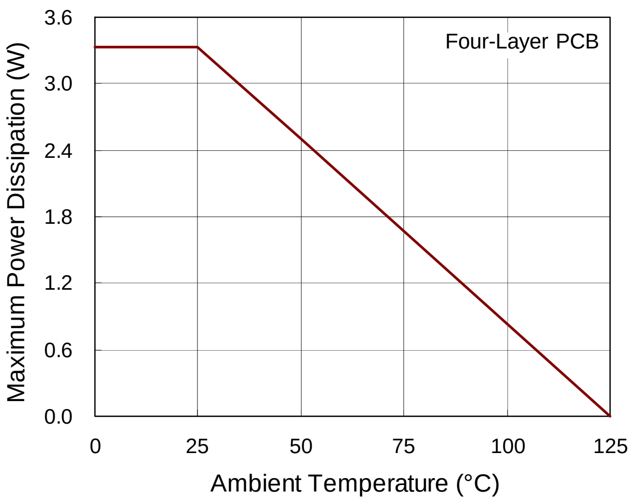


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short enough especially for the high current loop.
- Minimize the size of the LX node and keep it wide and shorter.
- The exposed pad of the chip should be connected to a strong ground plane for maximum thermal consideration.

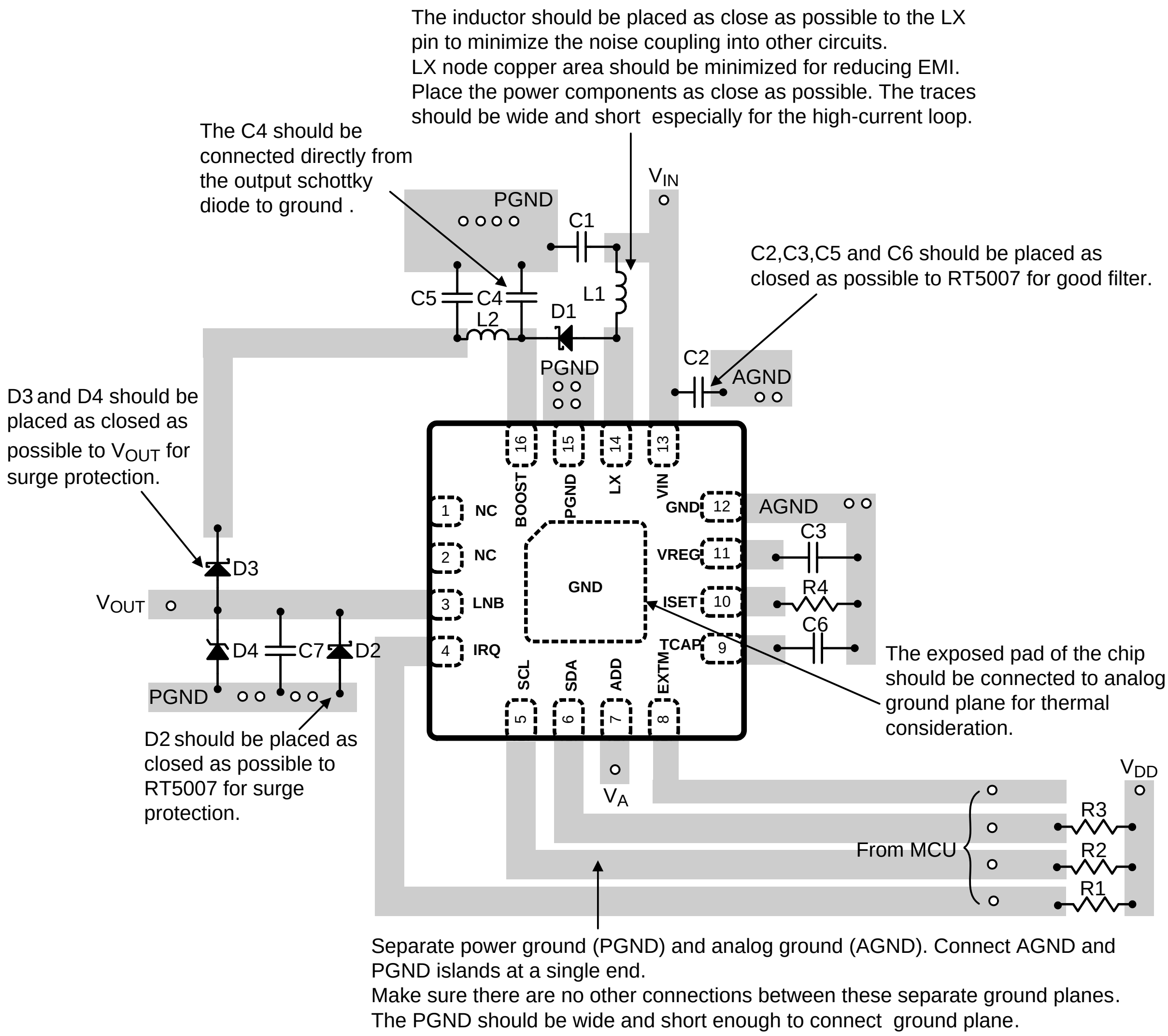
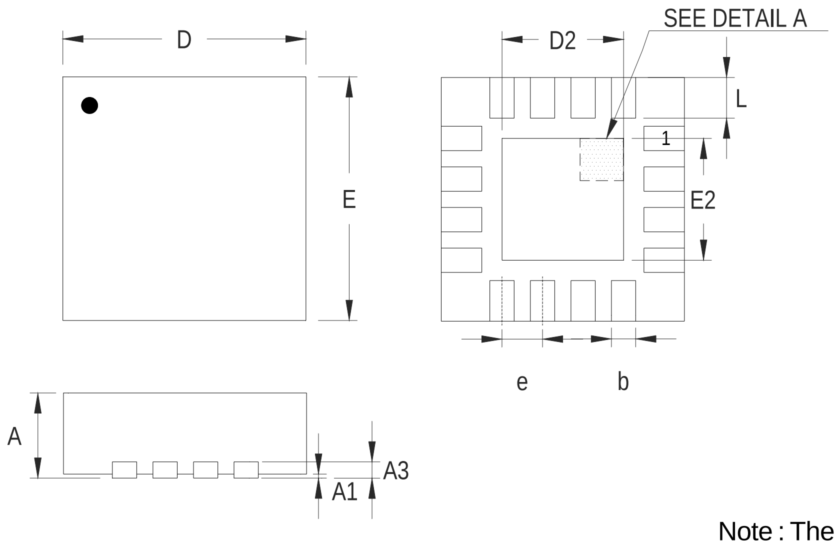
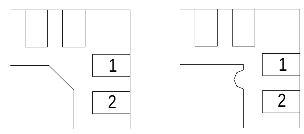


Figure 6. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789