7+6 Channels Power Management IC for DSC

General Description

The RT5014 is a complete power supply solution for digital still cameras and other hand held devices. The RT5014 is a multi-channel DC/DC power management unit including one synchronous step-up DC/DC converter with load disconnect (CH1), one selectable synchronous step-up/step-down DC/DC converter (CH2), two synchronous step-down DC/DC converters (CH3/4), one synchronous high voltage step-up DC/DC converter (CH5), one asynchronous inverting DC/DC converter (CH6) and one WLED driver in synchronous high voltage step-up mode or current regulator mode (CH7). Besides, the RT5014 also includes six LDO regulators: one RTC_LDO, one High Voltage LDO for CCD+ bias power (CH8), one high PSRR LDO for AFE power (CH9), and three generic LDOs (CH10 to CH12). All P-MOSFETs are integrated and all frequency compensation network needed by DC/DC converters are built-in. RT5014 uses one sequence selection pin SEQ to select five preset sequences and uses I^2C control interface to enable channels and adjust CH1/5/6/8/9/10/11/12 output voltage level and WLED dimming ratio and OVP threshold. RT5014 also includes a system reset function to monitor battery voltage.

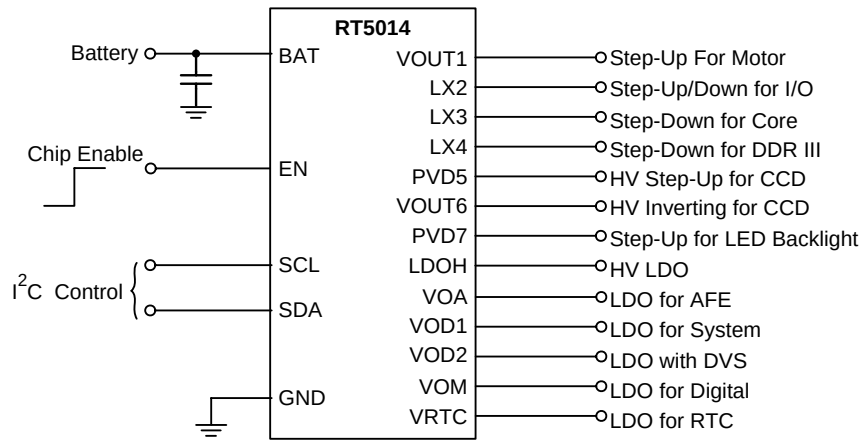
The RT5014 is designed to fulfill the applications for DSC as follows : CH1 is a synchronous step-up output for motor power. CH2 is a selectable synchronous step-up/step-down output for system I/O power. The operation mode is auto-selected by detecting external components topology. CH3 and CH4 are synchronous step-down outputs for DSP core and memory power supply. CH5 and CH8 HVLDO are for CCD+ bias power supply. CH6 is an asynchronous inverting output for negative CCD– bias power supply. CH7 is a WLED driver, auto-selected to be in synchronous high voltage step-up mode or current regulator mode.

Besides switching converters, RT5014 has some LDO regulators : CH9 is a LDO for AFE power. CH10 is 3.1V LDO for system, enabled in the preset power sequence. CH11 is a LDO enabled via I^2C i/f for memory card and supports Dynamic Voltage Scaling function. CH12 is a LDO for memory card or PLL. CH10 default voltage and enabling are controlled in power sequence selected by pin SEQ. And one keep-alive 3.3V LDO for RTC power supply.

The RT5014 provides over current protection, thermal shutdown protection, over voltage protection, over load protection and under voltage protection to achieve complete protection.

The RT5014 is available in the WQFN-40L 5x5 package.

Simplified Application Circuit



Features

- Input Voltage 1.8V to 5.5V
- 7-CH DC/DC Converters
- 6-CH Linear Regulator
  - One HVLDO, 4 LVLDO (for Memory Card, PLL, AFE, SYS), One RTC-LDO
- All Power Switches Integrated
- All Step-Up Converters with Load Disconnect Function
- All DC/DC Converters with Internal Frequency Compensation
- All DC/DC Converters with Pulse Skip Mode Function
- Fixed 2MHz Operating Frequency for CH1/2/3/4 (Motor, SYS, CORE, MEM)
- Fixed 1MHz Operating Frequency for CH5/6/7 (CCD+, CCD–, WLED)
- CH2 Sync. Step-Up/Step-Down Auto-Selected by External Topology
- CH7 WLED Driver in Synchronous Step-Up or Current Regulator Auto-Selected by External Topology
  - 32 Steps Brightness Control for WLED Driver
  - 3 Step-Up OVP Thresholds Selected in I^2C Register
- Five Built-in Power On/Off Sequence for CH1/2/3/4/10/ (9, 11, 12)
- Built-in Soft-Start Function
- I^2C Control Interface : Support Fast Mode up to 400Kb/s
- CH1/5/6/8 with Built-in Feedback Resistors and Programmable Output Voltage Levels
  - CH6 can Choose External Feedback Path
  - CH1 Supports Dynamic Voltage Scaling
- CH10 LDO Output Voltage Programmable by I^2C
  - Default Voltage Preset in Power Sequence
- CH11 LDO Output Voltage Programmable by I^2C
  - Enabled by I^2C
  - Supports Dynamic Voltage Scaling
- Rich Protection Functions :
  - Under Voltage Protection (UVP) (That is, Short Circuit Protection)
  - Over Load Protection (OLP)
  - Over Voltage Protection (OVP)
  - Over Current Protection (OCP)
  - Over Temperature Protection (OTP)
  - VDDM and Battery UVLO Function
  - Battery OVP Function
- Low Power Consumption (Sleep Mode) <20μA
- Built-in System Reset Function to Monitor Battery Voltage
- 40-Lead WQFN 5x5 Package
- RoHS Compliant and Halogen Free

Applications

- CCD-Sensor DSC
- CMOS-Sensor DV

Ordering Information

RT5014 □□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

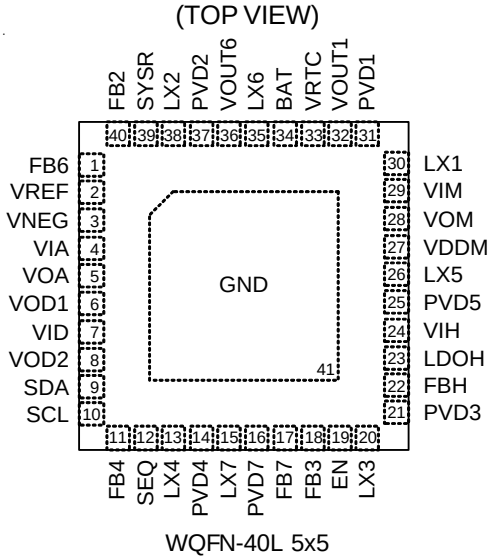
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT5014GQW : Product Number

YMDNN : Date Code

Pin Configurations



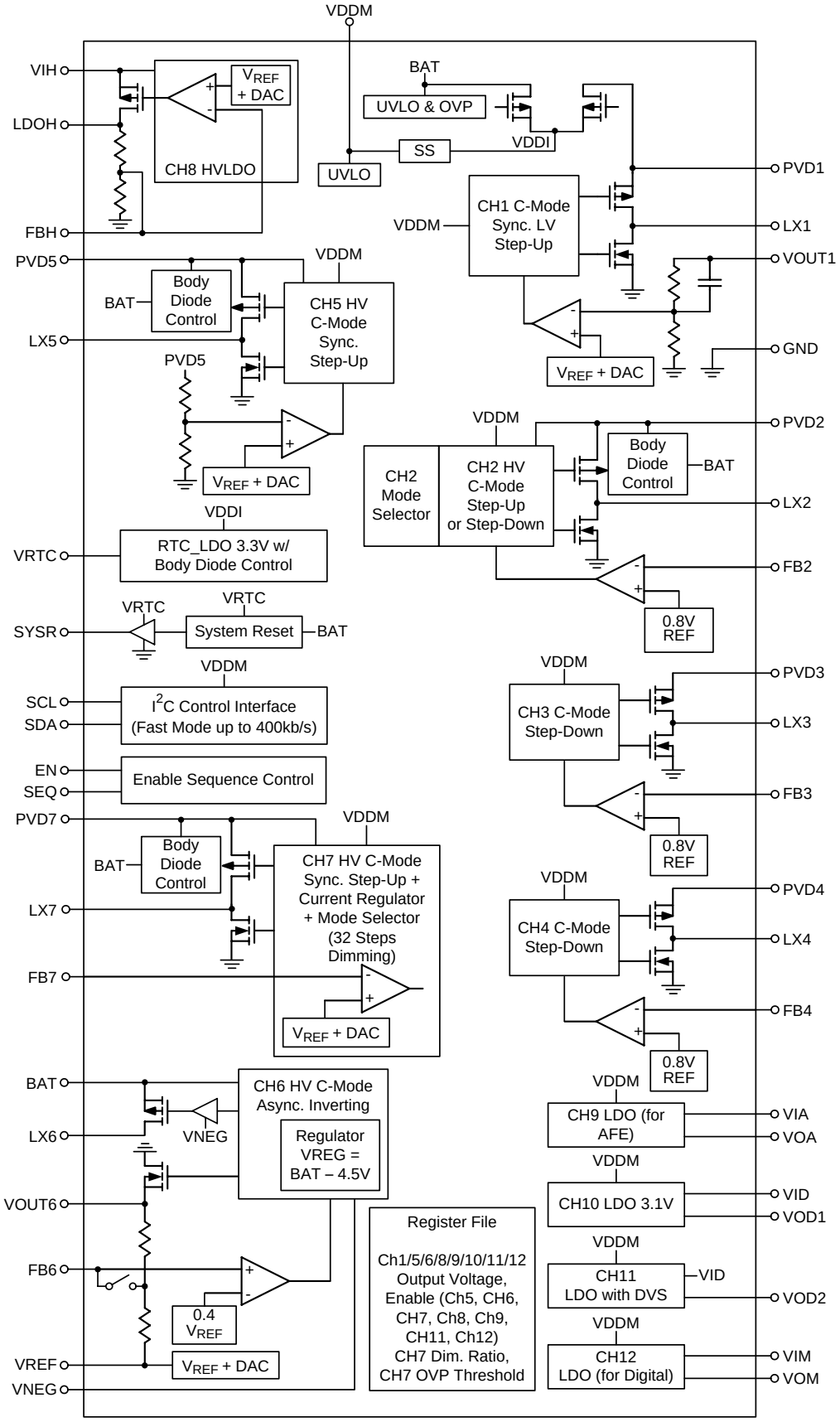
WQFN-40L 5x5

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB6	Feedback Input of CH6.
2	VREF	Output of CH6 Reference Voltage.
3	VNEG	Output Pin of Negative Regulator. The output voltage is regulated to BAT – 4.5V. It provides negative rail power for CH3, CH4, and CH6 P-MOSFET Driver. It needs a 0.1μF external decoupling capacitor.
4	VIA	CH9 LDO Power Input.
5	VOA	CH9 LDO Output.
6	VOD1	CH10 LDO Output.
7	VID	LDO Power Input of CH11 and CH10.
8	VOD2	CH11 LDO Output.
9	SDA	Data Signal Pin of I^2C Interface.
10	SCL	Clock Signal Pin of I^2C Interface.
11	FB4	Feedback Input of CH4.
12	SEQ	Input Pin of Power Sequence Selection. The Power Sequence is based on the external pull down resistance or voltage level at SEQ pin.
13	LX4	Switch Node of CH4.
14	PVD4	Power Input of CH4.
15	LX7	Switch Node of CH7 in Step-Up Mode or Current Output Port of CH7 in Current Source Mode.
16	PVD7	Power Output Pin of CH7 in Step-Up Mode or Power Input Port of CH7 in Current Source Mode.
17	FB7	Feedback Input of CH7 in Step-Up Mode and Current Source Mode.
18	FB3	Feedback Input of CH3.
19	EN	Enable Pin of CH1, CH2, CH3, CH4 and CH10. The power sequence is based an the setting of SEQ Pin.

Pin No.	Pin Name	Pin Function
20	LX3	Switch Node of CH3.
21	PVD3	Power Input of CH3.
22	FBH	Feedback Input of HVLDO.
23	LDOH	Output of HVLDO.
24	VIH	Power Input of HVLDO.
25	PVD5	Power Output of CH5.
26	LX5	Switch Node of CH5.
27	VDDM	IC Analog Power Pin.
28	VOM	CH12 LDO Output.
29	VIM	CH12 LDO Power Input.
30	LX1	Switch Node of CH1.
31	PVD1	Power Output of CH1.
32	VOUT1	Feedback Input of CH1 Output Voltage.
33	VRTC	RTC-LDO Power Output.
34	BAT	Battery Sense and Power Input Pin. The BAT pin must be connected to the power input of each converter (CH1 to CH7).
35	LX6	Switch Node of CH6.
36	VOUT6	Sense Input of CH6 Inverting Output Voltage.
37	PVD2	Power Input for Step-Down of CH2. Power Output for Step-Up of CH2.
38	LX2	Switch Node of CH2.
39	SYSR	Push-Pull Output Pin of System Reset to Monitor the Voltage Level at Pin BAT.
40	FB2	Feedback Input of CH2.
41 (Exposed Pad)	GND	Exposed PAD Should be Soldered to PCB and Connected to GND.

Function Block Diagram



Operation

The RT5014 is a complete power supply solution for digital still cameras and other hand held devices. It includes 7 DC/DC converters, one High Voltage LDO for CCD+ bias power, one high PSRR LDO for AFE power, three generic LDOs, and one RTC LDO.

CH1

Step-up synchronous current mode DC/DC converter with internal power MOSFETs and compensation network. The P-MOSFET can be controlled to disconnect the load. It is suitable for providing power to the motor.

CH2

Selectable synchronous step-up/step-down output for system I/O power. The operation mode is auto-selected by detecting external signals.

CH3

Step-down synchronous current mode DC/DC converter with internal power MOSFETs for DSP core power supply.

CH4

Step-down synchronous current mode DC/DC converter with internal power MOSFETs for memory power supply.

CH5

High voltage step-up synchronous current mode DC/DC converter with internal power MOSFET and compensation network. The P-MOSFET can be controlled to disconnect the load.

CH6

Asynchronous inverting current mode DC/DC converter with internal power MOSFET and compensation network. An external Schottky diode is required. This channel supplies the CCD negative bias.

CH7

WLED driver operating in either current source mode or synchronous step-up mode with internal power MOSFET and compensation network. The operation mode is determined via the I^2C interface.

CH8

High voltage LDO for CCD positive bias power supply.

CH9

High PSRR LDO for AFE power.

CH10

LDO for system, enabled in the preset power sequence.

CH11

LDO for memory card and supports Dynamic Voltage Scaling function.

CH12

Low input voltage LDO for memory card or PLL.

RTC LDO

Keep-alive 3.3V LDO for real-time clock.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VDDM ---------- –0.3V to 6V
- Switch Node Voltage, LX1, LX2, LX3, LX4 ---------- –0.3V to 6V
- Switch Node Voltage, LX5, PVD5, VIH, LDOH ---------- –0.3V to 24V
- Switch Node Voltage, LX7, PVD7 ---------- –0.3V to 26V
- Switch Node Voltage, VOUT6, LX6 ---------- (BAT – 16V) to (BAT + 0.3V)
- Negative Output Voltage VNEG ---------- (BAT – 6V) to (BAT + 0.3V)
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 3.64W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 125°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VDDM ---------- 2.7V to 5.5V
- Supply Input Voltage, BAT ---------- 1.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DDM} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
BAT Startup Voltage	V_{ST}	For bootstrap	1.5	--	--	V
BAT UVLO		Falling	--	1.4	--	V
BAT UVLO Hysteresis			--	0.07	--	V
VDDM Over Voltage Protection		Rising	5.85	6	6.15	V
VDDM OVP Hysteresis			--	0.25	--	V
VDDM UVLO		Rising	2.2	2.4	2.6	V
Supply Current						
Shutdown Supply Current into BAT (Include I_{DDQ} of RTC LDO)	$I_{OFF-BAT}$	EN = L, and PMU off, V_{BAT} = 3.3V	--	10	20	μA
CH1 + CH2 + CH3 + CH4 Supply Current into VDDM	I_{Q1234}	Not Switching, V_{EN} = 3.3V	--	--	2000	μA
CH5 Supply Current into VDDM	I_{Q5}	Not Switching, A5.EN5 = 1	--	--	500	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH6 Supply Current into VDDM	I_{Q6}	Not Switching, V_{BAT} = 3.3V, A5.EN6 = 1	--	--	500	μA
CH7 in Step-Up Mode Supply Current into VDDM	I_{Q7B}	Not Switching, A5.EN7 = 1	--	--	500	μA
CH7 in Current Source Mode Supply Current into VDDM	I_{Q7C}	A5.EN7 = 1, V_{PVD7} = 5V	--	--	400	μA
Oscillator						
CH1, 2, 3, 4 Operation Frequency	F_{OSC}		1800	2000	2200	kHz
CH5, 6, 7 Operation Frequency	F_{OSC2}	CH7 in Step-Up mode	900	1000	1100	kHz
CH1 LV Sync Step-Up						
Output Voltage Accuracy at VOUT1		Target voltage defined at A1.VOUT1	–1.5	--	1.5	%
Minimum On-Time for PSM			--	100	--	ns
Soft-Start Time		V_{VOUT1} = 0 to 5V	--	4	--	ms
Maximum Duty Cycle (Step-Up)		VOUT1 < Target defined in A1.VOUT1	80	83	86	%
On-Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, V_{PVD1} = 3.3V	--	200	300	mΩ
		N-MOSFET, V_{PVD1} = 3.3V	--	150	250	
Current Limit (Step-Up)			2.2	3	4	A
Over Voltage Protection at PVD1			5.82	6	6.18	V
Under Voltage protection at PVD1			--	BAT – 0.8	--	V
Under Voltage protection at VOUT1			1.95	2.25	2.55	V
Over Load protection at VOUT1		Target Voltage is defined in A1.VOUT1	--	Target – 0.6	--	V
Off Discharge Current at PVD1		V_{PVD1} = 5V, V_{VDDM} = 3.3V	--	50	--	mA
Discharge Finishing Threshold at VOUT1			--	0.6	--	V
CH2 LV Sync Step-Up or Step-Down Selectable						
Feedback Regulation Voltage at FB2			0.788	0.8	0.812	V
Minimum On-Time for PSM			--	100	--	ns
Soft-Start Time		V_{FB2} = 0 to 0.8V	--	4	--	ms
Maximum Duty Cycle		V_{FB2} = 0.75V (Step-Up)	80	83	86	%
		V_{FB2} = 0.75V (Step-Down)	--	--	100	
On-Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, V_{PVD2} = 3.3V	--	200	300	mΩ
		N-MOSFET, V_{PVD2} = 3.3V	--	150	250	
Current Limit		(Step-Down)	1.2	1.6	2	A
		(Step-Up)	2.2	3	4	
Over Voltage Protection at PVD2		CH2 Step-Up only	5.82	6	6.18	V
Under Voltage Protection at PVD2		CH2 Step-Up only	--	BAT – 0.8	--	V
Under Voltage Protection at FB2			0.25	0.3	0.35	V
Over Load Protection at FB2			0.65	0.7	0.75	V
Off Discharge Current at PVD2		V_{PVD2} = 3.3V, V_{VDDM} = 3.3V (Step-Up)	--	50	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Discharge Current at LX2		V_{LX2} = 3.3V, V_{VDDM} = 3.3V (Step-Down)	--	50	--	mA
Discharge Finishing Threshold at FB2		Both Step-Up and Step-Down	--	0.1	--	V
CH3 LV Sync Step-Down						
Feedback Regulation Voltage at FB3			0.788	0.8	0.812	V
Minimum On-Time for PSM			--	50	--	ns
Maximum Duty Cycle		V_{FB3} = 0.75V	--	--	100	%
Soft-Start Time		V_{FB3} = 0 to 0.8V	--	4	--	ms
On-Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, V_{PVD3} = 3.3V	--	250	400	mΩ
		N-MOSFET, V_{PVD3} = 3.3V	--	150	250	
Current Limit			1.5	2	2.5	A
Under Voltage Protection at FB3			0.35	0.4	0.45	V
Over Load Protection at FB3			0.65	0.7	0.75	V
Off Discharge Current at LX3		V_{LX3} = 1V, V_{VDDM} = 3.3V	--	20	--	mA
Discharge Finishing Threshold at FB3			--	0.1	--	V
CH4 LV Sync Step-Down						
Feedback Regulation Voltage at FB4			0.788	0.8	0.812	V
Minimum On-Time for PSM			--	50	--	ns
Maximum Duty Cycle		V_{FB4} = 0.75V	--	--	100	%
Soft-Start Time		V_{FB4} = 0 to 0.8V	--	4	--	ms
On-Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, V_{PVD4} = 3.3V	--	250	400	mΩ
		N-MOSFET, V_{PVD4} = 3.3V	--	250	400	
Current Limit			1.2	1.6	2	A
Under Voltage Protection at FB4			0.35	0.4	0.45	V
Over Load Protection at FB4			0.65	0.7	0.75	V
Off Discharge Current at LX4		V_{LX4} = 1.8V, V_{VDDM} = 3.3V	--	30	--	mA
Discharge Finishing Threshold at FB4			--	0.1	--	V
CH5 HV Sync Step-Up						
Dropout Voltage Accuracy at (PVD5 – LDOH)		Target voltage defined at A2.DV5 = 4'b0000 to 4'b0111	Target – 0.15	Target	Target + 0.15	V
		Target voltage defined at A2.DV5 = 4'b1000 to 4'b1111	Target – 0.25	Target	Target + 0.25	
Minimum On-Time for PSM			--	300	--	ns
Maximum Duty Cycle		VIH < Target	91	93	97	%
Soft-Start Time		V_{VIH} = 0 to 14V	--	10	--	ms
On-Resistance of MOSFET		P-MOSFET, V_{PVD5} = 10V	--	1.2	1.5	Ω
		N-MOSFET, V_{VDDM} = 3.3V	--	0.6	0.8	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit		N-MOSFET	0.9	1.2	1.6	A
Over Voltage Protection at PVD5			20	22	24	V
Under Voltage Protection at PVD5		Target voltage defined at A2.DV5 + A2.LDOH	--	DV5 + LDOH x 0.5	--	V
Over Load Protection at PVD5		Target voltage defined at A2.DV5 + A2.LDOH ≠ 4'b0000	--	Target – 2	--	V
		Target voltage defined at A2.DV5 + A2.LDOH = 4'b0000	--	Target – 1	--	
Off Discharge Current at PVD5		V_{PVD5} = 14V, V_{VDDM} = 3.3V	--	20	--	mA
Discharge Finishing Threshold at PVD5			--	0.5	--	V
CH8 High Voltage LDO						
Input Voltage Range (VIH)			3.3	--	24	V
Quiescent Current into VIH		V_{VIH} = 14V, V_{LDOH} = 13V, I_{OUT} = 0mA	--	--	200	μA
Soft-Start Time		V_{LDOH} = 0 to 13V	--	10	--	ms
Dropout Voltage (VIH – LDOH)		I_{OUT} = 30mA	--	--	0.2	V
Output Voltage Accuracy at LDOH		Target voltage defined at A2.LDOH	–1.5	--	1.5	%
Under Voltage Protection at LDOH		VDDM = 3.3V, Target voltage defined at A2.LDOH	--	Target x 0.5	--	V
Current Limit			100	150	200	mA
PSRR+		I_{OUT} = 20mA, V_{VIH} = 14V, V_{LDOH} = 13V, at 1kHz	--	–50	--	dB
Off Discharge Current at LDOH		V_{VDDM} = 3.3V	--	--	20	mA
Discharge Finishing Threshold at LDOH			--	0.5	--	V
CH6 HV Async Inverting						
Output Voltage Accuracy at VOUT6		Target voltage defined at A1.VOUT6 [2:0] ≠ 3'b111	–1.5	--	1.5	%
(VREF – FB6) Regulation Voltage		A1.VOUT6 [2:0] = 3'b111	0.828	0.84	0.852	V
Feedback Regulation Voltage at FB6			0.38	0.4	0.42	V
VREF Load Regulation		0μA < I_{REF} < 200μA	--	--	10	mV
(BAT – VNEG) Regulation Voltage of Negative Regulator		V_{BAT} = 3.3V	4.1	4.5	4.9	V
Minimum On-Time for PSM			--	300	--	ns
Maximum Duty Cycle		V_{FB6} = 0.3V	91	93	97	%
Soft-Start Time		V_{OUT6} = 0 to –7V	--	10	--	ms
On-Resistance of MOSFET		P-MOSFET, V_{BAT} = 3.3V	--	0.5	0.7	Ω
Current Limit		P-MOSFET	1	1.5	2	A
Over Voltage Protection at VOUT6			--	–13	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Protection at FB6			0.7	0.8	0.9	V
Over Load Protection at FB6			--	0.55	--	V
Off Discharge Current at VOUT6		V_{OUT6} = –7V	--	20	--	mA
Discharge Finishing Threshold at VOUT6			--	–0.12	--	V
CH7 WLED Driver						
Feedback Regulation Voltage at FB7 (Both Step-Up and Current)		A0.DIM7 [4:0] = 5'b11111	0.237	0.25	0.263	V
Minimum On-Time for PSM (Step-Up)			--	300	--	ns
Maximum Duty Cycle (Step-Up Mode)		V_{FB7} = 0.15V	91	93	97	%
On-Resistance of MOSFET		P-MOSFET, V_{PVD7} = 10V	--	2	3	Ω
		N-MOSFET, V_{VDDM} = 3.3V	--	0.9	1.1	
Current Limit (Step-Up Mode)		N-MOSFET, V_{VDDM} = 3.3V	0.6	0.8	1	A
Over Voltage Protection at PVD7 (Step-Up Mode)		A0.OVP7 [1:0] = 2'b00	8.3	9	10	V
		A0.OVP7 [1:0] = 2'b01	14.2	15	16	
		A0.OVP7 [1:0] = 2'b1X	24.5	25.5	26.5	
Off Discharge Current at PVD7 (Step-Up Mode)		V_{PVD7} = 10V, V_{VDDM} = 3.3V	--	20	--	mA
Discharge Finishing Threshold at PVD7		(Step-Up Mode)	--	BAT – 0.2	--	V
CH9 LDO						
Input Voltage Range (VIA)			2.7	--	5.5	V
Quiescent Current into VIA		V_{VIA} = 3.3V, I_{OUT} = 0mA	--	--	75	μA
Regulation Voltage VOA		V_{VIA} = 3.3V, I_{OUT} = 0mA, A3.VOA [2:0] = 3'b001	3.054	3.1	3.146	V
Dropout Voltage (VIA – VOA)		I_{OUT} = 100mA, V_{VOA} = 3.1V	--	--	0.1	V
Load Transient Output Voltage drop at VOA		V_{VOA} = 3.1V, Load current step from 10mA to 100mA, C_{OUT} = 1μF	--	--	10	mV
PSRR+		I_{OUT} = 10mA, V_{VIA} = 3.3V, V_{VOA} = 3.1V at 1kHz	--	–60	--	dB
Under Voltage Protection at VOA		Target voltage defined at A3.VOA	--	Target x 0.5	--	V
Maximum Output Current (Current Limit)		V_{VIA} = 3.3V, V_{VOA} = 3.1V	400	550	700	mA
Off Discharge Current at VOA		V_{VDDM} = 3.3V	--	--	10	mA
CH10 LDO						
Input Voltage Range (VID)			2.7	--	5.5	V
Quiescent Current into VID		V_{VID} = 3.3V, I_{OUT} = 0mA	--	--	75	μA
Regulation Voltage VOA		A3.VOA [2:0] = 3'b000 to 3'b011	–1.5	--	1.5	%
		A3.VOA [2:0] = 3'b100 to 3'b111	–2	--	2	
Dropout Voltage (VID – VOD1)		I_{OUT} = 100mA, V_{VOD1} = 3.1V	--	--	0.1	V
PSRR+		I_{OUT} = 10mA, V_{VID} = 3.3V at 1kHz	--	–40	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Protection at VOD1		Target voltage defined at A4.VOD1	--	Target x 0.5	--	V
Maximum Output Current (Current Limit)		V_{VID} = 3.3V	400	550	700	mA
Off Discharge Current at VOD1		V_{VDDM} = 3.3V	--	--	10	mA
CH11 LDO						
Input Voltage Range (VID)			2.7	--	5.5	V
Quiescent Current into VID		V_{VID} = 3.3V, I_{OUT} = 0mA	--	--	75	μA
Regulation Voltage VOD2		A4.VOD2 [2:0] = 3'b000 to 3'b011	–1.5	--	1.5	%
		A4.VOD2 [2:0] = 3'b100 to 3'b111	–2	--	2	
Dropout Voltage (VID – VOD2)		I_{OUT} = 100mA, V_{VOD2} = 3.1V	--	--	0.06	V
PSRR+		I_{OUT} = 10mA, V_{VID} = 3.3V, V_{VOD2} = 3.1V at 1kHz	--	–40	--	dB
Under Voltage Protection at VOD2		Target voltage defined at A4.VOD2	--	Target x 0.5	--	V
Maximum Output Current (Current Limit)		V_{VID} = 3.3V, V_{VOD2} = 3.1V	400	550	700	mA
Off Discharge Current at VOD2		V_{VDDM} = 3.3V	--	--	10	mA
CH12 LDO						
Input Voltage Range (VIM)			1.5	--	5.5	V
Quiescent Current into VIM		V_{VIM} = 3.3V, I_{OUT} = 0mA	--	--	75	μA
Regulation Voltage VOM		A3.VOM [2:0] = 3'b000 to 3'b011	–1.5	--	1.5	%
		A3.VOM [2:0] = 3'b100 to 3'b111	–2	--	2	
Dropout Voltage (VIM – VOM)		I_{OUT} = 100mA, V_{VOM} = 3.1V	--	--	0.06	V
PSRR+		I_{OUT} = 10mA, V_{VIM} = 3.3V, V_{VOM} = 3.1V, at 1kHz	--	–40	--	dB
Under Voltage Protection at VOM		Target voltage defined at A4.VOM	--	Target x 0.5	--	V
Maximum Output Current (Current Limit)		V_{VIM} = 3.3V, V_{VOM} = 3.1V	400	550	700	mA
Off Discharge Current at VOM		V_{VDDM} = 3.3V	--	--	10	mA
RTC LDO						
Standby Quiescent Current		V_{BAT} = 4.2V	--	3	6	μA
Lockout Current into VRTC	$I_{LO-VRTC}$	EN = L, and PMU off, V_{BAT} = 0V, V_{RTC} = 3.1V, V_{VDDM} = 0V	--	--	1	μA
Regulation Voltage at VRTC		I_{OUT} = 0mA	3.24	3.3	3.36	V
Maximum Output Current (Current Limit)		V_{BAT} = 4.2V	60	130	200	mA
Dropout Voltage at (BAT – VRTC)		I_{OUT} = 50mA	--	--	1000	mV
		I_{OUT} = 10mA	--	--	150	
		I_{OUT} = 3mA	--	--	60	
Control						
EN Input High Level Threshold			1.3	--	--	V
EN Input Low Level Threshold			--	--	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Pull Down Current			--	1	3	μA
SEQ Pull High Threshold for Power Sequence #0		V_{BAT} = V_{VDDM} = 1.8V	0.2	--	--	V
SEQ Pull Down Resistance for Power Sequence #1		V_{BAT} = V_{VDDM} = 1.8V	36	40	44	kΩ
SEQ Pull Down Resistance for Power Sequence #2		V_{BAT} = V_{VDDM} = 1.8V	9	10	11	kΩ
SEQ Pull Down Resistance for Power Sequence #3		V_{BAT} = V_{VDDM} = 1.8V	2.25	2.5	2.75	kΩ
SEQ Pull Down Resistance for Power Sequence #4		V_{BAT} = V_{VDDM} = 1.8V	--	0.63	0.69	kΩ
System RESET						
SYSR Falling Threshold at BAT		When V_{BAT} < 1.4V, SYSR goes low.	1.372	1.4	1.428	V
SYSR Threshold Hysteresis Gap at BAT			--	0.07	--	V
BAT Deglitching Time for SYSR			--	10	--	μs
SYSR Rising Delay Time		V_{RTC} = 1.6V	--	10	--	ms
SYSR Output High Voltage		V_{RTC} = 3.3V, I_{SYSR} = –1mA (Source)	V_{RTC} – 0.5	--	V_{RTC}	V
SYSR Output Low Voltage		V_{RTC} = 3.3V, I_{SYSR} = 1mA (Sink)	0	--	0.5	V
Protection						
Protection Fault Delay			--	100	--	ms
Thermal Shutdown	T_{SD}		125	155	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C

(V_{DDM} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I^2C						
SDA, SCLK Input High Level Threshold			1.4	--	--	V
SDA, SCLK Input Low Level Threshold			--	--	0.6	V
SCLK Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated	$t_{HD,STA}$		0.6	--	--	μs
LOW Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
HIGH Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition	$t_{SU,STA}$		0.6	--	--	μs
Data Hold Time	$t_{HD,DAT}$		0	--	0.9	μs
Data Set-Up Time	$t_{SU,DAT}$		100	--	--	ns
Set-Up Time for STOP Condition	$t_{SU,STO}$		0.6	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Bus Free Time between a STOP and START Condition	t_{BUF}		1.3	--	--	μs
Rise Time of both SDA and SCL Signals	t_R		20	--	300	ns
Fall Time of both SDA and SCL Signals	t_F		20	--	300	ns
SDA and SCL Output Low Sink Current	I_{OL}	SDA or SCL voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

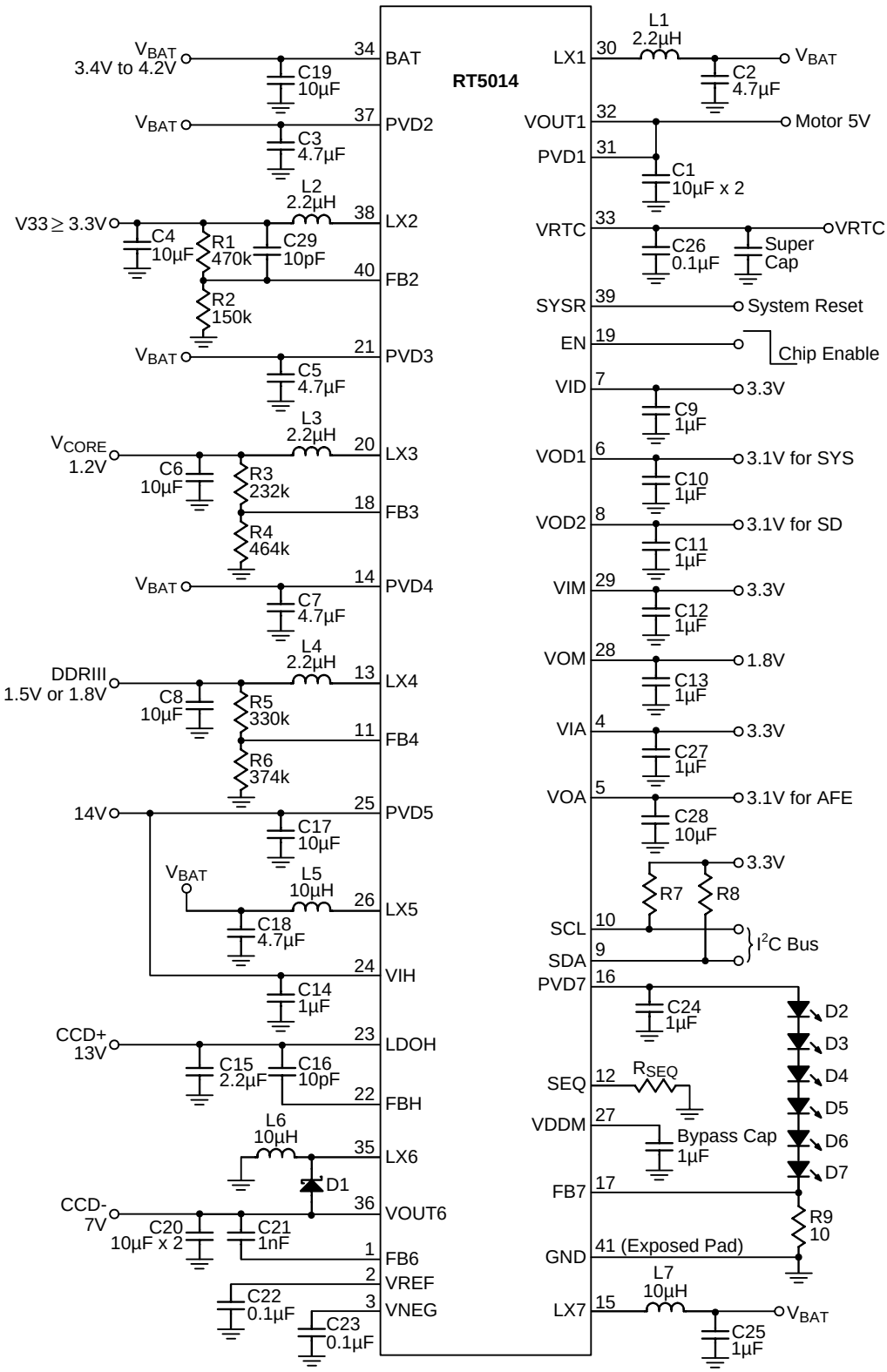


Figure 1. Typical Application Circuit for Li-ion Battery (3.4V to 4.2V)

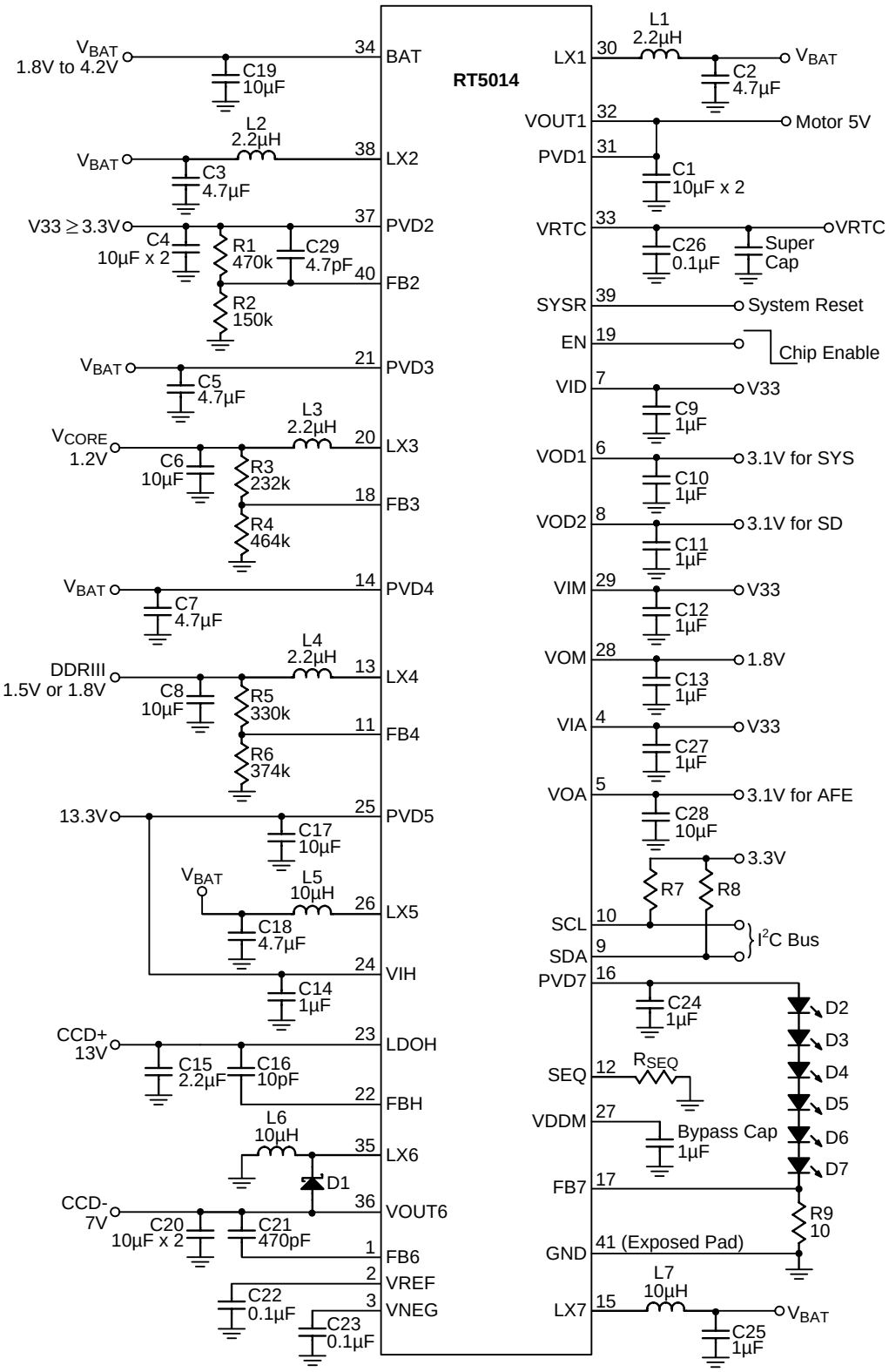


Figure 2. Typical Application Circuit for 2AA Battery (1.8V to 4.2V)

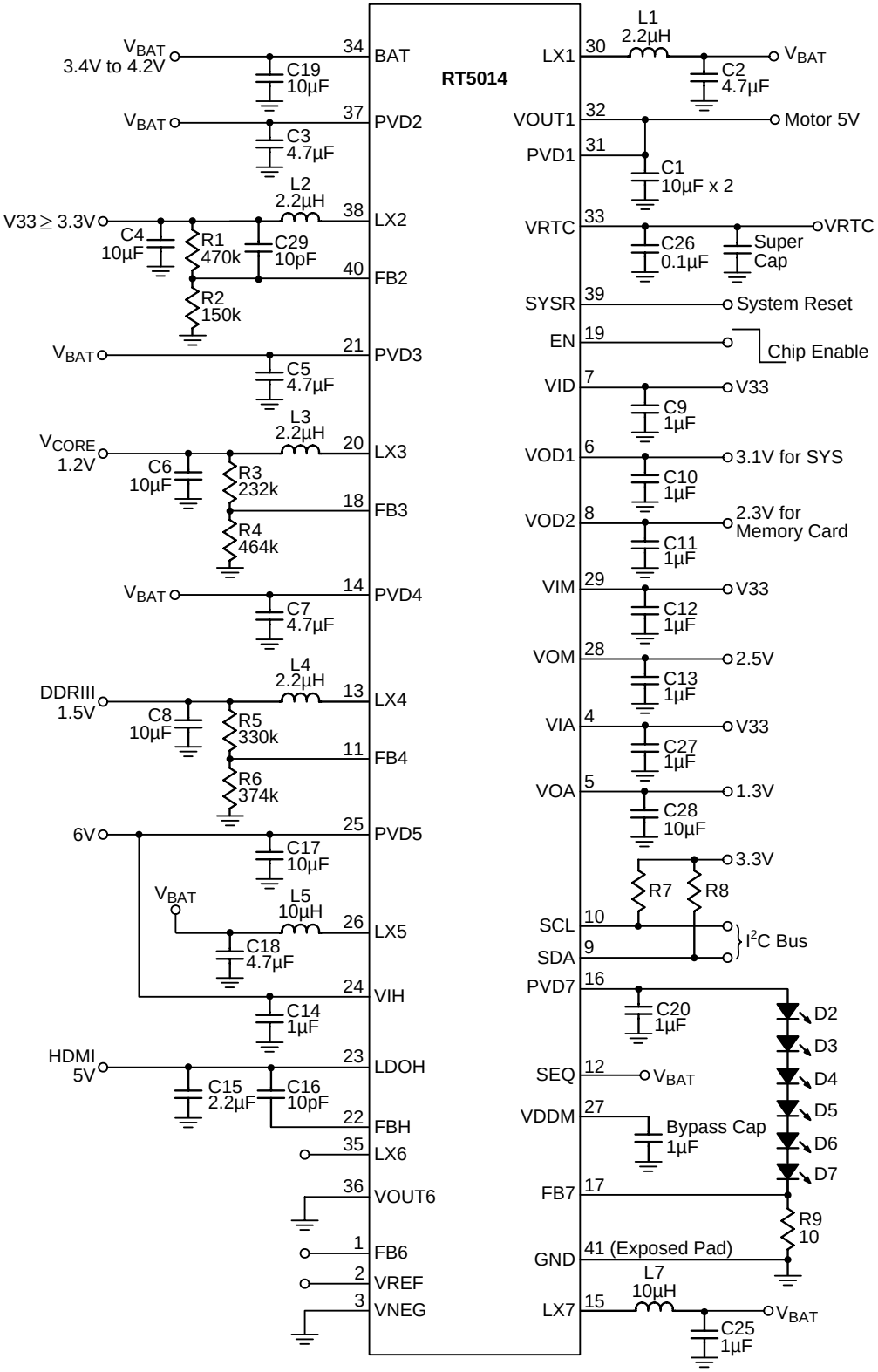


Figure 3. Typical Application Circuit for Ambarella A7 with Li-ion Battery (3.4V to 4.2V)

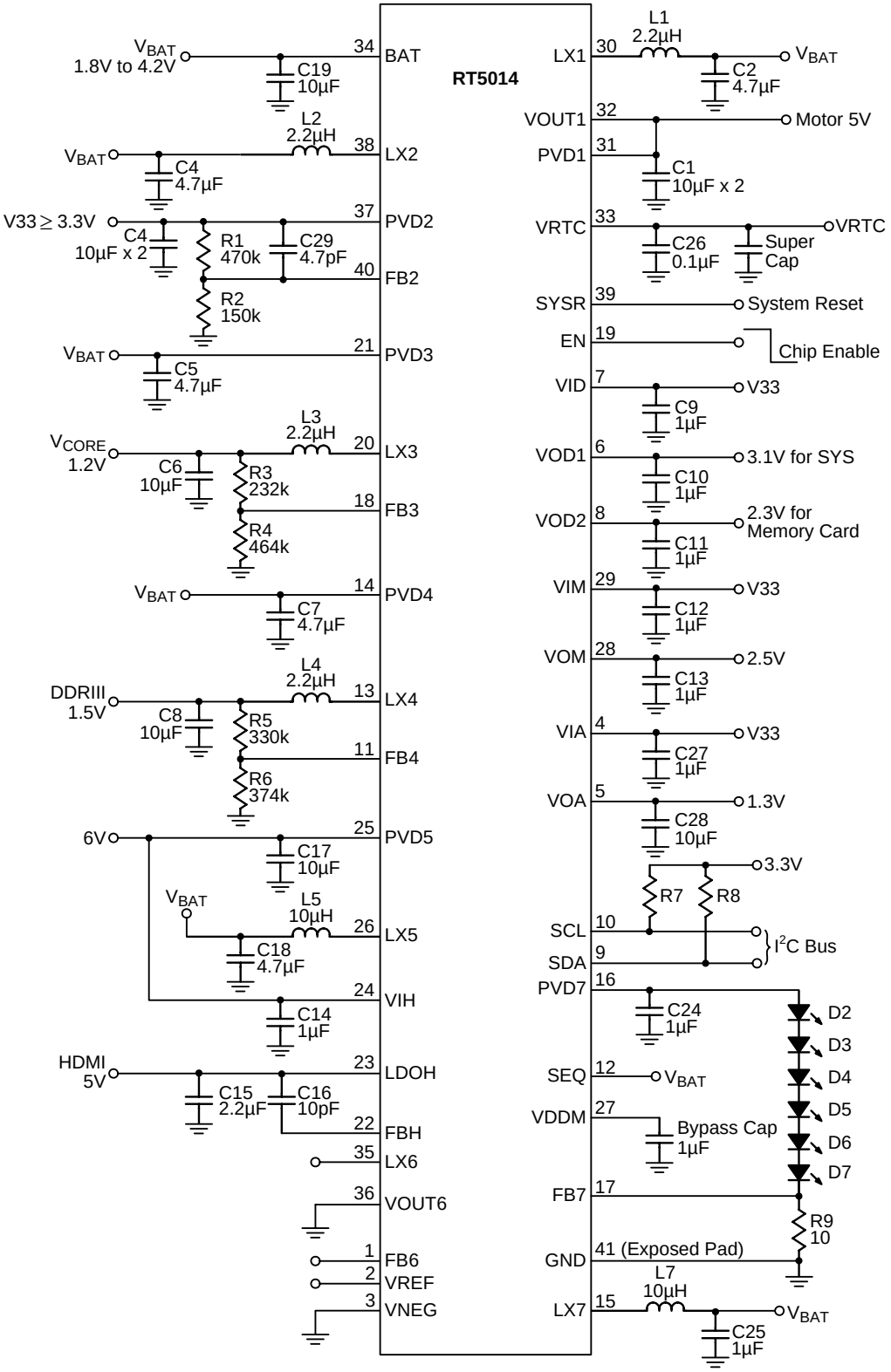


Figure 4. Typical Application Circuit for Ambarella A7 with 2AA Battery (1.8V to 4.2V)

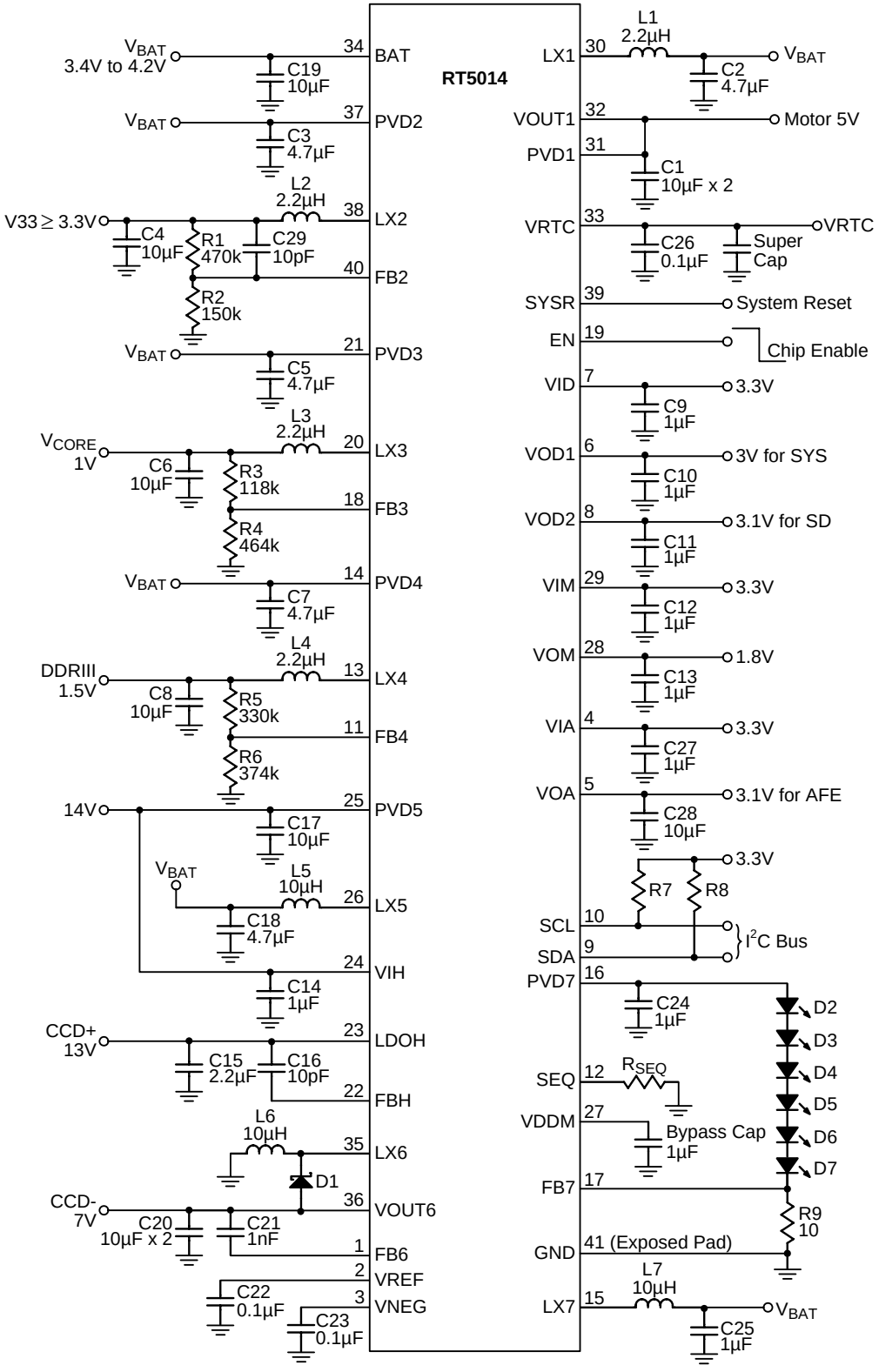


Figure 5. Typical Application Circuit for Ambarella A7L with Li-ion Battery (3.4V to 4.2V)

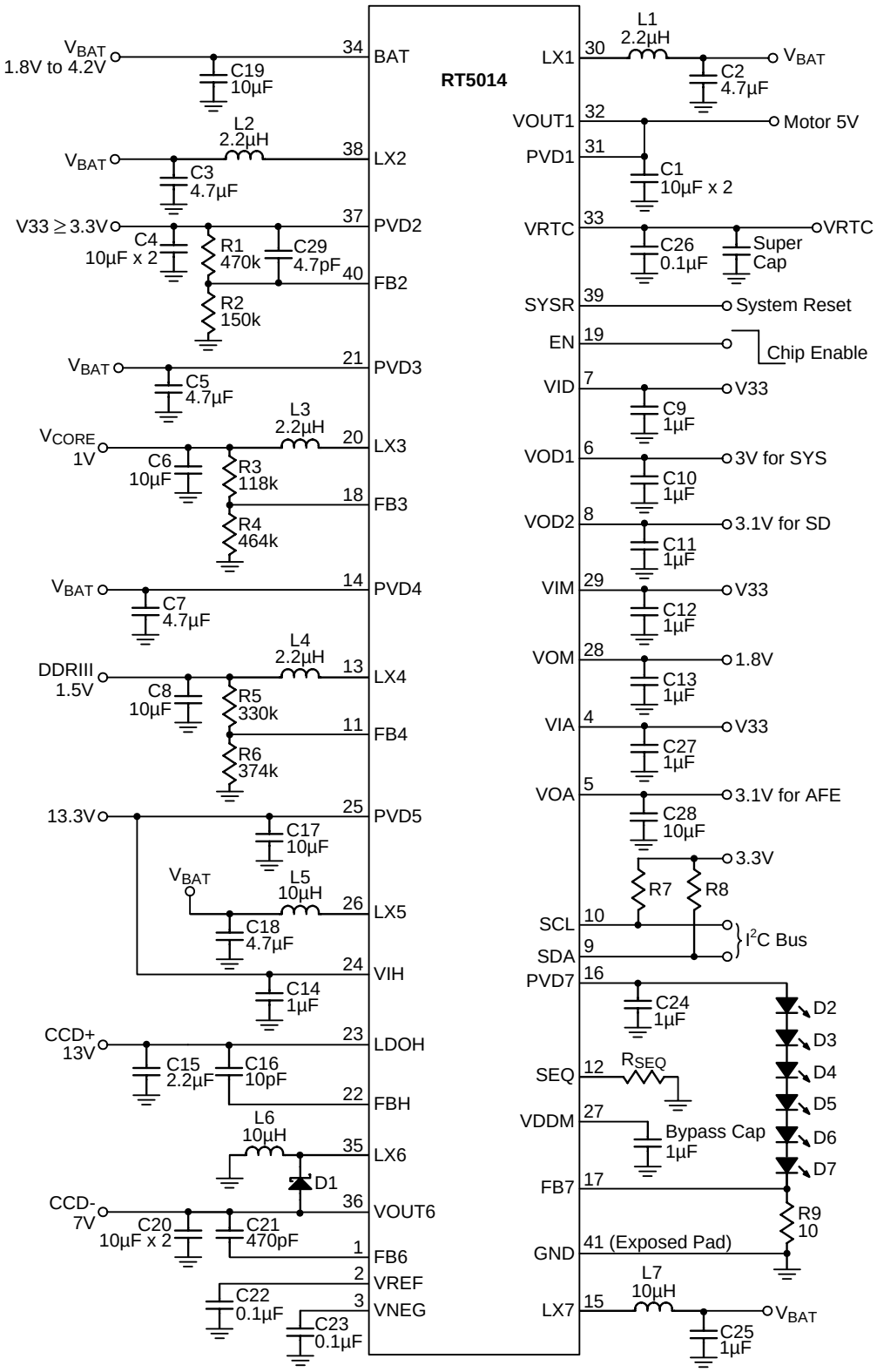
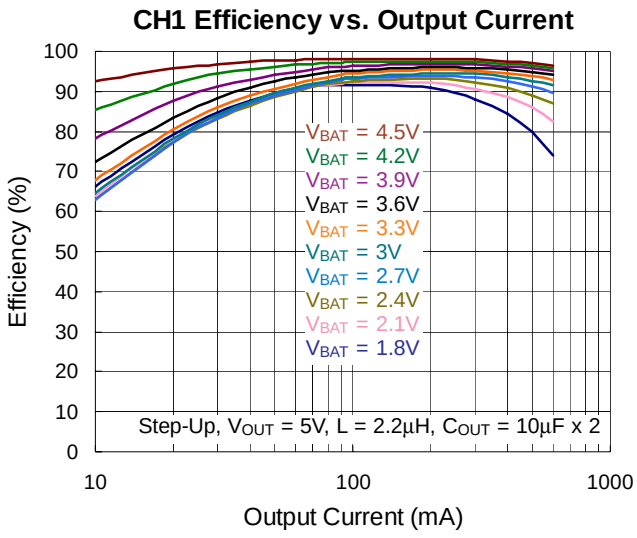
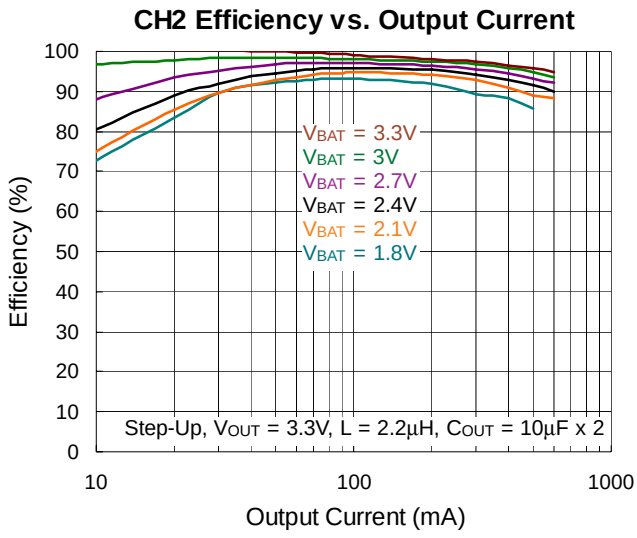
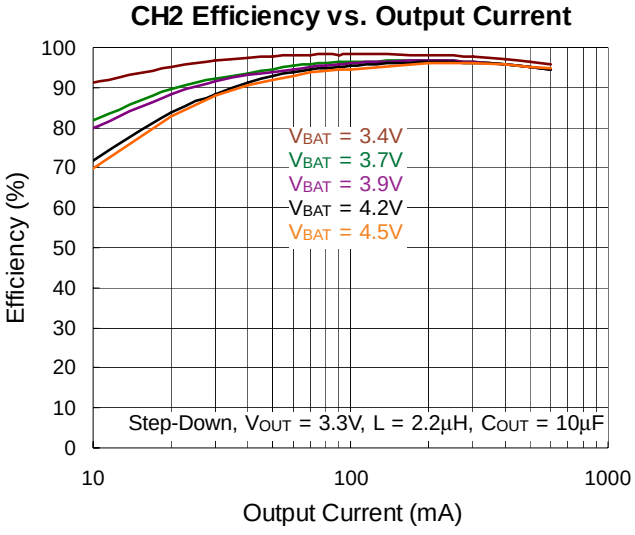


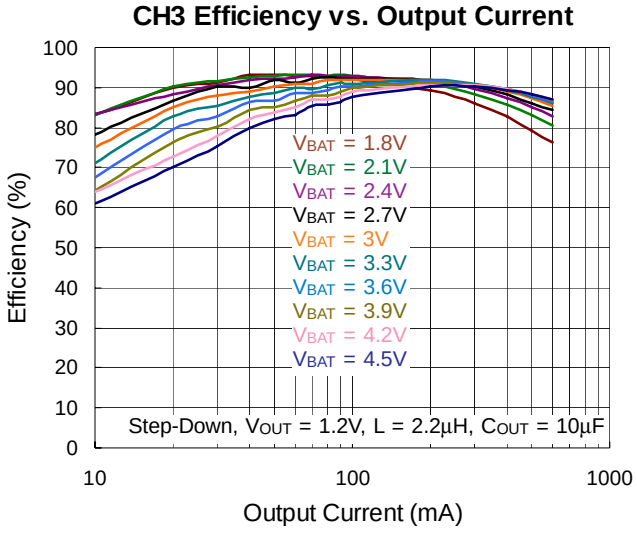
Figure 6. Typical Application Circuit for Ambarella A7L with 2AA Battery (1.8V to 4.2V)

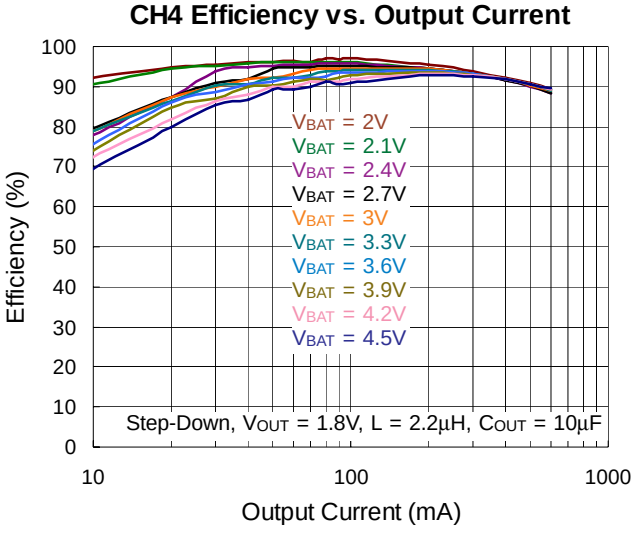
Typical Operating Characteristics

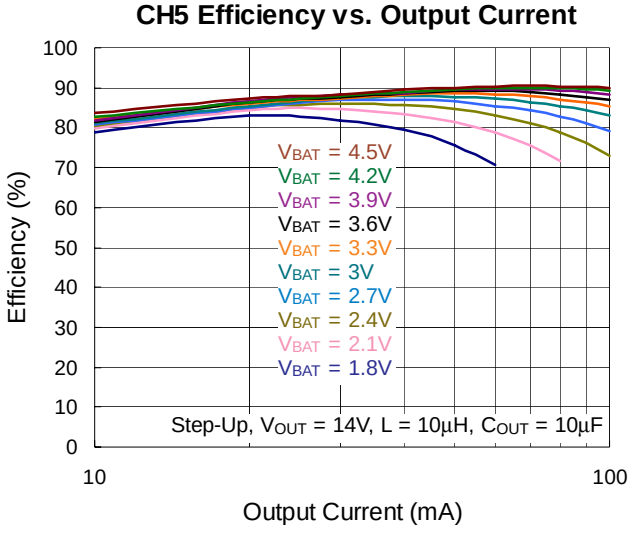




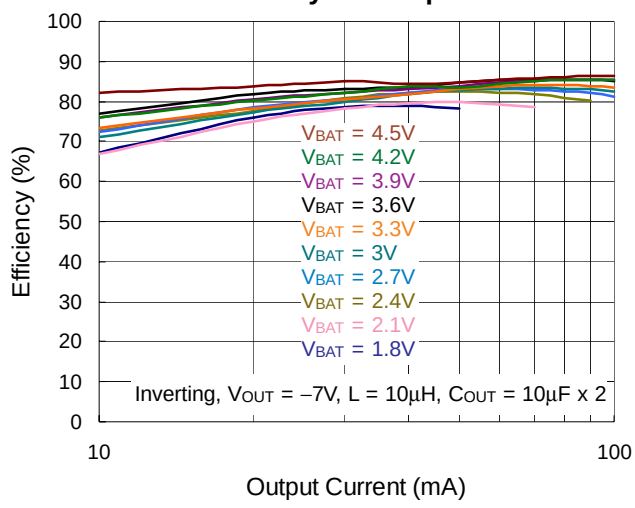




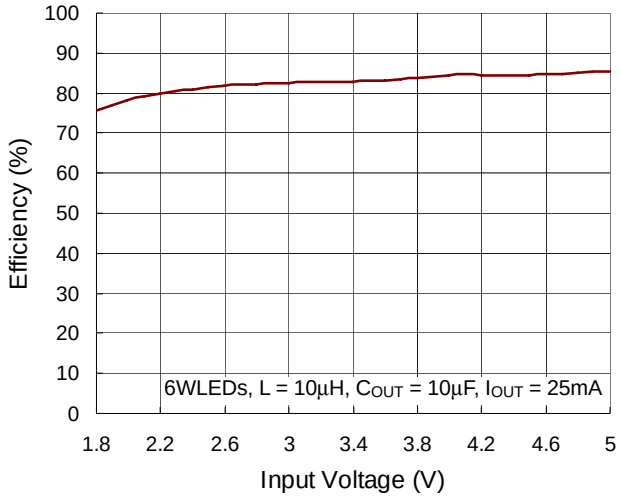




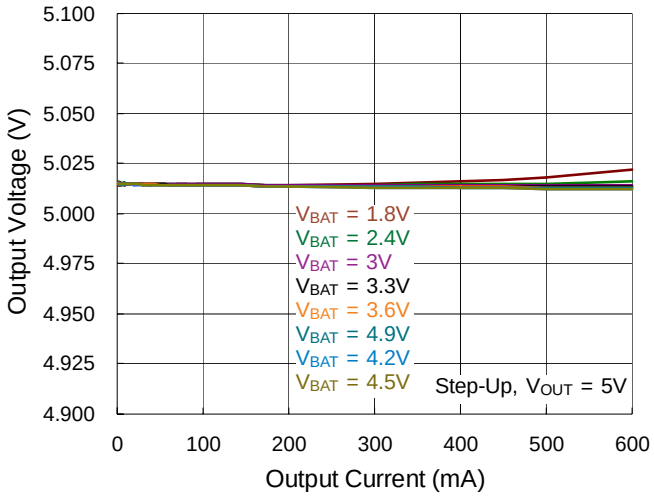
CH6 Efficiency vs. Output Current



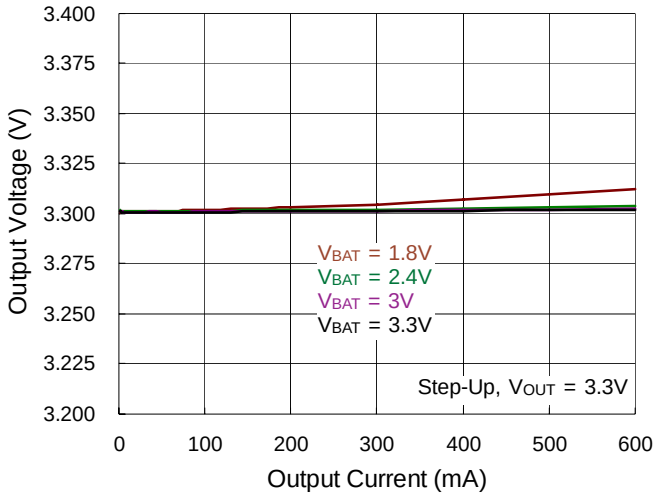
CH7 Efficiency vs. Input Voltage



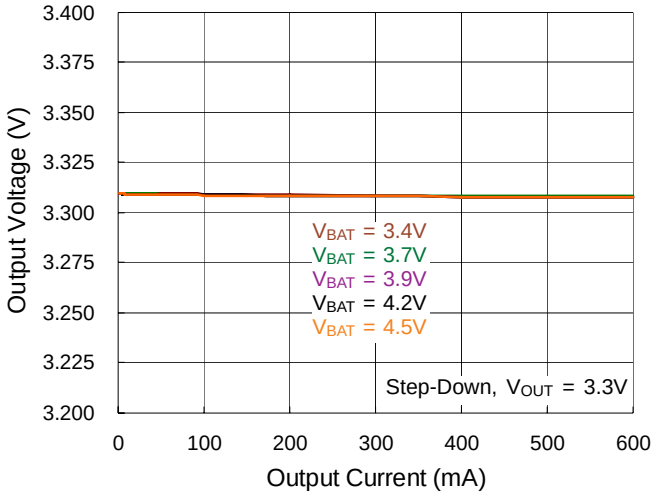
CH1 Output Voltage vs. Output Current



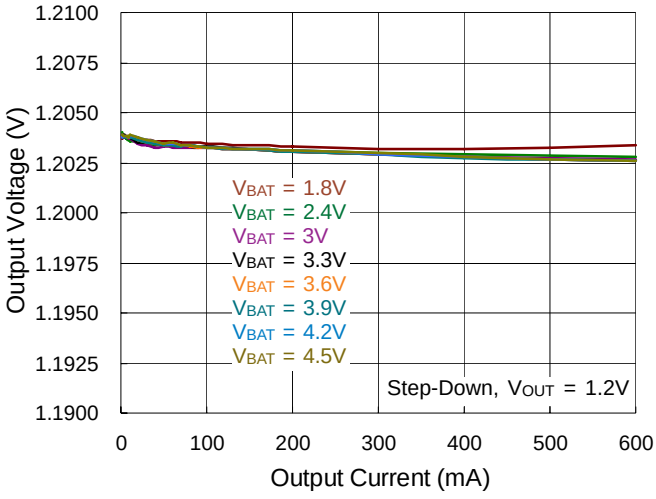
CH2 Output Voltage vs. Output Current



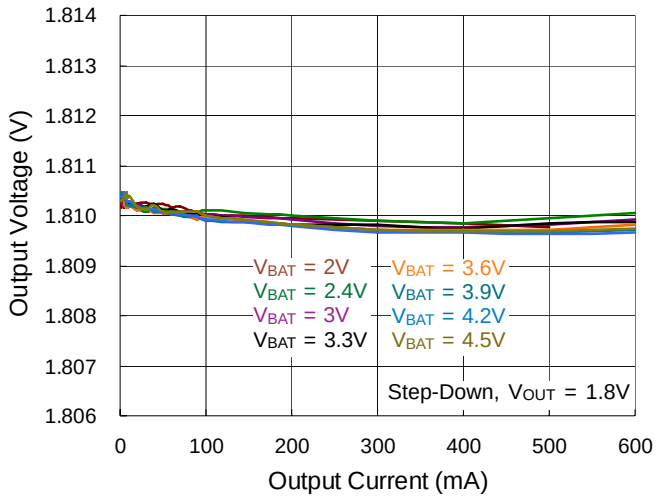
CH2 Output Voltage vs. Output Current



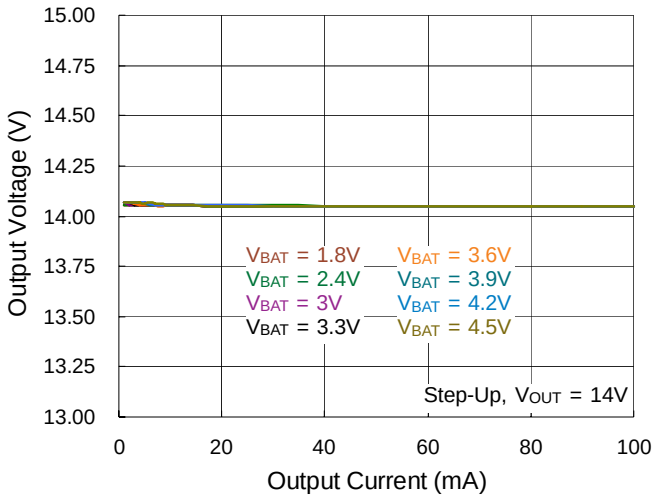
CH3 Output Voltage vs. Output Current



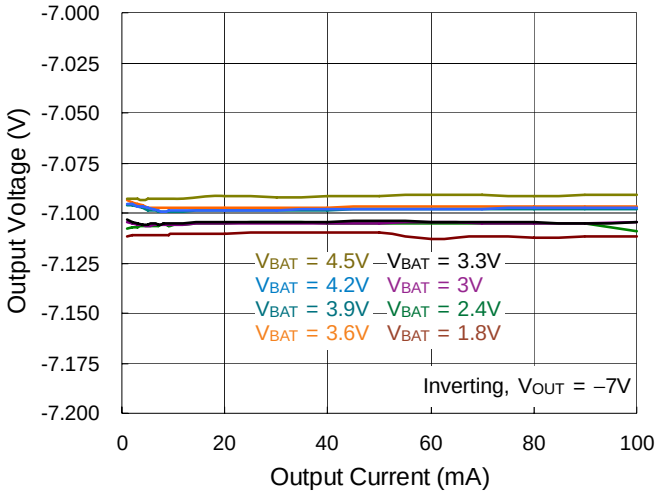
CH4 Output Voltage vs. Output Current



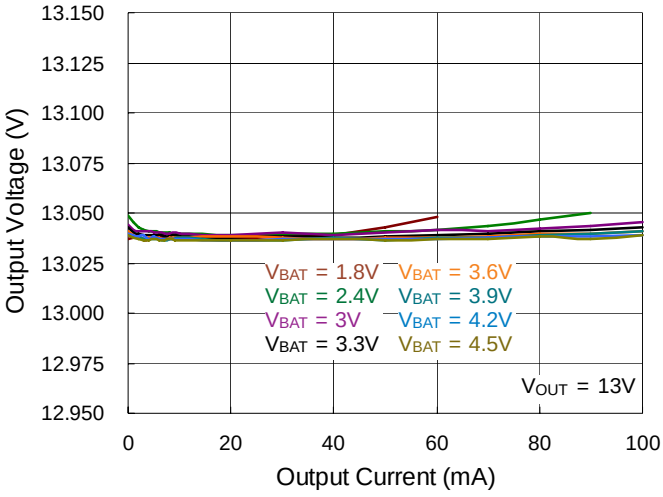
CH5 Output Voltage vs. Output Current



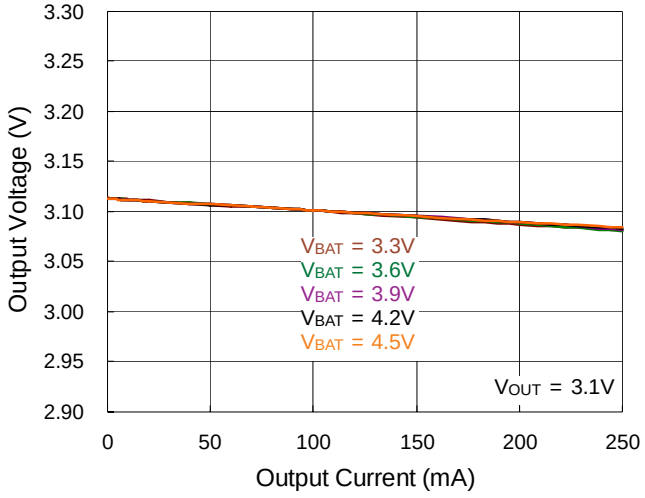
CH6 Output Voltage vs. Output Current



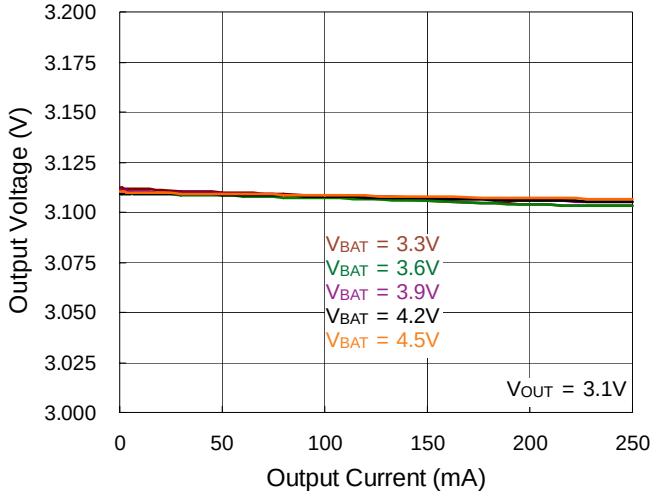
CH8 HV-LDO Output Voltage vs. Output Current



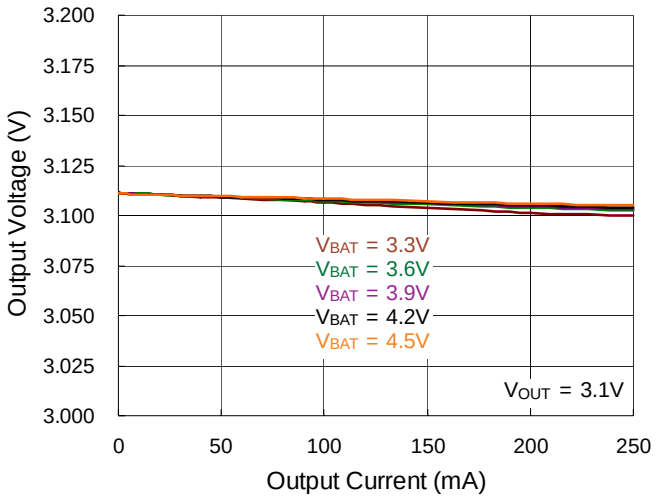
CH9 LDO Output Voltage vs. Output Current



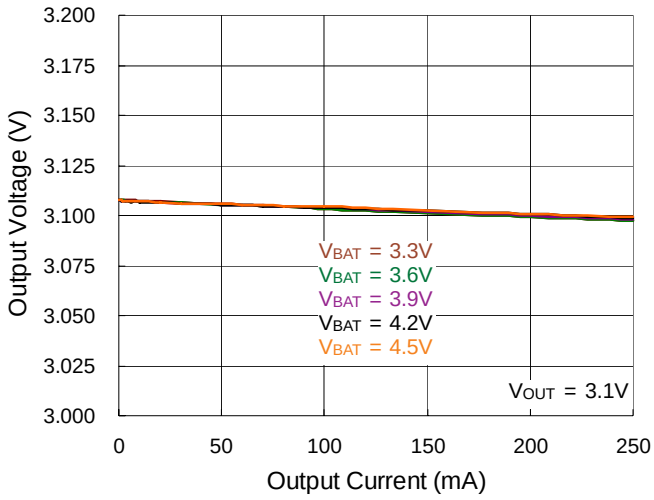
CH10 LDO Output Voltage vs. Output Current



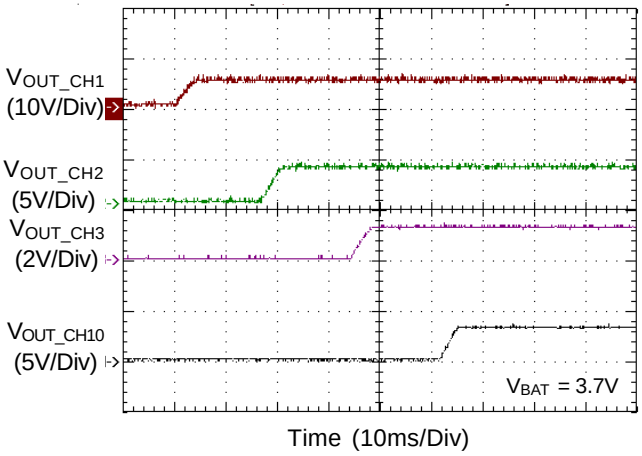
CH11 LDO Output Voltage vs. Output Current



CH12 LDO Output Voltage vs. Output Current



Power On Sequence 0



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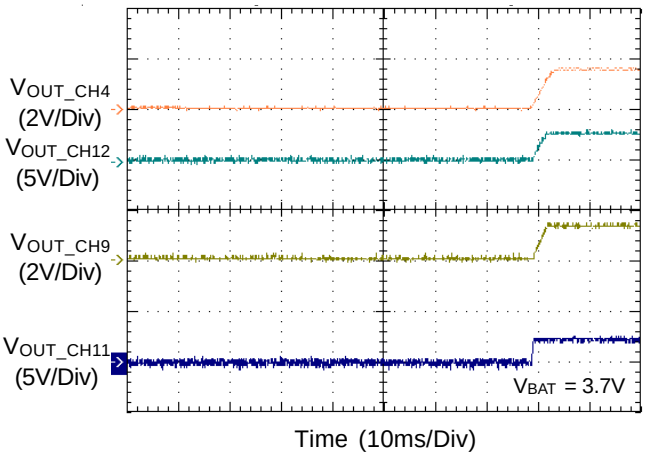
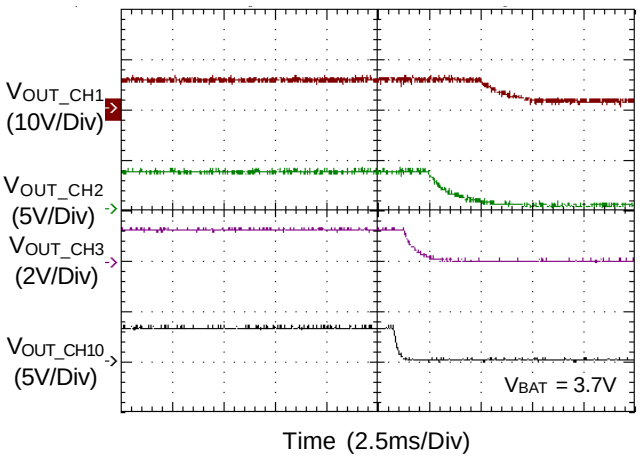


Power Off Sequence 0



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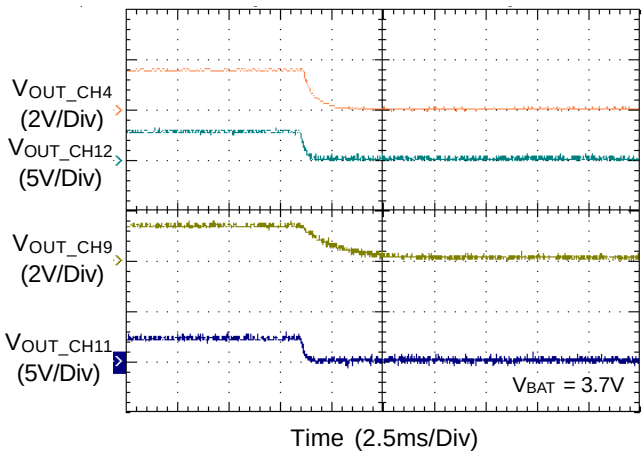
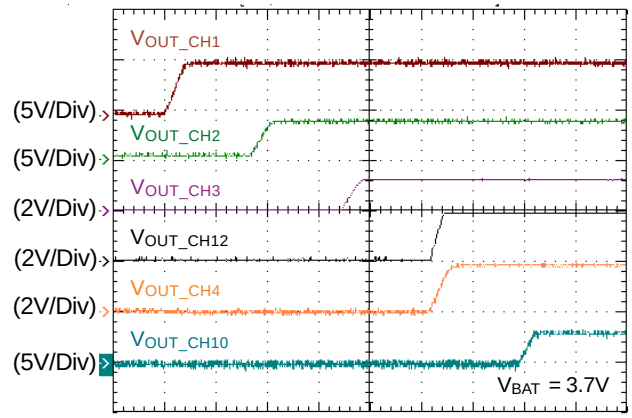
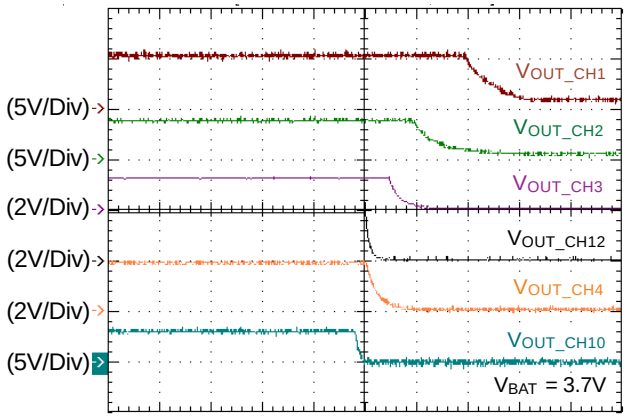


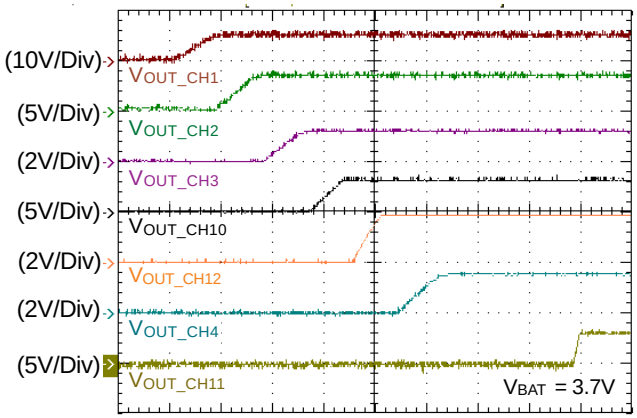
Power On Sequence 1



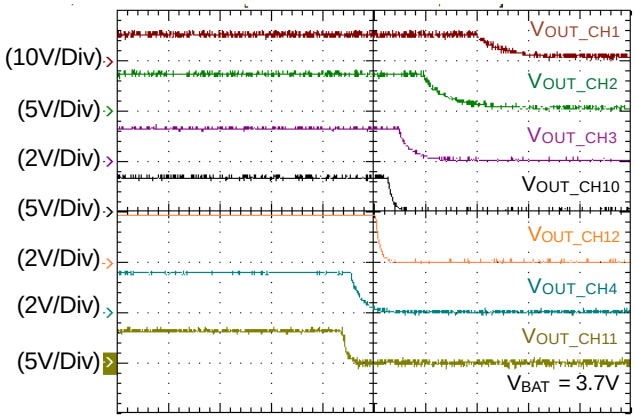
Power Off Sequence 1



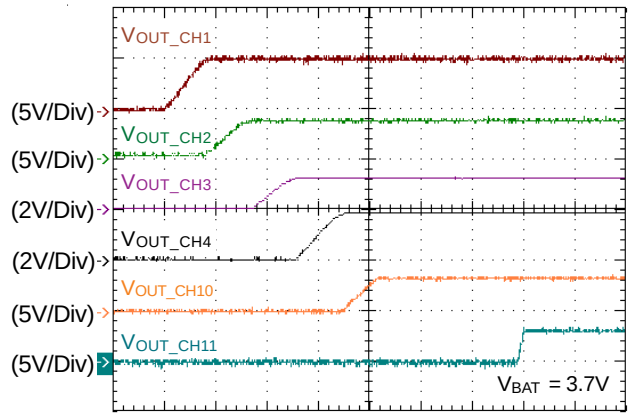
Power On Sequence 2



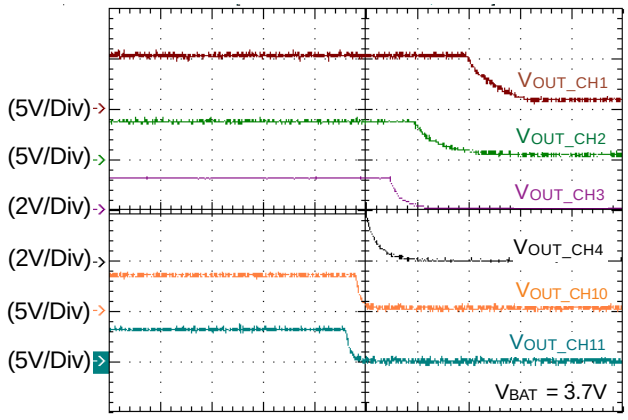
Power Off Sequence 2



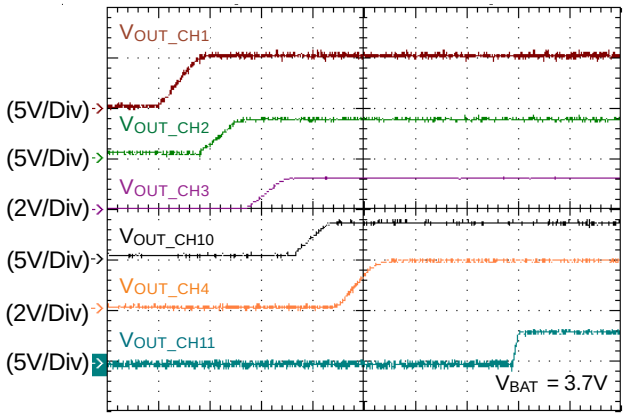
Power On Sequence 3



Power Off Sequence 3

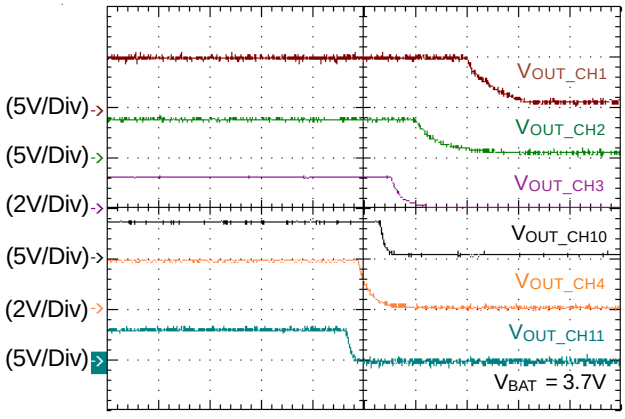


Power On Sequence 4



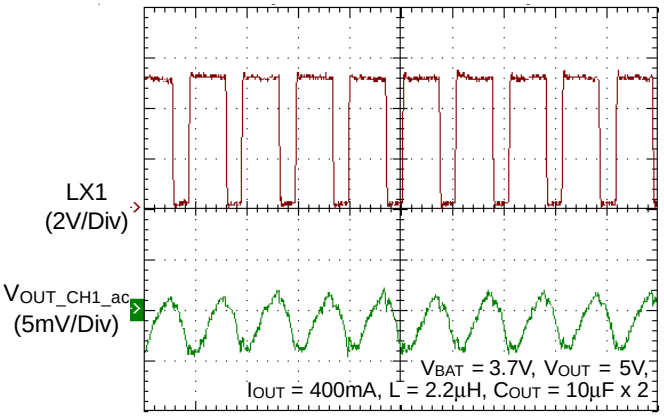
Time (5ms/Div)

Power Off Sequence 4



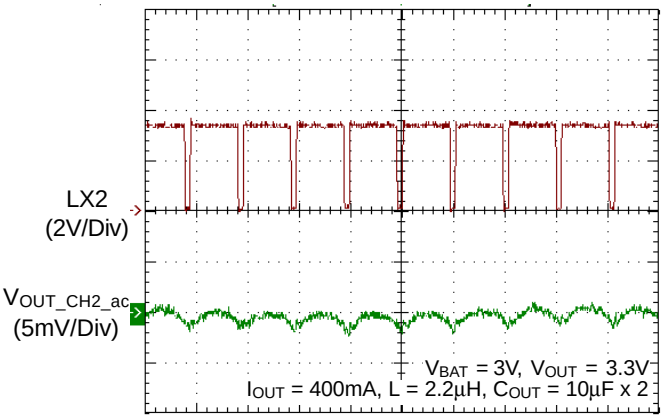
Time (2.5ms/Div)

CH1 Output Voltage Ripple



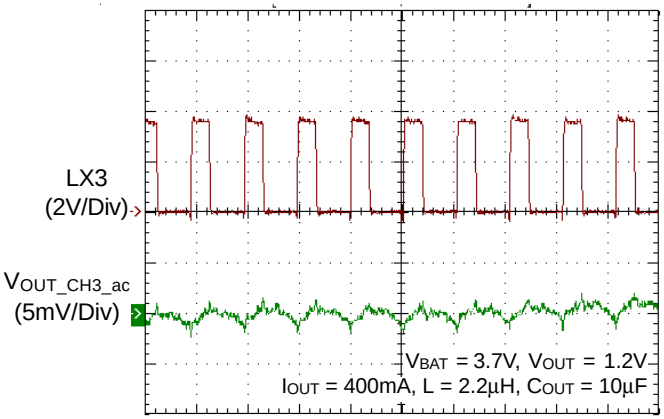
Time (500ns/Div)

CH2 Output Voltage Ripple



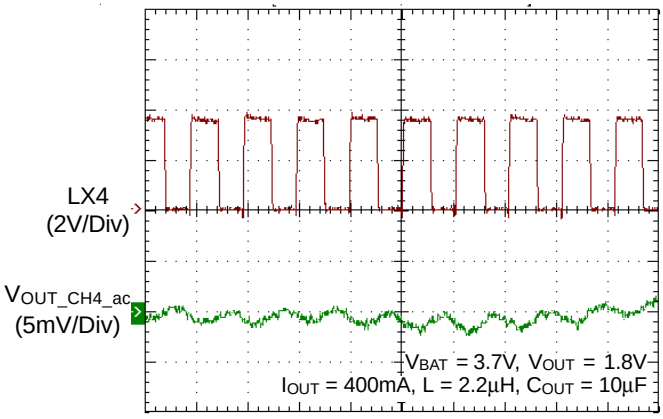
Time (1µs/Div)

CH3 Output Voltage Ripple



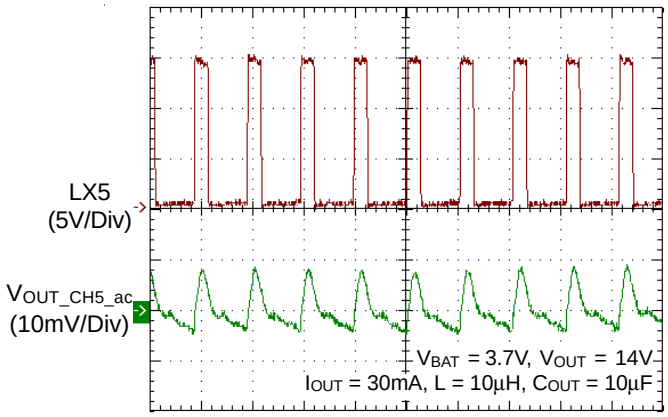
Time (500ns/Div)

CH4 Output Voltage Ripple

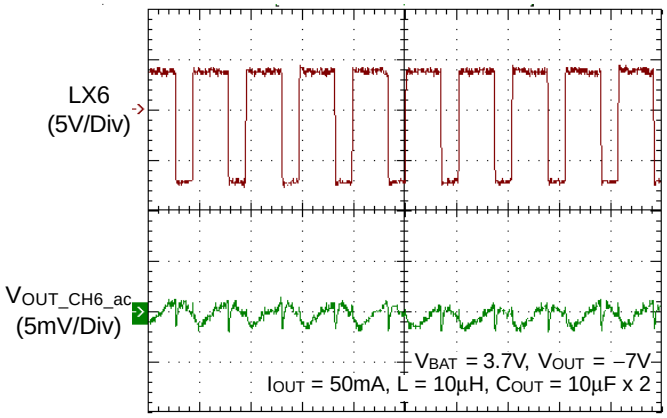


Time (500ns/Div)

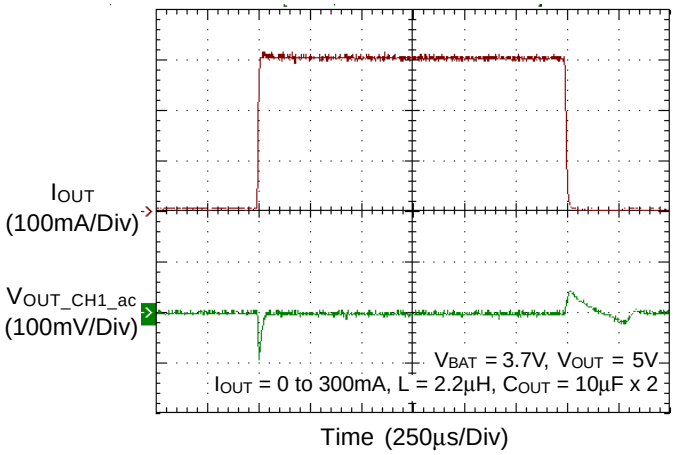
CH5 Output Voltage Ripple



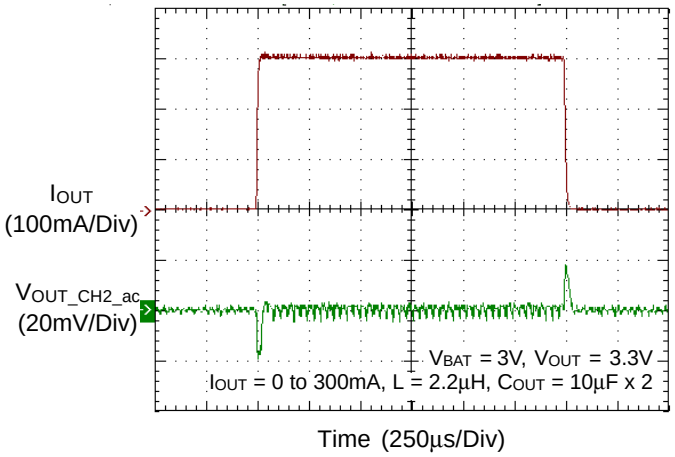
CH6 Output Voltage Ripple



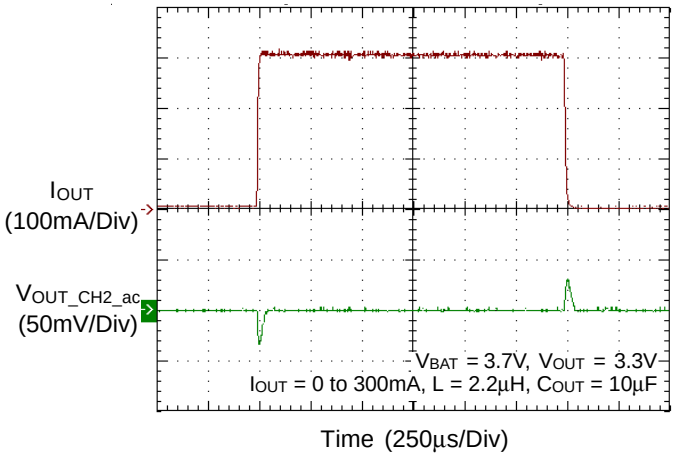
CH1 Load Transient Response



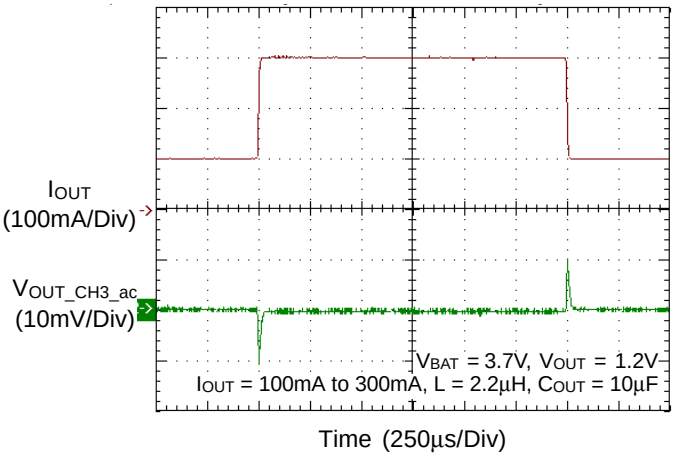
CH2 Load Transient Response



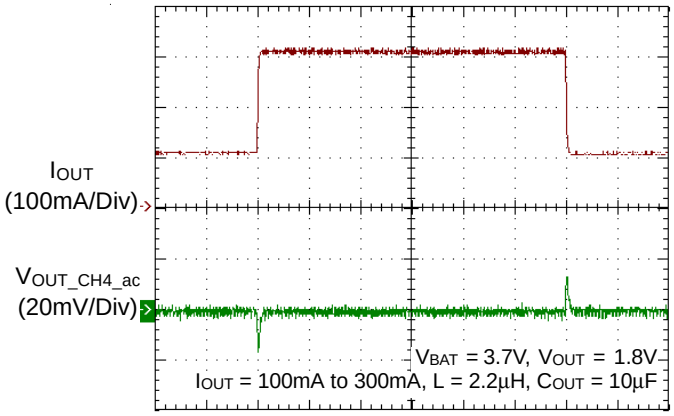
CH2 Load Transient Response



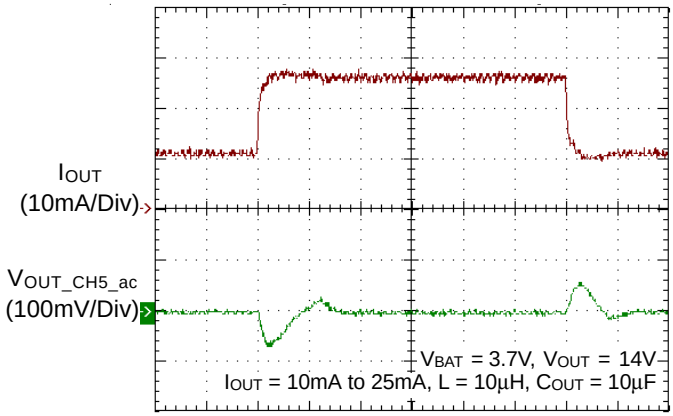
CH3 Load Transient Response



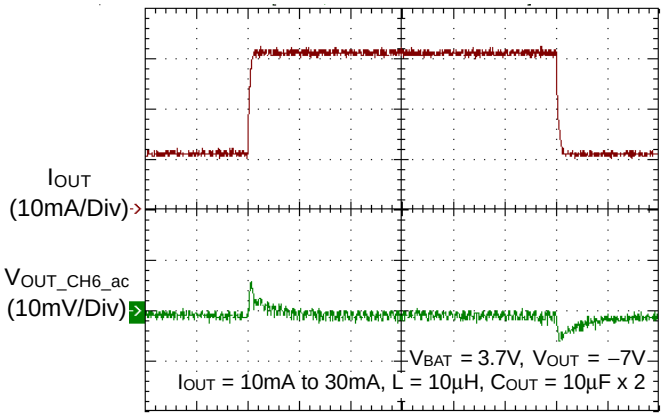
CH4 Load Transient Response



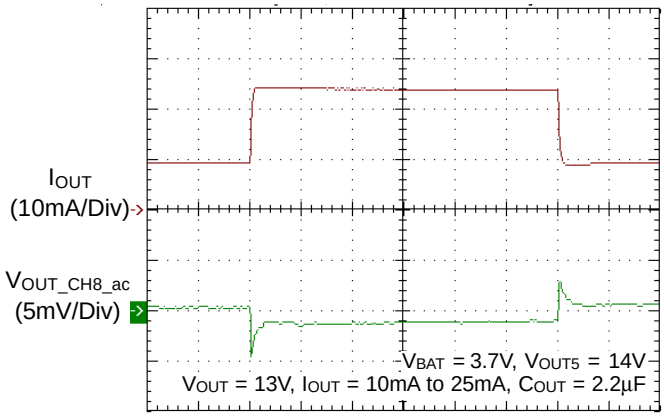
CH5 Load Transient Response



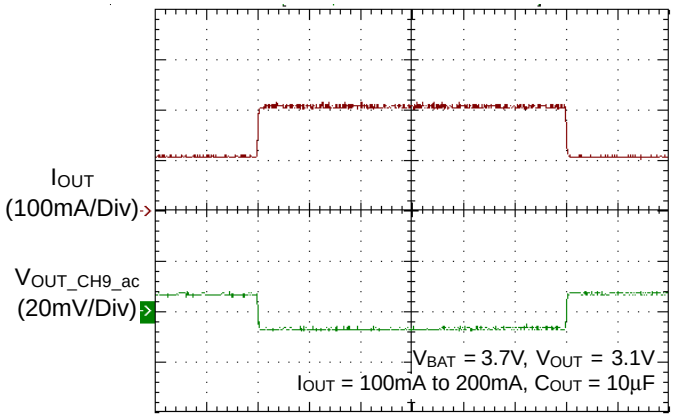
CH6 Load Transient Response



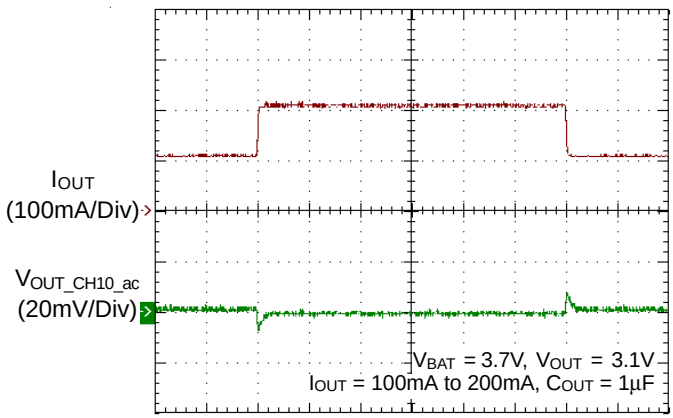
CH8 Load Transient Response



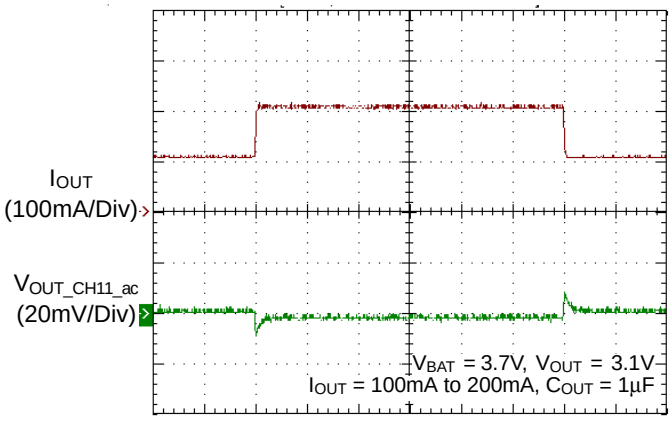
CH9 Load Transient Response



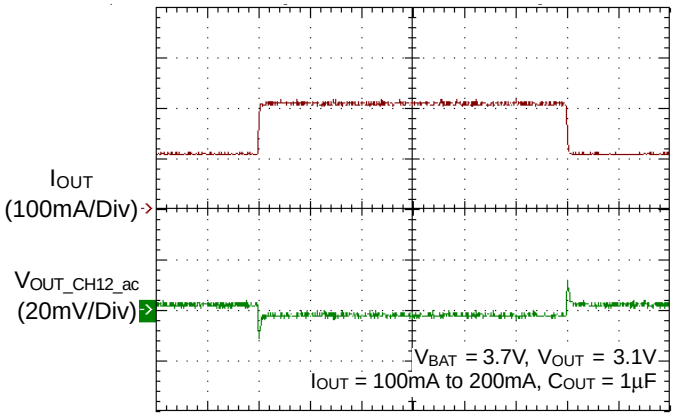
CH10 Load Transient Response



CH11 Load Transient Response



CH12 Load Transient Response



Application Information

The RT5014 is an integrated power solution for digital still cameras and other small handheld devices. It includes six DC/DC converters, a WLED driver, one RTC_LDO, one High Voltage LDO for CCD+ bias power, one high PSRR LDO for AFE power, and three generic LDOs.

CH1 : Synchronous Step-Up DC/DC Converter

The CH1 synchronous step-up DC/DC converter operates in fixed frequency current mode. It includes internal power MOSFETs, compensation network and feedback resistors. The P-MOSFET can be controlled to disconnect output loading. It is suitable for providing power to the motor. The output voltage of CH1 can be adjusted by the I^2C interface in the range of 3.6V to 5.3V.

	CH1 regulation voltage is selectable by I^2C interface. The default voltage is 5V.							
VOUT1	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	0000	3.6V	0001	3.7V	0010	3.8V	0011	3.9V
	0100	4V	0101	4.1V	0110	4.2V	0111	4.3V
	1000	4.4V	1001	4.5V	1010	4.6V	1011	4.7V
	1100	4.8V	1101	5V	1110	5.2V	1111	5.3V

CH2 : Synchronous Step-Up / Step-Down Selectable DC/DC Converter

The CH2 is a synchronous converter with step-up/step-down auto-select function for system I/O power. In either step-up or step-down, the converter operates in fixed frequency PWM mode, Continuous Conduction Mode (CCM), and Discontinuous Conduction Mode (DCM) with internal MOSFETs.

In step-up mode, the CH2 converter can disconnect the load from its input power node and discharges output node when it is turned off.

In step-down mode, the CH2 converter can be operated at 100% maximum duty cycle to extend the input operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode.

The output voltage can be set by the following equation :

$V_{OUT\_CH2} = (1 + R1 / R2) \times V_{FB2}$

where V_{FB2} is 0.8V typically.

CH3 : Synchronous Step-Down DC/DC Converter

The synchronous step-down DC/DC converter operates in fixed frequency PWM mode with integrated internal MOSFETs and compensation network. The CH3 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple.

The output voltage can be set by the following equation :

$V_{OUT\_CH3} = (1 + R3 / R4) \times V_{FB3}$

where V_{FB3} is 0.8V typically.

CH4 : Synchronous Step-Down DC/DC Converter

The synchronous step-down DC/DC converter operates at fixed frequency PWM mode with integrated internal MOSFETs and compensation network. The CH4 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple.

The output voltage can be set by the following equation :

$V_{OUT\_CH4} = (1 + R5 / R6) \times V_{FB4}$

where V_{FB4} is 0.8V typically.

CH5 : Synchronous Step-Up DC/DC Converter

CH5 is a high voltage synchronous step-up converter for the input power of CH8, high voltage LDO for CCD positive power. The converter operates at fixed frequency PWM mode, and CCM with integrated internal MOSFETs, compensation network and load disconnect function. The output voltage of CH5 is adjustable by the I^2C interface.

PVD5 = DV5 [3:0] + LDOH [3:0]

DV5 [3:0]	DV5 regulation voltage can be selectable by I^2C interface. The default voltage is 0.3V.							
	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	0000	0.2V	0001	0.3V	0010	0.4V	0011	0.5V
	0100	0.6V	0101	0.7V	0110	0.8V	0111	0.9V
	1000	1V	1001	1.5V	1010	2V	1011	2.5V
	1100	3V	1101	3.5V	1110	4V	1111	4.5V
	Note : PVD5 regulation voltage target = V(LDOH) + V(DV5)							
LDOH [3:0]	Define CH8 LDOH output voltage level. The default voltage is 9V.							
	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	0000	5V	0001	9V	0010	9.5V	0011	10V
	0100	10.5V	0101	11V	0110	11.5V	0111	12V
	1000	12.5V	1001	13V	1010	13.5V	1011	14V
	1100	14.5V	1101	15V	1110	15.5V	1111	16V

CH6 : INV DC/DC Converter

The asynchronous inverting current mode DC/DC converter integrates an internal P-MOSFET with internal compensation and needs an external Schottky diode to provide CCD negative power supply.

The output voltage of CH6 can be adjusted by the I^2C interface in the range of –5V to –8V.

VOUT6	CH6 regulation voltage can be selectable by I^2C interface. The default voltage is –5V.							
	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	000	–5V	001	–5.5V	010	–6V	011	–6.5V
	100	–7V	101	–7.5V	110	–8V	111	external
	Note : VOUT6 [2:0] = 111 (REF) means using external feedback network to define output voltage level.							

The output voltage using external feedback network can be set by the following equation.

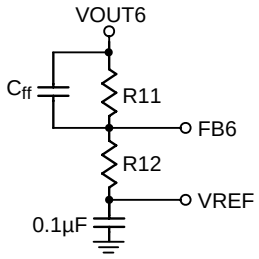
V_{OUT_CH6} = −(R11 / R12) x (0.84V) + 0.4V

where R11 and R12 are the feedback resistors connected

The feed forward capacitor can be estimated by the following equation.

$$C_{ff} = \frac{62.5 \times 10^{-6}}{R11}$$

For example, when R11 is 125kΩ, the available feed-forward capacitor is 470pF.



CH7 : WLED Driver

CH7 is a WLED driver that can operate in either current source mode or synchronous step-up mode, as determined by LX7 detection. When CH7 works in current source mode, it sources an LED current out of LX7 pin and regulates the current by FB7 voltage. The LED current is defined by the FB7 voltage as well as the external resistor between FB7 and GND. The FB7 regulation voltage can be set in 32 steps from 7.8mV to 250mV via I^2C interface. If CH7 works in synchronous step-up mode, it integrates synchronous step-up mode with an internal MOSFET and internal compensation. The LED current is also set via an external resistor and FB7 regulation voltage.

CH7 WLED Current Dimming Control

If CH7 is in synchronous step-up mode or current source mode, the WLED current is set by an external resistor. Regardless of the mode, dimming is always controlled by the I^2C interface. The WLED current can be set by the following equations :

I_{LED} (mA) = [250mV / R (W)] x (DIM7 [4:0] + 1) / 32

where R is the current sense resistor from FB7 to GND and (DIM7 [4:0] + 1) / 32 ratio refers to the I^2C control register file.

CH8 High Voltage LDO

CH8 is a high voltage LDO for CCD positive power. It is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH8 has an ON/OFF control which can be set by I^2C commands. The output voltage of CH8 is adjustable by the I^2C interface in the range of 5V to 16V.

	Define CH8 LDOH output voltage level. The default voltage is 9V.							
LDOH [3:0]	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	0000	5V	0001	9V	0010	9.5V	0011	10V
	0100	10.5V	0101	11V	0110	11.5V	0111	12V
	1000	12.5V	1001	13V	1010	13.5V	1011	14V
	1100	14.5V	1101	15V	1110	15.5V	1111	16V

CH9 : Low Voltage LDO

CH9 is a high PSRR LDO for AFE power. It is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH9 has an ON/OFF control which can be set by I²C commands. The output voltage of CH9 is adjustable by the I²C interface in the range of 1.3V to 3.3V.

VOA [2:0]	Define CH9 LDO preset output voltage level. The default voltage is 1.3V							
	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	000	3.3V	001	3.2V	010	3.1V	011	3V
	100	2.8V	101	2.5V	110	1.8V	111	1.3V

CH10 : Low Voltage LDO

CH10 is a low voltage LDO for system power. It is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH10 will turns on after CH1 to CH3 by power on/off sequence table. The output voltage of CH10 is adjustable by the I²C interface in the range of 1.2V to 3.2V.

VOD1 [2:0]	Define CH10 LDO output voltage level. The default voltage is 3.1V when SEQ #0, 2, 3, 4 or 3V when SEQ #1.							
	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	000	3.2V	001	3.1V	010	3V	011	2.8V
	100	2.5V	101	1.8V	110	1.3V	111	1.2V

CH11 : Low Voltage LDO

CH11 is a low voltage LDO for memory card power. It is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH11 has an ON/OFF control which can be set by I²C commands. The output voltage of CH11 is adjustable by the I²C interface in the range of 1.3V to 3.2V.

VOD2 [2:0]	Define CH11 LDO output voltage level. The default voltage is 2.3V when SEQ #0 or 3.1V when SEQ #1 to SEQ #4.							
	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	000	3.2V	001	3.1V	010	3V	011	2.8V
	100	2.5V	101	2.3V	110	1.8V	111	1.3V

CH12 : Low Voltage LDO

CH12 is a low voltage LDO for multiple purpose power. It is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH12 has an ON/OFF control which can be set by I²C commands. The output voltage of CH12 is adjustable by the I²C interface in the range of 1.2V to 3.2V.

VOM [2:0]	Define CH12 LDO preset output voltage level. The default voltage is 2.5V when SEQ #0, or 1.8V when SEQ #1 to SEQ #4.							
	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
	000	3.2V	001	3.1V	010	3V	011	2.8V
	100	2.5V	101	1.8V	110	1.3V	111	1.2V

RTC_LDO : Accuracy 3.3V LDO Output.

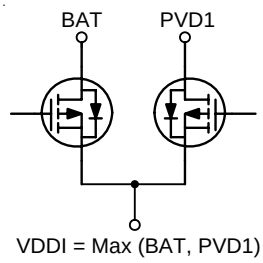
The RT5014 provides a 3.3V output LDO for real-time clock. The LDO features low quiescent current (3μA), reverse leakage prevention from output node and high output voltage accuracy. This LDO is always on, even when the system is shut down. For better stability, it is recommended to connect a 0.1μF capacitor to the VRTC pin. The RTC LDO includes pass transistor body diode control to avoid the VRTC node from back-charging into the input node VDDI.

Switching Frequency

The converters of CH1 to CH4 operate in PWM mode with 2MHz and CH5 to CH7 operates in PWM mode with 1MHz switching frequency.

VDDM Bootstrap

To support bootstrap function, the RT5014 provides a power selection circuit which selects the maximum voltage between BAT and PVD1 to support the power requirement at node VDDI. The RT5014 includes UVLO circuits to monitor VDDI and BAT voltage status.



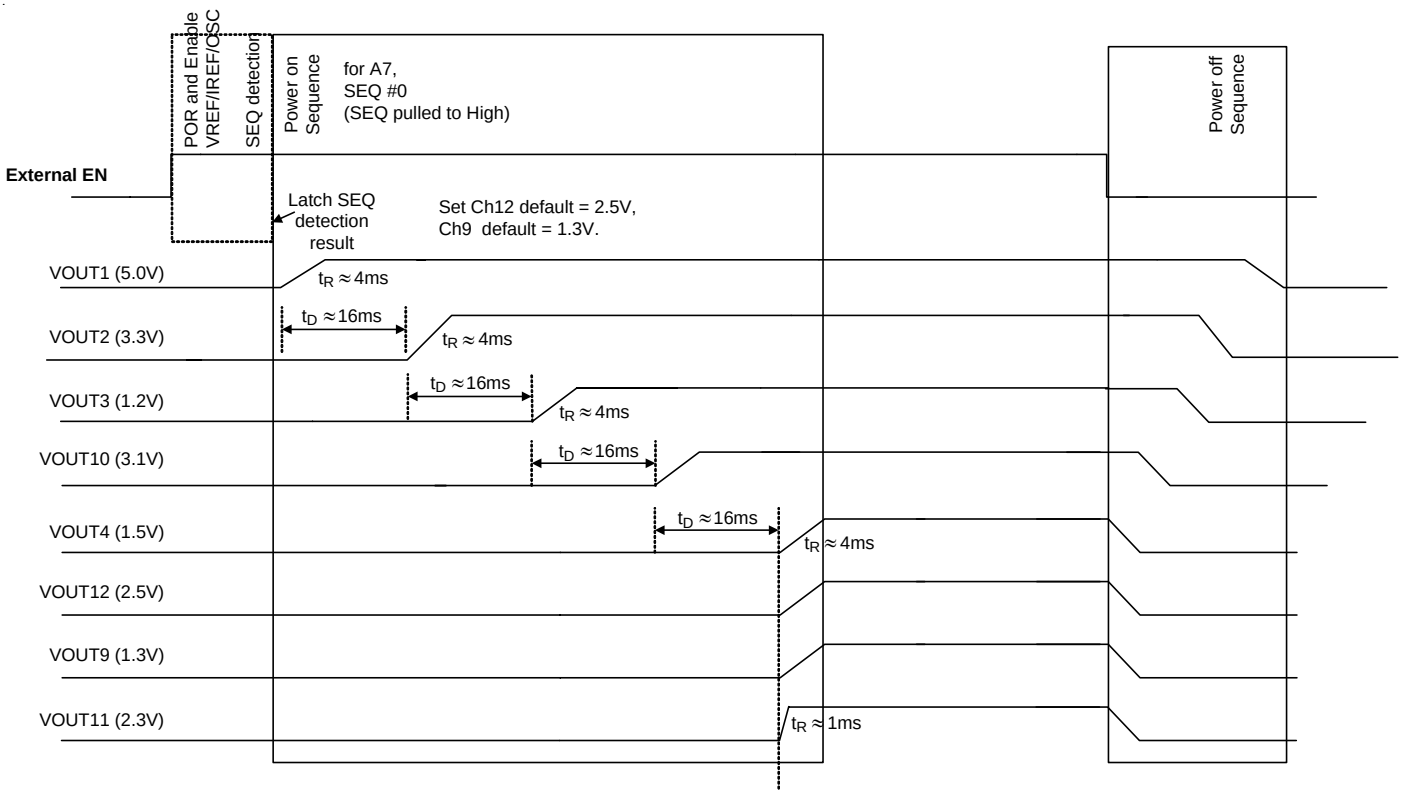
Power On/Off Sequence

SEQ pull down resistance R_{SEQ} defines Power on/off Sequence.

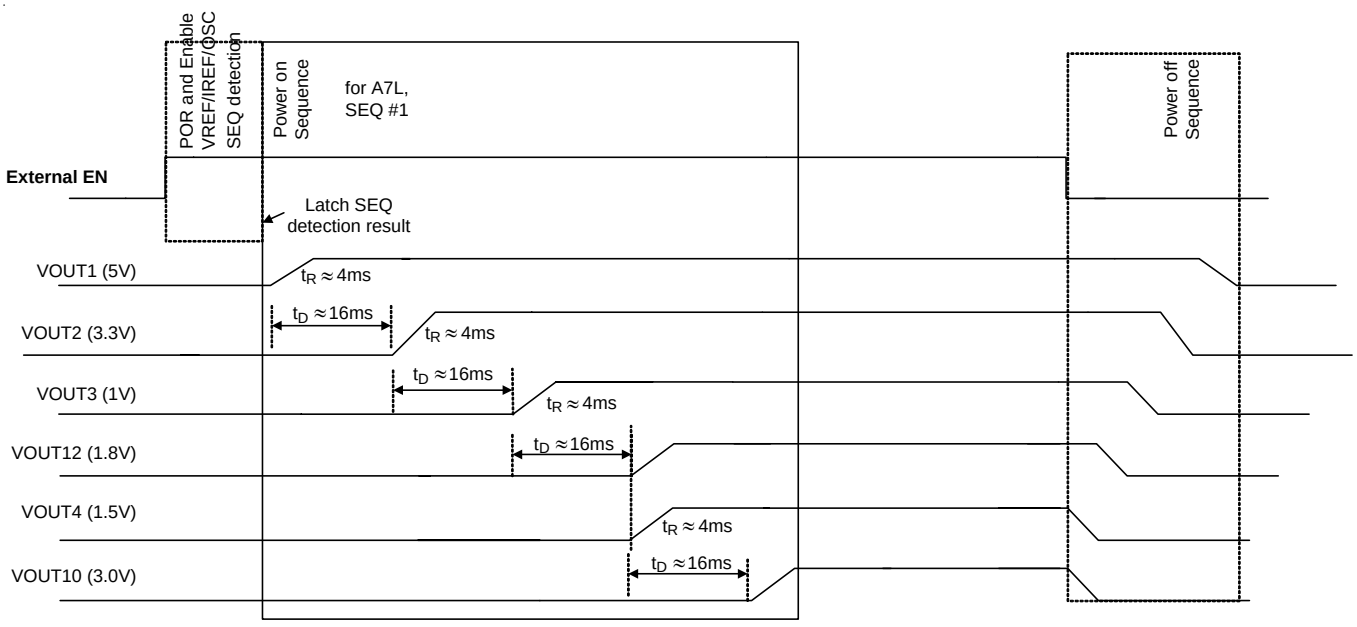
SEQ #	R_{SEQ} (kΩ) Range		
	Min	Typ	Max
SEQ #0	Short to Power (>0.2V)		
SEQ #1	36	40	44
SEQ #2	9	10	11
SEQ #3	2.25	2.5	2.75
SEQ #4	--	0.63	0.69

Typical soft-start and on/off sequence waveform.

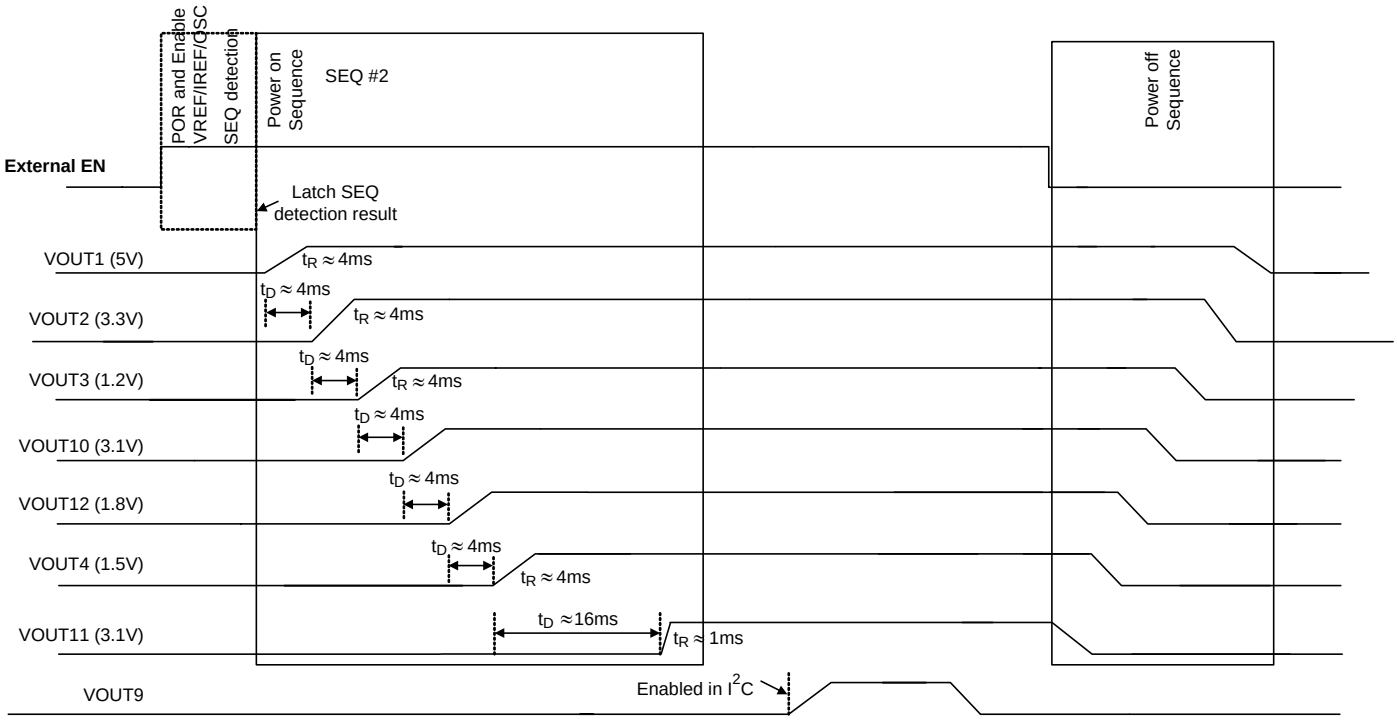
SEQ #0 : CH1 (5V) → CH2 (3.3V) → CH3 (1.2V) → CH10 (3.1V) → CH4 (1.5V), CH12 (2.5V), CH9 (1.3V), CH11 (2.3V) ; I²C EN9 and EN12 bits have no function (Ambarella A7).



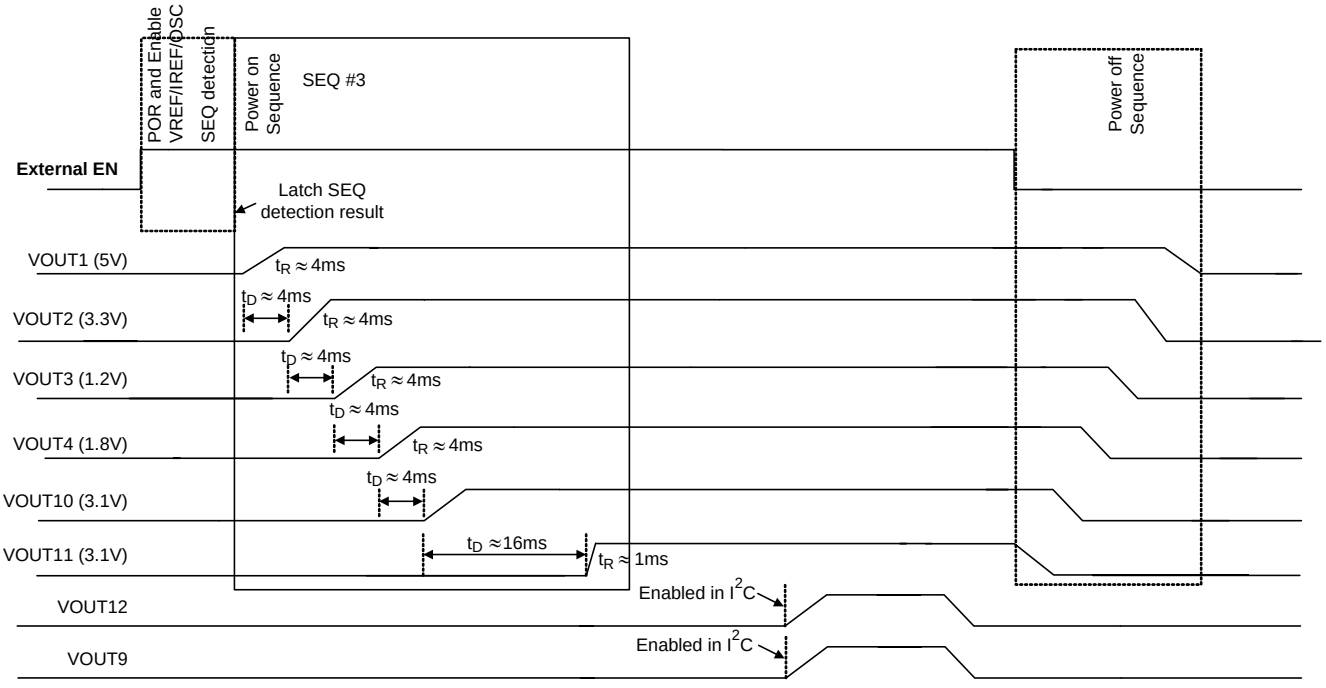
SEQ #1 : CH1 (5V) → CH2 (3.3V) → CH3 (1V) → CH12 (1.8V) → CH4 (1.5V) → CH10 (3V) ; I²C EN12 bit has no function (Ambarella A7L).



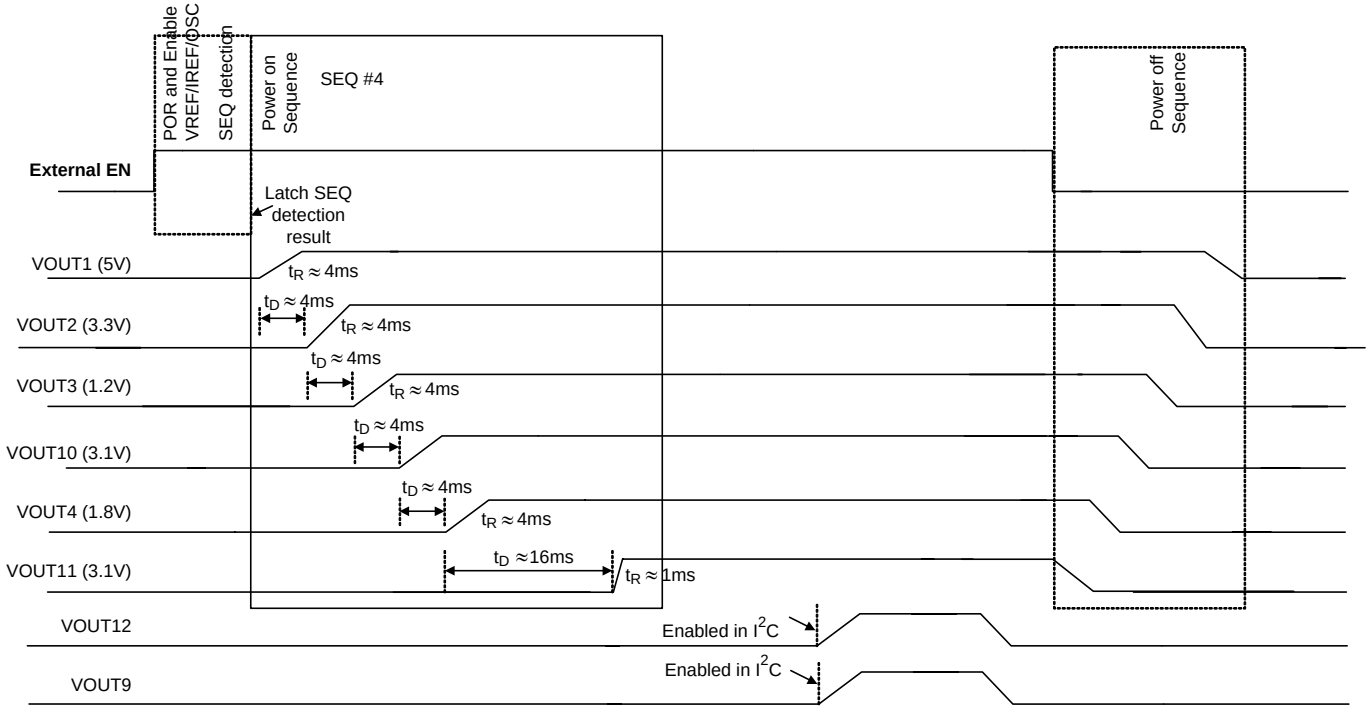
SEQ #2 : CH1 (5V) → CH2 (3.3V) → CH3 (1.2V) → CH10 (3.1V) → CH12 (1.8V) → CH4 (1.5V) → CH11 (3.1V); I²C EN12 bit have no function.



SEQ #3 : CH1 (5V) → CH2 (3.3V) → CH3 (1.2V) → CH4 (1.8V) → CH10 (3.1V) → CH11 (3.1V)



SEQ #4 : CH1 (5V) → CH2 (3.3V) → CH3 (1.2V) → CH10 (3.1V) → CH4 (1.8V) → CH11 (3.1V)



CH12 :

SEQ #0 : VOUT12 = 2.5V

SEQ #1 and SEQ #2 : VOUT12 = 1.8V

SEQ #3 and SEQ #4 : VOUT12 defined and enabled in I^2C (CH12 not in sequence)

CH11 :

SEQ #0 : VOUT11 = 2.3V

SEQ #1 : VOUT11 defined and enabled in I^2C (CH11 not in sequence) and VOUT11 has DVS function.

SEQ #2 to SEQ #4 : VOUT11 = 3.1V

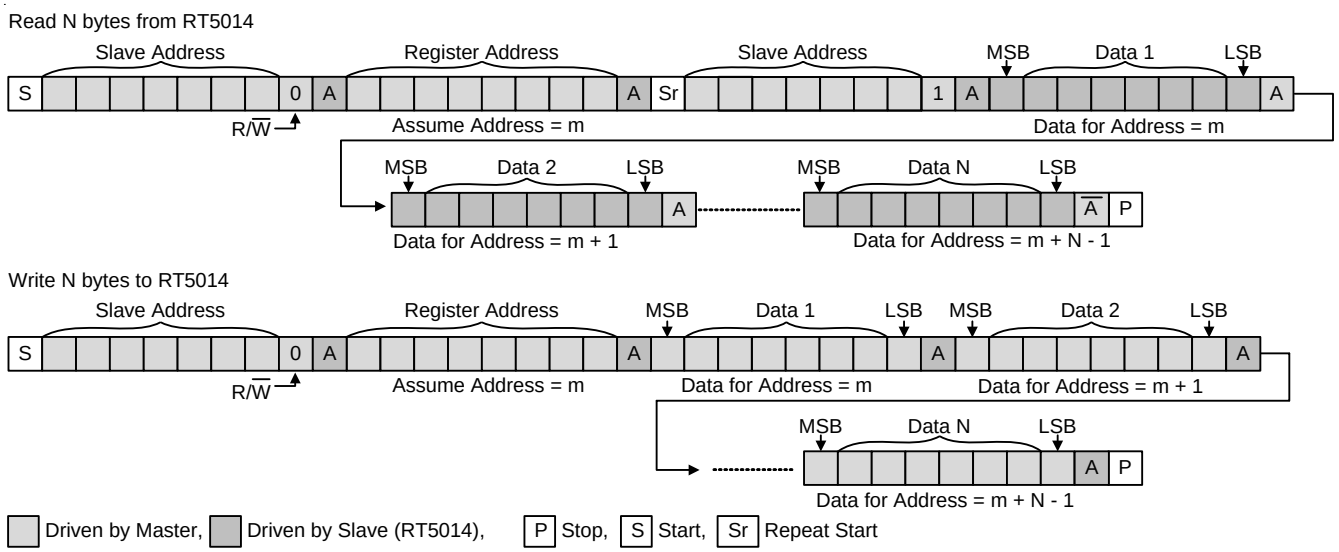
CH 9 :

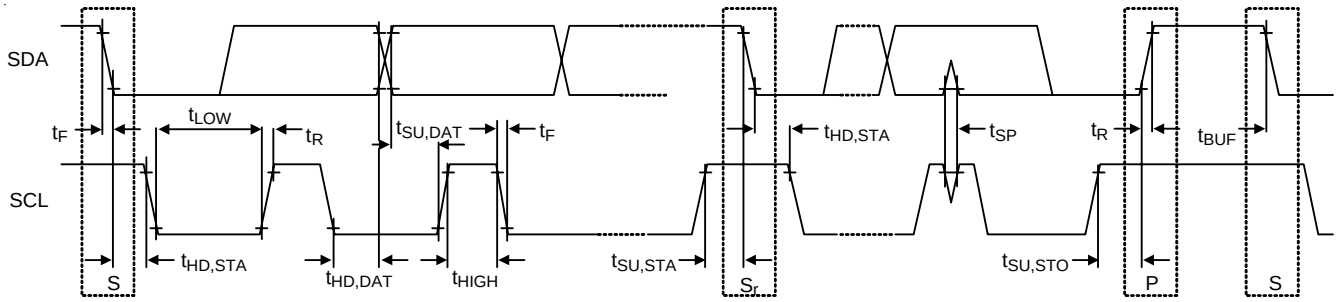
SEQ #0 : VOUT9 = 1.3V

SEQ #1 to SEQ #4 : VOUT9 defined and enabled in I^2C (CH9 not in sequence)

I²C Interface

RT5014 I²C slave address = 7'b0011000. I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :





I²C Register Map

Register Address	Register Address		b [7] (MSB)	b [6]	b [5]	b [4]	b [3]	b [2]	b [1]	b [0] (LSB)
A0	0x00	Meaning	Reserved	OVP7		DIM7 [4:0]				
		Default	0	0	0	1	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OVP7			CH7 allows user to select the OVP level by I²C interface							
			00 : OVP7 = 9V (Typ.), 10V(MAX)							
			01 : OVP7 = 15V (Typ.), 16V(MAX)							
			1X : OVP7 = 25V (Typ.), 26V(MAX)							
DIM7 [4:0]			Define FB7 regulation voltage							
			00000 to 11111 : CH7 dimming ratio : VFB7 = (DIM7 [4:0] + 1) / 32 x 0.25V							

Register Address	Register Address		b [7] (MSB)	b [6]	b [5]	b [4]	b [3]	b [2]	b [1]	b [0] (LSB)
A1	0x01	Meaning	VOUT1 [3:0]				Reserved	VOUT6 [2:0]		
		Default	1	1	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VOUT1			CH1 regulation voltage can be selectable by I²C interface. The default voltage is 5V.							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	3.6V	0001	3.7V	0010	3.8V	0011	3.9V
			0100	4V	0101	4.1V	0110	4.2V	0111	4.3V
			1000	4.4V	1001	4.5V	1010	4.6V	1011	4.7V
			1100	4.8V	1101	5V	1110	5.2V	1111	5.3V
VOUT6			CH6 regulation voltage can be selectable by I²C interface. The default voltage is –5V.							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	–5V	001	–5.5V	010	–6V	011	–6.5V
			100	–7V	101	–7.5V	110	–8V	111	external
			Note : VOUT6 [2:0] = 111 (REF) means using external feedback network to define output voltage level.							

Register Address	Register Address		b [7] (MSB)	b [6]	b [5]	b [4]	b [3]	b [2]	b [1]	b [0] (LSB)
A2	0x02	Meaning	DV5 [3:0]				LDOH [3:0]			
		Default	0	0	0	1	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DV5 [3:0]			DV5 regulation voltage can be selectable by I^2C interface. The default voltage is 0.3V.							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0.2V	0001	0.3V	0010	0.4V	0011	0.5V
			0100	0.6V	0101	0.7V	0110	0.8V	0111	0.9V
			1000	1V	1001	1.5V	1010	2V	1011	2.5V
			1100	3V	1101	3.5V	1110	4V	1111	4.5V
			Note : PVD5 regulation voltage target = V(LDOH) + V(DV5)							
LDOH [3:0]			Define CH8 LDOH output voltage level. The default voltage is 9V.							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	5V	0001	9V	0010	9.5V	0011	10V
			0100	10.5V	0101	11V	0110	11.5V	0111	12V
			1000	12.5V	1001	13V	1010	13.5V	1011	14V
			1100	14.5V	1101	15V	1110	15.5V	1111	16V

Register Address	Register Address		b [7] (MSB)	b [6]	b [5]	b [4]	b [3]	b [2]	b [1]	b [0] (LSB)
A3	0x03	Meaning	Reserved	VOA [2:0]			Reserved	VOM [2:0]		
		Default	0	1	1	1	0	See below		
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VOA [2:0]			Define CH9 LDO preset output voltage level. The default voltage is 1.3V							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	3.3V	001	3.2V	010	3.1V	011	3V
			100	2.8V	101	2.5V	110	1.8V	111	1.3V
VOM [2:0]			Define CH12 LDO preset output voltage level. The default voltage is 2.5V when SEQ #0, or 1.8V when SEQ #1 to SEQ #4.							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	3.2V	001	3.1V	010	3V	011	2.8V
			100	2.5V	101	1.8V	110	1.3V	111	1.2V

Register Address	Register Address		b [7] (MSB)	b [6]	b [5]	b [4]	b [3]	b [2]	b [1]	b [0] (LSB)
A4	0x04	Meaning	Reserved	VOD1 [2:0]			Reserved	VOD2 [2:0]		
		Default	0	See below			0	See below		
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VOD1 [2:0]			Define CH10 LDO output voltage level. The default voltage is 3.1V when SEQ #0, 2, 3, 4 or 3V when SEQ #1.							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	3.2V	001	3.1V	010	3V	011	2.8V
			100	2.5V	101	1.8V	110	1.3V	111	1.2V
VOD2 [2:0]			Define CH11 LDO output voltage level. The default voltage is 2.3V when SEQ #0 or 3.1V when SEQ #1 to SEQ #4.							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	3.2V	001	3.1V	010	3V	011	2.8V
			100	2.5V	101	2.3V	110	1.8V	111	1.3V

Register Address	Register Address		b [7] (MSB)	b [6]	b [5]	b [4]	b [3]	b [2]	b [1]	b [0] (LSB)
A5	0x05	Meaning	EN5	EN6	EN7	EN8	EN9	Reserved	EN11	EN12
		Default	0	0	0	0	0	0	See below	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
EN5			Enable/disable CH5 0 : Disable 1 : Enable							
EN6			Enable/disable CH6 0 : Disable 1 : Enable							
EN7			Enable/disable CH7 0 : Disable 1 : Enable							
EN8			Enable/disable CH8 0 : Disable 1 : Enable							
EN9			Enable/disable CH9 0 : Disable 1 : Enable							
EN11			Enable/disable CH11 0 : Disable 1 : Enable SEQ #1 : Default value is 0. SEQ #0, 2, 3, 4 : Default value is 1.							
EN12			Enable/disable CH12 0 : Disable 1 : Enable							

* RESET Moment :

Register A0 to A4 reset when (BAT UVLO or VDDM UVLO) and after PMU shutdown.

Register A5 reset after (EN = L or BAT/VDDM UVLO) and PMU shutdown completely.

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0	0x00	Meaning	Reserved	OVP7			DIM7 [4:0]			
		Default	0	0	0	1	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A1	0x01	Meaning	VOUT1 [3:0]				Reserved	VOUT6 [2:0]		
		Default	1	1	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A2	0x02	Meaning	DV5 [3:0]				LDOH [3:0]			
		Default	0	0	0	1	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A3	0x03	Meaning	Reserved	VOA [2:0]			Reserved	VOM [2:0]		
		Default	0	1	1	1	0	SEQ dependent		
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A4	0x04	Meaning	Reserved	VOD1 [2:0]			Reserved	VOD2 [2:0]		
		Default	0	SEQ dependent			0	SEQ dependent		
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A5	0x05	Meaning	EN5	EN6	EN7	EN8	EN9	Reserved	EN11	EN12
		Default	0	0	0	0	0	0	SEQ dependent	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.64W for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

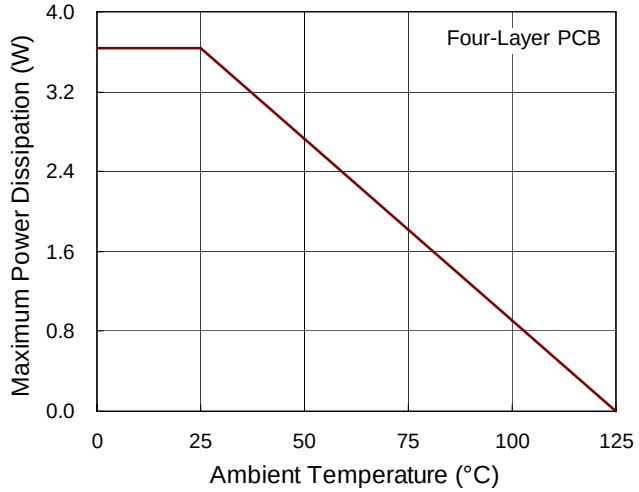


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT5014, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.

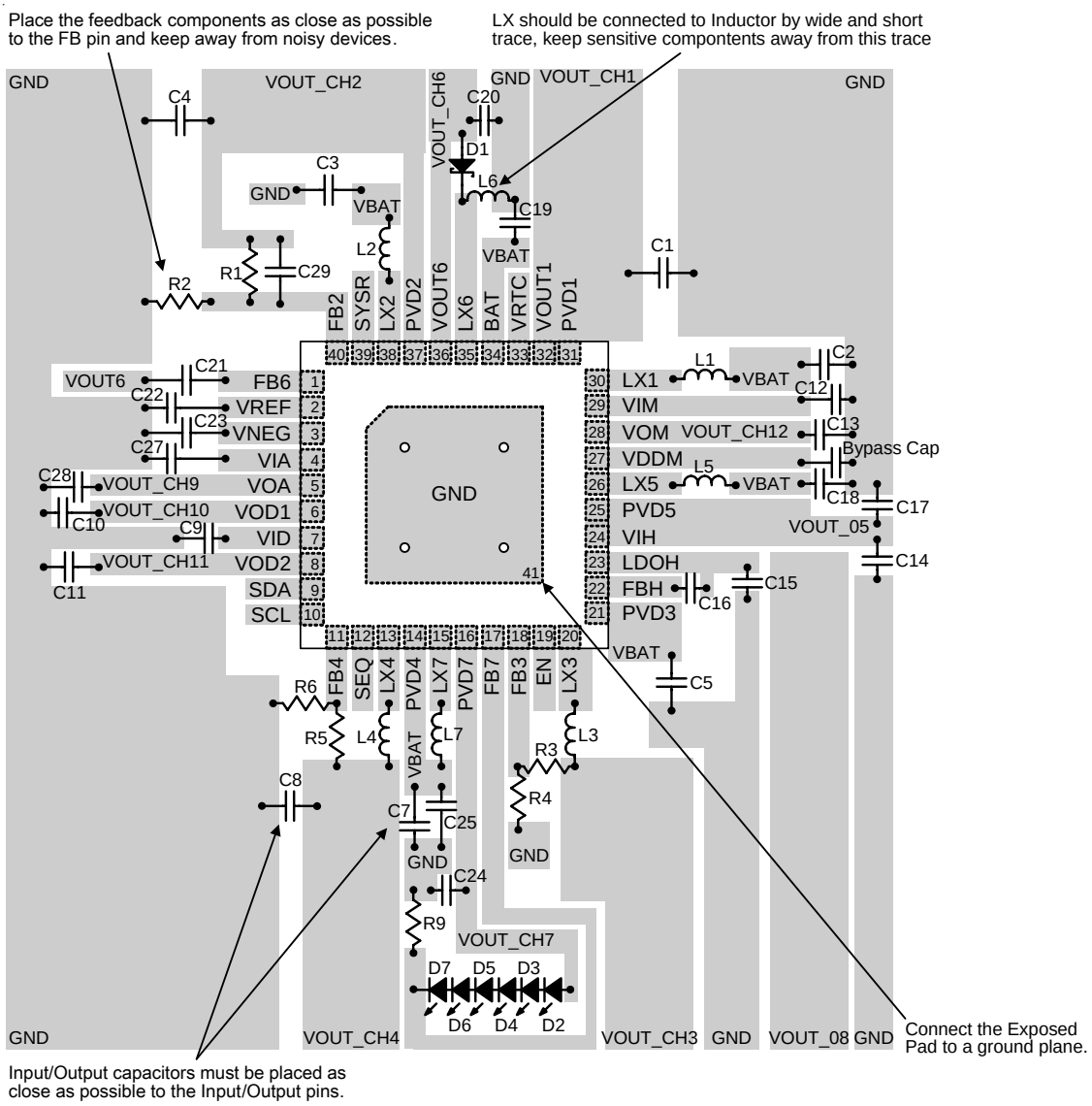
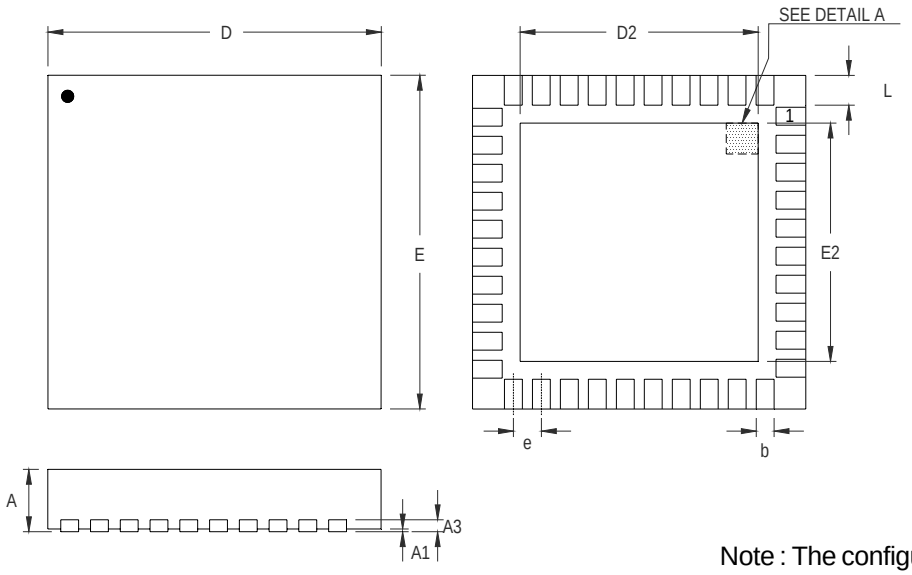


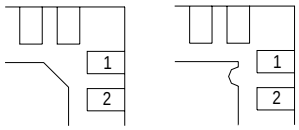
Figure 8. PCB Layout Guide

	Protection Type	Threshold (typical value)	Delay Time	Protection Methods	Reset Method
BAT	UVLO	BAT < 1.4V	No delay	Turn off whole IC	VDDM power reset or EN = low
VDDM	OVP	VDDM > 6V	100ms	Turn off whole IC	VDDM power reset or EN = low
	UVLO	VDDM < 2.4V	No delay	Turn off whole IC	VDDM power reset or EN = low
CH1 Step-Up	Current limit	N-MOSFET current > 3A	100ms	Turn off whole IC	VDDM power reset or EN = low
	PVD1 OVP	PVD1 > 6V	No delay	Turn off whole IC	VDDM power reset or EN = low
	PVD1 UVP	PVD1 < VBAT – 0.8V	100ms	Turn off whole IC	VDDM power reset or EN = low
	VOUT1 UVP	VOUT1 < 2.25V	No delay	Turn off whole IC	VDDM power reset or EN = low
	VOUT1 Over Load	VOUT1 < target – 0.6V	100ms	Turn off whole IC	VDDM power reset or EN = low
CH2 Step-Up	Current limit	N-MOSFET current > 3A	100ms	Turn off whole IC	VDDM power reset or EN = low
	PVD2 OVP	PVD2 > 6V	No delay	Turn off whole IC	VDDM power reset or EN = low
	PVD2 UVP	PVD2 < VBAT – 0.8V	100ms	Turn off whole IC	VDDM power reset or EN = low
	FB2 UVP	FB2 < 0.3V	No delay	Turn off whole IC	VDDM power reset or EN = low
	FB2 Over Load	FB2 < 0.7V	100ms	Turn off whole IC	VDDM power reset or EN = low
CH2 Step-Down	Current limit	P-MOSFET current > 1.6A	100ms	Turn off whole IC	VDDM power reset or EN = low
	FB2 UVP	FB2 < 0.3V	No delay	Turn off whole IC	VDDM power reset or EN = low
	FB2 Over Load	FB2 < 0.7V	100ms	Turn off whole IC	VDDM power reset or EN = low
CH3 Step-Down	Current limit	P-MOSFET current > 2A	100ms	Turn off whole IC	VDDM power reset or EN pin set to low
	FB3 UVP	FB3 < 0.4V	No delay	Turn off whole IC	VDDM power reset or EN = low
	FB3 Over Load	FB3 < 0.7V	100ms	Turn off whole IC	VDDM power reset or EN = low
CH4 Step-Down	Current limit	P-MOSFET current > 1.6A	100ms	Turn off whole IC	VDDM power reset or EN = low
	FB4 UVP	FB4 < 0.4V	No delay	Turn off whole IC	VDDM power reset or EN pin set to low
	FB4 Over Load	FB4 < 0.7V	100ms	Turn off whole IC	VDDM power reset or EN = low

	Protection Type	Threshold (typical value)	Delay Time	Protection Methods	Reset Method
CH5 Step-Up	Current limit	N-MOSFET current > 1.2A	100ms	Turn off whole IC	VDDM power reset or EN = low
	PVD5 OVP	PVDD5 > 22V	No delay	Turn off whole IC	VDDM power reset or EN = low
	PVD5 UVP	PVD5 < DV5 + LDOH x 0.5	100ms	Turn off whole IC	VDDM power reset or EN = low
	PVD5 Over Load	PVD5 < target – 2V for A2.LODH ≠ 4'b0000; PVD5 < target – 1V for A2.LODH = 4'b0000	100ms	Turn off whole IC	VDDM power reset or EN = low
CH6 Async Inverting	Current limit	P-MOSFET current > 1.5A	100ms	Turn off whole IC	VDDM power reset or EN = low
	VOUT6 OVP	PVD6 < –13V	No delay	Turn off whole IC	VDDM power reset or EN = low
	FB6 UVP	FB6 > 0.8V	100ms	Turn off whole IC	VDDM power reset or EN = low
	FB6 Over Load	FB6 > 0.55V	100ms	Turn off whole IC	VDDM power reset or EN = low
CH7 WLED	Current limit	N-MOSFET current > 0.8A	100ms	Turn off whole IC	VDDM power reset or EN = low
	PVD7 OVP	PVD7 > 9V for A0.OVP7 = 2'b00; PVD7 > 15V for A0.OVP7 = 2'b01; PVD7 > 25.5V for A0.OVP7 = 2'b1X	No delay	Turn off whole IC	VDDM power reset or EN = low
CH8 LDO	Current limit	P-MOSFET current > 120mA	No delay	Limit P-MOSFET Current	Reset by load
	LDOH UVP	LDOH < target x 0.5	No delay	Turn off whole IC	VDDM power reset or EN = low
CH9 LDO	Current limit	P-MOSFET current > 300mA	No delay	Limit P-MOSFET Current	Reset by load
	VOA UVP	VOA < target x 0.5	100ms	Turn off whole IC	VDDM power reset or EN = low
CH10 LDO	Current limit	P-MOSFET current > 300mA	No delay	Limit P-MOSFET Current	Reset by load
	VOD1 UVP	VOD1 < target x 0.5	100ms	Turn off whole IC	VDDM power reset or EN = low
CH11 LDO	Current limit	P-MOSFET current > 400mA	No delay	Limit P-MOSFET Current	Reset by load
	VOD2 UVP	VOD2 < target x 0.5	100ms	Turn off whole IC	VDDM power reset or EN = low
CH12 LDO	Current limit	P-MOSFET current > 400mA	No delay	Limit P-MOSFET Current	Reset by load
	VOM UVP	VOM < target x 0.5	100ms	Turn off whole IC	VDDM power reset or EN = low
RTC LDO	Current limit	P-MOSFET current > 130mA	No delay	Limit P-MOSFET Current	Reset by load
Thermal	Thermal shutdown	Temperature > 155°C	No delay	Turn off whole IC	Temperature < 135°C, VDDM power reset or EN = low

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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