

Integrated PMIC with 4-Channel Synchronous Buck Converters, 8 LDOs, and MTP Non-Volatile Memory for Industrial Applications

General Description

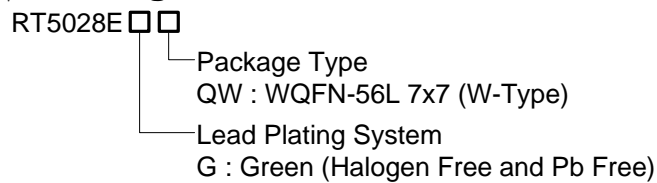
The RT5028E is a highly-integrated low-power high-performance analog SOC with PMIC in one single chip designed for industrial applications.

The RT5028E includes four synchronous step-down DC-DC converters and eight LDOs for system power.

The RT5028E also embeds one EEPROM (MTP) for setting sequence and timing etc.

Additionally, the RT5028E PMIC also includes one IRQ report.

Ordering Information



Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

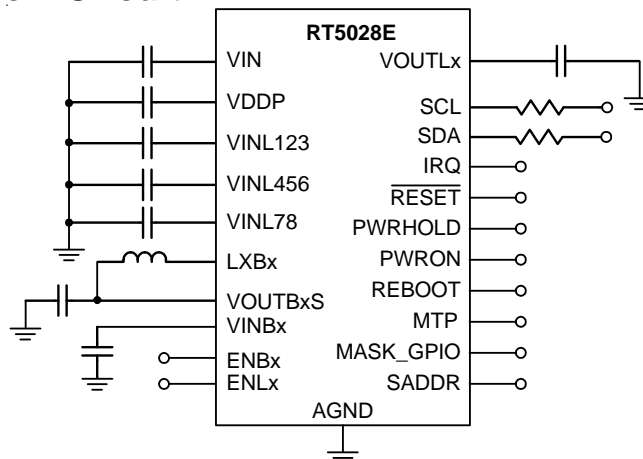
Features

- Input Voltage Operating Range is 3.3V to 5.5V
- Step-Down Regulator : V_{IN} Range is 3.3V to 5.5V
 - ▶ Max Current 2.4A/2A/1.6A/2A
 - ▶ Programmable Frequency from 500kHz to 2MHz
 - ▶ I²C Programmable Output Level
 - ▶ I²C Programmable Operation Mode (Force PWM or Auto PSM/PWM)
 - ▶ I²C Programmable Output Discharge Mode (Discharge or Flatting)
- Linear Regulators : V_{IN} Range is 2.5V to 5.5V
 - ▶ Max Current 0.3A
 - ▶ I²C Programmable Output Level
- Embedded 32Bytes MTP for Factory Tuning
 - ▶ External MTP Pin for Write Protection
- Sequence can be Controlled by I²C or Each EN Pins Defined by MASK_GPIO Pin
- OT/UVP/VIN LV/POWRON Press Time Interrupt (IRQ)
 - ▶ I²C Control Interface : Support Fast Mode up to 400kb/s
- RoHS Compliant and Halogen Free

Applications

- Industrial

Simplified Application Circuit



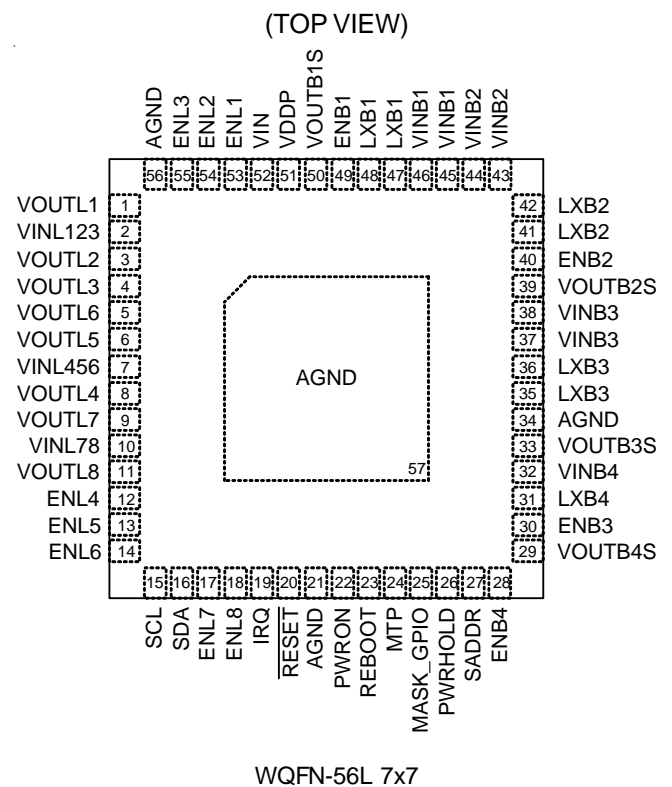
Marking Information



RT5028EGQW : Product Number

YMDNN : Date Code

Pin Configuration

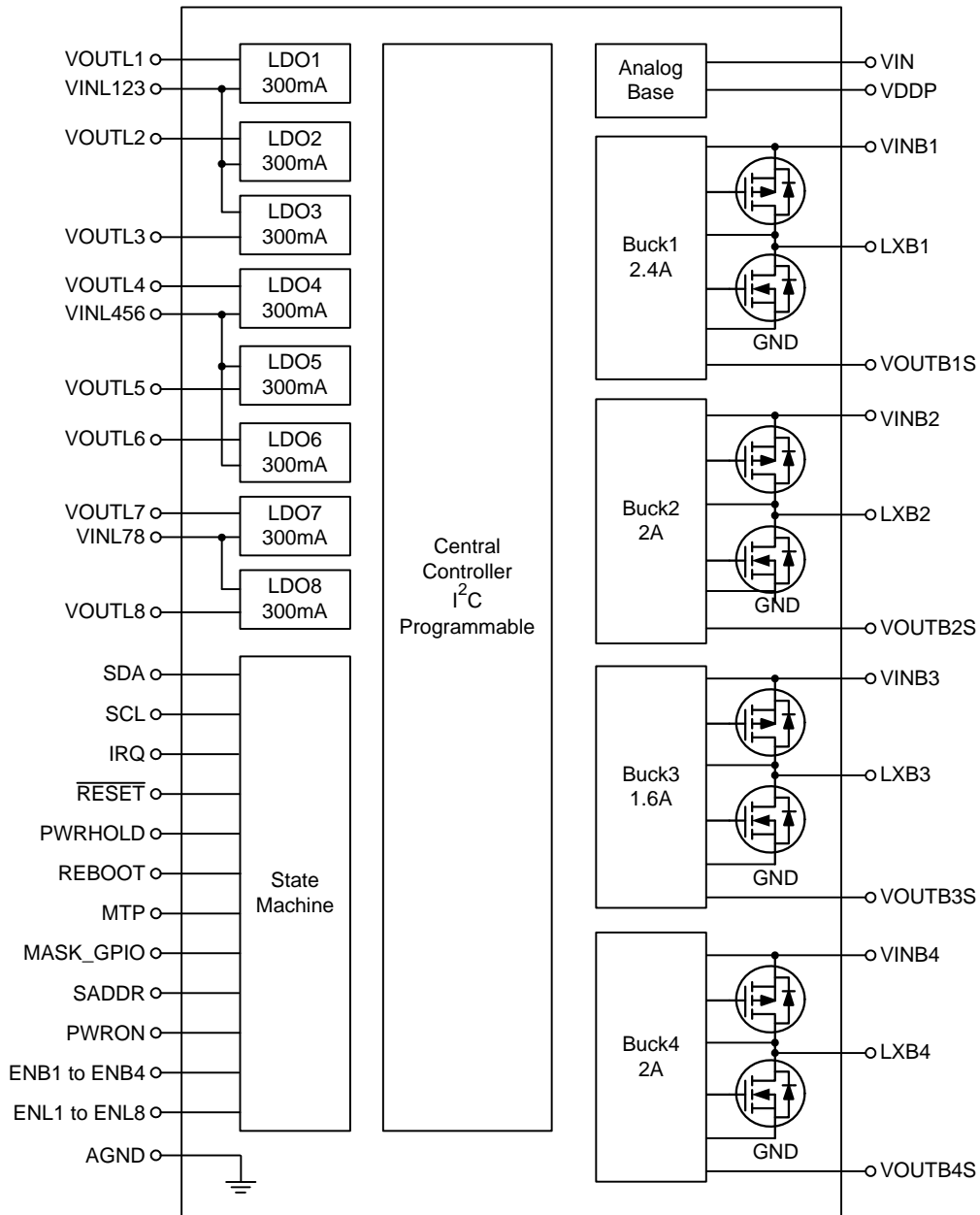


Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---------|----------|---|
| 1 | VOUTL1 | Output voltage regulation node for LDO1. |
| 2 | VINL123 | Input power for LDO1, LDO2 and LDO3. |
| 3 | VOUTL2 | Output voltage regulation node for LDO2. |
| 4 | VOUTL3 | Output voltage regulation node for LDO3. |
| 5 | VOUTL6 | Output voltage regulation node for LDO6. |
| 6 | VOUTL5 | Output voltage regulation node for LDO5. |
| 7 | VINL456 | Input power for LDO4, LDO5 and LDO6. |
| 8 | VOUTL4 | Output voltage regulation node for LDO4. |
| 9 | VOUTL7 | Output voltage regulation node for LDO7. |
| 10 | VINL78 | Input power for LDO7 and LDO8. |
| 11 | VOUTL8 | Output voltage regulation node for LDO8. |
| 12 | ENL4 | Enable control input for LDO4. Connect a 100kΩ pull-low resistor. |
| 13 | ENL5 | Enable control input for LDO5. Connect a 100kΩ pull-low resistor. |
| 14 | ENL6 | Enable control input for LDO6. Connect a 100kΩ pull-low resistor. |
| 15 | SCL | Clock input for I ² C. Open-drain output, connect a 10kΩ pull-up resistor. |

| Pin No. | Pin Name | Pin Function |
|---------------------------------|---------------------------|--|
| 16 | SDA | Data input for I ² C. Open-drain output, connect a 10kΩ pull-up resistor. |
| 17 | ENL7 | Enable control input for LDO7. Connect a 100kΩ pull-low resistor. |
| 18 | ENL8 | Enable control input for LDO8. Connect a 100kΩ pull-low resistor. |
| 19 | IRQ | Open-drain IRQ output node. |
| 20 | $\overline{\text{RESET}}$ | Reset output. |
| 21, 34, 56, 57 (Exposed Pad) | AGND | Analog ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation. |
| 22 | PWRON | Manual power on. Connect a 100kΩ pull-up resistor. |
| 23 | REBOOT | System power reboot. Connect a 100kΩ pull-low resistor. |
| 24 | MTP | MTP write protection. Connect a 100kΩ pull-low resistor, logic low is inhibited and logic high is permit to write. |
| 25 | MASK_GPIO | Select I ² C or use EN pin for Bucks and LDOs. Connect a 100kΩ pull-low resistor. As MASK_GPIO is high, ignore all EN pins. As MASK_GPIO is low, EN pins and I ² C both can control. EN pins priority is higher than I ² C. |
| 26 | PWRHOLD | Power hold input. Connect a 100kΩ pull-low resistor. |
| 27 | SADDR | I ² C slave address. Connect a 100kΩ pull-low resistor. |
| 28 | ENB4 | Enable control input for Buck4. Connect a 100kΩ pull-low resistor. |
| 29 | VOUTB4S | Output voltage regulation node for Buck4. |
| 30 | ENB3 | Enable control input for Buck3. Connect a 100kΩ pull-low resistor. |
| 31 | LXB4 | Internal switch node to output inductor connection for Buck4. |
| 32 | VINB4 | Input power for Buck4. |
| 33 | VOUTB3S | Output voltage regulation node for Buck3. |
| 35, 36 | LXB3 | Internal switch node to output inductor connection for Buck3. |
| 37, 38 | VINB3 | Input power for Buck3. |
| 39 | VOUTB2S | Output voltage regulation node for Buck2. |
| 40 | ENB2 | Enable control input for Buck2. Connect a 100kΩ pull-low resistor. |
| 41, 42 | LXB2 | Internal switch node to output inductor connection for Buck2. |
| 43, 44 | VINB2 | Input power for Buck2. |
| 45, 46 | VINB1 | Input power for Buck1. |
| 47, 48 | LXB1 | Internal switch node to output inductor connection for Buck1. |
| 49 | ENB1 | Enable control input for Buck1. Connect a 100kΩ pull-low resistor. |
| 50 | VOUTB1S | Output voltage regulation node for Buck1 |
| 51 | VDDP | Internal bias regulator voltage. External load on this pin is not allowed. |
| 52 | VIN | Input power for analog base. |
| 53 | ENL1 | Enable control input for LDO1. Connect a 100kΩ pull-low resistor. |
| 54 | ENL2 | Enable control input for LDO2. Connect a 100kΩ pull-low resistor. |
| 55 | ENL3 | Enable control input for LDO3. Connect a 100kΩ pull-low resistor. |

Functional Block Diagram



Operation

The RT5028E is a highly-integrated solution for industrial system including 4-CH step-down DC-DC converters and 8-CH LDOs. The RT5028E application mechanism will be introduced in later sections.

The power-on and power-off sequences can be controlled by I²C or each EN pin and detected in MASK_GPIO pin. When the MASK_GPIO pin is at Hi level, the PMIC follows the power-on sequence to turn on channels. When the MASK_GPIO pin is at Lo level, the channels of PMIC will be controlled by the EN pin.

Synchronous Step-Down DC-DC Converter

Four current mode synchronous step-down DC-DC converters operate with internal power MOSFETs, FB resistors and compensation network. These channels are suitable for core power in industrial system. They can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple. The operating frequency of step-down converter is adjustable from 500kHz to 2MHz and is controlled by I²C. Besides, the I²C interface also can be used to select different operation modes, On/Off Sequence, programmable the output voltage, RAMP control and discharge function. To enable AUTO Mode, it is used to improve the efficiency at light load. If the AUTO Mode is disabled, the converter operates in force PWM mode with fixed switching frequency.

Linear Regulator

Eight generic low voltage LDOs for multiple purpose power. The LDOs are stable over the entire operating load range with the use of external ceramic capacitors. The LDOs also have I²C programmable power on/off sequence and discharge function. The output voltage is adjustable by the I²C interface in the range of 1.6V to 3.6V.

Over-Temperature Protection

An Over-Temperature Protection (OTP) is contained in the device. The protection is triggered to force the device shutdown for protecting itself when the junction temperature exceeds 165°C typically. Once the junction temperature drops below the hysteresis 10°C typically, the device must be re-send PWRON to start system.

Output Under-Voltage Protection

The output under-voltage protection is implemented in order to prevent operation at low output voltage conditions. When the step-down DC-DC converters output voltage is lower than 1/2 x (V_{OUT}), the UVP event triggers and PMIC turns off immediately.

Absolute Maximum Ratings (Note 1)

- Analog Base Input Voltage, V_{IN} ----- -0.3V to 6V
- PMIC Input Voltage, $V_{INL123/456/78}$, $V_{INB1/2/3/4}$ ----- -0.3V to 6V
- PMIC Output Voltage, V_{OUTLx} , V_{OUTBxS} , $LXBx$ ----- -0.3V to 6V
- PMIC related Other Pins ----- -0.3V to 6V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 WQFN-56L 7x7 ----- 3.7W
- Package Thermal Resistance (Note 2)
 WQFN-56L 7x7, θ_{JA} ----- 27°C/W
 WQFN-56L 7x7, θ_{JC} ----- 7°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = 3.3\text{V}$ to 5.5V , $T_A = -40^\circ\text{C}$ to 85°C , unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------|-----------|--|-----|-----|-----|------------------|
| Operation Voltage of V_{IN} | | As $f_{SW} > 1\text{MHz}$, $3.3\text{V} \leq V_{IN} \leq 5.5\text{V}$. If $f_{SW} \leq 1\text{MHz}$, $V_{IN} \geq 4\text{V}$. | 3.3 | -- | 5.5 | V |
| PMIC | | | | | | |
| Quiescent Current | I_{IN} | $V_{IN} = 5\text{V}$, LDOs, Bucks are ON with No Load. | 300 | 450 | 600 | μA |
| | | $V_{IN} = 5\text{V}$, LDOs, Bucks are OFF. SCL = SDA = 0V | 5 | 20 | 40 | μA |
| Warning for Die Temperature | OTW | Temperature 1 | -- | 100 | -- | $^\circ\text{C}$ |
| | | Temperature 2 | -- | 125 | -- | |
| Over-Temperature Protection | OTP | | -- | 165 | -- | $^\circ\text{C}$ |
| OTP and Warning Hysteresis | | | -- | 10 | -- | $^\circ\text{C}$ |
| Input Pull-low 100k Resistor | R_{Low} | $V_{IN} = 5\text{V}$, Temperature = -40°C to 125°C | 70 | 115 | 160 | $\text{k}\Omega$ |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit | |
|--|---------------------|---|---|------|-----|--------|-----|
| Buck1 to Buck4 | | | | | | | |
| Input Voltage | V _{INB} | | 3.3 | -- | 5.5 | V | |
| Output Voltage | V _{OUTB} | Buck1 I ² C Programmable per step 25mV | 0.7 | -- | 1.8 | V | |
| | | Buck2 I ² C Programmable per step 25mV | 0.7 | -- | 1.8 | | |
| | | Buck3 I ² C Programmable per step 50mV | 0.7 | -- | 3.6 | | |
| | | Buck4 I ² C Programmable per step 50mV | 0.7 | -- | 3.6 | | |
| Consumption Current | I _{VINB} | AUTO Mode I _{OUT} = 0mA, Each Buck | 10 | 20 | 40 | μA | |
| Efficiency Peak | Eff | V _{OUT} = 1.2V, V _{IN} = 3.6V | I _{LOAD} = CCM | -- | 88 | -- | % |
| | | | I _{LOAD} = 1mA | -- | 80 | -- | |
| Output Voltage Accuracy | V _{OUTAcc} | 3.1V < V _{IN} < 5.5V, 1mA < I _{OUT} < I _{MAX} | As V _{OUTB1S} to V _{OUTB4S} ≥ 1V. | -3 | -- | 3 | %mV |
| | | | As V _{OUTB1S} to V _{OUTB4S} < 1V. | 30 | -- | 30 | |
| Output Voltage Ripple | V _{Rip} | I _{OUT} = 1mA, C _{OUT} = 10μF, 2MHz | | -- | 25 | -- | mV |
| | | I _{OUT} = 1A, C _{OUT} = 10μF, 2MHz | | -- | 8 | -- | |
| Output Voltage Temperature Coefficient | | | -- | ±100 | -- | ppm/°C | |
| Switching Frequency | f _{sw} | I ² C Programmable | 0.43 | -- | 2 | MHz | |
| Switching Frequency Accuracy | | 1MHz < f _{sw} | -10 | -- | 10 | % | |
| | | f _{sw} ≤ 1MHz | -20 | -- | 20 | | |
| Suggest Inductor | L _{Buck} | | -- | 2.2 | -- | μH | |
| Peak Current Limit | OCP | Buck1 | 3.1 | 4.4 | 5.8 | A | |
| | | Buck2 | 2.8 | 4 | 5.2 | | |
| | | Buck3 | 2.6 | 3.7 | 4.8 | | |
| | | Buck4 | 2.8 | 4.1 | 5.3 | | |
| Under-Voltage Protection | UVP | V _{OUTB1S} to V _{OUTB4S} < 0.66 x (V _{OUT} Target) | 56 | 66 | 76 | % | |
| Maximum Output Current | I _{MAX} | Buck1 | 2.4 | -- | -- | A | |
| | | Buck2 | 2 | -- | -- | | |
| | | Buck3 | 1.6 | -- | -- | | |
| | | Buck4 | 2.0 | -- | -- | | |
| Output Transient Response | V _{peak} | 0.8A to 1.6A at 20μs, V _{OUT} = 1.2V Buck1 and Buck2 | -4 | -- | 4 | % | |
| High-Side On-Resistance | R _{pon} | V _{IN} = 3.7V | 50 | 150 | 250 | mΩ | |
| Low-Side On-Resistance | R _{nnon} | V _{IN} = 3.7V | 40 | 110 | 160 | mΩ | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit | |
|--|------------------------------------|---|---|------------|------|--------|---|
| LDO1 to LDO8 | | | | | | | |
| Input Voltage for VINL123/456/78 | V _{INL} | | 2.5 | -- | 5.5 | V | |
| Output Voltage LDO123/78 | V _{OUTL} | 3.1V ≤ V _{IN} ≤ 5.5V, 50μA ≤ I _{OUT} ≤ I _{MAX} | -3% | 1.6 to 3.6 | 3% | V | |
| Output Voltage LDO456 | V _{OUTL} | 3.1V ≤ V _{IN} ≤ 5.5V, 50μA ≤ I _{OUT} ≤ I _{MAX} | -3% | 3 to 3.6 | 3% | V | |
| Output Current | I _{OUT} | | 300 | -- | -- | mA | |
| Output Short Current | I _{sht} | | 330 | 450 | 600 | mA | |
| Voltage Difference | V _{IN} - V _{OUT} | V _{IN} > 3.1V | V _{IN} = V _{SET} , I _{OUT} = I _{OUTMAX} | 0.05 | 0.1 | 0.3 | V |
| | | V _{IN} > 2.5V | | 0.05 | 0.11 | 0.5 | |
| Output Voltage Temperature Coefficient | | | -- | ±100 | -- | ppm/°C | |
| Supply Current | I _{SS} | I _{OUT} = 0mA | 10 | 35 | 60 | μA | |
| Shutdown Current | I _{OFF} | | 0 | 1 | 2 | μA | |
| Line Regulation | | Input 3V to 5V, load = 100mA | 0 | 1 | 5 | mV | |
| Load Regulation | | V _{IN} = 5V, Load 100mA to 300mA | 0 | 0.1 | 1 | % | |
| Transient Response | ΔV _{OUT} | 50μA ↔ I _{OUTMAX} / 2 (Δt = 1μs) | -- | 50 | -- | mV | |
| Ripple Rejection | | f = 10kHz, I _{OUT} = I _{OUTMAX} / 2 | -- | 60 | -- | dB | |
| Rising Time | | V _{OUT} ≥ 0.7 × V _{Target} , I _{OUT} = 0mA | 150 | 220 | 300 | μs | |
| Falling Time | | V _{OUT} ≤ 0.3 × V _{Target} , I _{OUT} = 0mA | 300 | 600 | 1000 | μs | |
| I²C Interface and Control Input Pin Electrical Characteristics | | | | | | | |
| Voltage Output Low | V _{OL} | | -- | -- | 0.4 | V | |
| Input Voltage | High-Level | V _{IH} | 1.5 | -- | -- | V | |
| | Low-Level | V _{IL} | -- | -- | 0.4 | | |
| SCL Clock | SCL | | -- | -- | 400 | kHz | |

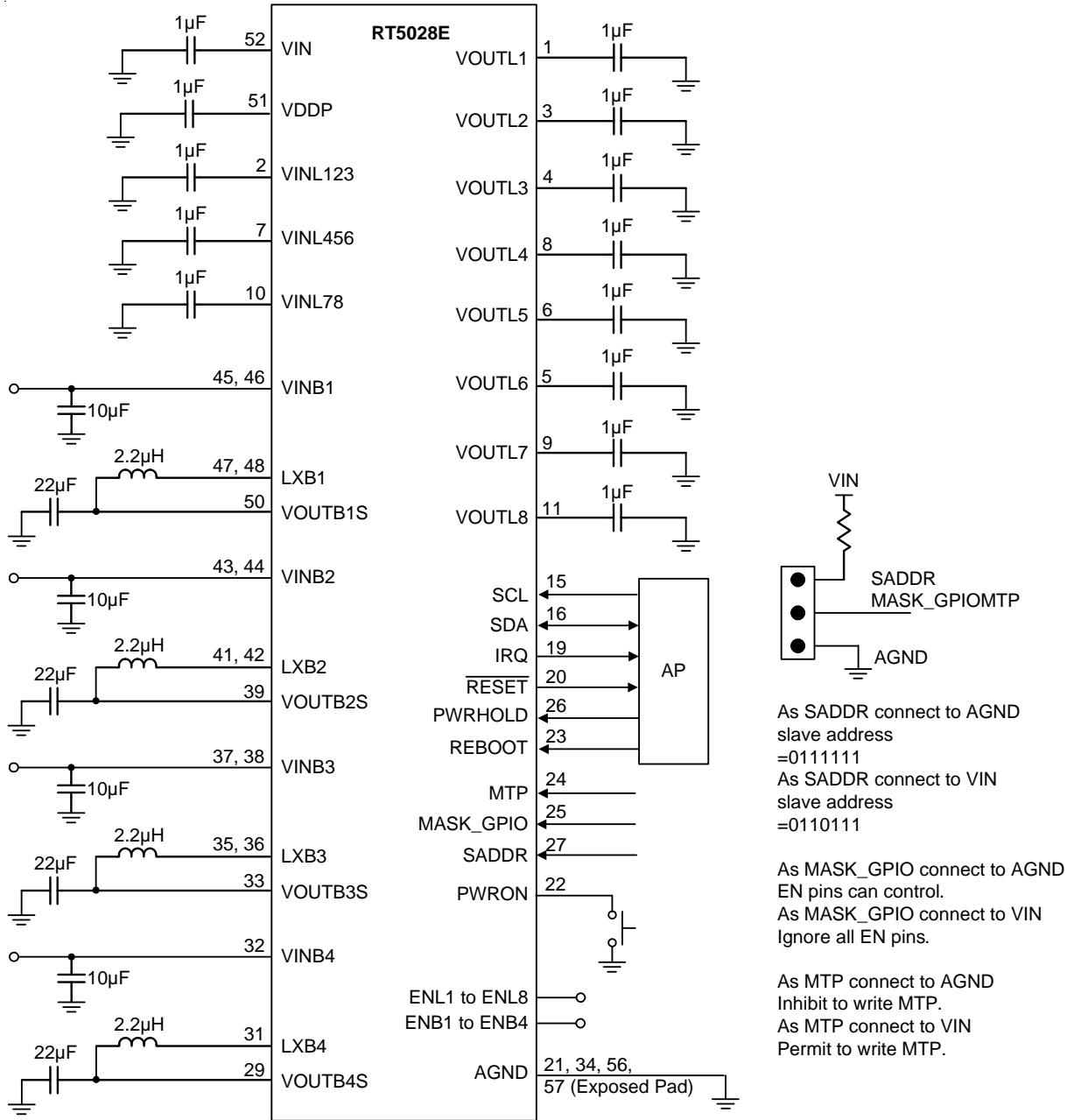
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

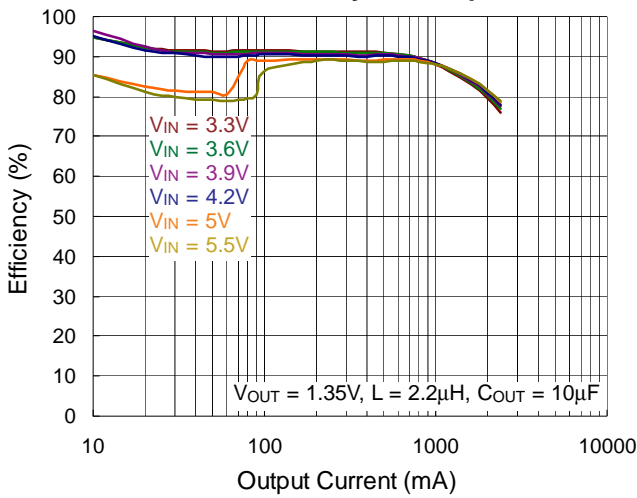
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

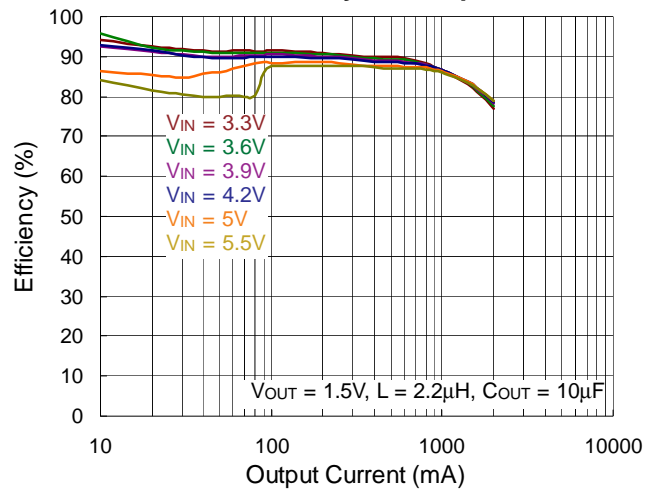


Typical Operating Characteristics

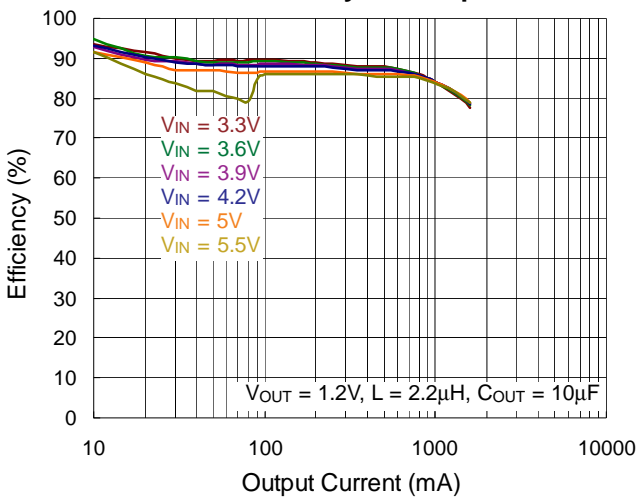
CH1 Buck Efficiency vs. Output Current



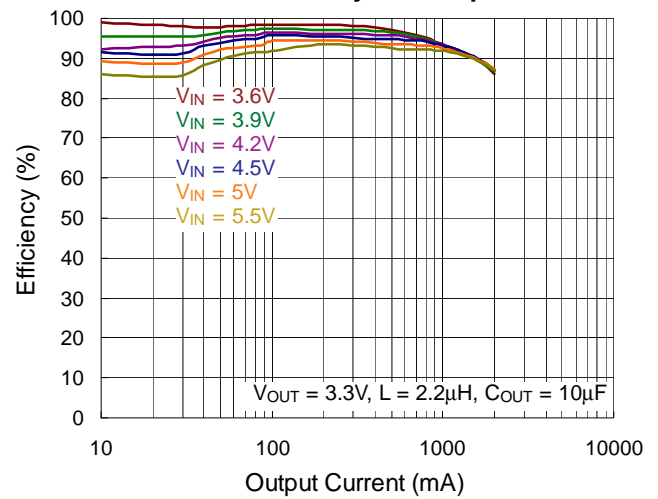
CH2 Buck Efficiency vs. Output Current



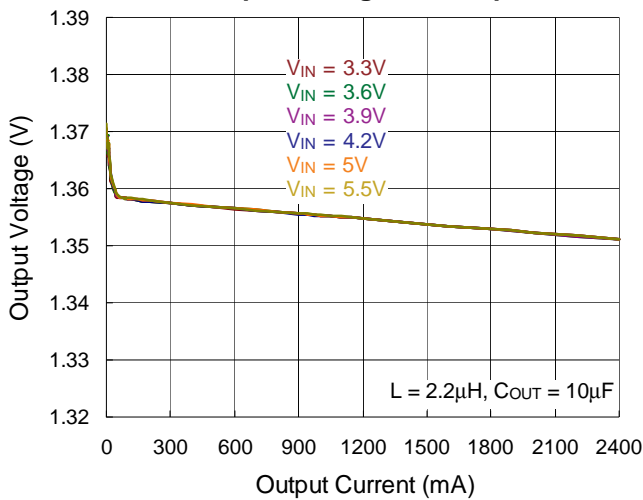
CH3 Buck Efficiency vs. Output Current



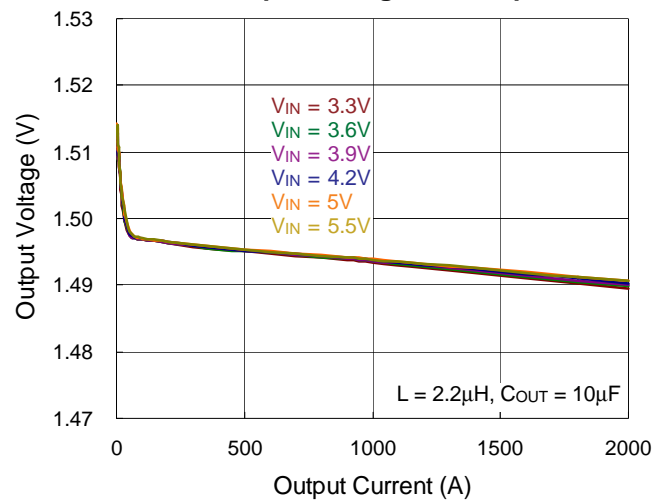
CH4 Buck Efficiency vs. Output Current



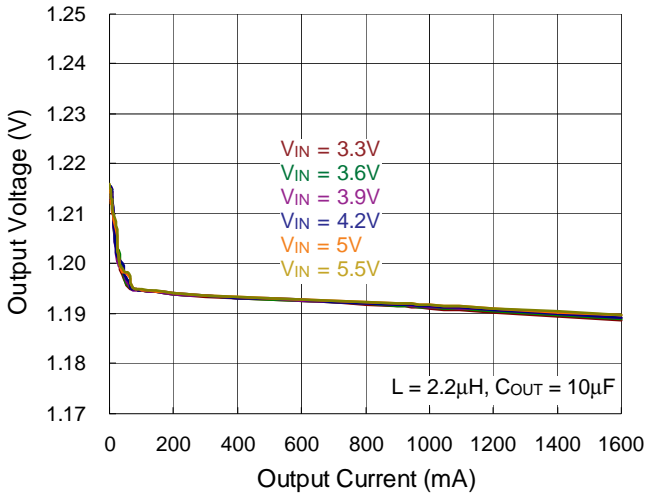
CH1 Buck Output Voltage vs. Output Current



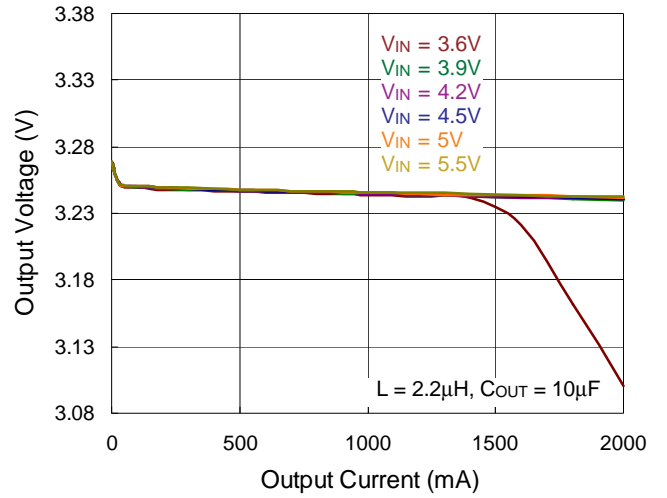
CH2 Buck Output Voltage vs. Output Current



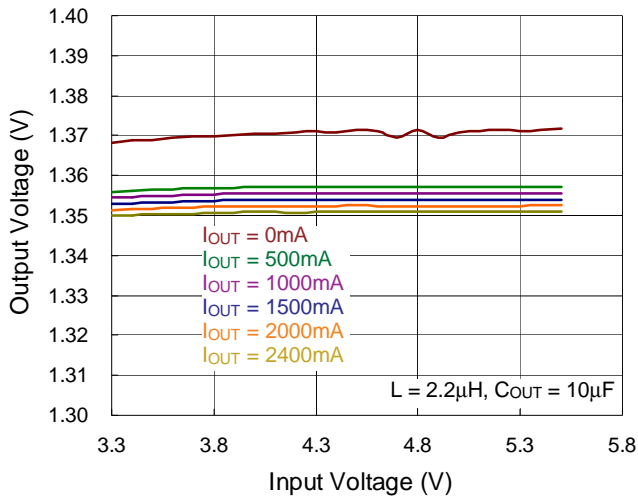
CH3 Buck Output Voltage vs. Output Current



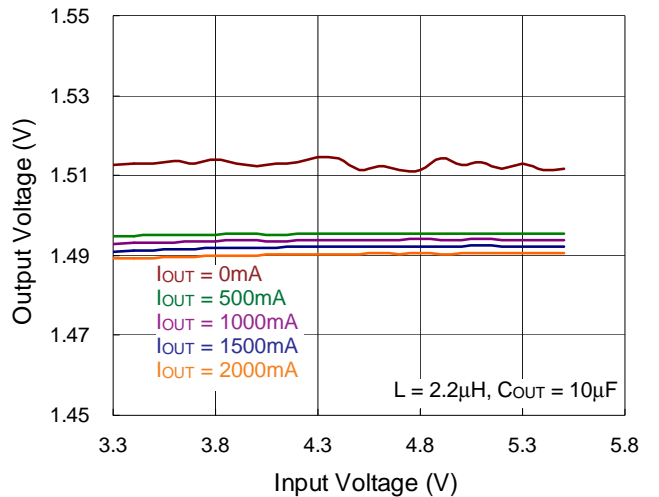
CH4 Buck Output Voltage vs. Output Current



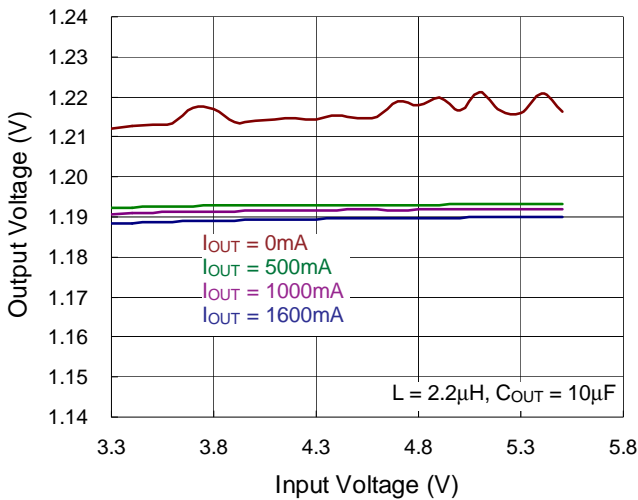
CH1 Buck Output Voltage vs. Input Voltage



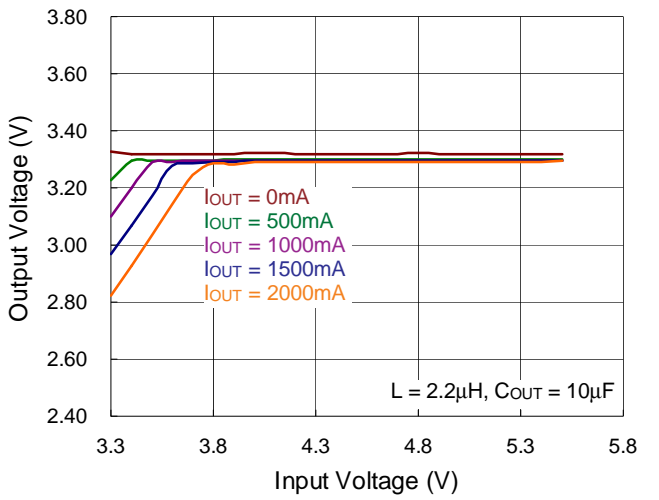
CH2 Buck Output Voltage vs. Input Voltage



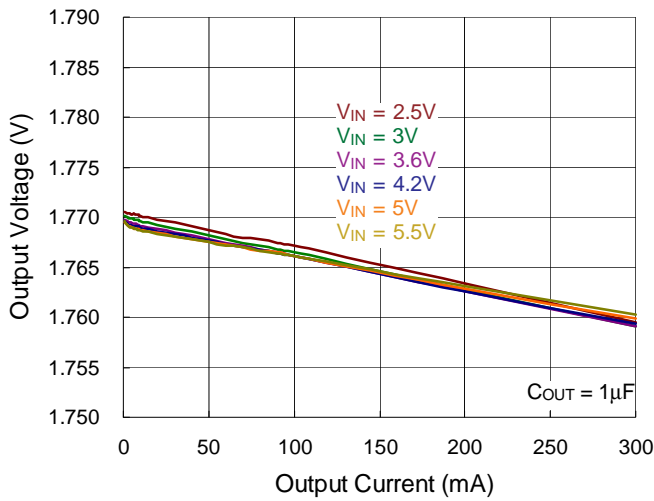
CH3 Buck Output Voltage vs. Input Voltage



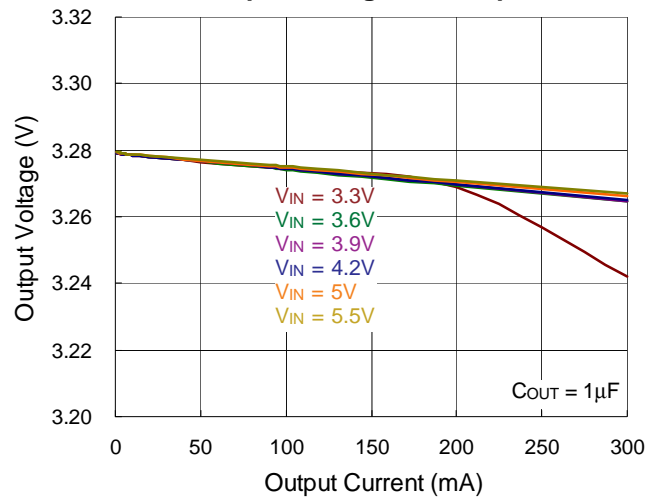
CH4 Buck Output Voltage vs. Input Voltage



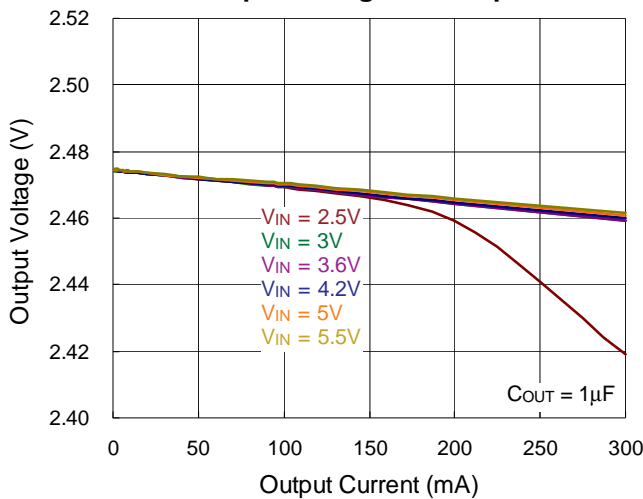
LDO2 Output Voltage vs. Output Current



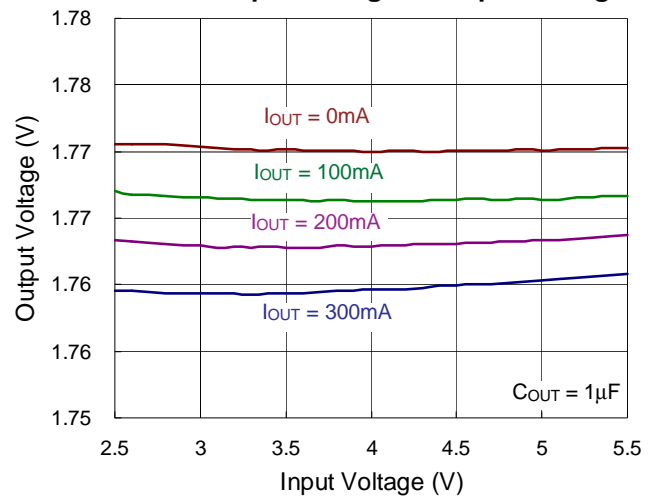
LDO5 Output Voltage vs. Output Current



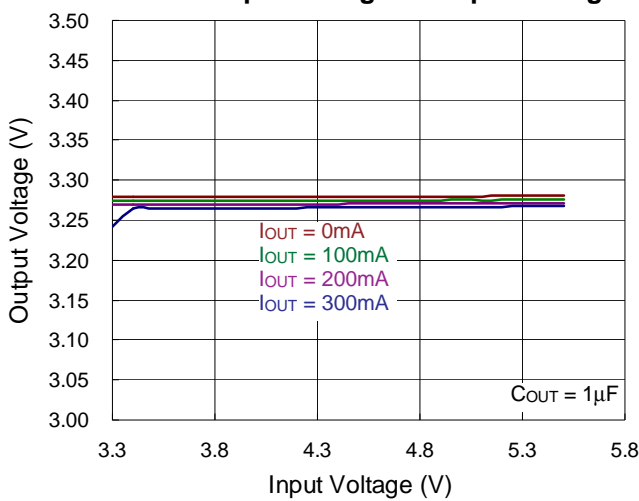
LDO7 Output Voltage vs. Output Current



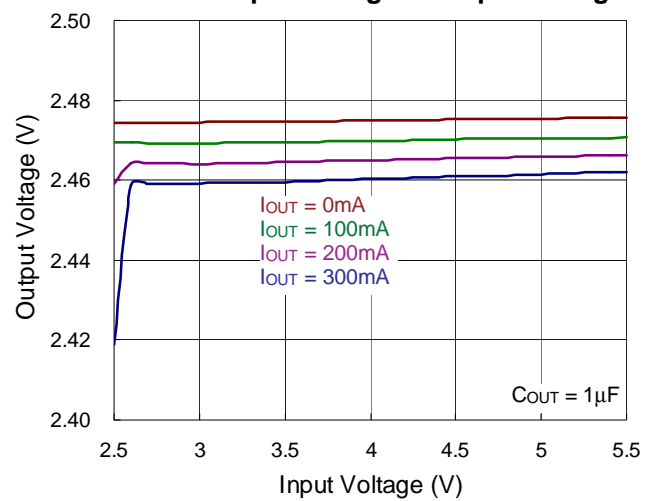
LDO2 Output Voltage vs. Input Voltage



LDO5 Output Voltage vs. Input Voltage



LDO7 Output Voltage vs. Input Voltage



Application Information

The RT5028E is a highly-integrated solution for industrial system including PMIC and memory system. The RT5028E application mechanism and I²C compatible interface are introduced in later sections. The system's slave address is 0110111 (As SADDR = high) or 0111111(As SADDR = low).

PMIC - Power management system provides 8 low dropout linear regulator and 4 high efficiency synchronous step-down DC-DC converters. Power-On and Power-Off sequences are control by PWRON and $\overline{\text{RESET}}$ input pins.

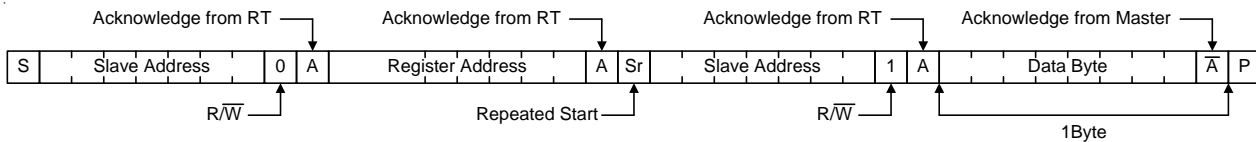
Detail time sequence control is described in Power ON/OFF diagram. The I²C interface can program individual regulator output voltage as well as on/off control and voltage setting.

I²C Interface Timing Diagram

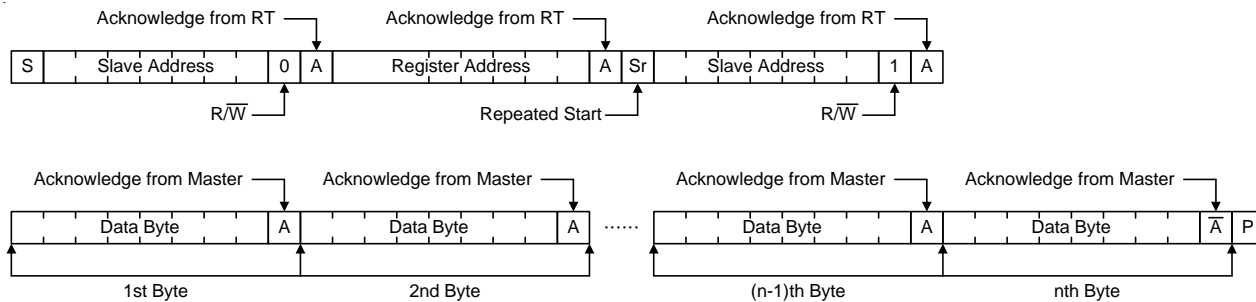
The RT5028E acts as an I²C -bus slave. The I²C-bus master configures the settings for all function blocks by sending command bytes to the RT5028E via the 2-wire I²C-bus. The I²C timing diagrams are list in the following.

Read Function

Reading One Indexed Byte of Data from RT (With 1-Byte)

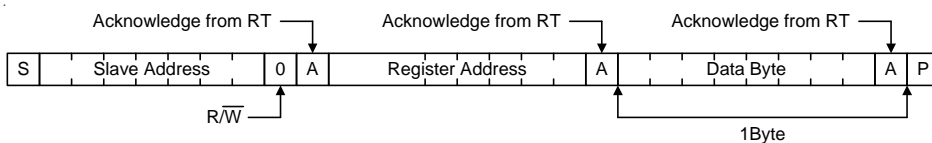


Reading n Indexed Words of Data from RT (With N-Byte)

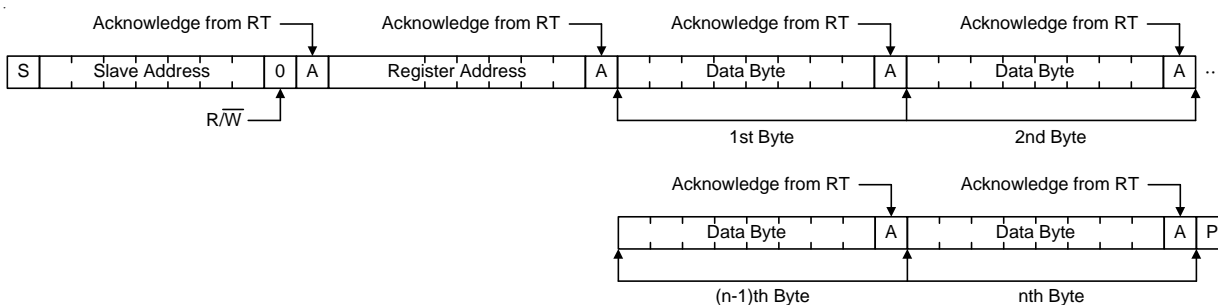


Write Function

Writing One Byte of Data to RT (With 1-Byte)



Writing n Bytes of Data to RT (With N-Byte)

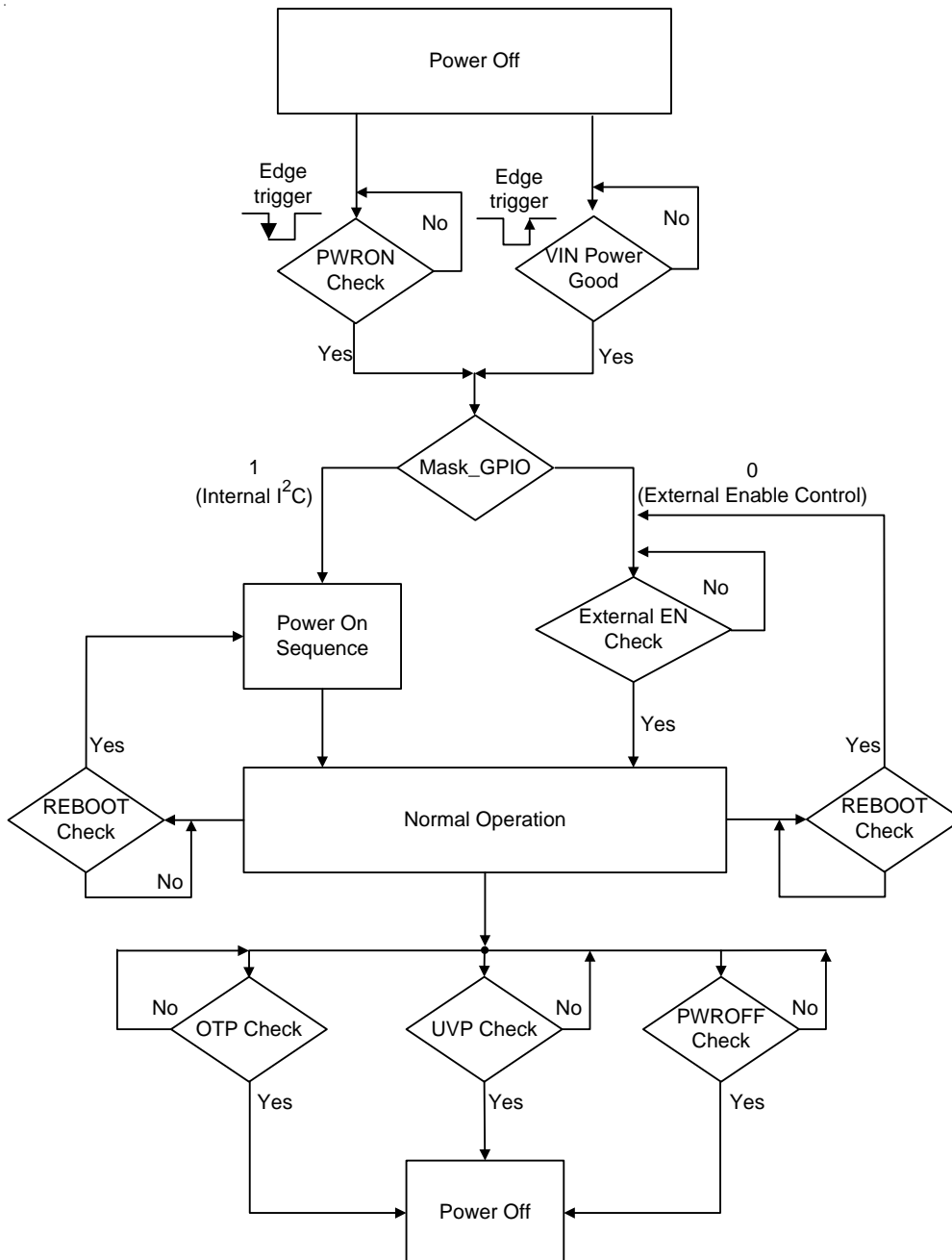


PMIC

Power Channels Control Methodology

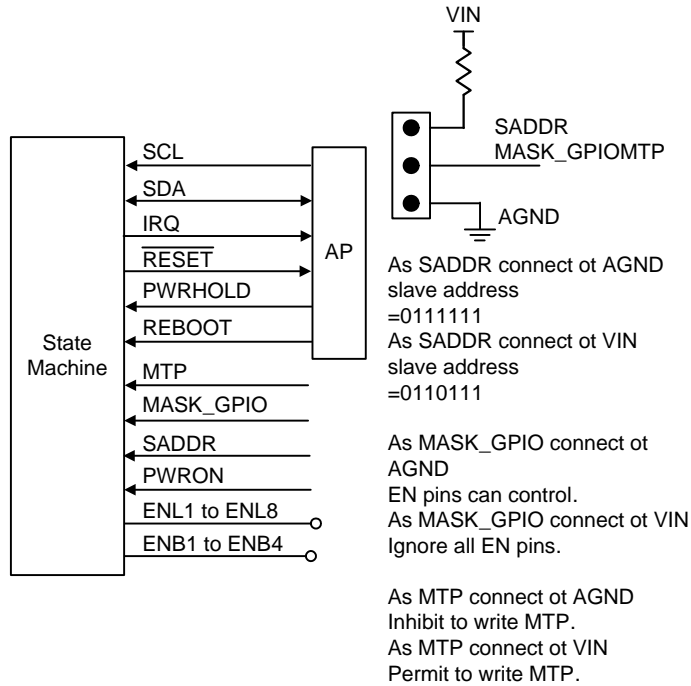
When VIN power Good or PWRON event occurs, the PMIC will follow the power on sequence to turn on channels. During normal operation, users can use the REBOOT pin

to restart PMIC again. Another PWROFF event, OTP or UVP occurs, PMIC will execute the power off. In the RT5028E PMIC, the UVP event will be set out when the Buck1 to Buck4s' output voltage is lower than $1/2 \times (V_{OUT})$.



PMIC - POWER ON/OFF Setting

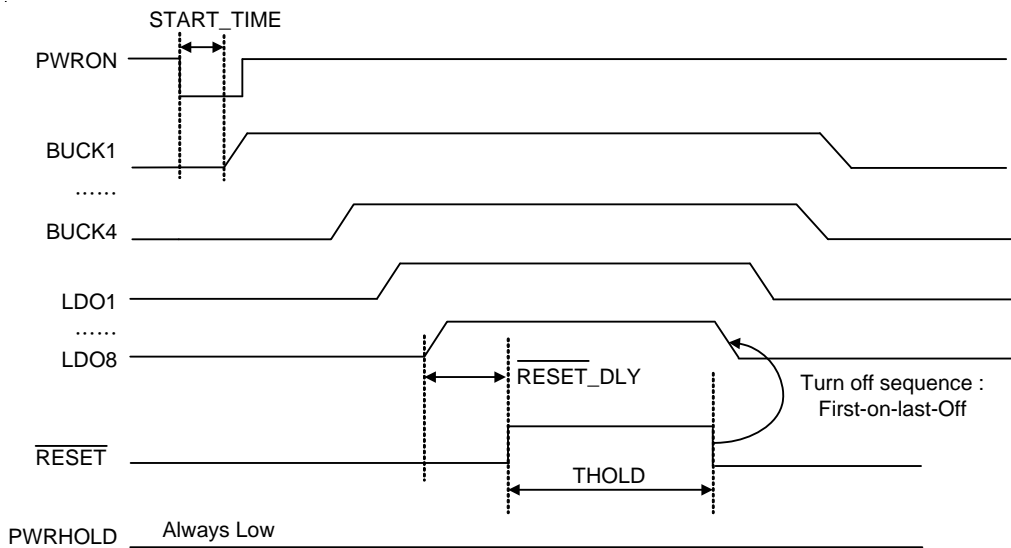
The circuit setting for communication between the RT5028E and AP is showed as below.



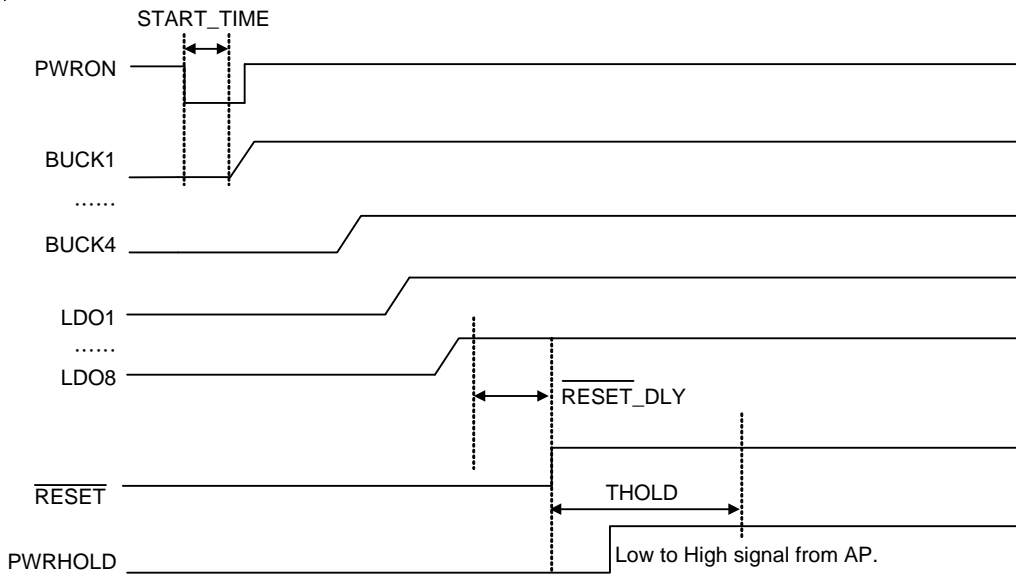
Power Hold Function

When the "PWRHOLD" signal does not come during THOLD time, the RT5028E will do shutdown sequence.

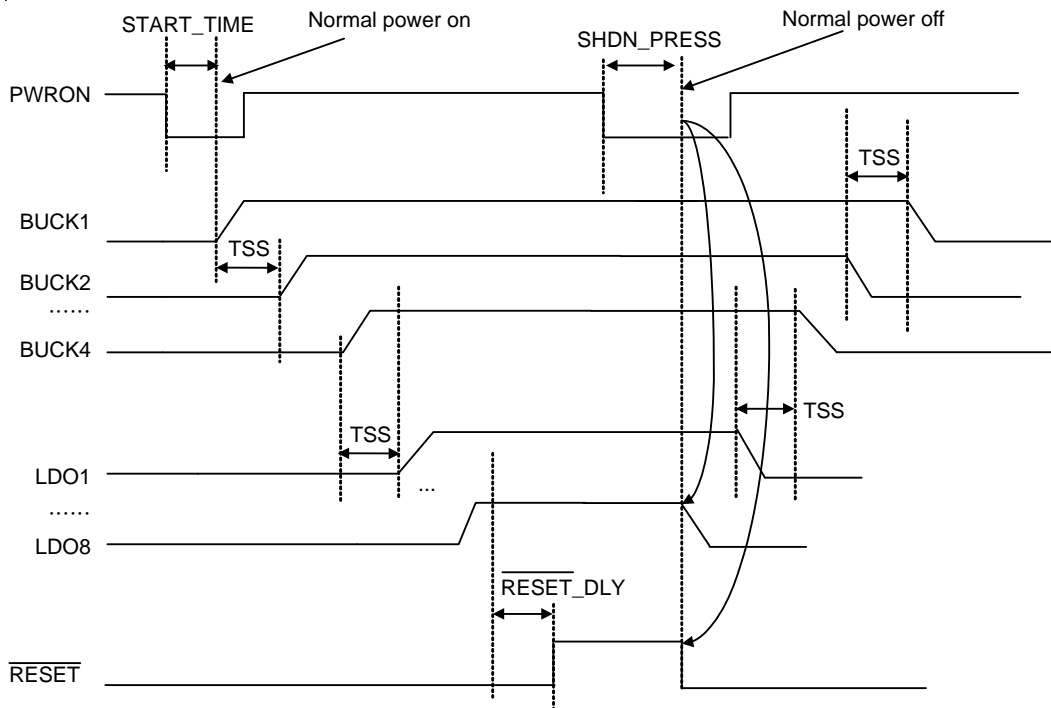
If users want to disable power hold function, set "DisTHOLD" bit in I²C register 10 bit[0] to disable this function. In the timing diagram below, the "THOLD" and "RESET_DLY" can be set by MTP program.



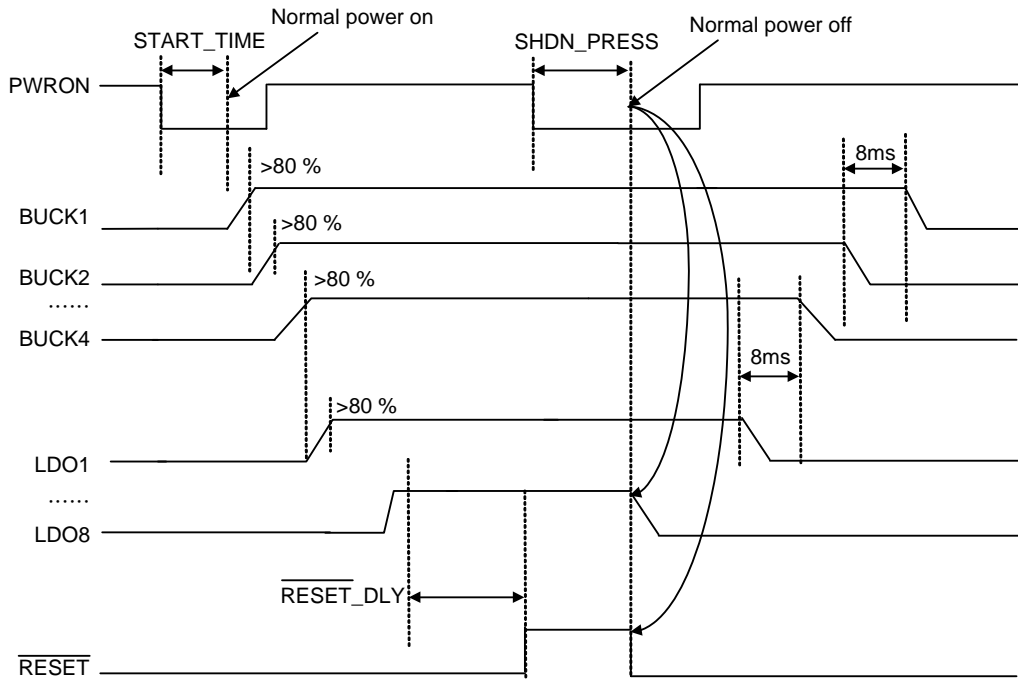
When AP sends the "PWRHOLD" signal during THOLD time, the RT5028E will keep power-on.



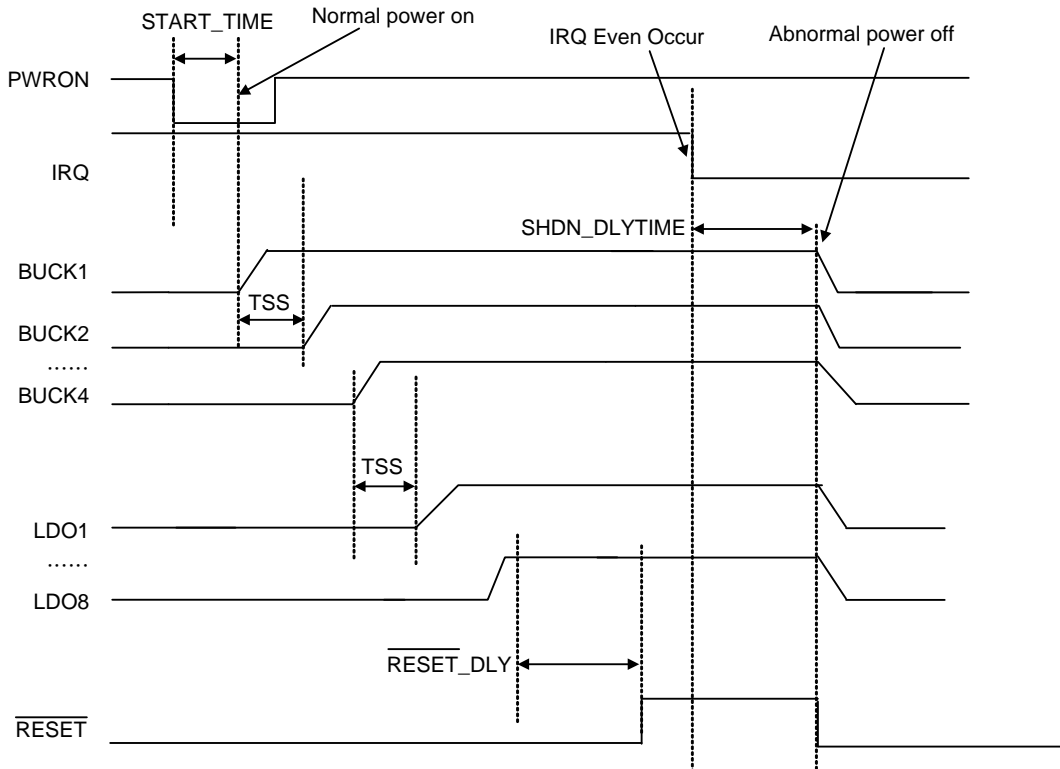
Timing Based ON/OFF Sequence



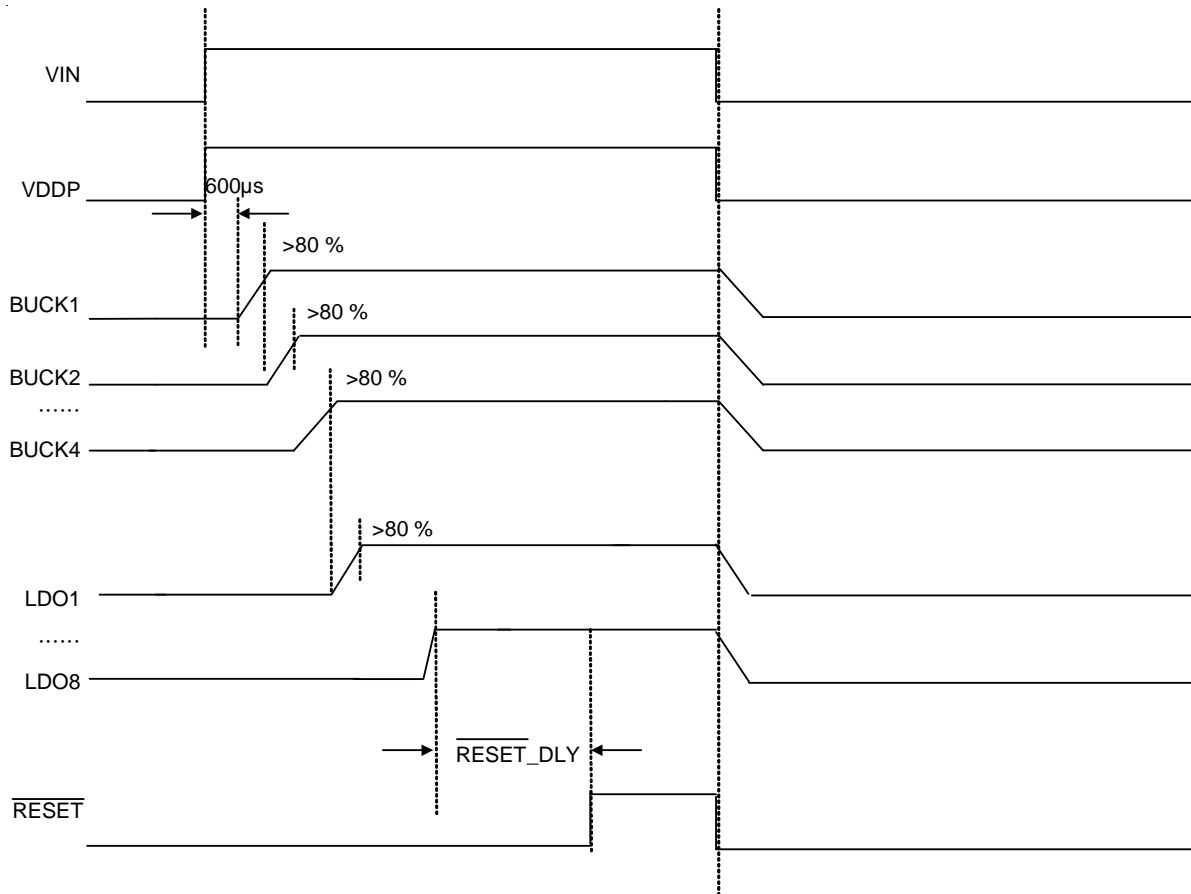
Level Based ON/OFF Sequence



Abnormal OFF



Based ON/OFF Sequence by VIN



PMU On/Off Sequence Setting

In the RT5028E, users can set the power on/off sequence and output voltage by I²C register 0x01 to 0x04 for Buck output voltage, 0x07 to 0x0E for LDO output voltage and 0x2C to 0x32 for startup sequence setting.

In the table below, users must set one by one (continues number) and missing code is not allowed.

If users miss sequence code, the RT5028E will wait for next channel and the IC will be hold in waiting status.

| | Output Voltage Setting | Startup Sequence Setting | Startup Enable Method (Soft-Start Control) |
|-------|-------------------------------|---------------------------------|---|
| Buck1 | Buck1Output[5:0] | Buck1_Seq[3:0] | [10] |
| | [000000] | [0001] | |
| Buck2 | Buck2Output[5:0] | Buck2_Seq[3:0] | |
| | [101100] | [0010] | |
| Buck3 | Buck3Output[5:0] | Buck3_Seq[3:0] | |
| | [000000] | [0011] | |
| Buck4 | Buck4Output[5:0] | Buck4_Seq[3:0] | |
| | [101100] | [0100] | |
| LDO1 | LDO1OUT[6:0] | LDO1_Seq[3:0] | |
| | [0000000] | [0101] | |
| LDO2 | LDO2OUT[6:0] | LDO2_Seq[3:0] | |
| | [0101000] | [0110] | |
| LDO3 | LDO3OUT[6:0] | LDO3_Seq[3:0] | |
| | [0000000] | [0111] | |
| LDO4 | LDO4OUT[6:0] | LDO4_Seq[3:0] | |
| | [0101000] | [1000] | |
| LDO5 | LDO5OUT[6:0] | LDO5_Seq[3:0] | |
| | [0000000] | [1001] | |
| LDO6 | LDO6OUT[6:0] | LDO6_Seq[3:0] | |
| | [0101000] | [1010] | |
| LDO7 | LDO7OUT[6:0] | LDO7_Seq[3:0] | |
| | [0000000] | [1011] | |
| LDO8 | LDO8OUT[6:0] | LDO8_Seq[3:0] | |
| | [0101000] | [1100] | |

Note :

* Output Voltage Setting: fill relative binary code to set the output voltage.

* Startup Sequence Setting :

“0000” denotes no operation (disable).

“0001” denotes first-startup.

“1100 to 1111” denotes last-startup.

If same number, it means startup at the same time.

*Startup Enable Method :

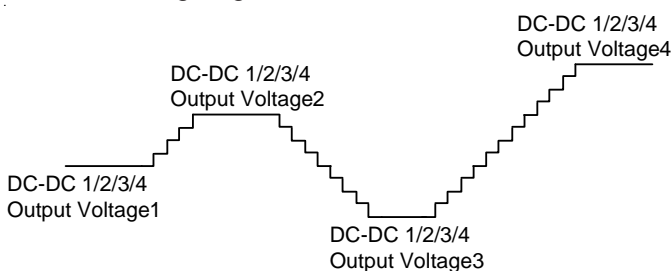
[01] to [11] : each startup enable interval time (1ms, 4ms, 8ms).

[00] : start end voltage (the output voltage's 80%)

Synchronous Step-Down DC-DC Converter

Four current mode synchronous step-down DC-DC converters operate with internal power MOSFETs and compensation network. These channels supply the power core chip of portable system. They can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple. The operating frequency range of step-down converter is 0.5MHz to 2MHz.

Four step-down converters have RAMP control function as the following diagram.

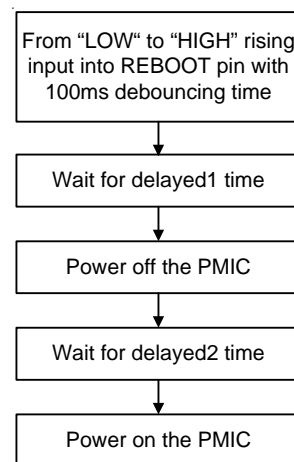


REBOOT Function

As the REBOOT pin is set from low to high, the REBOOT function will be active. The REBOOT's FSM is shown as below. It concludes 100ms de-bouncing time and delay1/delay2 power off delay time.

Table 1. REBOOT Input Control Setting

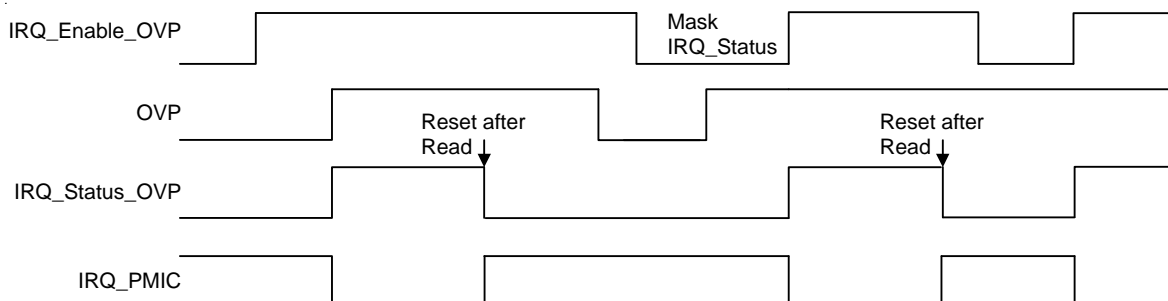
| | Description | Default |
|----------|--|---------|
| delayed2 | 00 : 100ms 10 : 1s | 10 |
| delayed1 | 01 : 500ms 11 : 2s | 10 |
| Action | delayed1 power-off then delayed2 power-on PMIC | |



IRQ Table

We summarize all IRQ items in the register table. All IRQ_status registers are implemented as reset after read. If IRQ_enable bit is Low, the IRQ_status bit will not update status. IRQ_enable will mask IRQ_status to trigger IRQ_PMIC Low, so the system can decide which interrupt is necessary.

Waveform - (when the other IRQ_status are low)



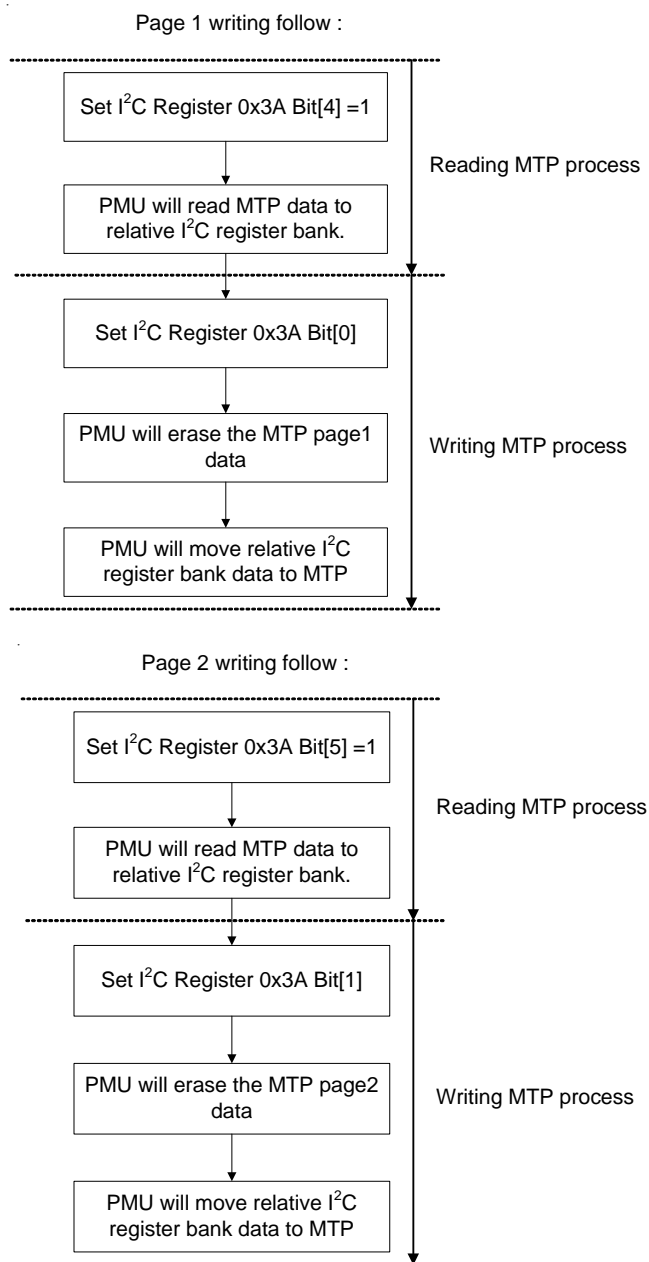
Waveform - (when the other IRQ_status are low)

* OTW125/OTW100 means the 125°C/100°C pre-warming over temperature. It only change IRQ status bits and don't trigger IRQ pin.

EEPROM (MTP) Control Flow

The RT5028E embeds 32 bytes MTP memory, and it allows users to save some I²C register bank data to MTP. When the I²C register 0x3A Bit[0]/Bit[1] is wrote to "1", the MTP Page1/Page2 will execute erase process firstly.

Because the erase process will be done in every writing time, the MTP data will be missed. So it would be best for users to read data from MTP to I²C first before executing writing process.



Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-56L 7x7 package, the thermal resistance, θ_{JA} , is 27°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (27^\circ\text{C/W}) = 3.7\text{W for a WQFN-56L 7x7 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

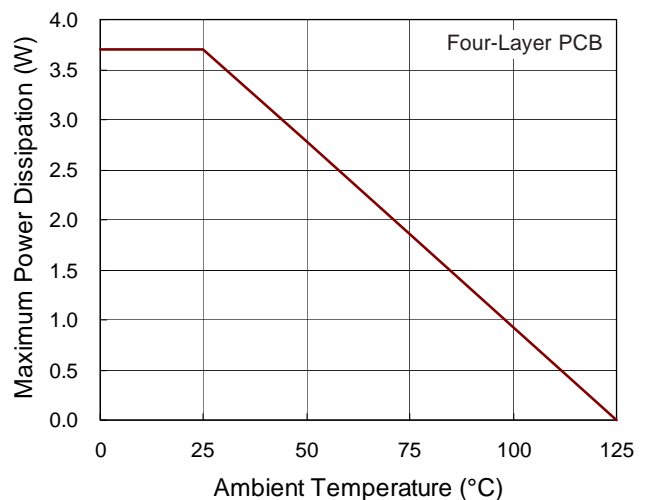


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT5028E, the following PCB layout guidelines must be strictly followed.

- ▶ Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- ▶ Keep the main power traces as wide and short as possible.
- ▶ The switching node area connected to LX and inductor should be minimized for lower EMI.
- ▶ Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- ▶ Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

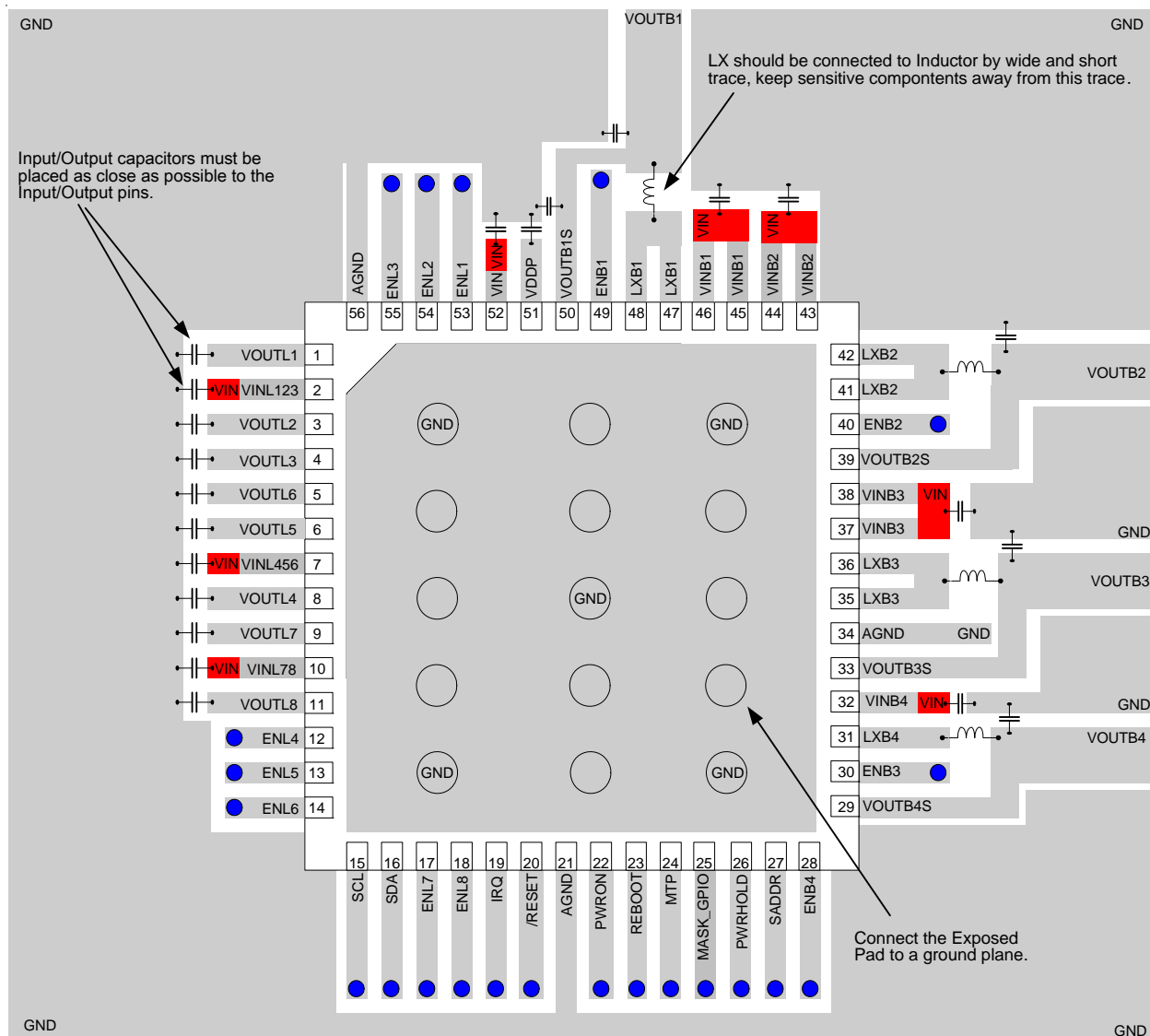


Figure 2. PCB Layout Guide

Table 2. I²C Register Table

| Detail Description | | | | |
|--------------------|------------------|--|------------|-------------|
| Address | 00 | Device ID | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:4] | VENDOR_ID | Vendor Identification : Richtek : 1000b | R | 1000 |
| [3:0] | CHIP_REV | Chip Revision | R | 0001 |
| Address | 01 | BUCKcontrol1 | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:2] | Buck1Output[5:0] | Buck1 output voltage regulation 000000 : 0.7V, 25mV per step 000001 : 0.725V ... 101100 : 1.8V ... 111111 : 1.8V | R/W | Option |
| [1:0] | Buck1VRC | VRC setting 00 : 25mV/10μs, 01 : 50mV/10μs, 10 : 100mV/10μs, 11 : 200mV/10μs | R/W | Option |
| Address | 02 | BUCKcontrol2 | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:2] | Buck2Output[5:0] | Buck2 output voltage regulation 000000 : 0.7V, 25mV per step 000001 : 0.725V ... 101100 : 1.8V ... 111111 : 1.8V | R/W | Option |
| [1:0] | Buck2VRC | VRC setting 00 : 25mV/10μs, 01 : 50mV/10μs, 10 : 100mV/10μs, 11 : 200mV/10μs | R/W | Option |
| Address | 03 | BUCKcontrol3 | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:2] | Buck3Output[5:0] | Buck3 output voltage regulation 000000 : 0.7V, 50mV per step 000001 : 0.75V ... 111010 : 3.6V ... 111111 : 3.6V | R/W | Option |
| [1:0] | Buck3VRC | VRC setting 00 : 50mV/10μs, 01 : 100mV/10μs, 10 : 200mV/10μs, 11 : 400mV/10μs | R/W | Option |

| Address | 04 | BUCKcontrol4 | | | |
|---------|------------------|---|-----|-------------|--|
| Bit | Name | Description | R/W | Reset Value | |
| [7:2] | Buck4Output[5:0] | Buck4 output voltage regulation 000000 : 0.7V, 50mV per step 000001 : 0.75V ... 111010 : 3.6V ... 111111 : 3.6V | R/W | Option | |
| [1:0] | Buck4VRC | VRC setting 00 : 50mV/10μs, 01 : 100mV/10μs, 10 : 200mV/10μs, 11 : 400mV/10μs | R/W | Option | |
| Address | 05 | VRC Control | | | |
| Bit | Name | Description | R/W | Reset Value | |
| 7 | Buck1VRC_EN | Buck1 VRC 0 : disable - voltage ramps up to target voltage with one time 1 : enable - voltage ramps up to target voltage with slope control | R/W | Option | |
| 6 | Buck2VRC_EN | Buck2 VRC 0 - disable - voltage ramps up to target voltage with one time 1 - enable - voltage ramps up to target voltage with slope control | R/W | Option | |
| 5 | Buck3VRC_EN | Buck3 VRC 0 : disable - voltage ramps up to target voltage with one time 1 : enable - voltage ramps up to target voltage with slope control | R/W | Option | |
| 4 | Buck4VRC_EN | Buck4 VRC 0 : disable - voltage ramps up to target voltage with one time 1 : enable - voltage ramps up to target voltage with slope control | R/W | Option | |
| [3:0] | Reserved | | R/W | 0000 | |
| Address | 06 | BUCK Mode | | | |
| Bit | Name | Description | R/W | Reset Value | |
| 7 | Buck1mode | Buck1 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | 1 | |
| 6 | Buck2mode | Buck2 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | 1 | |
| 5 | Buck3mode | Buck3 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | 1 | |

| | | | | |
|---------|--------------|---|-----|-------------|
| 4 | Buck4mode | Buck4 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | 1 |
| 3 | Buck1oms | Buck1 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 2 | Buck2oms | Buck2 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 1 | Buck3oms | Buck3 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 0 | Buck4oms | Buck4 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| Address | 07 | LDOcontrol1 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO1OUT[6:0] | LDO1 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 0101000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 08 | LDOcontrol2 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO2OUT[6:0] | LDO2 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 0101000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 09 | LDOcontrol3 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO3OUT[6:0] | LDO3 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 0101000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |

| Address | 0A | LDOcontrol4 | | |
|---------|--------------|---|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO4OUT[6:0] | LDO4 output voltage regulation 0000000 : 3 V, 25mV per step 0000001 : 3.025V ... 0011000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0B | LDOcontrol5 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO5OUT[6:0] | LDO5 output voltage regulation 0000000 : 3V, 25mV per step 0000001 : 3.025V ... 0011000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0C | LDOcontrol6 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO6OUT[6:0] | LDO6 output voltage regulation 0000000 : 3.0V, 25mV per step 0000001 : 3.025V ... 0011000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0D | LDOcontrol7 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO7UT[6:0] | LDO7 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 0101000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |

| Address | 0E | LDOcontrol8 | | |
|---------|---------------|---|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO8T[6:0] | LDO8 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 0101000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0F | LDOs off mode state | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | LDO8oms | LDO8 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 6 | LDO7oms | LDO7 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 5 | LDO6oms | LDO6 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 4 | LDO5oms | LDO5 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 3 | LDO4oms | LDO4 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 2 | LDO3oms | LDO3 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 1 | LDO2oms | LDO2 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| 0 | LDO1ms | LDO1 output off mode state 0 : floating 1 : Ground-discharged | R/W | 1 |
| Address | 10 | REBOOT/PWRHOLD delay time control | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:6] | Delayed2[1:0] | Delayed2 setting (00 : 100ms/01 : 500ms/10 : 1s/11 : 2s) | R/W | Option |
| [5:4] | Delayed1[1:0] | Delayed1 setting (00 : 100ms/01 : 500ms/10 : 1s/11 : 2s) | R/W | Option |
| [3:2] | THOLD[1:0] | THOLD setting (00 : 100ms/01 : 500ms/10 : 1s/11 : 2s) | R/W | Option |
| 1 | Reserved | | R/W | 0 |
| 0 | DisTHOLD | Ignore THOLD Time. 0 : Keep PWRHOLD function. 1 : Ignore PWRHOLD function. | R/W | Option |

| Address | 11 | | ON Event Setting | | |
|---------|--------------|--|----------------------|-------------|--|
| Bit | Name | Description | R/W | Reset Value | |
| [7:5] | On_Event | Powered on because of 000 : PWRON key-pressed 001 : VIN plugged in 010 : from REBOOT pin event 111 : No event happen | R | 111 | |
| [4:0] | Reserved | | R/W | 0 | |
| Address | 12 | | VIN UVLO/Buck On/Off | | |
| Bit | Name | Description | R/W | Reset Value | |
| [7:5] | VOFF setting | VIN UVLO 2.8V to 3.5V per 0.1V to power off PMIC 000 : 2.8V 001 : 2.9V 010 : 3V 011 : 3.1V (Default) 100 : 3.2V 101 : 3.3V 110 : 3.4V 111 : 3.5V | R/W | Option | |
| 4 | Reserved | | R/W | 0 | |
| 3 | Buck4 | Buck4 control (0 : Disable Buck4/1 : Enable Buck4) | R/W | Option | |
| 2 | Buck3 | Buck3 control (0 : Disable Buck3/1 : Enable Buck3) | R/W | Option | |
| 1 | Buck2 | Buck2 control (0 : Disable Buck2/1 : Enable Buck2) | R/W | Option | |
| 0 | Buck1 | Buck1 control (0 : Disable Buck1/1 : Enable Buck1) | R/W | Option | |
| Address | 13 | | LDOs On/Off | | |
| Bit | Name | Description | R/W | Reset Value | |
| 7 | LDO8 | LDO8 control (0 : Disable LDO8 / 1 : Enable LDO8) | R/W | Option | |
| 6 | LDO7 | LDO7 control (0 : Disable LDO7 / 1 : Enable LDO7) | R/W | Option | |
| 5 | LDO6 | LDO6 control (0 : Disable LDO6 / 1 : Enable LDO6) | R/W | Option | |
| 4 | LDO5 | LDO5 control (0 : Disable LDO5 / 1 : Enable LDO5) | R/W | Option | |
| 3 | LDO4 | LDO4 control (0 : Disable LDO4 / 1 : Enable LDO4) | R/W | Option | |
| 2 | LDO3 | LDO3 control (0 : Disable LDO3 / 1 : Enable LDO3) | R/W | Option | |
| 1 | LDO2 | LDO2 control (0 : Disable LDO2 / 1 : Enable LDO2) | R/W | Option | |
| 0 | LDO1 | LDO1 control (0 : Disable LDO1 / 1 : Enable LDO1) | R/W | Option | |

| Address | 14 | PWRON(Power On Key) time Parameters Setting / RESET delay | | |
|---------|--------------|---|------------|-------------|
| Bit | Name | Description | R/W | Reset Value |
| [7:6] | START_TIME | Startup time setting 00 : 100us (pressing time - low level) 01 : 100ms 10 : 1s 11 : 2s | R/W | Option |
| [5:4] | L_PRESS_TIME | Long-press time setting (after Power-On, 00 : 1s (falling edge to rising edge) 01 : 1.5s 10 : 2s 11 : 2.5s Sending short/long-press IRQ to CPU ex :1.5s => low time < 1.5s (short IRQ) => low time > 1.5s but < 6s(shutdown time) (long IRQ) => low time > 6s(shutdown time) (shutdown) | R/W | Option |
| [3:2] | SHDN_PRESS | Key-press forced shutdown time setting 00 : 4s (pressing time : low level) 01 : 6s 10 : 8s 11 : 10s | R/W | Option |
| [1:0] | RESET_DLY | RESET signal delay after the last power startup is done 00 : 10ms 01 : 50ms 10 : 100ms 11 : 200ms | R/W | Option |
| Address | 15 | SHDN Control | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | SHDN_CTRL | Power Off setting by CPU, after set, 100ms delayed power off 0 : Normal operation 1 : Disable the PMIC output | R/W | Option |
| 6 | SHDN_TIMING | Disable Buck/LDO only for normal power off (SHDN_CTRL=1) 0 : disable at the same time 1 : contrary to the startup timing (first_on-last_off) | R/W | Option |
| [5:4] | SHDN_DLYTIME | Delayed shutdown time after send the (PWRON)key-press-forced-shutdown IRQ (when IRQ is disable, there is no delay) 00 : 100ms 01 : 500ms 10 : 1s 11 : 2s | R/W | Option |
| [3:0] | Reserved | | R/W | 0000 |

| Address | 16 | Powered off conditions enable setting | | |
|---------|---------------|--|------------|-------------|
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | BCK1LV_ENSHDN | Buck1 output voltage low SHDN 0 : disable this event. 1 : enable this event | R/W | 0 |
| 6 | BCK2LV_ENSHDN | Buck2 output voltage low SHDN 0 : disable this event. 1 : enable this event | R/W | 0 |
| 5 | BCK3LV_ENSHDN | Buck3 output voltage low SHDN 0 : disable this event. 1 : enable this event | R/W | 0 |
| 4 | BCK4LV_ENSHDN | Buck4 output voltage low SHDN 0 : disable this event. 1 : enable this event | R/W | 0 |
| 3 | PWRON_ENSHDN | PWRON key-pressed forced SHDN 0 : disable this event. 1 : enable this event | R/W | 1 |
| 2 | OT_ENSHDN | Over temperature SHDN 0 : disable this event. 1 : enable this event | R/W | 1 |
| 1 | VINLV_ENSHDN | VIN voltage low (VOFF) (Set by reg) SHDN 0 : disable this event. 1 : enable this event | R/W | 0 |
| 0 | Reserved | | R/W | 0 |
| Address | 17 | OFF Event (Only reset by POR) | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:4] | OFF_Event | Powered off because of (Only shows last power-off event) 0000 : VIN voltage low (VOFF) (Set by reg) 0001 : Buck1 output voltage low 0010 : Buck2 output voltage low 0011 : Buck3 output voltage low 0100 : PWRON key-pressed forced shutdown 0101 : Power Off register setting 0110 : Over temperature event 0111 : Reboot restart. 1000 : Buck4 output voltage low 1001 : PWR_HOLD fail. 1010 : No event happen. 1111 : No event happen | R | 1111 |
| [3:0] | Reserved | | R | 0000 |
| Address | 18 to 27 | 16 bytes registers Data Cache (Only reset by POR) | | |
| | | | R/W | 0 |

| IRQ_PMIC (Power Channels) | | | | |
|---------------------------|-------------|---|------------|-------------|
| Address | 28 | IRQ Enable1 | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | OT_IRQ | Internal over-temperature was triggered, IRQ enable | R/W | 1 |
| 6 | Bck1LV_IRQ | Buck1 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 5 | Bck2LV_IRQ | Buck2 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 4 | Bck3LV_IRQ | Buck3 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 3 | Bck4LV_IRQ | Buck4 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 2 | PWRONSP_IRQ | PWRON short press, IRQ enable (32μs deglitch time) | R/W | 0 |
| 1 | PWRONLP_IRQ | PWRON long press, IRQ enable (32μs deglitch time) | R/W | 0 |
| 0 | SYSLV_IRQ | VIN voltage is lower than V _{OFF} , IRQ enable | R/W | 0 |
| Address | 29 | IRQ Status1 | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | OT | Internal over-temperature | R | 0 |
| 6 | Bck1LV | Buck1 output voltage equal 66% x V _{Target} | R | 0 |
| 5 | Bck2LV | Buck2 output voltage equal 66% x V _{Target} | R | 0 |
| 4 | Bck3LV | Buck3 output voltage equal 66% x V _{Target} | R | 0 |
| 3 | Bck4LV | Buck4 output voltage equal 66% x V _{Target} | R | 0 |
| 2 | PWRONSP | PWRON short press (32μs deglitch time) | R | 0 |
| 1 | PWRONLP | PWRON long press (32μs deglitch time) | R | 0 |
| 0 | VINLV | VIN voltage is lower than V _{OFF} | R | 0 |
| Address | 2A | IRQ Enable2 | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | KPSHDN_IRQ | Key-press forced shutdown, IRQ enable | R/W | 1 |
| 6 | PWRONR_IRQ | PWRON press rising edge, IRQ enable | R/W | 0 |
| 5 | PWRONF_IRQ | PWRON press falling edge, IRQ enable | R/W | 0 |
| [4:0] | Reserved | | R | 0000 |
| Address | 2B | IRQ Status2 | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | KPSHDN | Key-press forced shutdown | R | 0 |
| 6 | PWRONR | PWRON press rising edge | R | 0 |
| 5 | PWRONF | PWRON press falling edge | R | 0 |
| [4:2] | Reserved | | R | 000 |
| 1 | OTW125 | Internal 125°C pre-warning over-temperature. | R | 0 |
| 0 | OTW100 | Internal 100°C pre-warning over-temperature. | R | 0 |

| Address | 2C | | PMU On/Off Sequence1 | | |
|---------|----------------|--|----------------------|------------|-------------|
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | | Read/Write | Reset Value |
| [7:4] | Buck2_Seq[3:0] | Setting Buck2 on/off sequence priority | | R/W | Option |
| [3:0] | Buck1_Seq[3:0] | Setting Buck1 on/off sequence priority | | R/W | Option |
| Address | 2D | | PMU On/Off Sequence2 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | | Read/Write | Reset Value |
| [7:4] | Buck4_Seq[3:0] | Setting Buck4 on/off sequence priority | | R/W | Option |
| [3:0] | Buck3_Seq[3:0] | Setting Buck3 on/off sequence priority | | R/W | Option |
| Address | 2E | | PMU On/Off Sequence3 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | | Read/Write | Reset Value |
| [7:4] | LDO2_Seq[3:0] | Setting LDO2 on/off sequence priority | | R/W | Option |
| [3:0] | LDO1_Seq[3:0] | Setting LDO1 on/off sequence priority | | R/W | Option |
| Address | 2F | | PMU On/Off Sequence4 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | | Read/Write | Reset Value |
| [7:4] | LDO4_Seq[3:0] | Setting LDO4 on/off sequence priority | | R/W | Option |
| [3:0] | LDO3_Seq[3:0] | Setting LDO3 on/off sequence priority | | R/W | Option |
| Address | 30 | | PMU On/Off Sequence5 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | | Read/Write | Reset Value |
| [7:4] | LDO6_Seq[3:0] | Setting LDO6 on/off sequence priority | | R/W | Option |
| [3:0] | LDO5_Seq[3:0] | Setting LDO5 on/off sequence priority | | R/W | Option |
| Address | 31 | | PMU On/Off Sequence5 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | | Read/Write | Reset Value |
| [7:4] | LDO8_Seq[3:0] | Setting LDO8 on/off sequence priority | | R/W | Option |
| [3:0] | LDO7_Seq[3:0] | Setting LDO7 on/off sequence priority | | R/W | Option |
| Address | 32 | | Soft-Start Control | | |
| Bit | Name | Description | | Read/Write | Reset Value |
| [7:6] | Reserved | | | R | Option |

| | | | | |
|---------|---|---|------------|-------------|
| [5:2] | Soft-Start End Control @ MASK_GPIO = 0 (External Enable pin define) | 0000 : First turn on channel decide the RESET_DLY time. 0001 : Buck1 decide the RESET_DLY time. 0100 : Buck1 decide the RESET_DLY time. 0101 : LDO1 decide the RESET_DLY time. 1100 : LDO8 decide the RESET_DLY time. 1111 : LDO8 decide the RESET_DLY time. | R/W | Option |
| [1:0] | Soft-Start Voltage level / time soft-start control. | Voltage Level 00 : When output voltage arrives to 80% V _{Target} , next channel will turn on. Soft-start time interval (TSS) : 01 : 1ms 10 : 4ms 11 : 8ms | R/W | Option |
| Address | 33 | Buck Syn-Clock Control | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:6] | VCO_VRC | VCO input voltage slop. 00: 25mV/10μs, 01: 25mV/20μs 10: 25mV/40μs, 11: 25mV/80μs Note : The VCO's voltage input range is 0.375V to 1.8V and the output frequency is 450kHz to 2MHz. | R/W | Option |
| [5:0] | VCO_DVS | VCO input voltage DVS control 000000 : 0.375V (450kHz) 111001 : 1.8V (2MHz) 111111 : 1.8V (2MHz) | R/W | Option |
| Address | 34 | Buck Syn-Clock Spread Spectrum Control | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:1] | Reserved | | R/W | 0000000 |
| 0 | SSOSC | Buck Clock Spread Spectrum Control 0 : Disable spread spectrum function. 1 : Turn on spread spectrum function. | R/W | Option |
| Address | 3A | EEPROM (MTP) Control | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:6] | Reserved | | R/W | 00 |
| 5 | MTP Page 2 Read | Read MTP Page 2 | R | 0 |
| 4 | MTP Page 1 Read | Read MTP Page 1 | R | 0 |
| [3:2] | Reserved | | R/W | 00 |
| 1 | MTP Page 2 write | Write MTP Page 2, and MTP also needs to be logic high. | W | 0 |
| 0 | MTP Page 1 write | Write MTP Page 1, and MTP also needs to be logic high. | W | 0 |

Table 3. I²C to MTP Mapping Table
MTP Page-1

| MTP Address | I ² C Register Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|-------------|-----------------------------------|-----------------|------------------|--------------|--------------|--------------|----------|----------|----------|----------|
| 0X00 | 0X01 | Function | BUCKcontrol1 | | | | | | | |
| | | Meaning | Buck1Output[5:0] | | | | | | Buck1VRC | |
| | | Default | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | B | B |
| 0X01 | 0X02 | Function | BUCKcontrol2 | | | | | | | |
| | | Meaning | Buck2Output[5:0] | | | | | | Buck2VRC | |
| | | Default | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | B | B |
| 0X02 | 0X03 | Function | BUCKcontrol3 | | | | | | | |
| | | Meaning | Buck3Output[5:0] | | | | | | Buck3VRC | |
| | | Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | B | B |
| 0X03 | 0X04 | Function | BUCKcontrol4 | | | | | | | |
| | | Meaning | Buck4Output[5:0] | | | | | | Buck4VRC | |
| | | Default | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | B | B |
| 0X0D | 0X05 | Function | VRC Control | | | | | | | |
| | | Meaning | Buck1V RC_EN | Buck2V RC_EN | Buck3V RC_EN | Buck4V RC_EN | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |
| 0X04 | 0X07 | Function | LDOcontrol1 | | | | | | | |
| | | Meaning | Reserved | LDO1OUT[6:0] | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |

| MTP Address | I ² C Register Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|-------------|-----------------------------------|-----------------|-------------|--------------|------|------|------|------|------|-----|
| 0X05 | 0X08 | Function | LDOcontrol2 | | | | | | | |
| | | Meaning | Reserved | LDO2OUT[6:0] | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |
| 0X06 | 0X09 | Function | LDOcontrol3 | | | | | | | |
| | | Meaning | Reserved | LDO3OUT[6:0] | | | | | | |
| | | Default | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |
| 0x07 | 0x0A | Function | LDOcontrol4 | | | | | | | |
| | | Meaning | Reserved | LDO4OUT[6:0] | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |
| 0x08 | 0x0B | Function | LDOcontrol5 | | | | | | | |
| | | Meaning | Reserved | LDO5OUT[6:0] | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |
| 0x09 | 0x0C | Function | LDOcontrol6 | | | | | | | |
| | | Meaning | Reserved | LDO6OUT[6:0] | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |
| 0x0A | 0x0D | Function | LDOcontrol7 | | | | | | | |
| | | Meaning | Reserved | LDO7OUT[6:0] | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |
| 0x0B | 0x0E | Function | LDOcontrol8 | | | | | | | |
| | | Meaning | Reserved | LDO8OUT[6:0] | | | | | | |
| | | Default | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | A | A | A | A | A | A | A |

| MTP Address | I ² C Register Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|-------------|-----------------------------------|-----------------|--|----------|----------|----------|----------|----------|----------|----------|
| 0x0C | 0x12 | Function | VIN UVLO (update default value after power on) | | | | | | | |
| | | Meaning | VOFF setting | | | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | B | B | B | B | B |
| 0x0F | No mapping | Function | x | | | | | | | |
| | | Meaning | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |

MTP Page-2

| MTP Address | I ² C Register Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|-------------|-----------------------------------|-----------------|---|-------------|---------------|------|----------------|----------|-----------|----------|
| 0x00 | 0x10 | Function | REBOOT/PWRHOLD delay time control | | | | | | | |
| | | Meaning | Delayed2[1:0] | | Delayed1[1:0] | | THOLD | | Reserved | DisTHOLD |
| | | Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |
| 0x01 | 0x14 | Function | PWRON time Parameters Setting / RESET delay | | | | | | | |
| | | Meaning | START_TIME | | L_PRESS_TIME | | SHDN_PRESS | | RESET_DLY | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | A | A |
| 0x02 | 0x15 | Function | SHDN Control | | | | | | | |
| | | Meaning | SHDN_CTRL | SHDN_TIMING | SHDN_DLYTIME | | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |
| 0x03 | 0x2C | Function | PMU On/Off Sequence1 | | | | | | | |
| | | Meaning | Buck2_Seq[3:0] | | | | Buck1_Seq[3:0] | | | |
| | | Default | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | A | A |
| 0x04 | 0x2D | Function | PMU On/Off Sequence2 | | | | | | | |
| | | Meaning | Buck4_Seq[3:0] | | | | Buck3_Seq[3:0] | | | |
| | | Default | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | A | A |
| 0x05 | 0x2E | Function | PMU On/Off Sequence3 | | | | | | | |
| | | Meaning | LDO2_Seq[3:0] | | | | LDO1_Seq[3:0] | | | |
| | | Default | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | A | A |

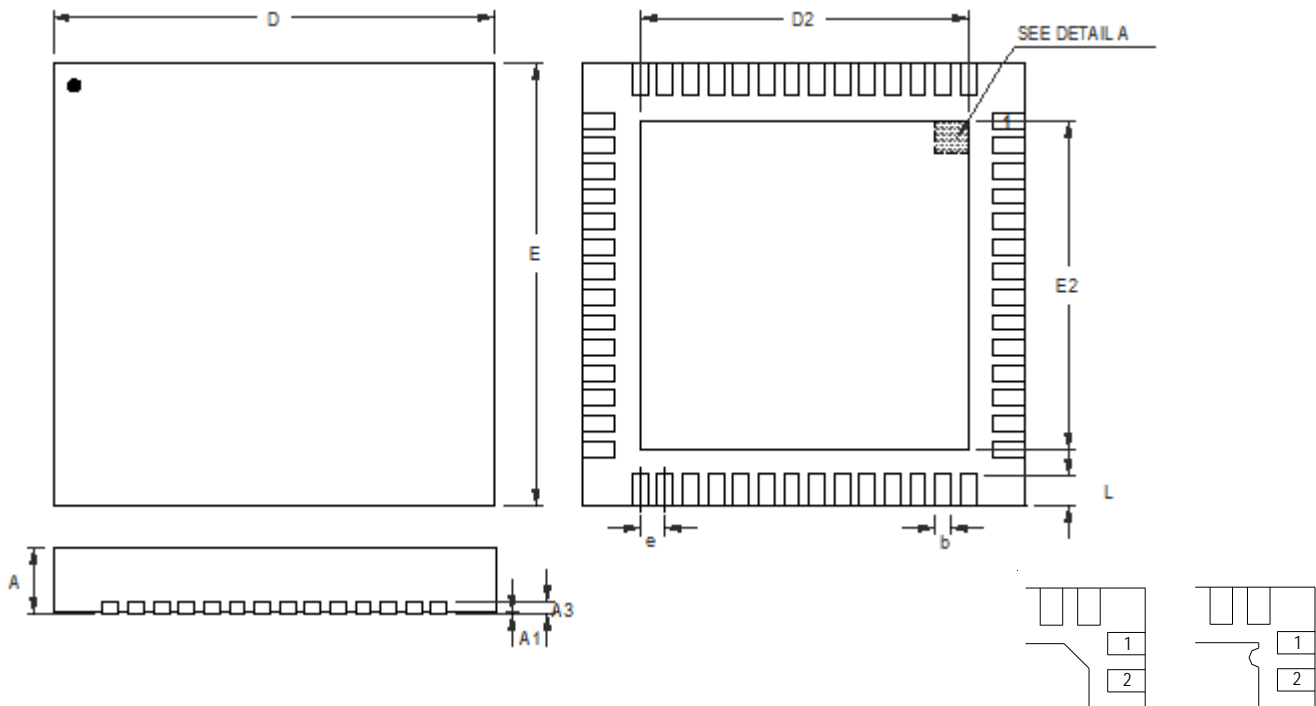
| MTP Address | I ² C Register Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|-------------|-----------------------------------|-----------------|--|----------|------------------------------------|----------|---------------|----------|--------------------|----------|
| 0x06 | 0x2F | Function | PMU On/Off Sequence4 | | | | | | | |
| | | Meaning | LDO4_Seq[3:0] | | | | LDO3_Seq[3:0] | | | |
| | | Default | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | A | A |
| 0x07 | 0x30 | Function | PMU On/Off Sequence5 | | | | | | | |
| | | Meaning | LDO6_Seq[3:0] | | | | LDO5_Seq[3:0] | | | |
| | | Default | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | A | A |
| 0x08 | 0x31 | Function | PMU On/Off Sequence6 | | | | | | | |
| | | Meaning | LDO8_Seq[3:0] | | | | LDO7_Seq[3:0] | | | |
| | | Default | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | A | A | A | A | A | A | A | A |
| 0x09 | 0x32 | Function | Soft-Start Control | | | | | | | |
| | | Meaning | Reversed | Reversed | Soft-Start End Select @MASK_GPIO=1 | | | | Soft-Start Control | |
| | | Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | A | A | A | A | B | B |
| 0x0A | 0x33 | Function | Buck Syn-Clock Control | | | | | | | |
| | | Meaning | VCO_VRC | | | | VCO_DVS | | | |
| | | Default | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | A | A | A | A | A | A |
| 0x0B | 0x34 | Function | Buck Syn-Clock Spread Spectrum Control | | | | | | | |
| | | Meaning | Reversed | Reversed | Reversed | Reversed | Reversed | Reversed | Reversed | SSOSC |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |
| 0x0C | No mapping | Function | x | | | | | | | |
| | | Meaning | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |

| MTP Address | I ² C Register Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|-------------|-----------------------------------|-----------------|----------|----------|----------|----------|----------|----------|----------|----------|
| 0x0D | No mapping | Function | x | | | | | | | |
| | | Meaning | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |
| 0x0E | No mapping | Function | x | | | | | | | |
| | | Meaning | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |
| 0x0F | No mapping | Function | x | | | | | | | |
| | | Meaning | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | | Reset Condition | B | B | B | B | B | B | B | B |

Reset Condition

| | |
|---|--|
| A | Reset by MTP (Register 0x12 VOFF Setting). |
| B | Reset when VIN < 1.7V. |

Outline Dimension



DETAIL A

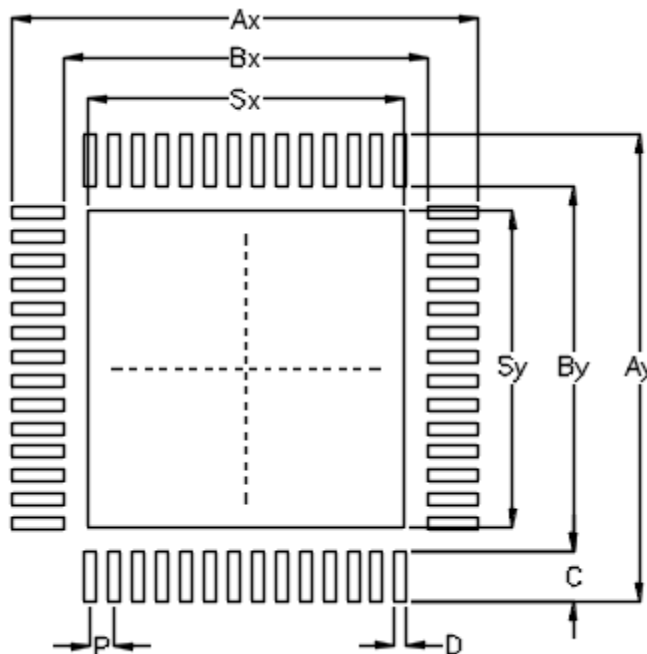
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 6.900 | 7.100 | 0.272 | 0.280 |
| D2 | 5.150 | 5.250 | 0.203 | 0.207 |
| E | 6.900 | 7.100 | 0.272 | 0.280 |
| E2 | 5.150 | 5.250 | 0.203 | 0.207 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 56L QFN 7x7 Package

Footprint Information



| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | Tolerance |
|------------------|---------------|--------------------------|------|------|------|------|------|------|------|------|-----------|
| | | P | Ax | Ay | Bx | By | C | D | Sx | Sy | |
| V/W/U/XQFN7*7-56 | 56 | 0.40 | 7.80 | 7.80 | 6.10 | 6.10 | 0.85 | 0.20 | 5.30 | 5.30 | ±0.05 |

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