Multi-Output Integrated Chip (MOIC) for Intel Braswell Platform

General Description

RT5041AB integrates 2 buck converters, 3 LDOs and 2 power switches in one package. This MOIC is designed for Braswell M/D SOC. Braswell M/D SOC controls the power sequence by simple I/O. RT5041AB has UVLO, OVP, UVP, OTP and current limit protections. RT5041AB is available in WQFN-28L 4x4 package.

Ordering Information

RT5041AB□□

- Package Type
  QW : WQFN-28L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

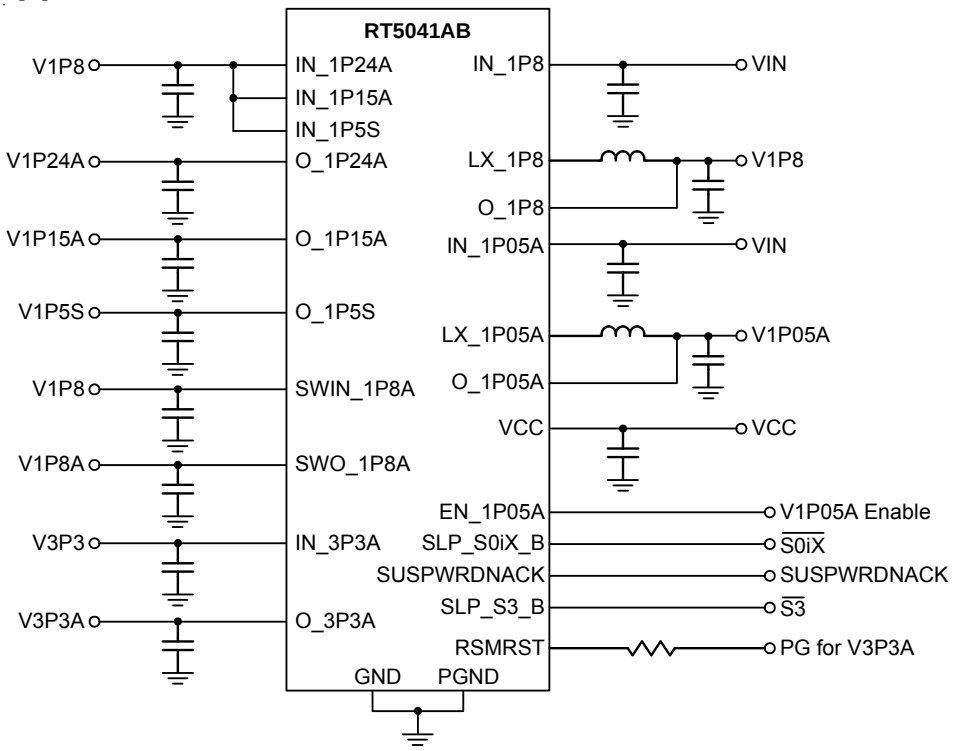
Features

- **2 Channels Low Power Consumption Step-Down DC/DC Converters**
- **Low On-Resistance for DC/DC Converters**
  - **50mΩ of High Side MOSFET**
  - **45mΩ of Low Side MOSFET**
- **3 Channels LDO Voltage Regulators**
- **2 Channels Switches**
- **Input Voltage Range : 2.7V to 5.5V**
- **Internal Soft-Start and Soft-Discharge**
- **Cycle-by-Cycle Current Limit and UVP**
- **Thermal Shutdown**

Applications

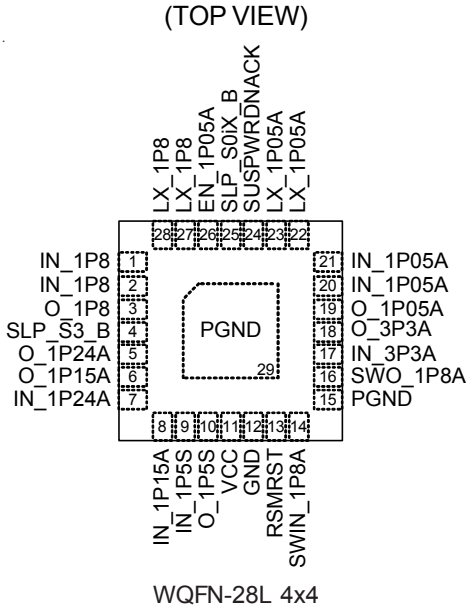
- Ultra book and Tablet Computers

Simplified Application Circuit



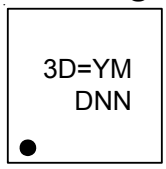
Pin Configurations

(TOP VIEW)



WQFN-28L 4x4

Marking Information



3D= : Product Code

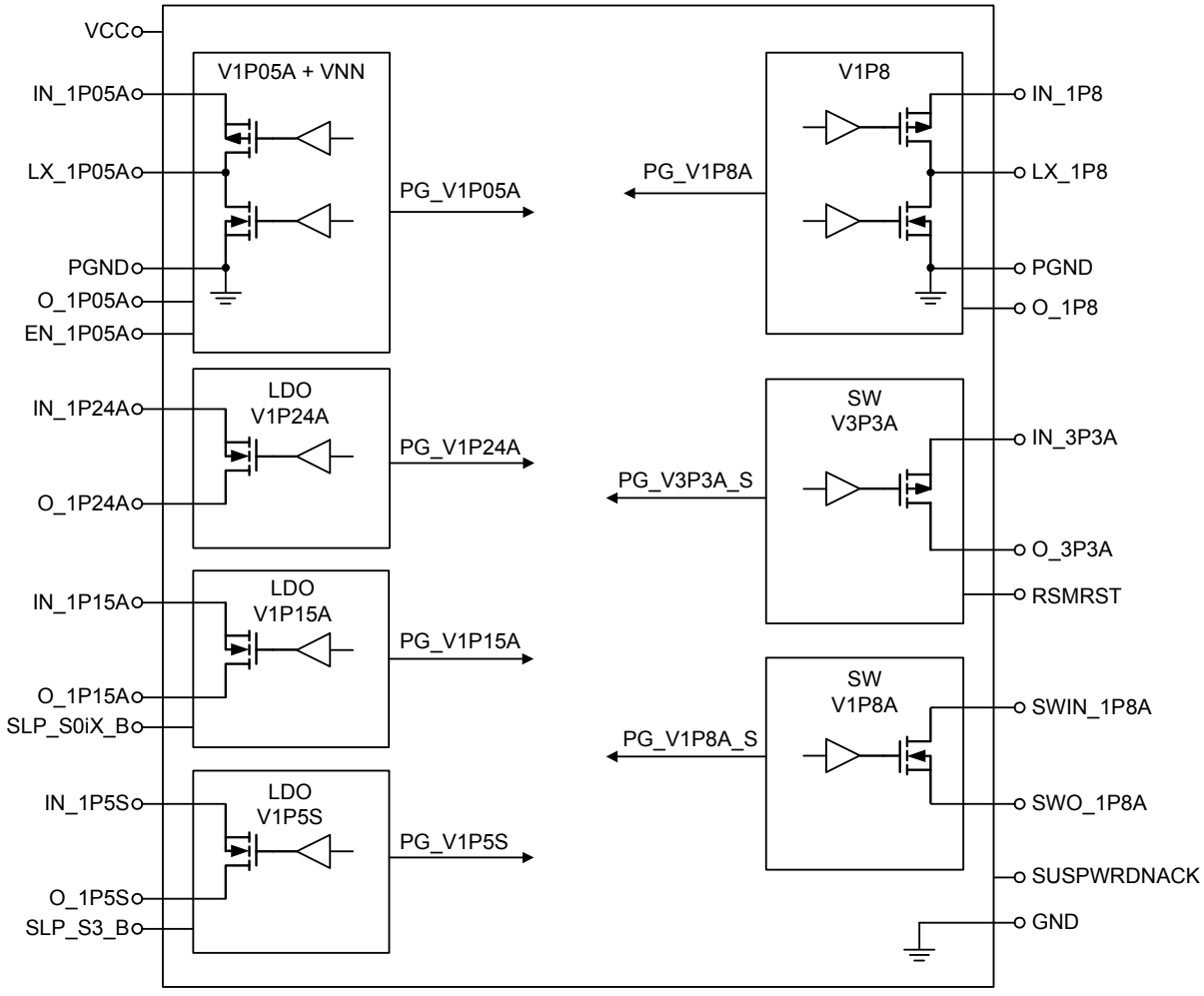
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	IN_1P8	Input Voltage for V1P8 Buck Converter.
3	O_1P8	Output Voltage Feedback of V1P8 Buck Converter.
4	SLP_S3_B	Enable Signal for V1P5S LDO.
5	O_1P24A	LDO Output for V1P24A.
6	O_1P15A	LDO Output for V1P15A.
7	IN_1P24A	LDO Input for V1P24A.
8	IN_1P15A	LDO Input for V1P15A.
9	IN_1P5S	LDO Input for V1P5S.
10	O_1P5S	LDO Output for V1P5S.
11	VCC	Analog Power for Internal Circuit.
12	GND	Analog Ground.
13	RSMRST	Power Good Signal for V3P3A Switch.
14	SWIN_1P8A	Switch Input for V1P8A.
15, 29 (Exposed Pad)	PGND	Power Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
16	SWO_1P8A	Switch Output for V1P8A.
17	IN_3P3A	Switch Input for V3P3A.
18	O_3P3A	Switch Output for V3P3A.
19	O_1P05A	Output Voltage Feedback for V1P05A Buck Converter.
20, 21	IN_1P05A	Input Voltage for V1P05A Buck Converter.
22, 23	LX_1P05A	Phase Node for V1P05A Buck Converter.
24	SUSPWRDNACK	Disable Signal for All Power Rails.

Pin No.	Pin Name	Pin Function
25	SLP_S0iX_B	Input Pin. LDO_V1P15A will recognize this first rising edge during power up sequence to achieve SLP_S0iX_B function. When SLP_S0iX_B = High, LDO_V1P15A_VOUT = 1.15V. When SLP_S0iX_B = Low, LDO_V1P15A_VOUT = 0.75V.
26	EN_1P05A	Enable Signal for RT5041AB. Start to power up all voltage rails with a sequence.
27, 28	LX_1P8	Phase Node for V1P8 Buck Converter.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, IN_1P8, IN_1P05A, IN_3P3A ---------- –0.3V to 6V
- Supply Input Voltage, IN_1P24A, IN_1P15A, IN_V1P5S, IN_V1P8A ---------- –0.3V to 6V
- Supply Voltage, VCC ---------- –0.3V to 6V
- Switch Node Voltage, LX_V1P05A, LX_V1P8 ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-28L 4x4 ---------- 3.5W
- Package Thermal Resistance (Note 2)
  WQFN-28L 4x4, θ_{JA} ---------- 28.5°C/W
  WQFN-28L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
- HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, IN_1P05A, IN_1P8 ---------- 2.7V to 5.5V
- Supply Input Voltage, IN_1P24A, IN_1P15A, IN_1P5S ---------- 1.8V to 2V
- Supply Input Voltage, IN_3P3A ---------- 3.3V to (V_{CC} – 2)V
- Supply Input Voltage, SWIN_1P8A ---------- 1.8V to (V_{CC} – 2)V
- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, No load, for every voltage rails unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MOIC						
Supply Voltage	V_{CC}		4.5	--	5.5	V
Shutdown Current	I_{SHDN}	V_{EN_1P05A} = 0V	--	--	5	μA
UVLO Threshold	V_{UVLO}		--	--	4	V
UVLO Hysteresis	V_{UVLO_HYS}		--	150	--	mV
Enable Input High Voltage	V_{EN_H}	Measured V_{EN_1P05A}, $V_{SUSPWRDNACK}$, $V_{SLP\_S3\_B}$, $V_{SLP\_S0iX\_B}$	1	--	V_{CC}	V
Enable Input Low Voltage	V_{EN_L}	Measured V_{EN_1P05A}, $V_{SUSPWRDNACK}$, $V_{SLP\_S3\_B}$, $V_{SLP\_S0iX\_B}$	--	--	0.4	V
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	T_{SD_HYS}		--	25	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CONVERTER_V1P8 (4.1A)						
Supply Voltage	V_{IN}		2.7	--	5.5	V
Supply Quiescent Current	I_Q	Enabled, no switching.	0	20	55	μA
Output Voltage	V_{OUT}	CCM	1.799	1.818	1.836	V
Soft-Start Time	T_{SS}	10% to 90% V_{OUT}	0.58	0.9	1.35	ms
Switch On Resistance	$R_{DS(ON),H}$	V_{IN} = 5V	30	50	85	mΩ
Switch On Resistance	$R_{DS(ON),L}$	V_{IN} = 5V	30	45	75	mΩ
Current Limit	I_{OC}	Inductor valley current	4.7	6	8.8	A
Switching Frequency	f_{SW}		1	1.2	1.4	MHz
Minimum Off Time	T_{OFF}		--	120	--	ns
OVP Trip Threshold	V_{OVP}	OVP detected	115	120	125	%
OVP Deglitch Time (Note 5)	T_{OVD}		--	5	--	μs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Deglitch Time (Note 5)	T_{UVD}		--	5	--	μs
Discharge Resistance	R_{DIS}	EN = Low, V_{TEST} = 1V	--	1	--	Ω
CONVERTER_V1P05A (4.6A)						
Supply Voltage	V_{IN}		2.7	--	5.5	V
Supply Quiescent Current	I_Q	Enabled, no switching.	0	20	55	μA
Output Voltage	V_{OUT}	CCM	1.039	1.05	1.06	V
Soft-Start Time	T_{SS}	10% to 90% V_{OUT}	0.58	0.9	1.35	ms
Switch On Resistance	$R_{DS(ON),H}$	V_{IN} = 5V	30	50	85	mΩ
Switch On Resistance	$R_{DS(ON),L}$	V_{IN} = 5V	30	45	75	mΩ
Current Limit	I_{OC}	Inductor valley current	5.2	6	8.8	A
Switching Frequency	f_{SW}		1	1.2	1.4	MHz
Minimum Off Time	T_{OFF}		--	120	--	ns
OVP Trip Threshold	V_{OVP}	OVP detected	115	120	125	%
OVP Deglitch Time (Note 5)	T_{OVD}		--	5	--	μs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Deglitch Time (Note 5)	T_{UVD}		--	5	--	μs
Discharge Resistance	R_{DIS}	EN = Low, V_{TEST} = 1V	--	1.8	--	Ω
LDO_V1P24A (1A)						
Supply Voltage	V_{IN}		1.6	--	2	V
Supply Current (Quiescent)	I_Q	Enabled	0	20	50	μA
Output Voltage	V_{OUT}	V_{IN} = 1.8V	1.227	1.24	1.252	V
Soft-Start Time	T_{SS}	10% to 90% V_{OUT}	0.33	0.5	0.67	ms
Dropout Voltage	V_{DROP}	I_{OUT} = 0.9A	20	200	300	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit	I_{OC}		1.1	1.5		A
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Deglitch Time (Note 5)	T_{UVD}		--	5	--	μs
Discharge Resistance	R_{DIS}	EN = Low, V_{TEST} = 1V	--	6	--	Ω
Power Supply Rejection Rate		I_{OUT} = 100mA, f = 100Hz	--	–60	--	dB
		I_{OUT} = 100mA, f = 10kHz	--	–30	--	
LDO_V1P15A (1A)						
Supply Voltage	V_{IN}		1.6	--	2	V
Supply Quiescent Current	I_Q	Enabled	0	20	50	μA
Output Voltage	V_{OUT}	V_{IN} = 1.8V, $V_{SLP\_S0iX\_B}$ = 1	1.138	1.15	1.161	V
		V_{IN} = 1.8V, $V_{SLP\_S0iX\_B}$ = 0	0.735	0.75	0.765	
Soft-Start Time	T_{SS}	10% to 90% V_{OUT}	0.33	0.5	0.67	ms
Slew Rate		Ramp up from 0.75V to 1.15V	--	42	--	V/ms
Dropout Voltage	V_{DROP}	I_{OUT} = 1A	20	400	500	mV
Current Limit	I_{OC}		1.1	1.5	2.05	A
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Deglitch Time (Note 5)	T_{UVD}		--	5	--	μs
Discharge Resistance	R_{DIS}	EN = Low, V_{TEST} = 1V	--	6	--	Ω
Power Supply Rejection Rate		I_{OUT} = 100mA, f = 100Hz	--	–60	--	dB
		I_{OUT} = 100mA, f = 10kHz	--	–30	--	
LDO_V1P5S (0.1A)						
Supply Voltage	V_{IN}		1.6	--	2	V
Supply Quiescent Current	I_Q	Enabled	0	20	50	μA
Output Voltage	V_{OUT}	V_{IN} = 1.8V	1.485	1.5	1.515	V
Soft-Start Time	T_{SS}	10% to 90% V_{OUT}	0.33	0.5	0.67	ms
Dropout Voltage	V_{DROP}	I_{OUT} = 100mA	5	20	100	mV
Current Limit	I_{OC}		0.15	0.2	0.55	A
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Deglitch Time (Note 5)	T_{UVD}		--	5	--	μs
Discharge Resistance	R_{DIS}	EN = Low, V_{TEST} = 1V	--	6	--	Ω
Power Supply Rejection Rate		I_{OUT} = 100mA, f = 100Hz	--	–60	--	dB
		I_{OUT} = 100mA, f = 10kHz	--	–30	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SW_V3P3A (450mA)						
Supply Voltage	V_{IN}		2.7	3.3	V_{CC} – 2	V
Supply Quiescent Current	I_Q	V_{EN_1P05A} = 2V	0	5	25	μA
On-state Resistance	$R_{DS(ON)}$	V_{IN} = 3.333V, I_{OUT} = 100mA	--	90	--	mΩ
Soft-Start Time	T_{SS}	10% to 90% V_{OUT}	40	300	510	μs
Dropout Voltage	V_{DROP}	I_{OUT} = 400mA	--	33	--	mV
Current Limit	I_{OC}		0.55	1	2.6	A
UVP Trip Threshold	V_{UVP}	UVP detected	--	60	--	%
UVP Deglitch Time (Note 5)	T_{UVD}		--	5	--	μs
Discharge Resistance	R_{DIS}	EN = Low, V_{TEST} = 1V	--	6	25	Ω
SW_V1P8A (1A)						
Supply Voltage	V_{IN}		1.6	1.8	V_{CC} – 2	V
Supply Current (Quiescent)	I_{QC}	V_{EN_1P05A} = 2V	0	5	25	μA
On-state Resistance	$R_{DS(ON)}$	V_{IN} = 1.818V, I_{OUT} = 100mA	--	60	--	mΩ
Soft-Start Time	T_{SS}	10% to 90% V_{OUT}	40	300	455	μs
Dropout Voltage	V_{DROP}	I_{OUT} = 300mA	--	18	--	mV
Current Limit	I_{OC}		1.1	1.4	2.6	A
UVP Trip Threshold	V_{UVP}	UVP detected	--	60	--	%
UVP Deglitch Time (Note 5)	T_{UVD}		--	5	--	μs
Discharge Resistance	R_{DIS}	EN = Low, V_{TEST} = 1V	--	6	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

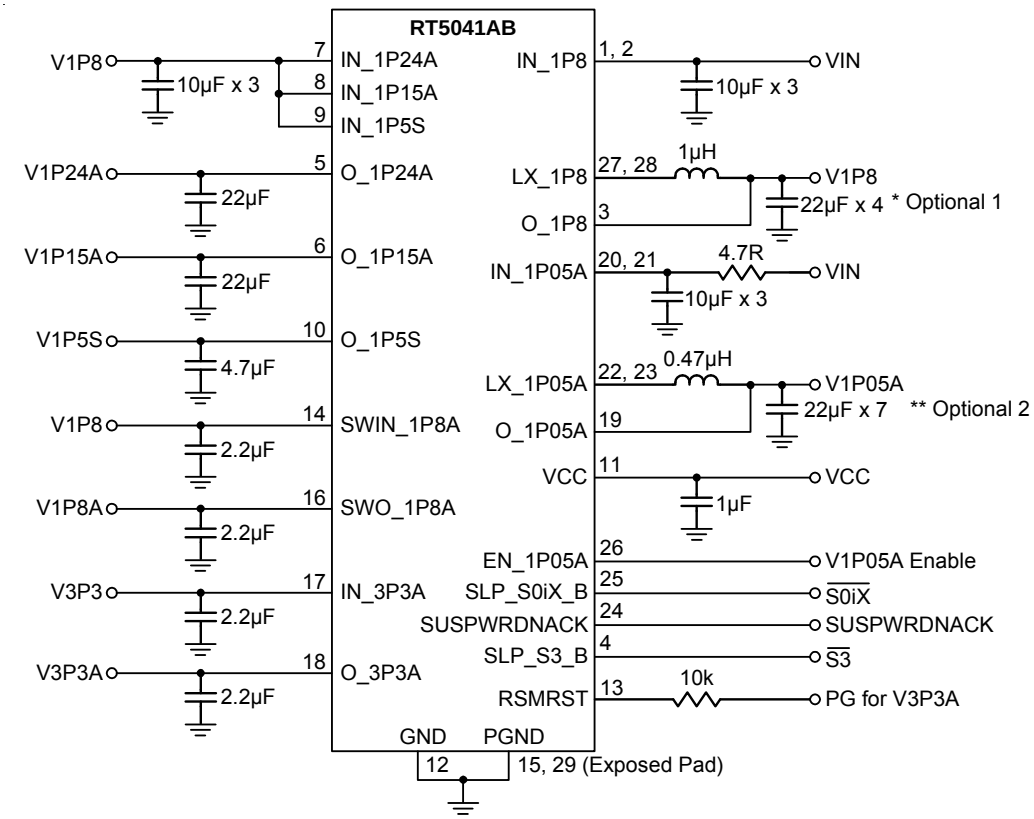
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

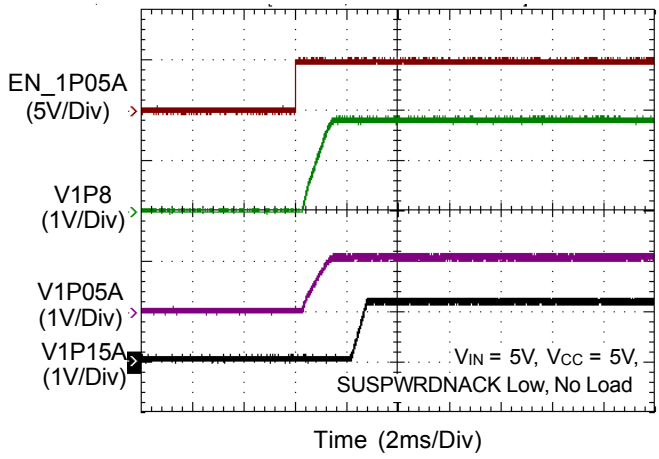
Typical Application Circuit



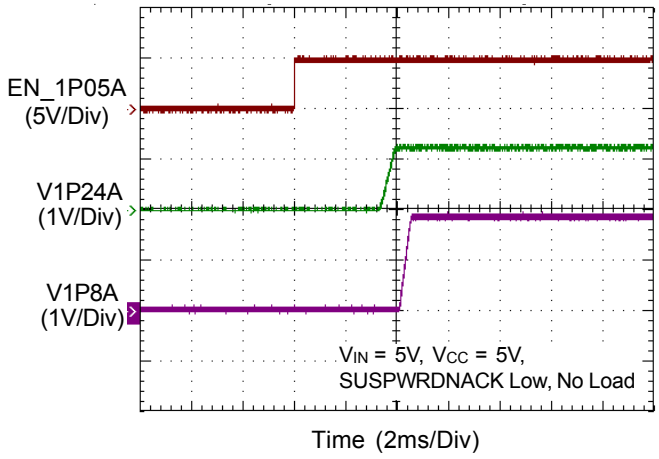
* For Intel transient test condition, Loading = 2.6A to 4.1A, SR = 1.5A/µs.
** For Intel transient test condition, Loading = 2.35A to 4.6A, SR = 2.25A/µs.

Typical Operating Characteristics

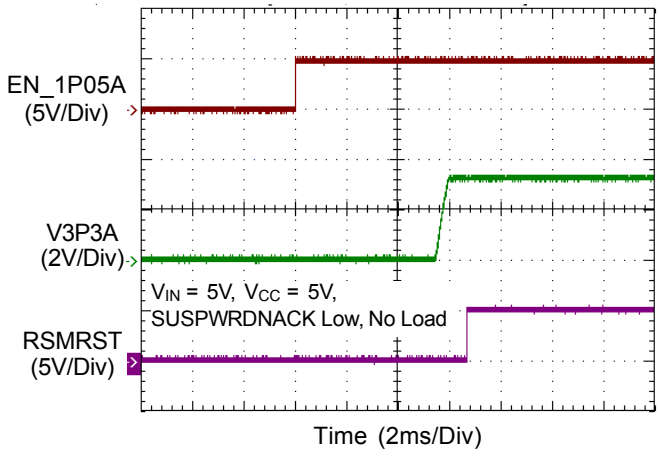
Power On from EN_1P05A



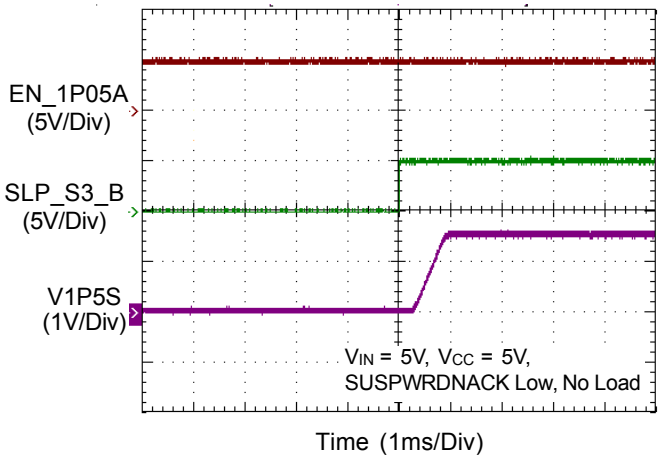
Power On from EN_1P05A



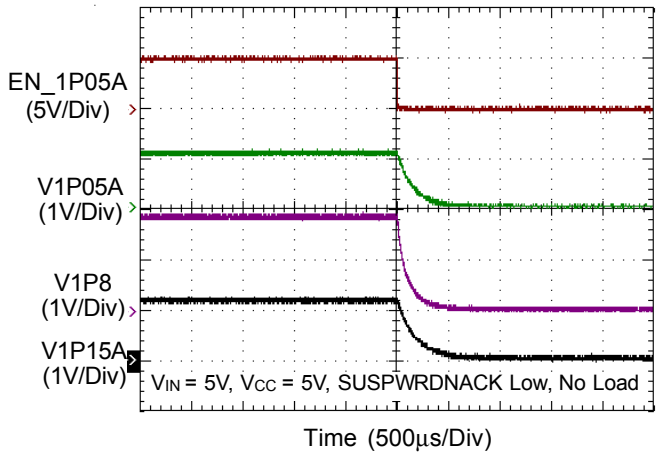
Power On from EN_1P05A



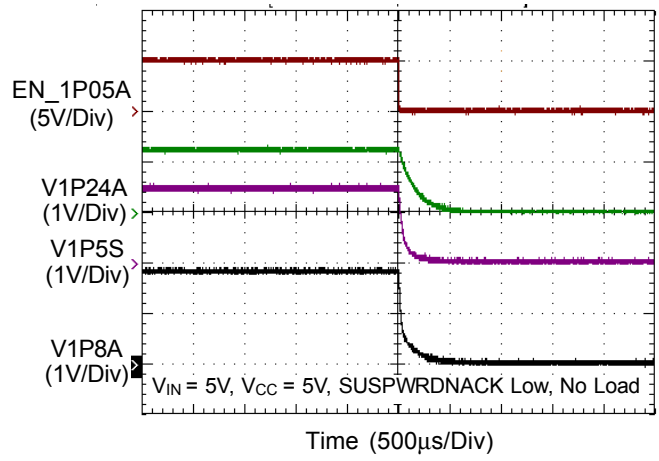
Power On from V1P5S



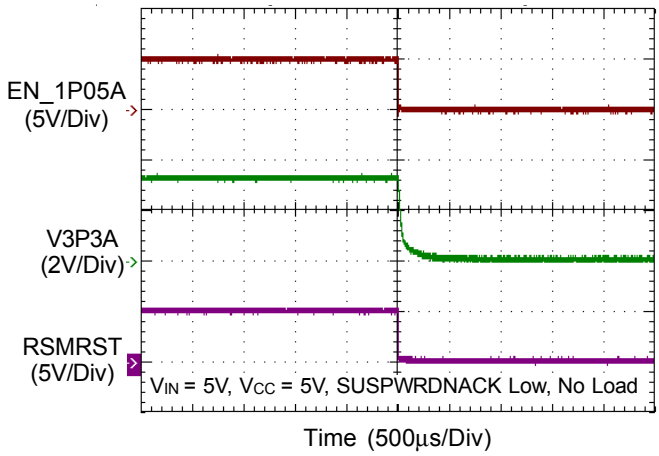
Power Off EN_1P05A



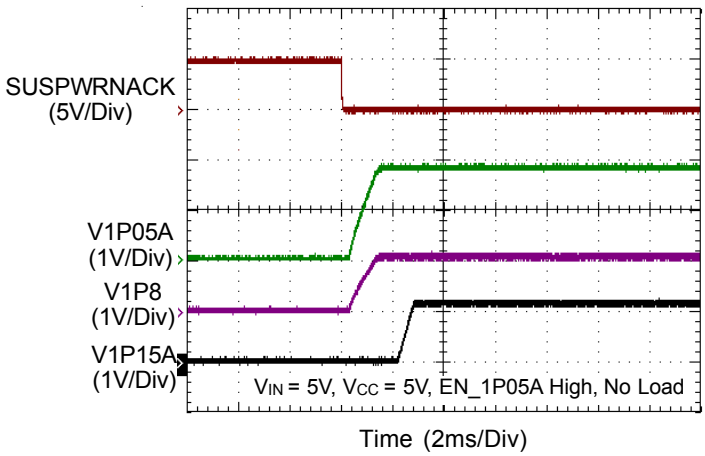
Power Off EN_1P05A



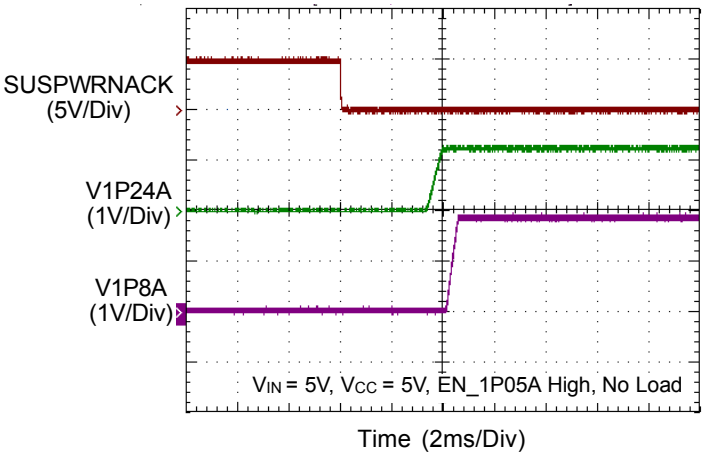
Power Off EN_1P05A



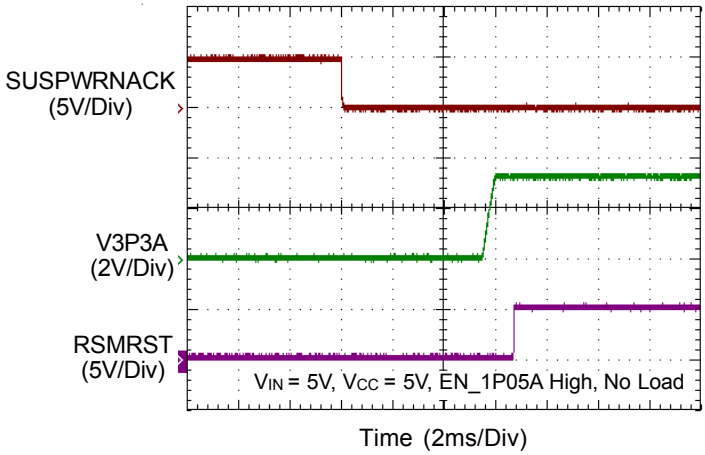
Power On from SUSPWRNACK



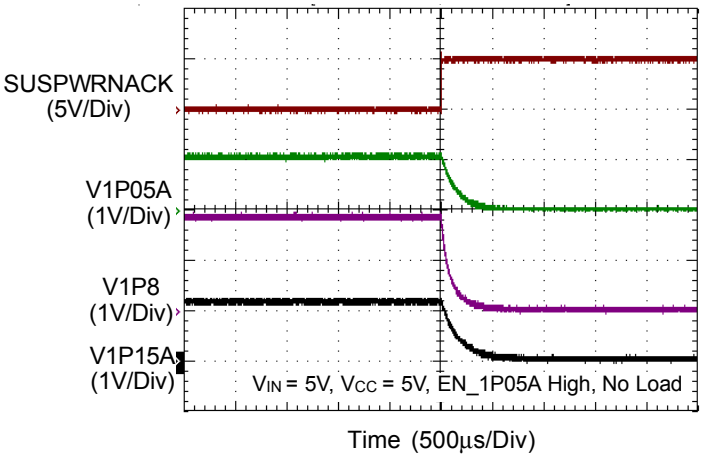
Power On from SUSPWRNACK



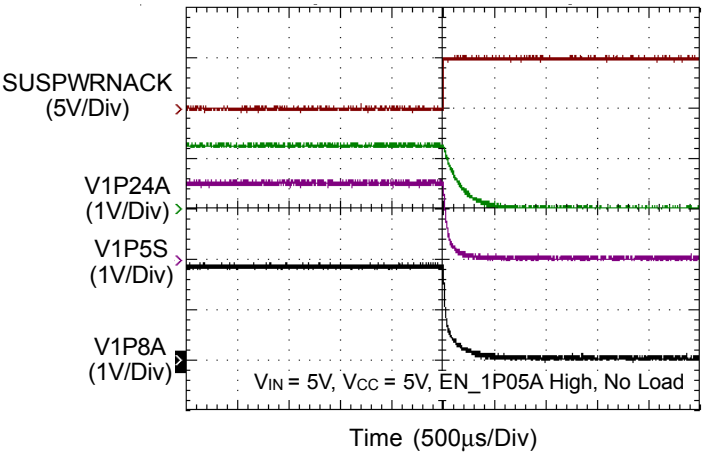
Power On from SUSPWRNACK



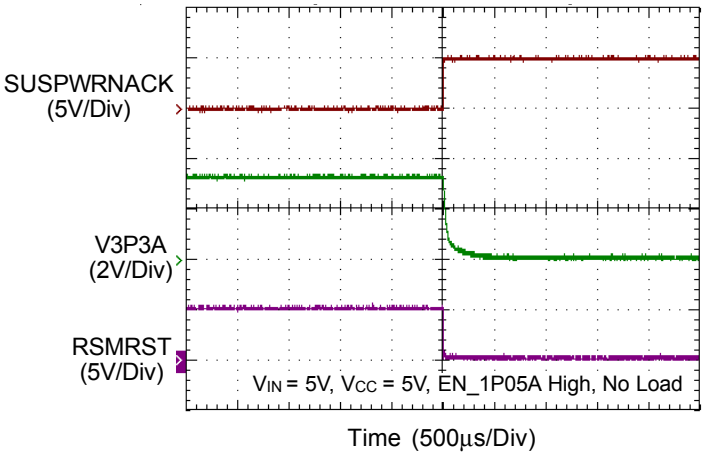
Power Off SUSPWRNACK



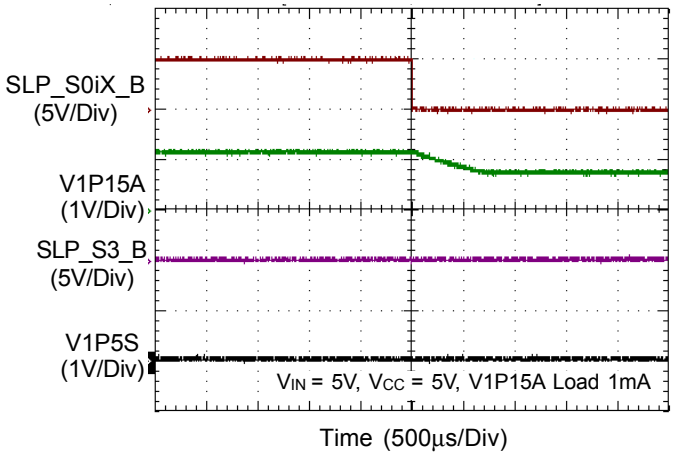
Power Off SUSPWRNACK



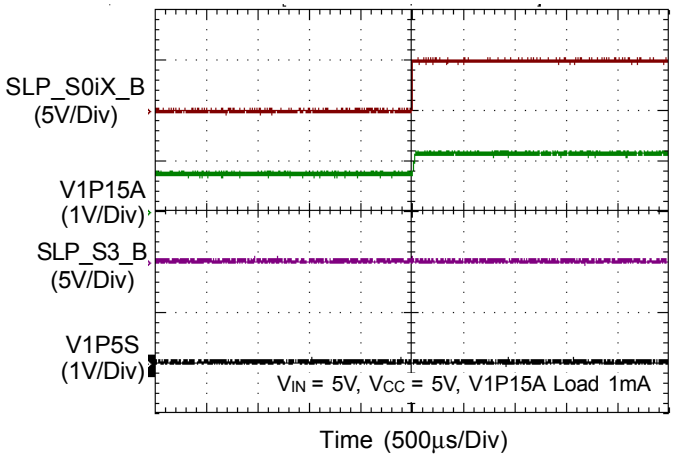
Power Off SUSPWRNACK



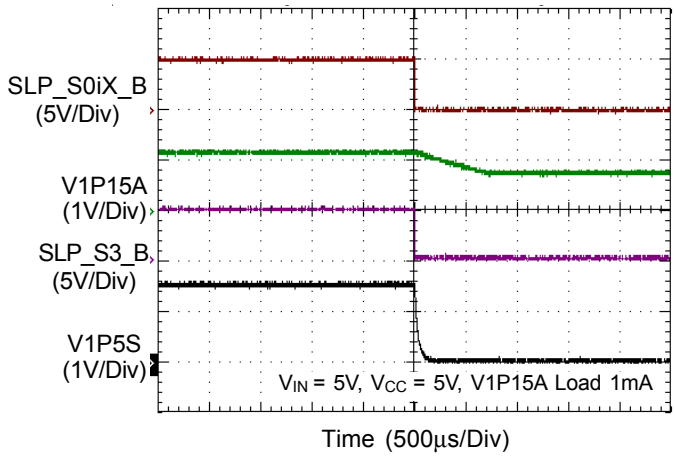
S0iX Enter Sequence



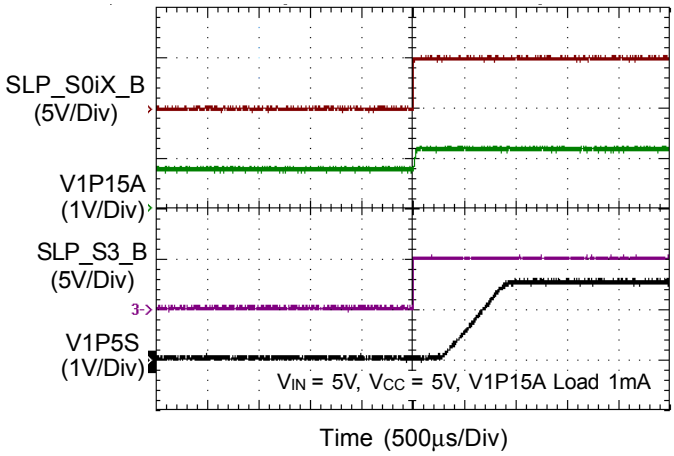
S0iX Exit Sequence



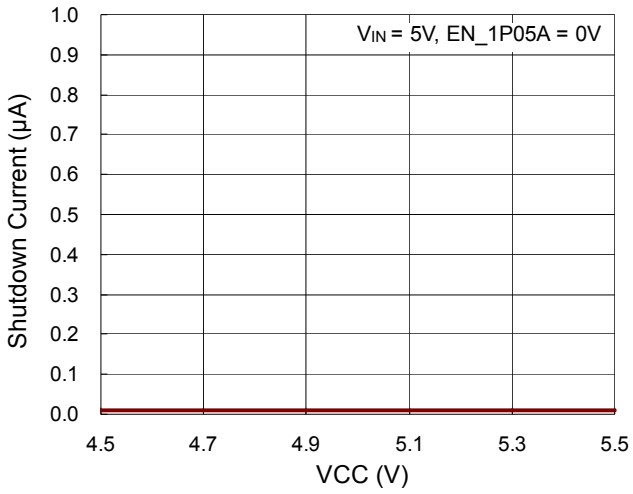
S3 (S4/S5) Enter Sequence



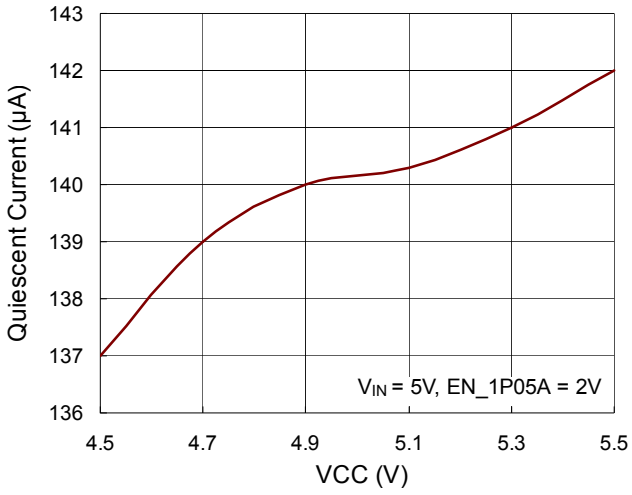
S3 (S4/S5) Exit Sequence



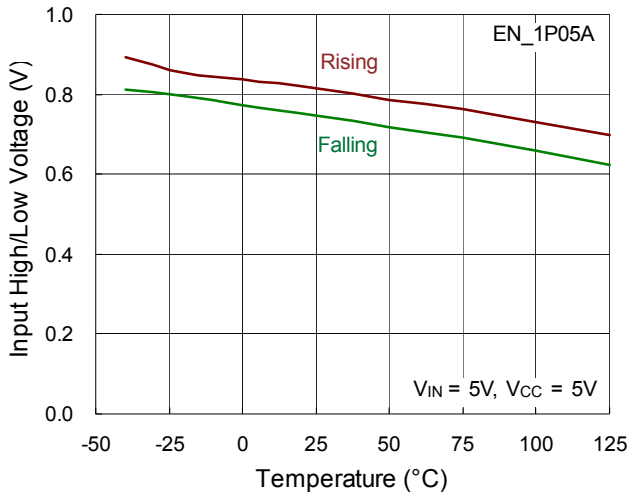
Shutdown Current vs. VCC



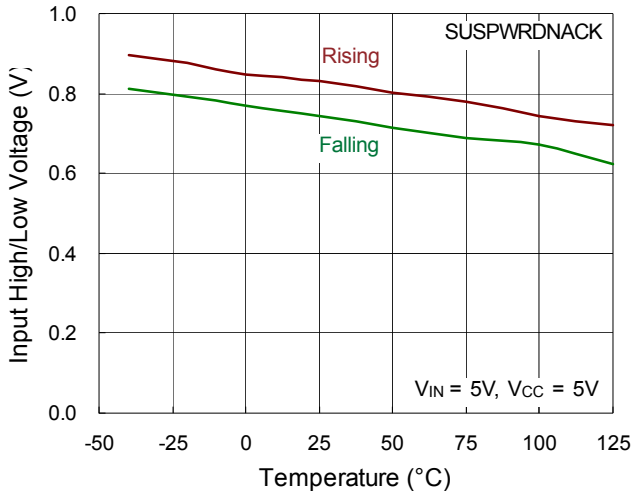
Quiescent Current vs. VCC



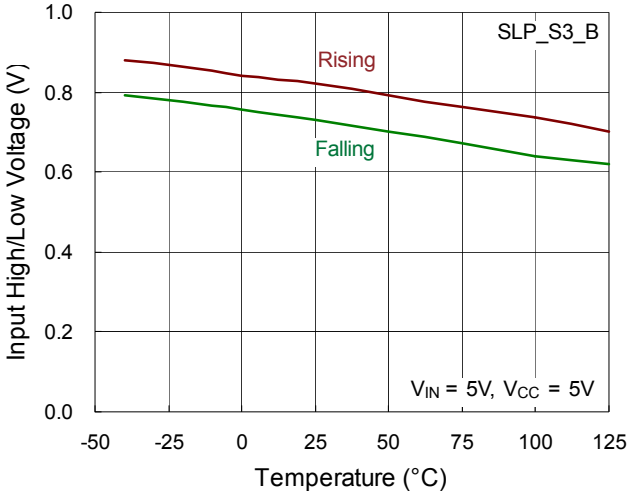
Input High/Low Voltage vs. Temperature



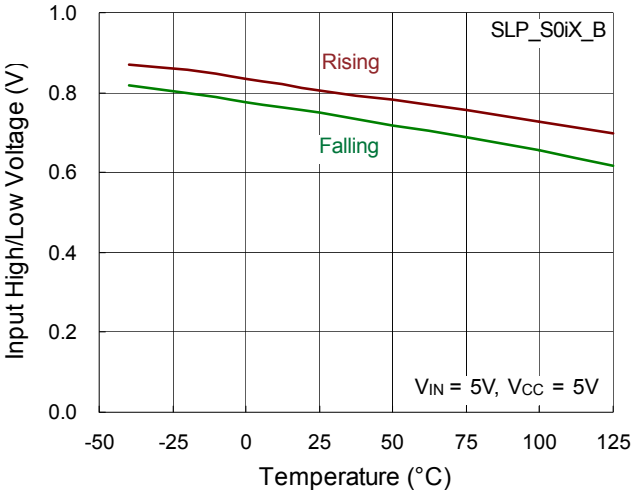
Input High/Low Voltage vs. Temperature



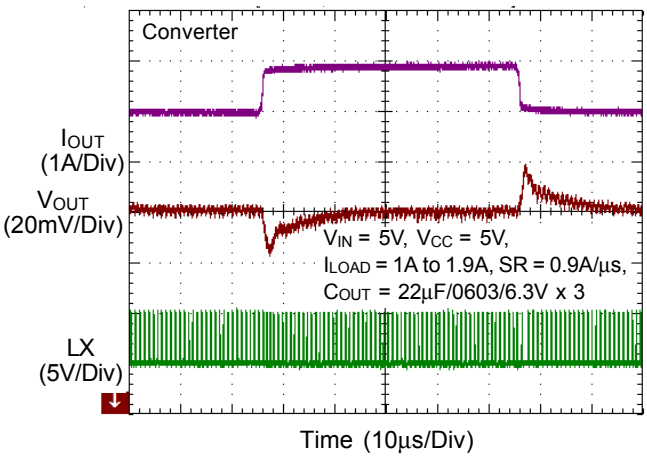
Input High/Low Voltage vs. Temperature



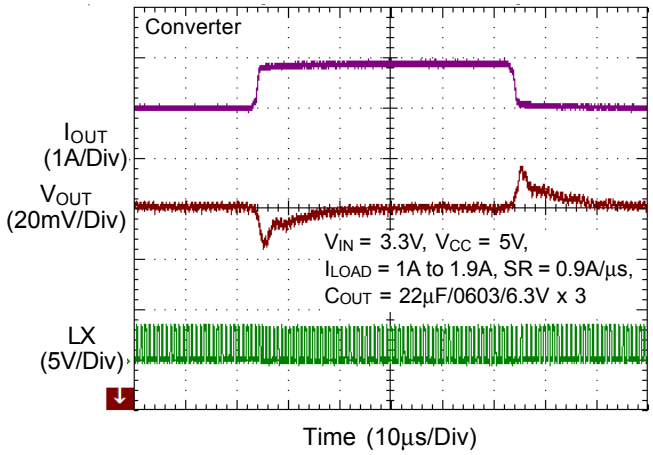
Input High/Low Voltage vs. Temperature



V1P05A Load Transient Response



V1P05A Load Transient Response



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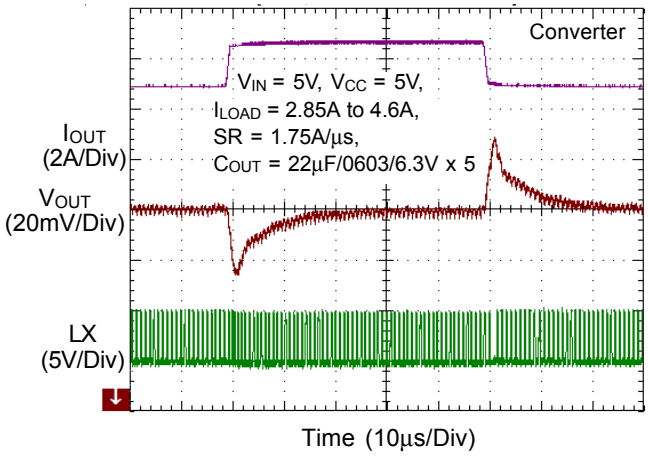

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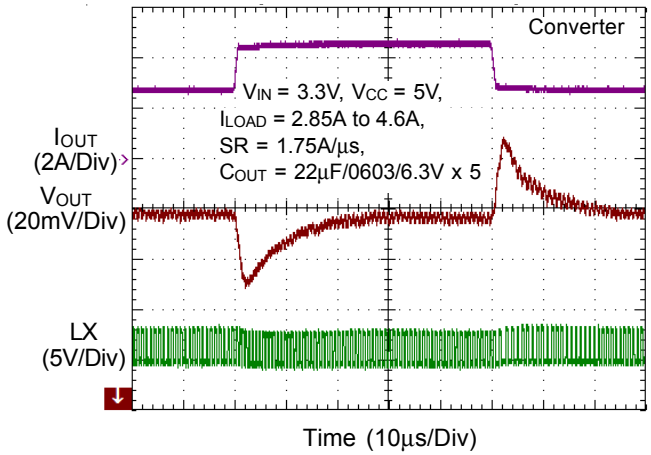
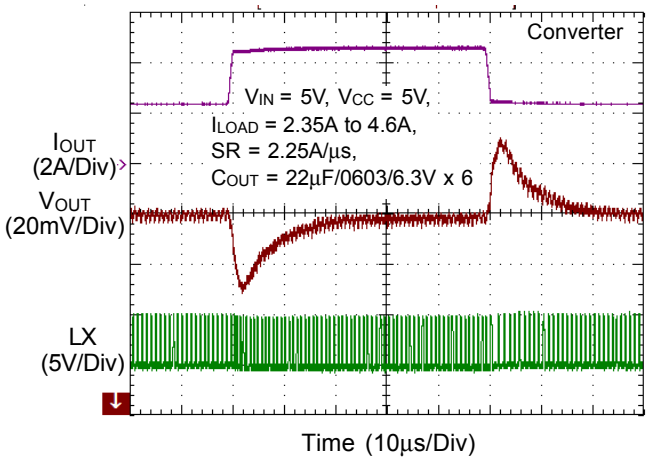


V1P05A Load Transient Response



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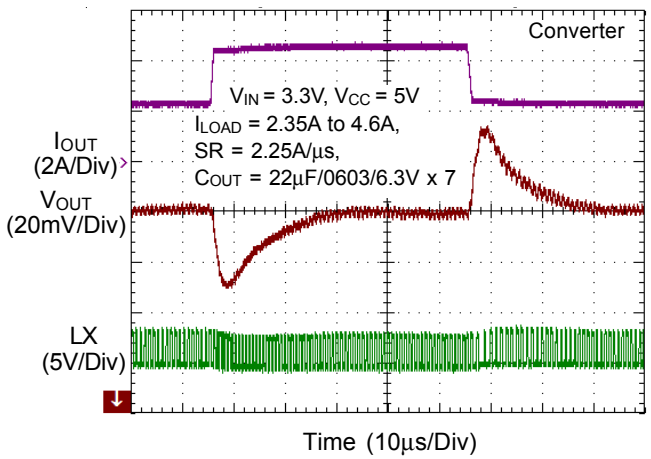
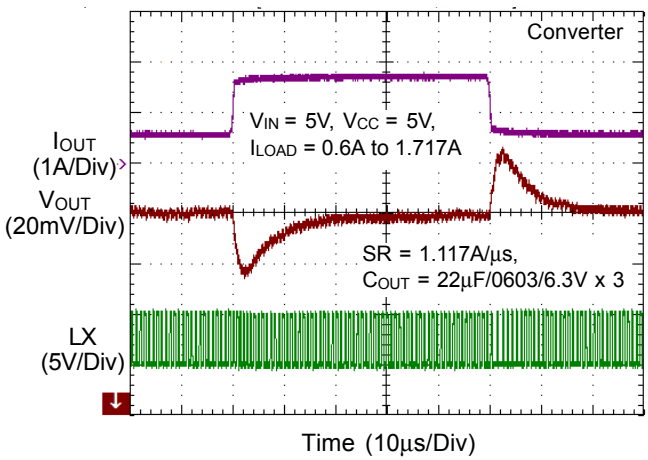
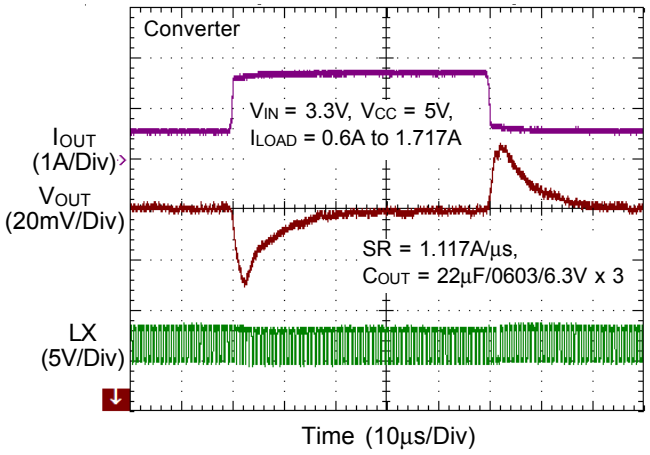


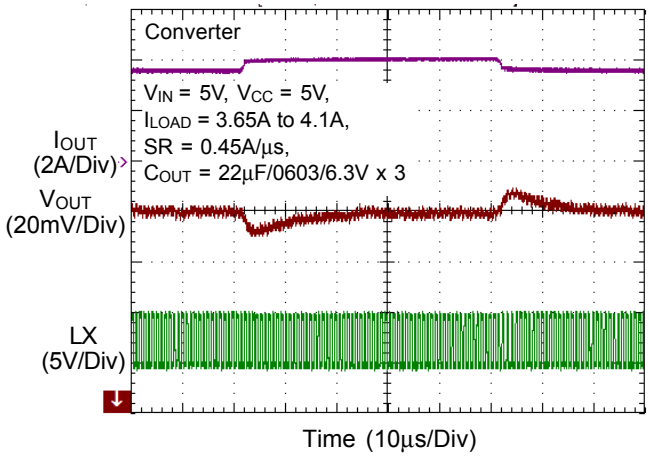
V1P8 Load Transient Response



V1P8 Load Transient Response



V1P8 Load Transient Response



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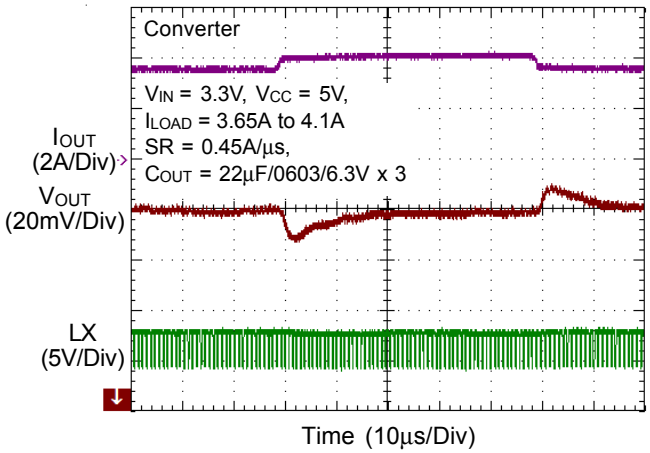

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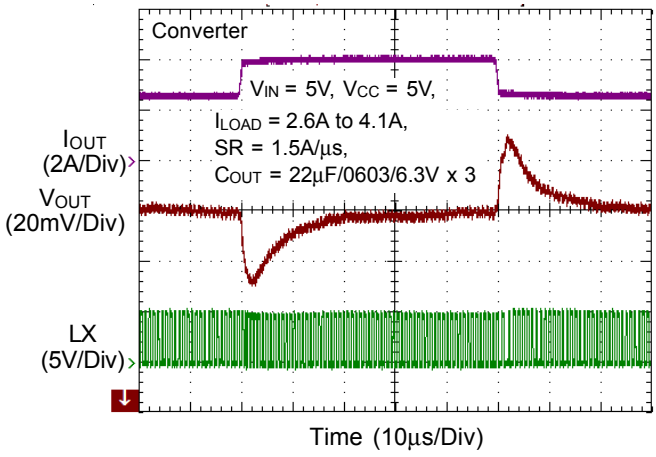
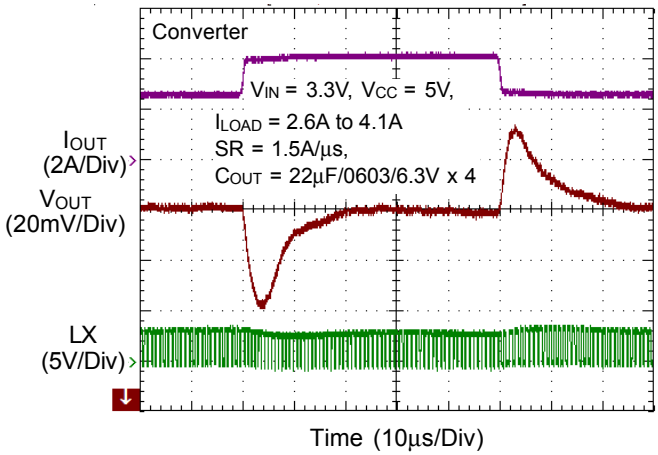
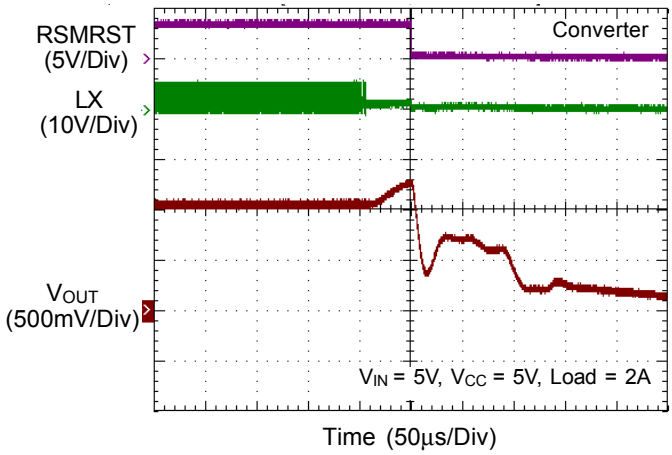


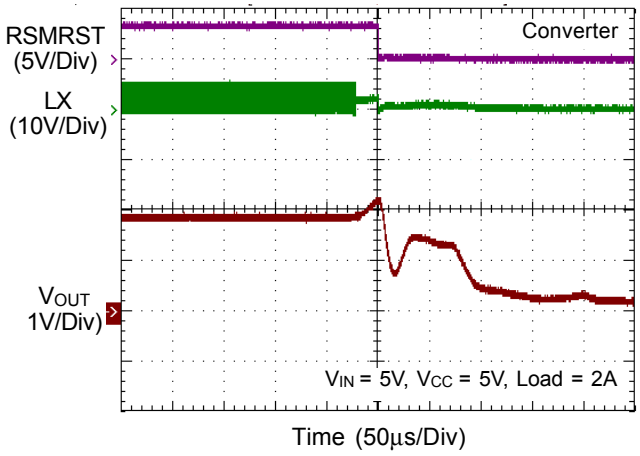
V1P8 Load Transient Response



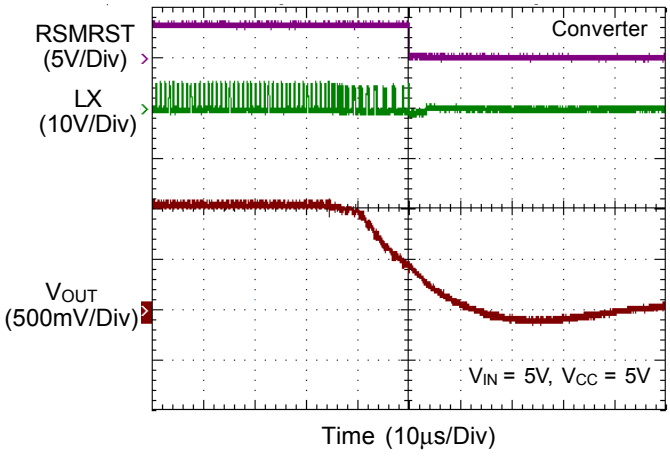
V1P05A OVP



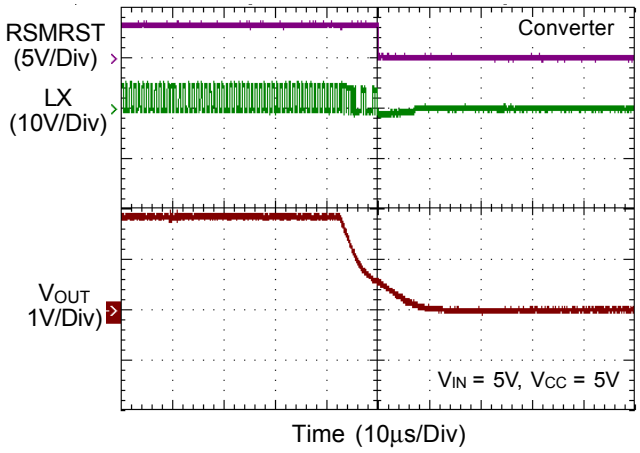
V1P8 OVP



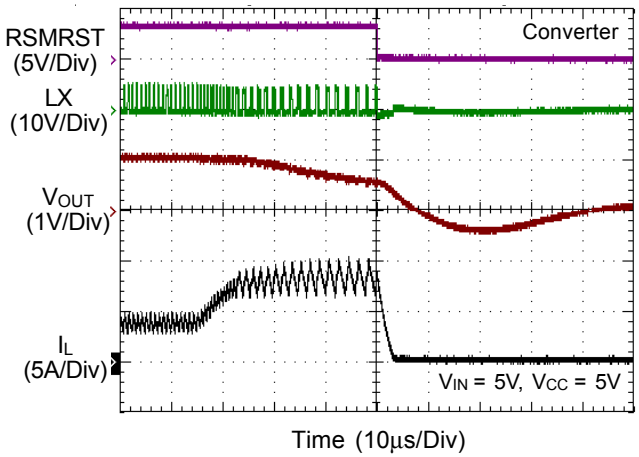
V1P05A UVP



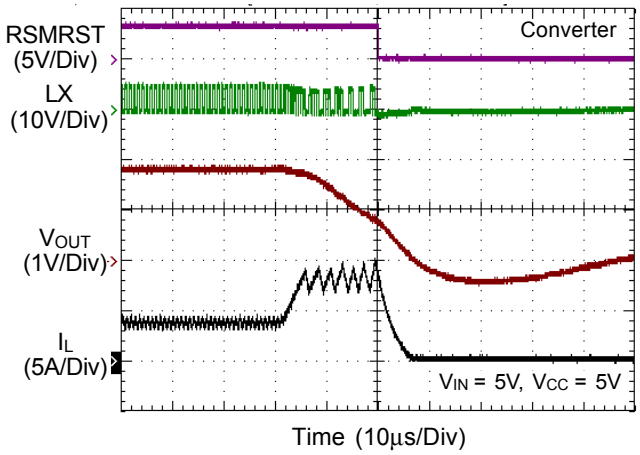
V1P8 UVP



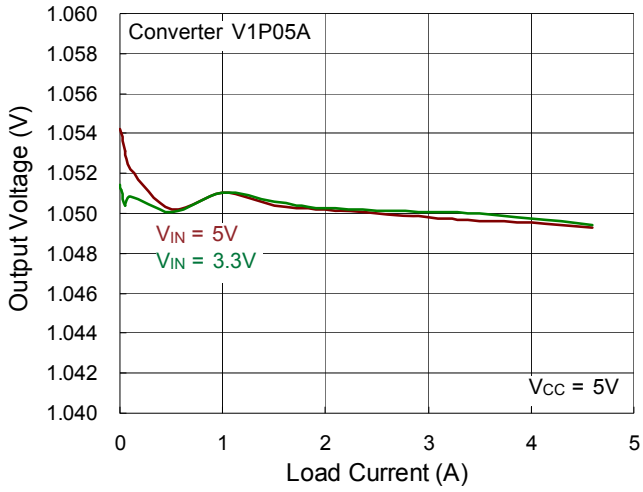
V1P05A OCP



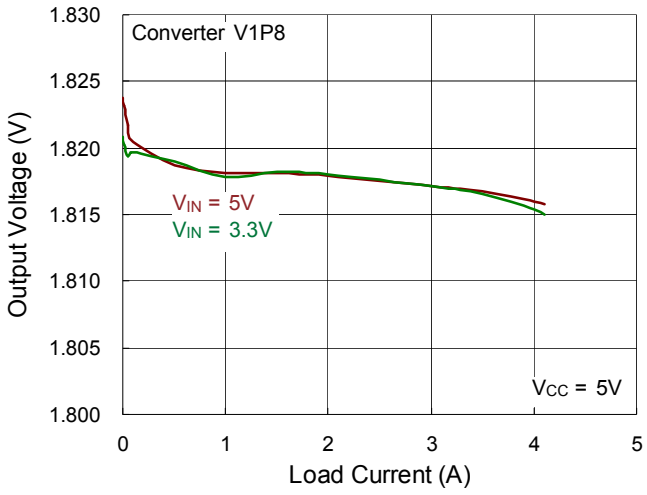
V1P18 OCP



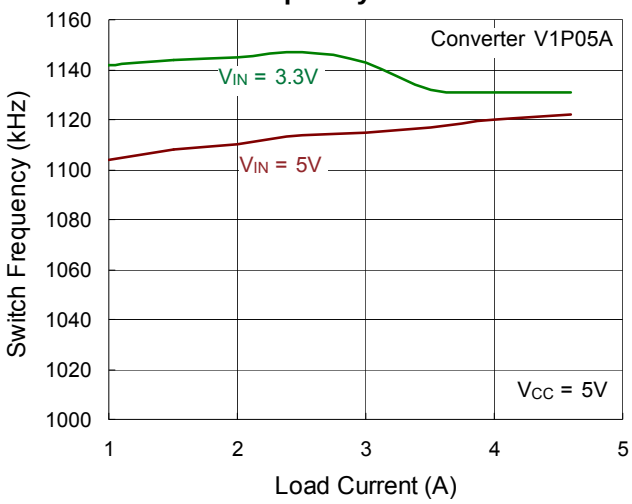
Output Voltage vs. Load Current



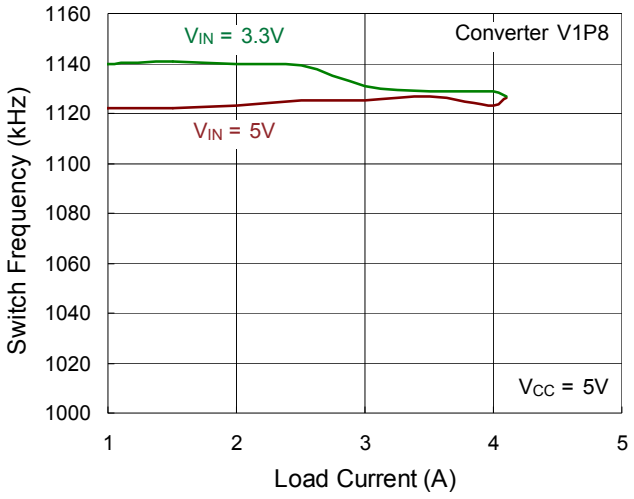
Output Voltage vs. Load Current



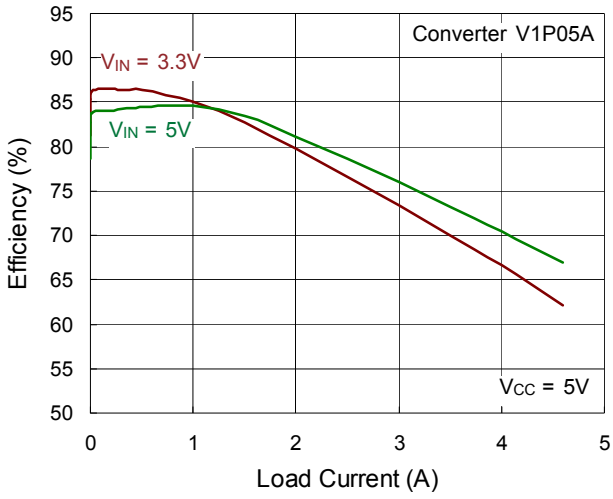
Switch Frequency vs. Load Current



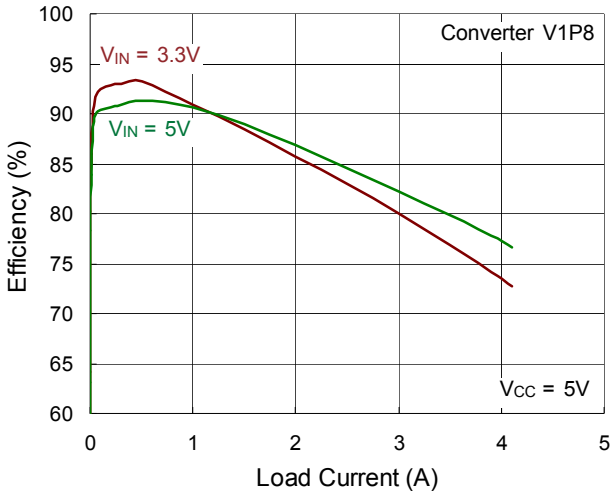
Switch Frequency vs. Load Current



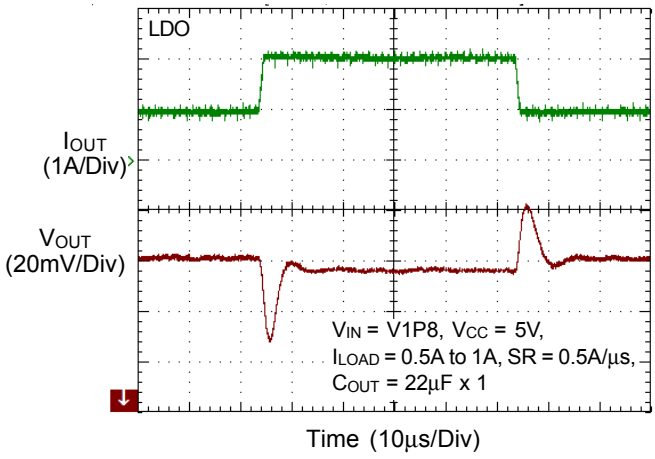
Efficiency vs. Load Current



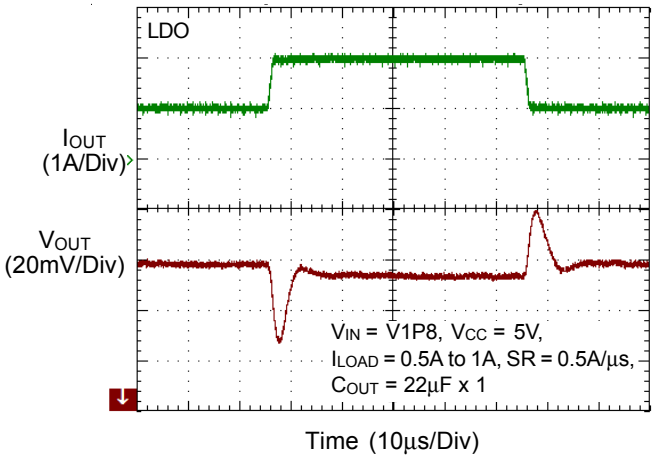
Efficiency vs. Load Current



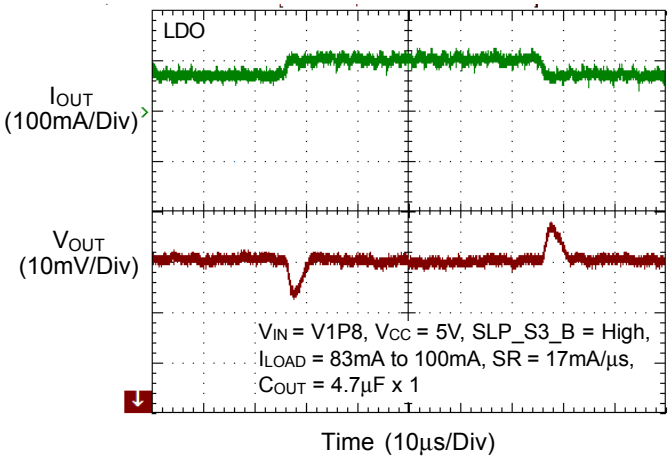
V1P15A Load Transient Response



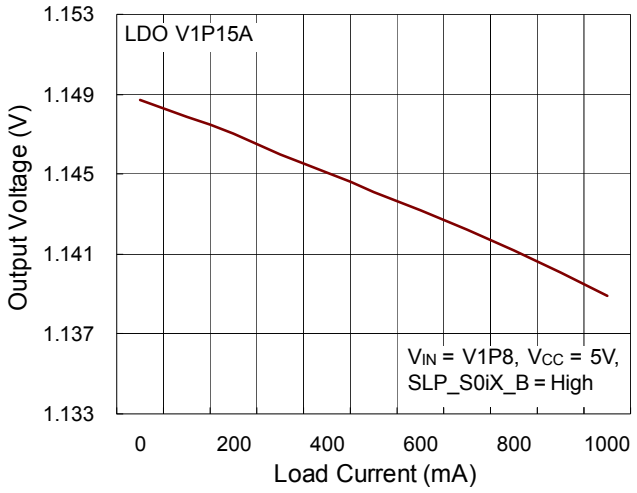
V1P24A Load Transient Response



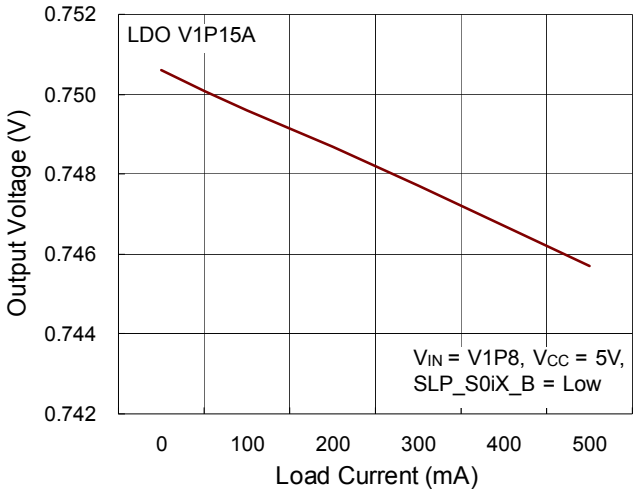
V1P5S Load Transient Response



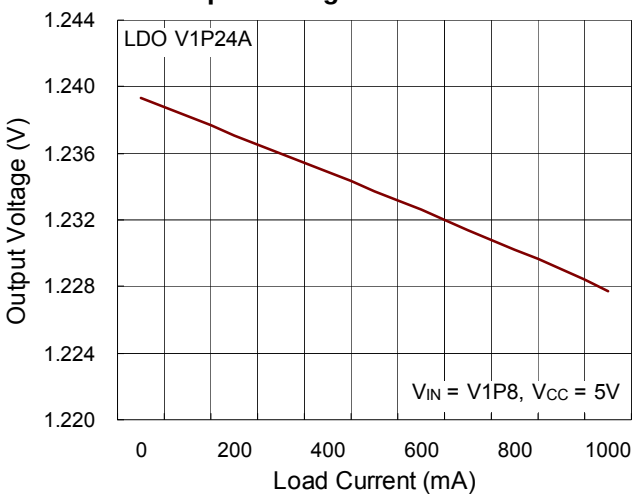
Output Voltage vs. Load Current



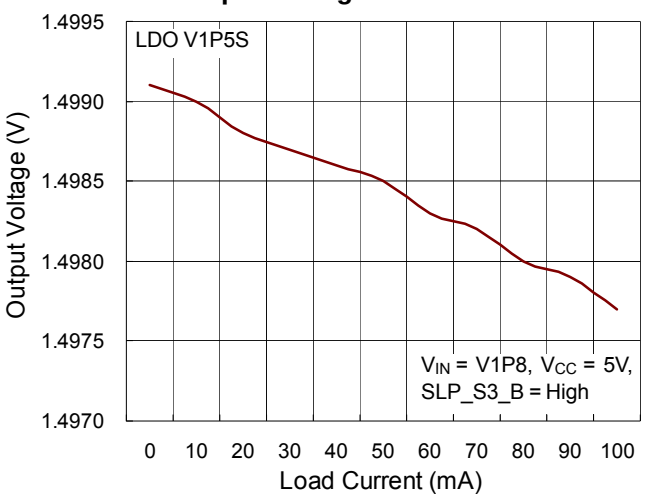
Output Voltage vs. Load Current



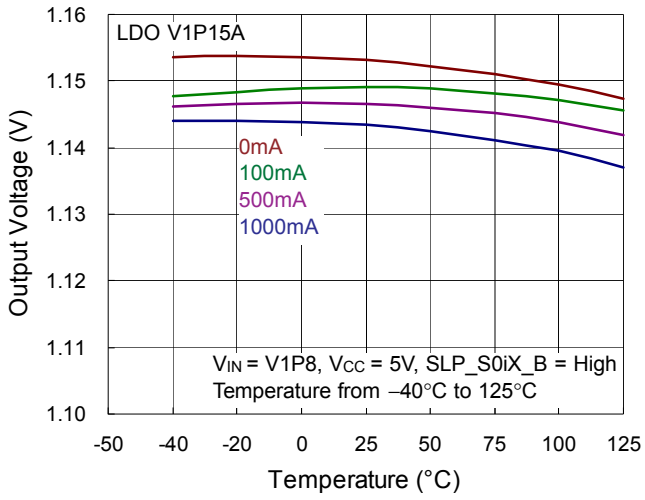
Output Voltage vs. Load Current



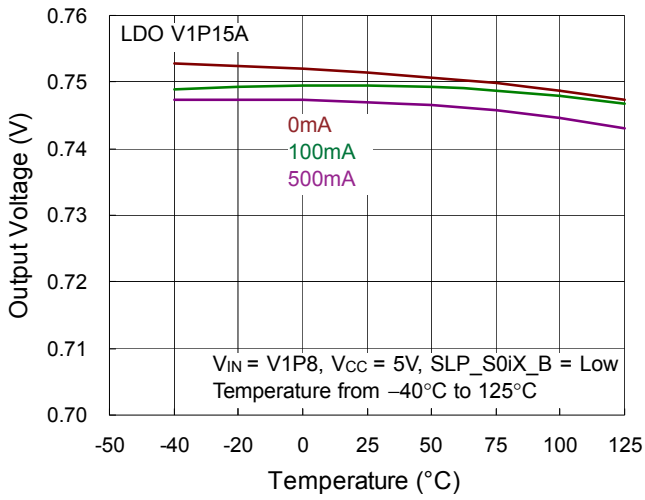
Output Voltage vs. Load Current



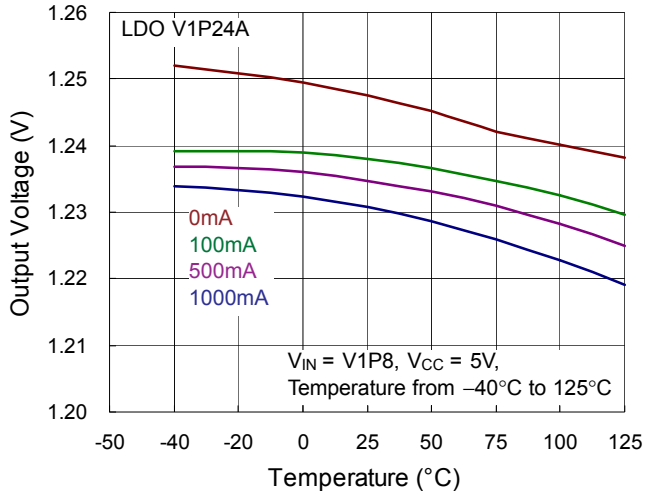
Output Voltage vs. Temperature



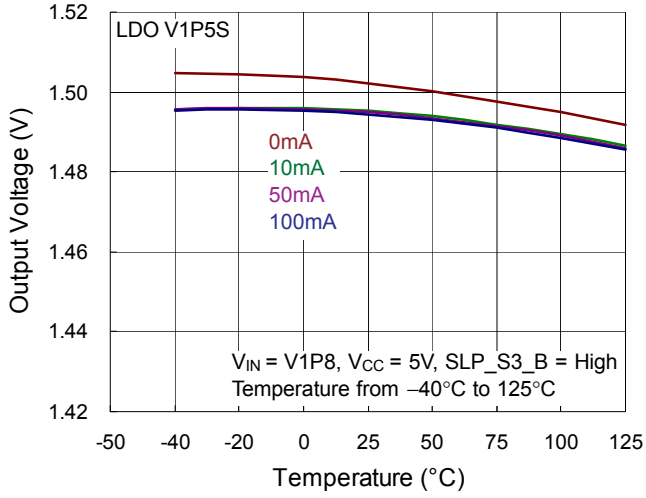
Output Voltage vs. Temperature



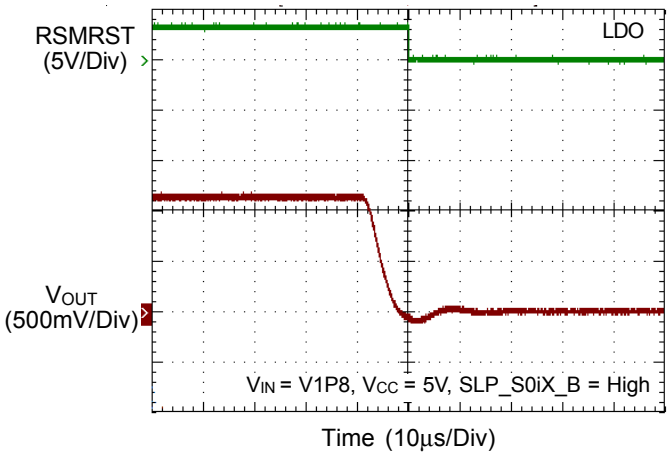
Output Voltage vs. Temperature



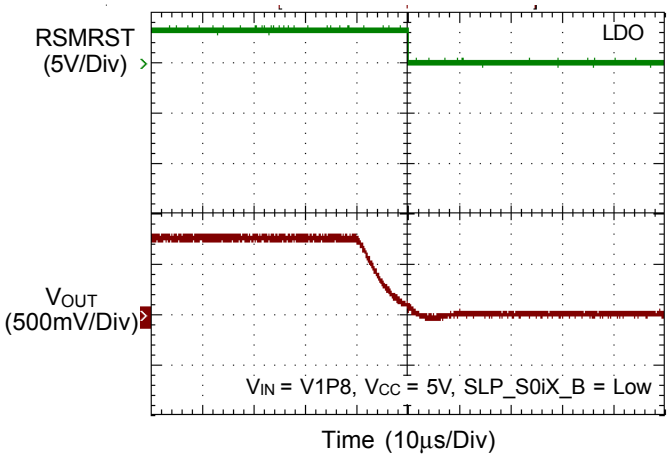
Output Voltage vs. Temperature



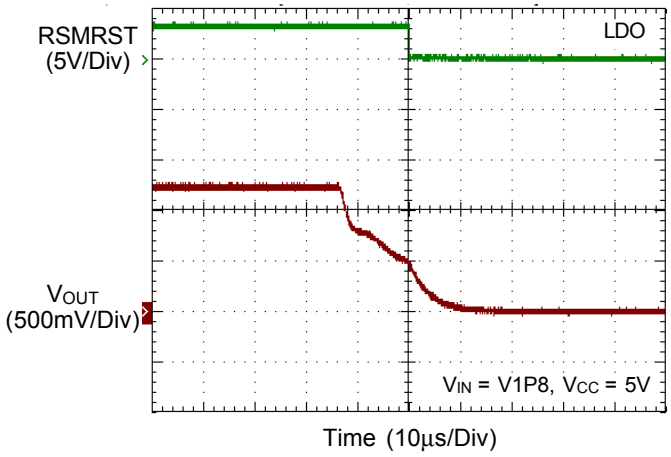
V1P15A UVP



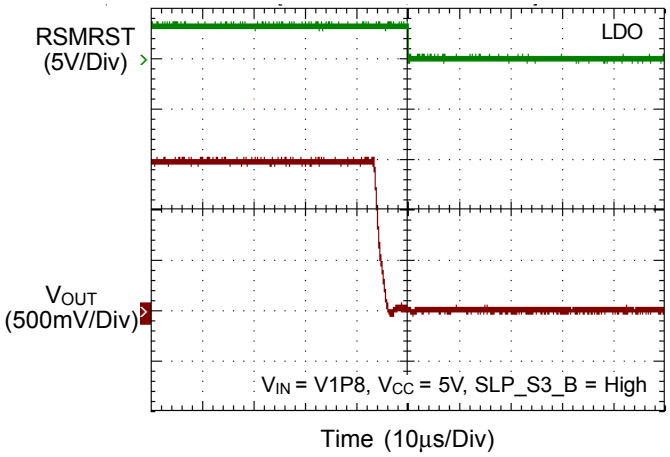
V1P15A UVP



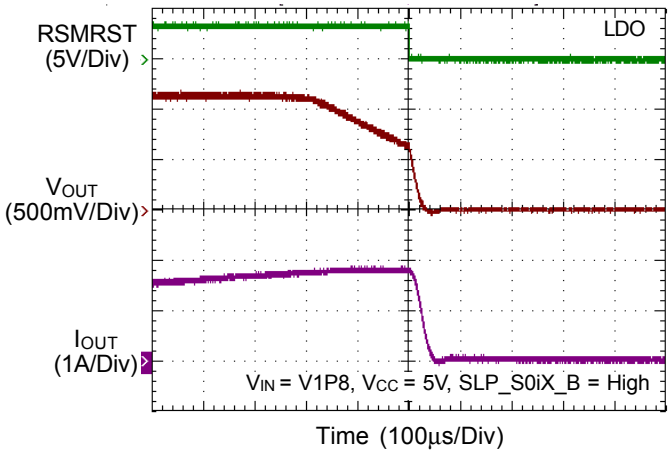
V1P24A UVP



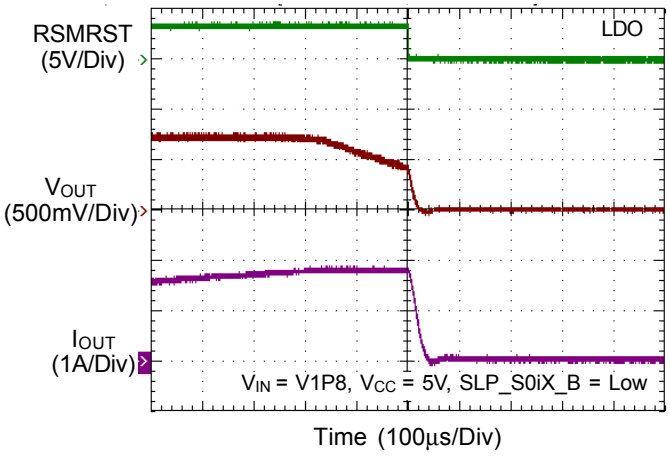
V1P5S UVP



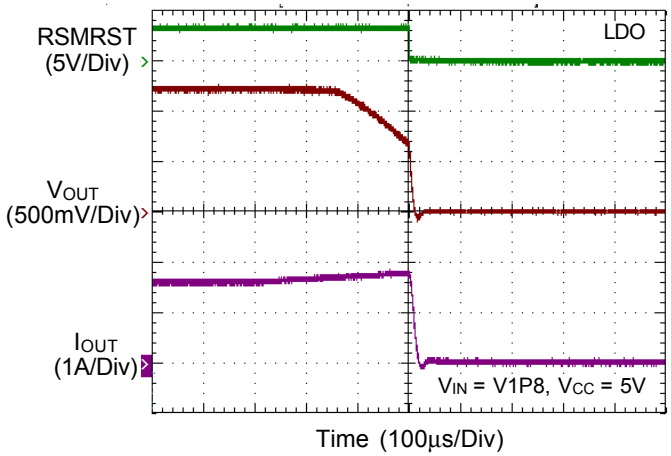
V1P15A OCP



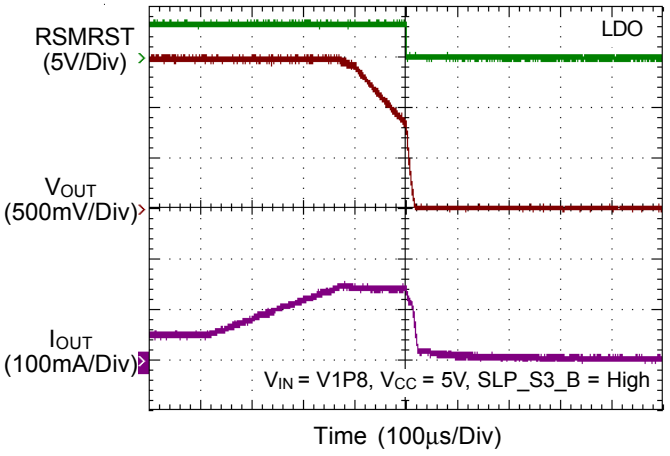
V1P15A OCP



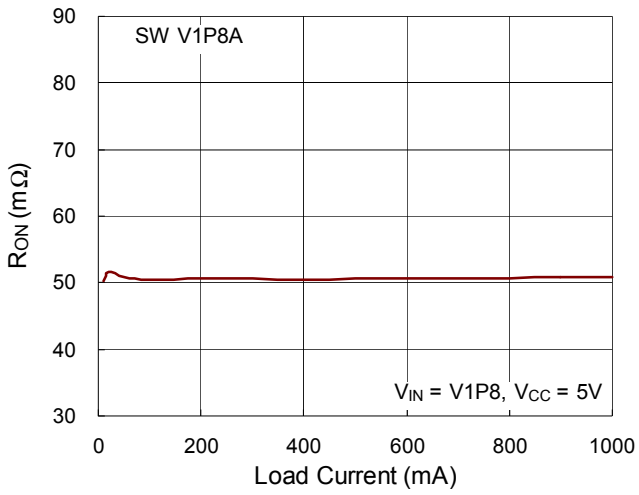
V1P24A OCP



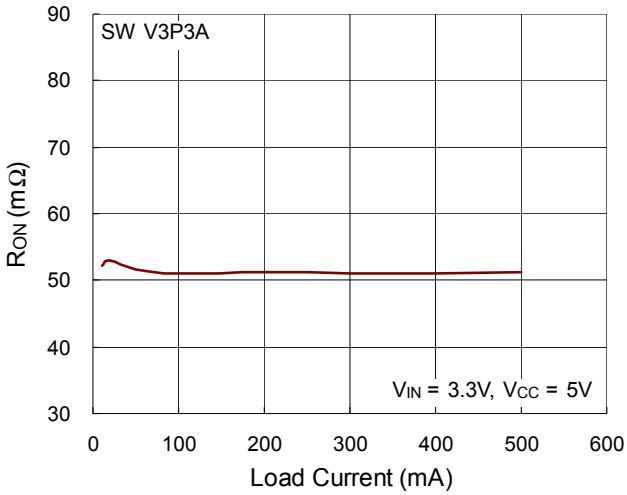
V1P5S OCP



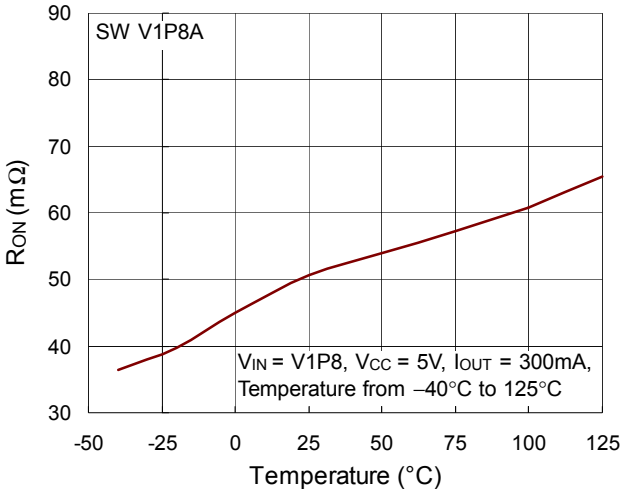
R_{ON} vs. Load Current



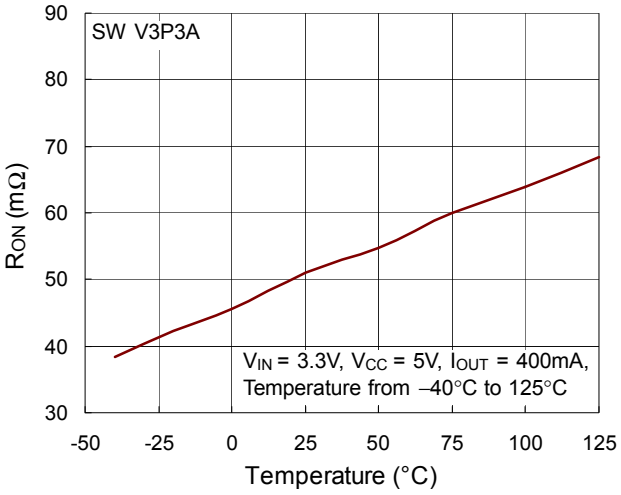
R_{ON} vs. Load Current



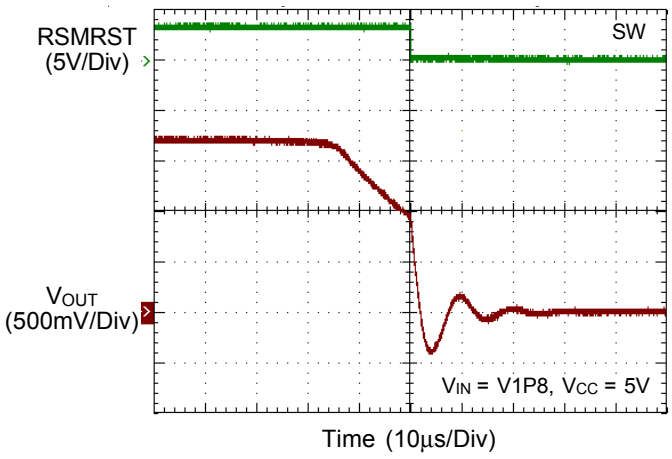
R_{ON} vs. Temperature



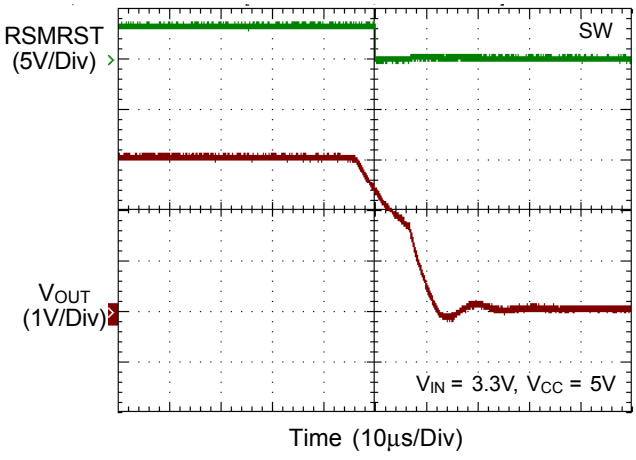
R_{ON} vs. Temperature



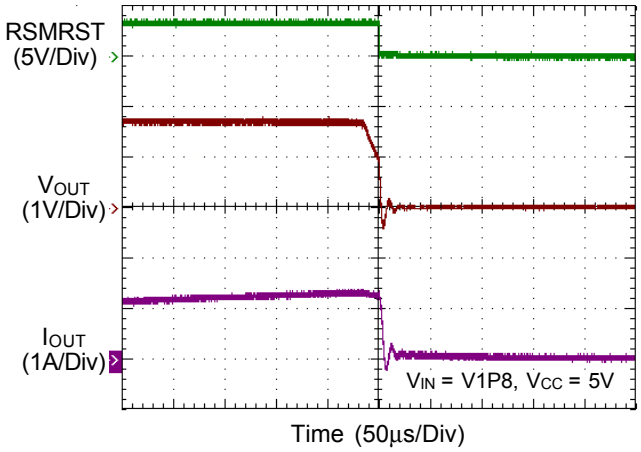
V1P8A UVP



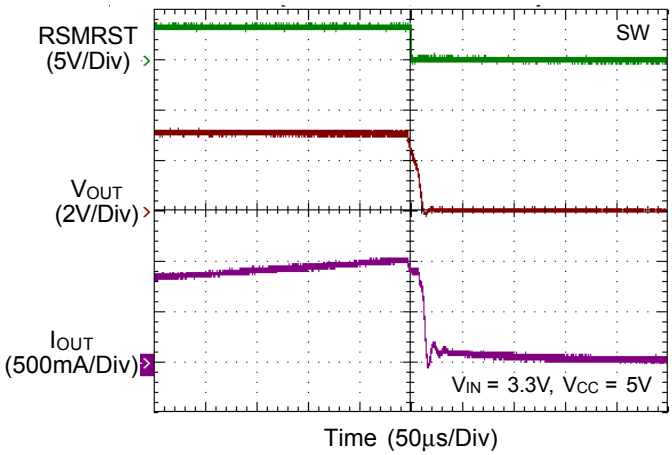
V3P3A UVP



V1P8A OCP



V3P3A OCP



Application Information

RT5041AB is a MOIC (Multi Output Integrated Circuit) and is an integral part of the Braswell Platform focused on power solution integration to minimize system board area. The simplicity of MOIC allows easy adoption without any system firmware changes and can be a direct replacement of most of the SOC VR rails.

Power Path

The RT5041AB is an integrated power solution for the Braswell platform. It includes two DC to DC Buck converters, three Linear Dropout regulators and two power switches. Expect Core power, DDR power and System 3V/5V power, RT5041AB package the rest power paths into one.

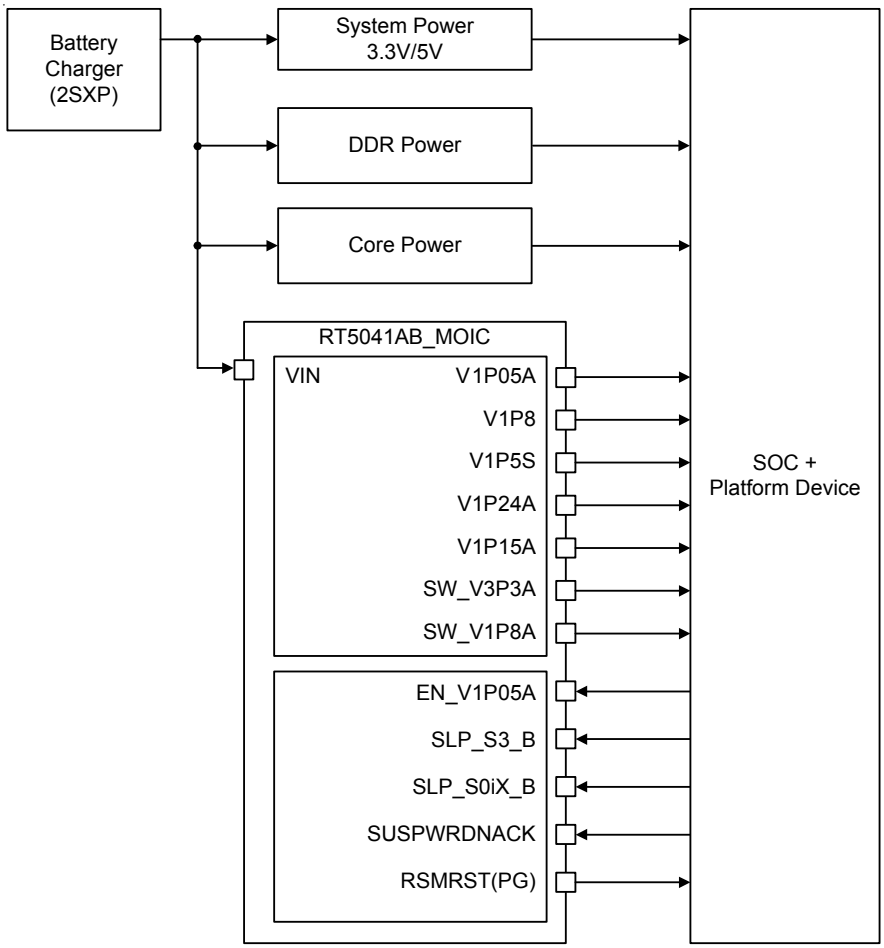


Figure 1. Simplified MOIC Power Rails Apply

All data of the power paths provided by RT5041AB device is listed as Table 1.

Table1. Power Path

Resource Name	Type	Voltage Range	Peak Current Rating
V1P05A	Buck Converter	1.05V	4600mA
V1P8	Buck Converter	1.8V	4100mA*
V1P5S	LDO	1.5V	100mA
V1P24A	LDO	1.24V	1000mA
V1P15A	LDO	0.75V / 1.15V	1000mA**
V3P3A	Switch	3.3V	450mA
V1P8A	Switch	1.8V	1000mA

* V_{IN} = 5V only

** V_{OUT} @ 1.15V

Buck Converter

RT5041AB applies two synchronous step-down buck converters with both integrated a P-Channel high side MOSFET and a N-Channel low side MOSFET. The converter control scheme is based on current mode constant-on-time (COT) architecture, which has fast transient response and minimizes external components. Based on the internal current ramp information, it can used multi-layer ceramic capacitors (MLCC) as the output capacitors without high-ESR bulk or virtual ESR network required for the loop stability.

Buck converters of RT5041AB applies Power-Saving feature by automatic enabling diode emulation mode (DEM) as load decrease. When the load makes converter work at continuous current mode (CCM) the frequency is fixed at 1.2MHz.

A soft-start function is built inside. The internal current source charges an internal capacitor to make the soft-start ramp voltage. When buck converter powers up, the output voltage will track the internal ramp voltage during soft-start interval to prevent inrush current.

When EN_1P05A goes low to let buck converters shutdown mode occur, or the output under-voltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

The buck converters have a full set of protection.

Buck Over-Current Protection

The OCP is implemented using a cycle-by-cycle valley detected control circuit. The switch current is monitored by measuring the low-side voltage between the LX pin and PGND. The voltage is proportional to the switch current and the on-resistance of the low-side MOSFET. To improve accuracy, the low-side voltage sensing is temperature compensated.

When high side MOSFET turn-on, the high-side switch current increases at a linear rate and determines by VIN, VOUT, TON and inductance. And when low side MOSFET turn-on, the low-side switch current decreases linearly. The average value of the switch current is the output load current. If the sensing voltage of the low-side MOSFET is above the voltage proportional to the current limit, the converter keeps the low-side turn on until the sensing voltage falls below the voltage proportional to the current limit and start a new switching cycle.

Buck Output Under-Voltage Protection

When the over current limit is active, the output voltage falls. If the output voltage falls under 60% of the reference voltage, the UVP comparator signal goes high and an internal UVP counter start to count. If the counted timing is over the UVP delay time, the high-side and low-side MOSFET will turn off and latched. The way to cannel the latched behavior is to re-enable RT5041AB or re-give VCC power of RT5041AB.

Buck Output Over-Voltage Protection

When the output voltage exceeds 120% of the reference, the OVP comparator signal goes high and an internal OVP counter start to count. If the counted timing is over the OVP delay time, the low-side MOSFET will continue to turn on and latched.

Buck Over-Temperature Protection

RT5041AB monitors the temperature of buck converters. If the temperature of the buck converter is over 150°C the OTP circuit acts and makes all power rails of RT5041AB shutdown. They recover back with power-up sequence when the temperature of buck converters is low to 125°C.

Linear Dropout Regulator

The RT5041AB includes three high performance linear dropout regulators. The peak current rating is designed for short period current, not for thermal design current.

LDOs of RT5041AB also have soft-start function. An internal current source charges an internal capacitor to make the soft-start ramp voltage. When LDOs power up, the output voltage will track the internal ramp voltage during soft-start interval to prevent inrush current.

When enable signals go low to let LDOs shutdown mode occur, or the output under-voltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

RT5041AB has two enable signals SLP_S3_B and SLP_S0iX_B to control LDO_V1P5S and LDO_V1P15A respectively to meet the S3/S4 and S0iX power saving mode status of Braswell platform. If SLP_S3_B signal goes high, LDO_V1P5S powers on; otherwise, the LDO_V1P5S keeps off. When RT5041AB powers up from internal power up sequence, LDO_V1P15A will raise up to 1.15V with ignoring SLP_S0iX_B signal until device detecting the first rising edge of the signal. After detecting the first rising edge of the SLP_S0iX_B if the SLP_S0iX_B signal goes high, LDO_V1P15A keeps 1.15V. And if it goes low, LDO_V1P15A changes to 0.75V.

The LDO contains an independent current limit and under voltage protection circuit to prevent unexpected applications. The current limit circuit monitors the current of the path from input to output by a current sensing circuit and controls the pass transistor's gate voltage. When the path current is over the current limit, the current limit circuit fixes the gate voltage to limit the output current. And if the output voltage is less than 60% of VOUT, the UVP circuit will shutdown the LDO and latched. Re-enable RT5041AB device to disable the latched status.

Power Switch

There are also two power switches within RT5041AB. SW_V3P3A is a P-Channel power switch MOSFET, and SW_V1P8A is a N-Channel power switch MOSFET.

Power switches of RT5041AB have soft-start function, too. An internal current source charges an internal capacitor to make the soft-start ramp voltage. When power switches turn on, the output voltage will track the internal ramp voltage during soft-start interval to prevent inrush current.

When EN_1P05A goes low to let power switches shutdown mode occur, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

SW_V3P3A and SW_1P8A also apply current limit protection and under voltage protection function. The current limit circuitry prevents damage to the power switch MOSFET and the backend device but can deliver load current up to the current limit threshold. And if the output voltage is less than 2.7V for SW_V3P3A or 1.2V for SW_V1P8A, the RT5041AB will shutdown and latched.

RSMRST

RSMRST is an open-drain output and requires a pull-up resistor. RSMRST is actually a power good output signal for monitoring SW_V3P3A. RSMRST pulls up if SW_V3P3A is above 90% of its nominal voltage; otherwise the RSMRST goes low.

SUSPWRDNACK

SUSPWRDNACK is an active high dedicated input signal that tells the RT5041AB to turn off the power rails. If pull up SUSPWRDNACK signal high to turn off power rails and pull low again, the all power rails will raise up with the power up sequence. This signal will work when EN_1P05A goes high.

MOIC VR STATUS

RT5041AB MOIC has three controlled enable pins EN_1P05A, SLP_S0iX_B and SLP_S3_B for changing the voltage rails (VR) status to match the different power saving mode In the Braswell platform. The VR power status is shown directly as the Table 2.

Table2. MOIC Voltage Rails Power Status

Voltage Rails	S0	S0iX	S3	S4/S5
V1P05A	ON	ON	ON	ON
V1P8	ON	ON	ON	ON
V1P5S	ON	ON	OFF	OFF
V1P24A	ON	ON	ON	ON
V1P15A	ON @ 1.15V	ON @ 0.75V	ON @ 0.75V	ON @ 0.75V
V3P3A	ON	ON	ON	ON
V1P8A	ON	ON	ON	ON

According to Table 2, set three control signals to high for satisfying S0 mode; for case S0iX mode, give a low level voltage to SLP_S0iX_B to change LDO_V1P15A voltage from 1.15V to 0.75V. If the system need move into S3 or S4/S5 status, set SLP_S0iX_B and SLP_S3_B to low to make the action. The relations of the control signals and the VR power status are shown in the Table 3.

Table3. Control Pin Truth Table for VR Power Status

Status	EN_1P05A	SLP_S0iX_B	SLP_S3_B
S0	High	High	High
S0iX	High	Low	High
S3	High	Low	Low
S4/S5	High	Low	Low
OFF	Low	X	X

MOIC SEQUENCING

Power-Up Sequence

When EN_1P05A comes to high RT5041AB starts an internal power-up-sequence to enable most voltage rails. After RSMRST signal going to high, the power-up-sequence completes. Note that LDO_V1P5S is not included in the internal power up sequence.

SLP_S0iX_B signal should come after V1P8, if use V1P8 power rail as the input of LDO_V1P5S. MOIC will monitor LDO_V1P5S internal power good signal when SLP_S3_B goes high. If MOIC detects fault of any internal power good during the power up sequence, RT5041AB will be latched.

Power-Off Sequence

There are two signals, EN_1P05A and SUSPWRDNACK, can make all power rails of RT5041AB go to off mode. When use EN_1P05A to disable RT5041AB, all the output signals and power rails will be off at the same time. If use SUSPWRDNACK signal to power off all VRs, the RSMRST will fall down after SW_V3P3A being under 85% of its output voltage.

S0iX Mode and S3(S4/S5) Mode Power Status

RT5041AB is able to meet power saving requirement of the sleep mode on the Braswell platform.

From S0 mode to S0iX mode, SLP_S0iX_B goes low; from S0 mode to S3 (S4/S5) mode, SLP_S0iX_B and SLP_S3_B both go to low.

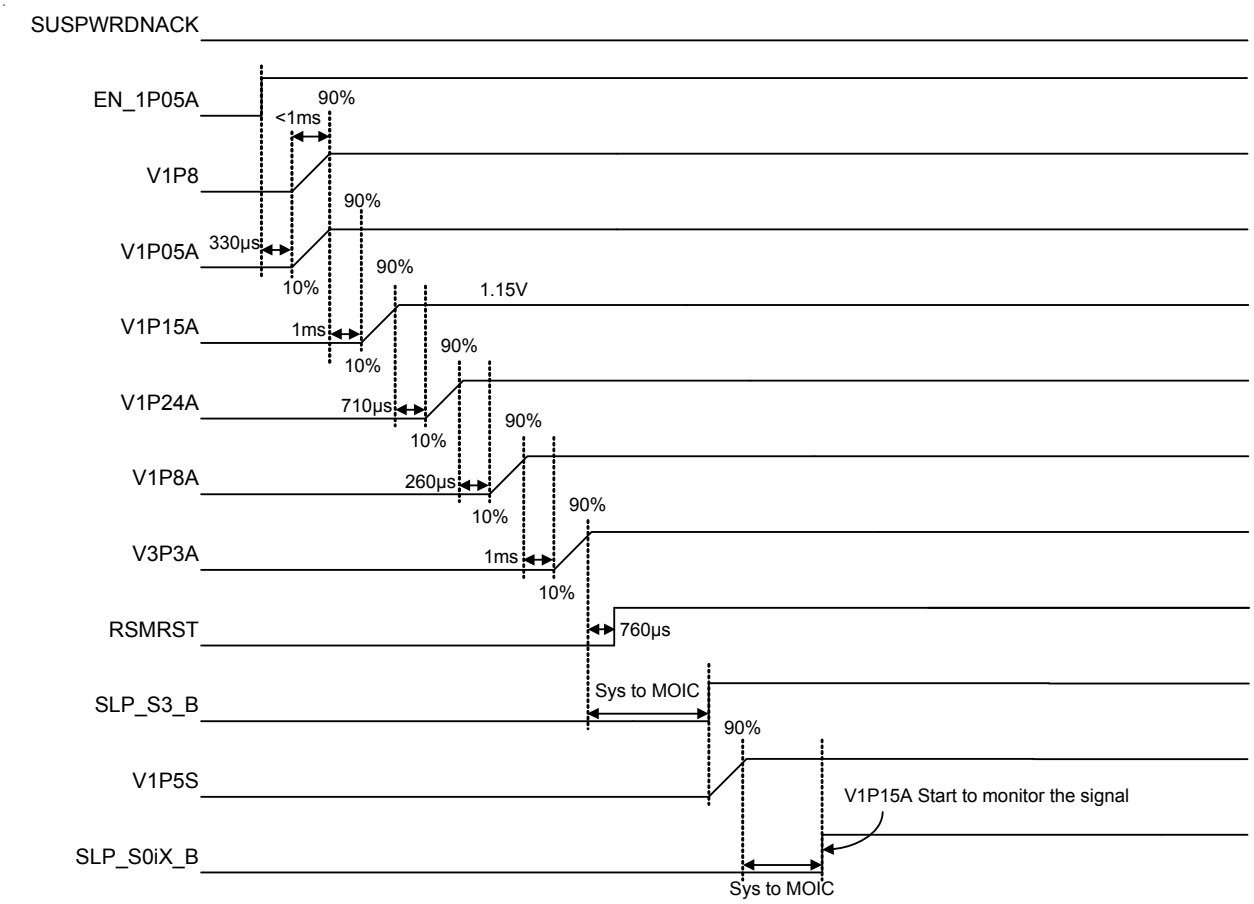


Figure 2. Power-Up Sequence

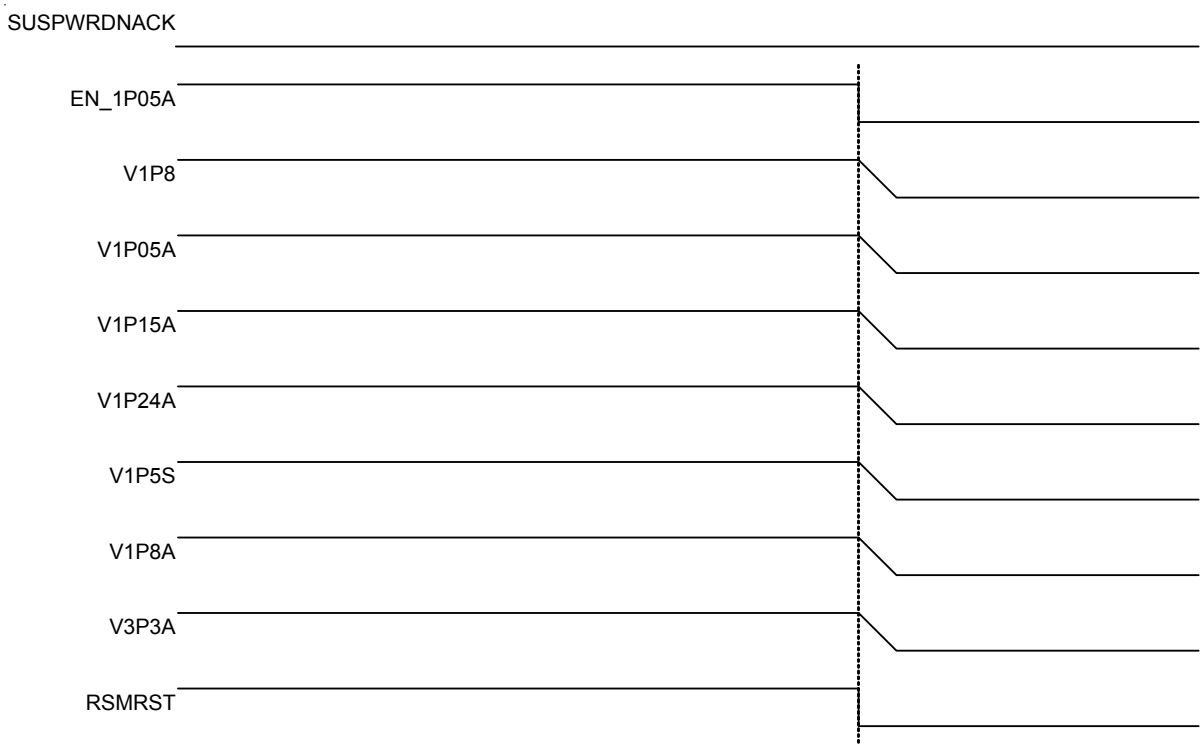


Figure 3. Power-Off Sequence with EN_V1P05A Going Low

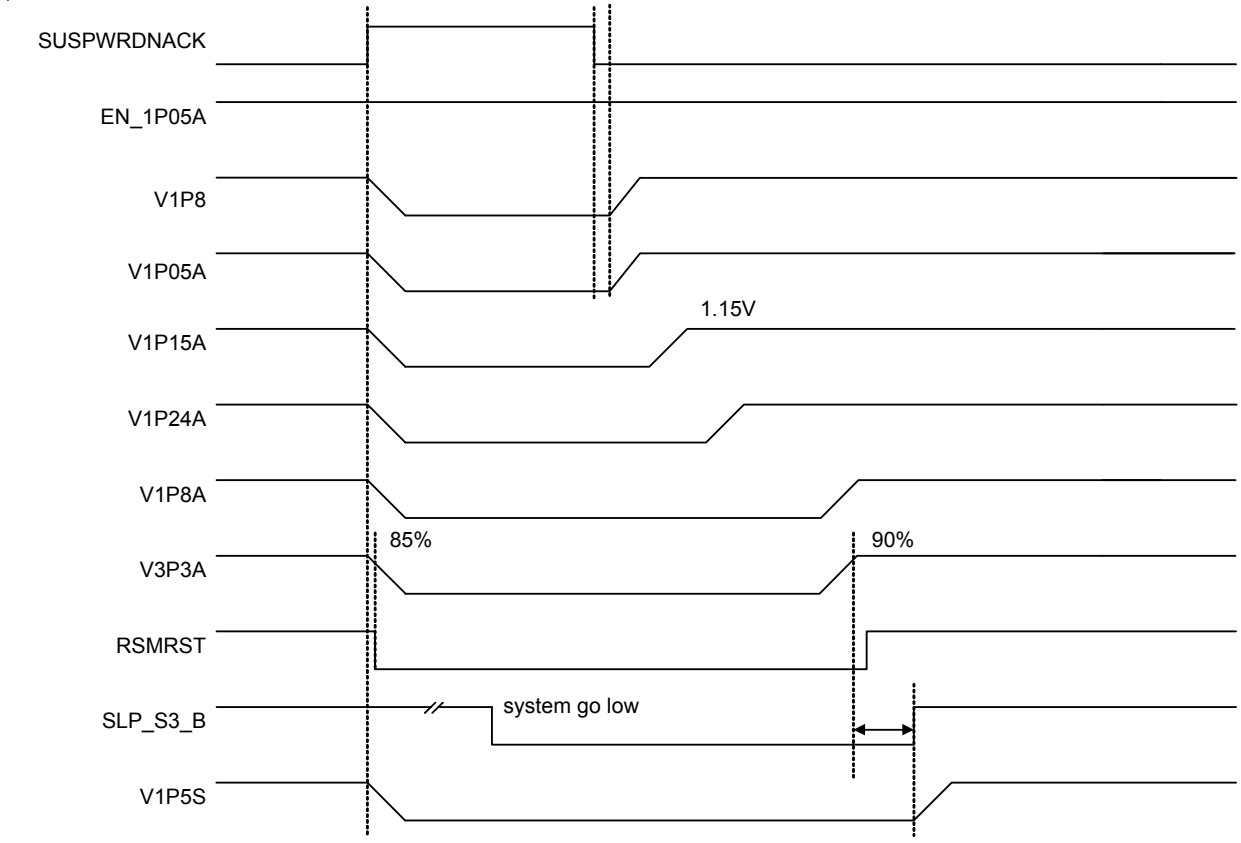


Figure 4. Power Off and Up Sequence with SUSPWRDNACK Going Low and then High

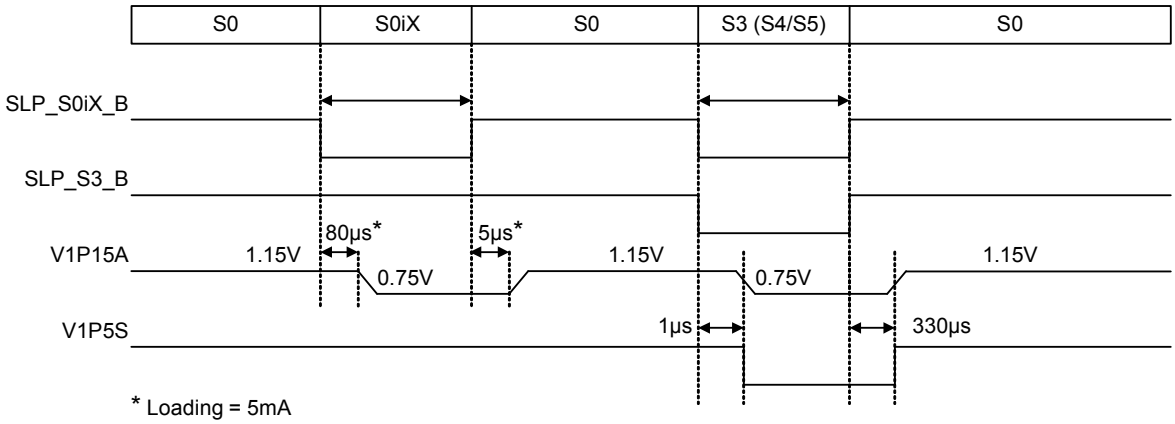


Figure 5. S0iX, S3 (S4/S5) Enter/Exit Sequence

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-28L 4x4 package, the thermal resistance, θ_{JA}, is 28.5°C/W on a standard four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (28.5°C/W) = 3.5W for WQFN-28L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

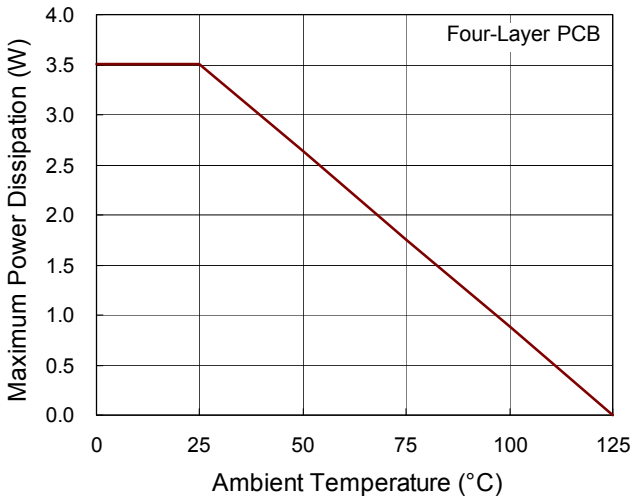


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout.

Power components should be placed on the same side of board, with power traces routed on the same layer. If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths and use multiple vias for interconnection. When vias are used to connect PCB layers in the high current loop, multiple vias should be used to minimize via impedance.

Certain points must be considered before starting a layout using the RT5041AB.

- Make the traces of the main current paths as short and wide as possible.
- Place input decoupling capacitors as close as possible as to IN_1P8 and IN_1P05A. This cap provide the instant current into this pin when the internal MOSFET switching. It is preferable to connect the decoupling capacitors directly to the pins without using vias.
- Place the inductors close LX_1P05A and LX_1P8 to minimize the radiation noise, and the copper area should be minimized. However, the copper area is provided a heat sink to the internal MOSFET. Don't make the area of the node small by using narrow traces, using wide and short traces instead.
- For feedback signals O_1P05A and O_1P8, the sensing point which detects the output voltage must be connected after output capacitor and keep the trace far away from the switching node or inductor. Place the feedback network as close to the chip as possible.
- Place the bypass capacitor close to IN_1P24A, IN_1P15A, IN_1P5S, IN_1P8A, and IN_3P3A.
- Place the filter capacitor close to O_1P24A, O_1P15A, O_1P5S, O_1P8A, and O_3P3A to minimize trace inductance.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.
- An example of PCB layout guide is shown in Figure 7 for reference.

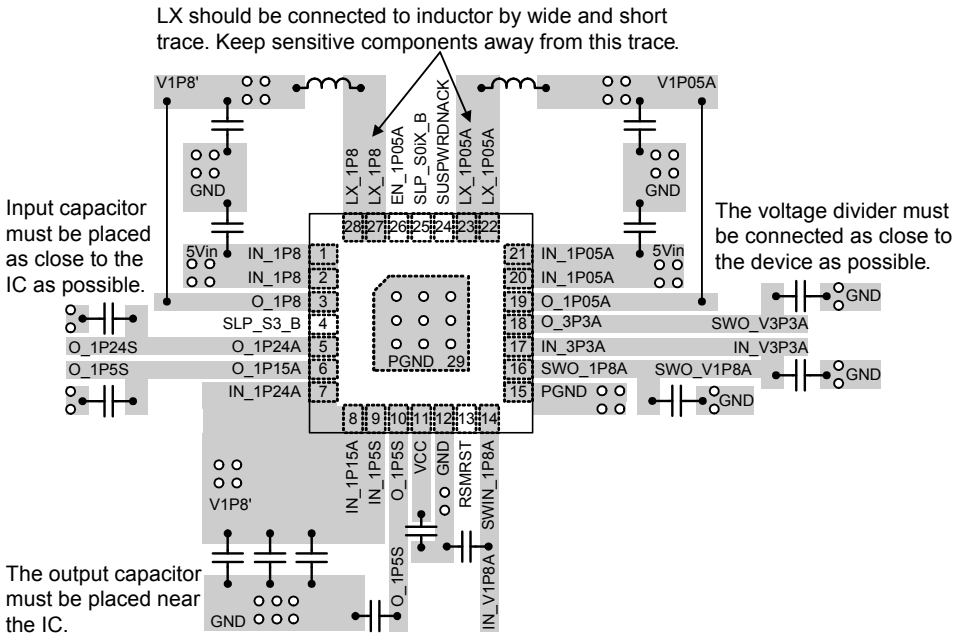
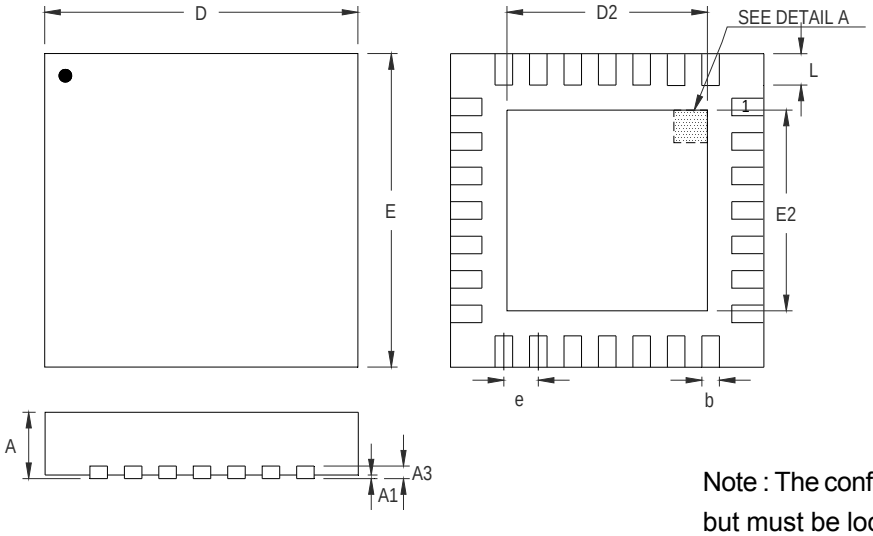
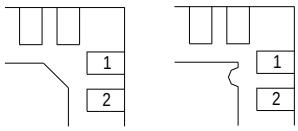


Figure 7. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.350	2.450	0.093	0.096
E	3.900	4.100	0.154	0.161
E2	2.350	2.450	0.093	0.096
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 28L QFN 4x4 Package

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