Power Management Units for INTEL APL Platform

General Description

The RT5074A is a Power Management Integrated Circuit (PMIC) which integrates 3 buck controllers (VNN, VCCGI, VDDQ), 3 buck converters (VCCRAM, V1P8A, V1P24A), 1 Switch (V1P8U/V1P8S) and 1 LDO (VTT) to make it a cost effective solution for Intel Apollolake (APL) platform.

The RT5074A is available in a WQFN-52L 6x6 small foot print package.

Applications

- Chrome Book and Tablet Computer

Ordering Information

RT5074A □□

Package Type
QW : WQFN-52L 6x6 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

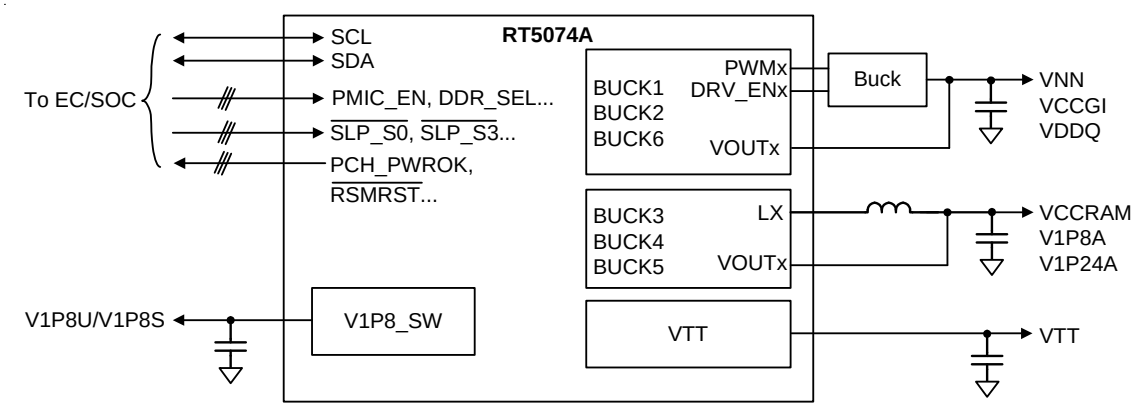
- **3-CH Buck Controller**
- **3-CH Buck Converters**
- **1-CH Switch**
- **1-CH VTT LDO**
- **I²C Slave Controller**
- **Interrupt Controller**
- **Internal Soft-Start to Reduce Inrush Current**
- **Integrated Sequencing Control for Apollolake**
- **Fast Transient Response**
- **Pure MLCC Cap Stable**
- **OVP, UVP, OCP for Buck Converter/Controller**
- **Support LPDDR3, DDR3L and LPDDR4**
- **Support S0iX State for Win8 Connected Standby or Android Mobile System**
- **Cost Effective 52-Lead WQFN Package**

Marking Information

RT5074AGQW : Product Number

YMDNN : Date Code

Simplified Application Circuit



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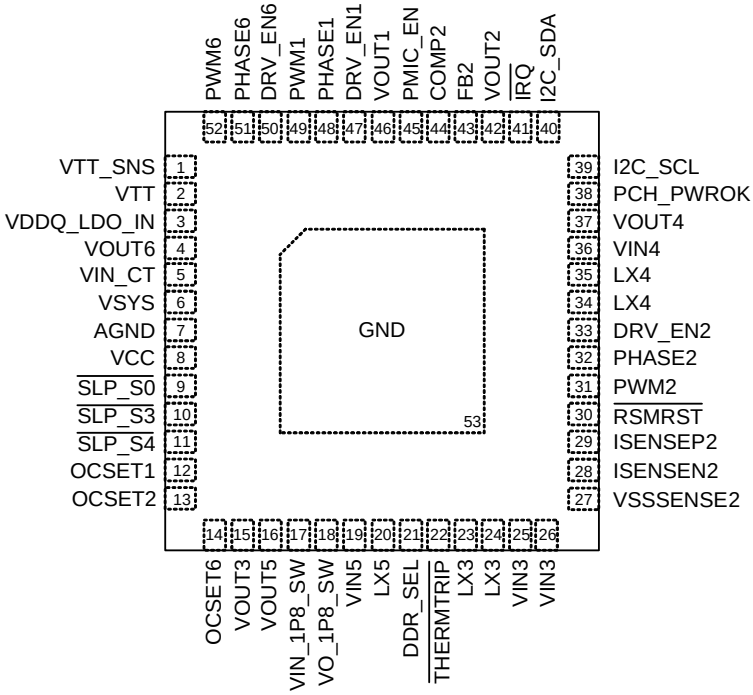
Pin Configuration

(TOP VIEW)



WQFN-52L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VTT_SNS	VTT feedback sense pin.
2	VTT	VTT output.
3	VDDQ_LDO_IN	VTT (VDDQ/2) input.
4	VOUT6	Buck6 (VDDQ) output feedback pin.
5	VIN_CT	On time setting pin. Connected this pin to V_{BATA}.
6	VSYS	System voltage detection. Connected this pin to V_{BATA}.
7	AGND	Analog ground.
8	VCC	VCC pin.
9	$\overline{\text{SLP_S0}}$	Power state pin.
10	$\overline{\text{SLP_S3}}$	Power state pin.
11	$\overline{\text{SLP_S4}}$	Power state pin.
12	OCSET1	Buck1 over-current setting pin. Connect a resistor from this pin to GND to set current limit threshold. Tie to VCC to disable buck 1.
13	OCSET2	Buck2 over-current setting pin. Connect a resistor from this pin to GND to set current limit threshold. Tie to VCC to disable buck 2.
14	OCSET6	Buck6 over-current setting pin. Connect a resistor from this pin to GND to set current limit threshold. Tie to VCC to disable buck 6.
15	VOUT3	Buck3 output voltage feedback pin.

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Pin No.	Pin Name	Pin Function
16	VOUT5	Buck5 output voltage feedback pin.
17	VIN_1P8_SW	Switch V1P8 input.
18	VO_1P8_SW	Switch V1P8 output.
19	VIN5	Buck5 power input.
20	LX5	Switch node for buck5 converter.
21	DDR_SEL	DDR voltage select pin.
22	$\overline{\text{THERMTRIP}}$	Thermal shutdown control input pin from SoC.
23, 24	LX3	Switch node for buck3 converter.
25, 26	VIN3	Buck3 power input.
27	VSSSENSE2	Remote GND of buck2.
28	ISENSEN2	Negative input pin of current sense of buck2.
29	ISENSEP2	Positive input pin of current sense of buck2.
30	$\overline{\text{RSMRST}}$	Always on rail power good signal.(Open Drain)
31	PWM2	PWM output of buck2 for external driver.
32	PHASE2	Switch node sense pin for buck2 controller.
33	DRV_EN2	Enable signal of buck2 for external driver.
34, 35	LX4	Switch node for buck4 converter.
36	VIN4	Buck4 (V1P8A) power input.
37	VOUT4	Buck4 (V1P8A) output feedback pin.
38	PCH_PWROK	Power good signal for all rail except buck2. (Open Drain)
39	I2C_SCL	I^2C clock pin.
40	I2C_SDA	I^2C data pin.
41	$\overline{\text{IRQ}}$	Interrupt pin. (Active low)
42	VOUT2	Buck2 (VCCGI) output voltage feedback pin.
43	FB2	Feedback pin of buck2.
44	COMP2	Comp pin of buck2.
45	PMIC_EN	Enable pin.
46	VOUT1	Buck1 output voltage feedback.
47	DRV_EN1	Enable signal of buck1 for external driver.
48	PHASE1	Switch node sense pin for buck1 controller.
49	PWM1	PWM output of buck1 for external driver.
50	DRV_EN6	Enable signal of buck6 for external driver.
51	PHASE6	Switch node sense pin for buck6 controller.
52	PWM6	PWM output of buck6 for external driver.
53 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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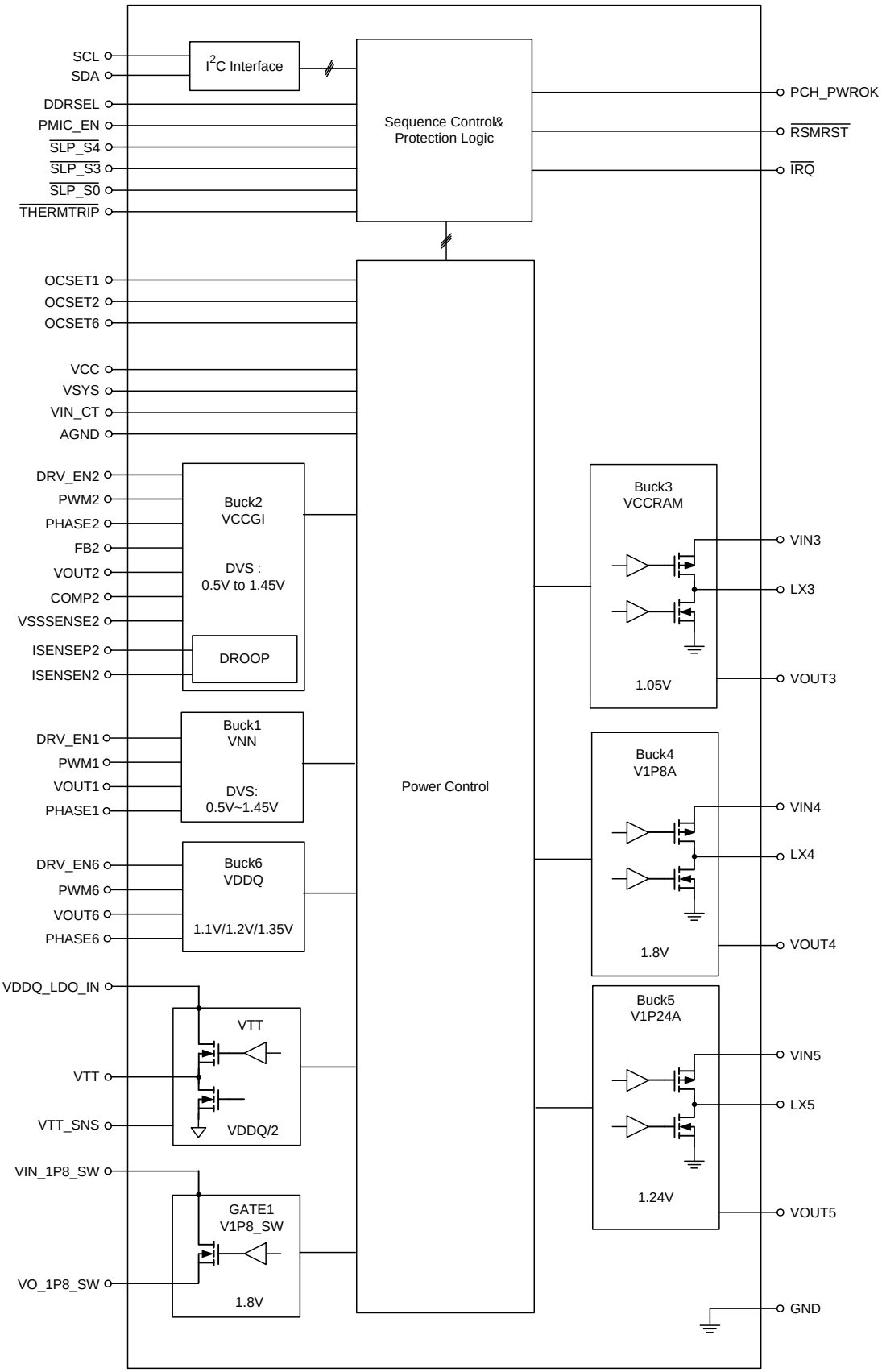
Functional Block Diagram



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Operation

The RT5074A is a PMIC (Power Management Integrated Circuit) and is an integral part of the Apollo Lake Platform focused on power solution integration to minimize system board area. It includes three DC to DC buck converters, three DC to DC buck controllers, one Linear Dropout regulators and one power switches.

Buck Converter

The three synchronous step-down buck converters with all integrated a P-channel high side MOSFET and a N-channel low-side MOSFET. The control scheme is based on current mode Constant-On-Time (COT) architecture, which has fast transient response and minimizes external components. The buck converters have a full set of protection (OCP / UVP / OVP).

Buck Controller

The three synchronous step-down buck controllers are pure controller without integrating driver of MOSFET. The buck1 and buck6 control scheme is based on Advanced Constant-On-Time (ACOT^{TM}) architecture, the buck2 is COMPCOT control scheme. which has fast transient response and minimizes external components. The buck controllers have a full set of protection (OCP / UVP / OVP).

Linear Dropout Regulator

The RT5074A includes one high performance linear dropout (LDO) regulators. The peak current rating is designed for short period current, not for thermal design current. The LDO contains an independent current-limit and under-voltage protection circuit to prevent unexpected applications. When the path current is over the current limit, the current limit circuit fixes the gate voltage to limit the output current. And if the output voltage is less than 60% of VOUT, the UVP circuit will shutdown all rails and latched. The way to cancel the latched behavior is to re-enable the RT5074A or re-give VCC power of the RT5074A.

Power Switch

There are one power switches :

V1P8U are N-channel power switch MOSFET. The power switch apply current-limit protection and under-voltage protection function. The current limit circuit prevents damage to the power switch MOSFET and backend device but can deliver load current up to the current limit threshold. And if the output voltage is less than the under-voltage threshold, the RT5074A will shutdowns all rails and latched. The way to cancel the latched behavior is to re-enable the RT5074A or re-give VCC power of the RT5074A.

Over-Temperature Protection

If the temperature of the RT5074A is over 150°C, the OTP circuit acts and makes all power rails shutdown and latched. The way to cancel the latched behavior is to re-enable the RT5074A or re-give VCC power of the RT5074A.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN_CT , VSYS ---------- –0.3V to 24V
- Supply Input Voltage , VCC to GND ---------- –0.3V to 6V
- AGND to GND ---------- –0.3V to 0.3V
- LX PIN , LX3 , LX4 , LX5
  DC ---------- –0.3V to 6.3V
  <50ns ---------- –2.5V to 9V
- PHASE PIN , PHASE1 , PHASE2 , PHASE6
  DC ---------- –0.3V to 24.3V
  <100ns ---------- –5V to 36V
- Others ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-52L 6x6 ---------- 3.77W
- Package Thermal Resistance (Note 2)
  WQFN-52L 6x6 , θ_{JA} ---------- 26.5°C/W
  WQFN-52L 6x6 , θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- Switch Input Voltage, VIN_1P8_SW ---------- 1.6V to (V_{CC} - 2)V
- VTT Input Voltage, VDD_LDO_IN ---------- 1V to 1.5V
- Supply Input Voltage, VIN_CT , VSYS ---------- 5V to 23V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, V_{SYS} = 7.4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PMIC						
Supply Voltage VCC						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{SHDN}	PMIC_EN = 0V	--	5	--	μA
	I_{VCC}	PMIC_EN = 2V, no switching $\overline{SLP_Sx}$ = 0V	--	0.65	--	mA

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VCC POR/UVLO Threshold							
POR Threshold		V_{CC_POR}		3.85	4.1	4.35	V
UVLO Threshold		V_{CC_UVLO}		3.55	3.8	4.05	V
Logic Threshold							
PMIC_EN/$\overline{SLP_S4}$ / $\overline{SLP_S3}$ / $\overline{SLP_S0}$ / $\overline{THERMTRIP}$ Input High Voltage		V_{EN_H}		1	--	--	V
PMIC_EN/$\overline{SLP_S4}$ / $\overline{SLP_S3}$ / $\overline{SLP_S0}$ / $\overline{THERMTRIP}$ Input Low Voltage		V_{EN_L}		--	--	0.4	V
PMIC_EN/$\overline{SLP_S4}$ / $\overline{SLP_S3}$ / $\overline{SLP_S0}$ Input Leakage Current		I_{EN_H}	V_{EN} = 2V	–1	0	1	μA
			V_{EN} = 0V	–1	0	1	μA
DDR_SEL Input Voltage	High Level	$V_{DDR_SEL_H}$		2.5	--	--	V
	Low Level	$V_{DDR_SEL_L}$		--	--	0.4	V
DDR_SEL Input Floating Level		$V_{DDR_SEL_Hi-Z}$	V_{CC} = 5V	1.3	--	1.9	V
Minimum VDDQ Turn on Delay		t_{VDDQ_RDY}	Min. delay from V1P8 ramp up to VDDQ start ramp up, DDR_SEL = Low or Floating	2.6	3.2	--	ms
V1P8 Turn off Delay Time		t_{1P8_FDY}	Delay time from SLP_S4_B go low to V1P8 turn off, DDR_SEL = Low or Floating	33	40	58	ms
VSYS UVLO							
UVLO Threshold		V_{SYS_UVLO}		--	2.5	--	V
VSYS POR Threshold		V_{SYS_POR}		--	2.7	--	V
Input Current		I_{VSYS}	V_{SYS} = 19V, V_{CC} = 5V	--	2	--	μA
			V_{SYS} = 8.4V, V_{CC} = 5V	--	0.9	--	μA
			VCC < VCC_UVLO	--	0	--	μA
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		T_{SD_HYS}		--	25	--	°C
Power Good Indicator							
$\overline{RSMRST}$ Go High Delay		$t_{\overline{RSMRST}_RDY}$	All of "A" rail ready to $\overline{RSMRST}$ high	12	16	--	ms
$\overline{RSMRST}$ Pull Low Voltage		$V_{\overline{RSMRST}_LOW}$	$I_{\overline{RSMRST}_LOW}$ = 10mA	--	--	0.13	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PCH_PWROK Go High Delay Default Value	$t_{PWROK_RDY_DFT}$	Typical PCH_PWROK go high Delay	80	100	120	ms
PCH_PWROK Pull Low Voltage	V_{PWROK_LOW}	I_{PWROK_LOW} = 10mA	--	--	0.3	V
$\overline{IRQ}$ Pull Low Voltage	$V_{\overline{IRQ}_LOW}$	I_{PWROK_LOW} = 10mA	--	--	0.3	V
Buck3 --- VCCRAM (1.05V, I_{MAX} = 3A)						
Supply Voltage						
Supply Voltage	V_{IN3}		3	--	5.5	V
Reference and Soft-Start						
Output Voltage Scaling			1.0395	1.05	1.0605	V
Soft-Start Time	t_{SS}	VCCRAM from 10% to 90%	--	0.85	--	ms
$R_{DS(ON)}$						
Switch On Resistance	$R_{DS(ON)_H}$		--	90	--	mΩ
Switch On Resistance	$R_{DS(ON)_L}$		--	60	--	mΩ
Current Limit						
Current Limit	I_{LIM}		4	5	--	A
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}		--	1.2	--	MHz
Minimum Off-Time	t_{OFF_MIN}		--	80	--	ns
Protections						
OVP Trip Threshold	V_{OVP}	OVP detect	--	135	--	%
OVP Propagation Delay	t_{OVPDLY}		--	5	--	µs
UVP Trip Threshold	V_{UVP}	UVP detect	--	60	--	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	µs
Discharge Resistance	R_{DIS}	BUCK3_DIS[1:0] = 00, Hi-Z	1.5	--	--	kΩ
		BUCK3_DIS[1:0] = 01	--	100	--	Ω
		BUCK3_DIS[1:0] = 10	--	200	--	Ω
		BUCK3_DIS[1:0] = 11	--	500	--	Ω

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Buck4 ---V1P8A (1.8V, I_{MAX} = 1.5A)						
Supply Voltage						
Supply Voltage	V_{IN4}		3	--	5.5	V
Reference and Soft-Start						
Output Voltage Default	V_{OUT}		1.782	1.8	1.818	V
Soft-Start Time	t_{SS}	V1P8A from 10% to 90%	--	0.75	--	ms
$R_{DS(ON)}$						
Switch On Resistance	$R_{DS(ON)_H}$		--	90	--	mΩ
Switch On Resistance	$R_{DS(ON)_L}$		--	60	--	mΩ
Current Limit						
Current Limit	I_{LIM}		4	5	--	A
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}		--	1.2	--	MHz
Minimum Off-Time	t_{OFF_MIN}		--	80	--	ns
Protections						
OVP Trip Threshold	V_{OVP}	OVP detect	--	135	--	%
OVP Propagation Delay	t_{OVPDLY}		--	5	--	µs
UVP Trip Threshold	V_{UVP}	UVP detect	--	60	--	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	µs
Discharge Resistance	R_{DIS}	BUCK4_DIS[1:0] = 00, Hi-Z	1.5	--	--	kΩ
		BUCK4_DIS[1:0] = 01	--	100	--	Ω
		BUCK4_DIS[1:0] = 10	--	200	--	Ω
		BUCK4_DIS[1:0] = 11	--	500	--	Ω
Buck5 V1P24A (1.24V, I_{MAX} = 1.5A)						
Supply Voltage						
Supply Voltage	V_{IN5}		3	--	5.5	V
Reference and Soft-Start						
Output Voltage Default	V_{OUT}		1.2276	1.24	1.2524	V
Soft-Start Time	t_{SS}	V1P24A from 10% to 90%	--	1	--	ms

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$R_{DS(ON)}$						
Switch On Resistance	$R_{DS(ON),H}$		--	120	--	mΩ
Switch On Resistance	$R_{DS(ON),L}$		--	80	--	mΩ
Current Limit						
Current Limit	I_{LIM}		2	3	--	A
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}		--	1.2	--	MHz
Minimum Off-Time	t_{OFF_MIN}		--	80	--	ns
Protections						
OVP Trip Threshold	V_{OVP}	OVP detect	--	135	--	%
OVP Propagation Delay	t_{OVPDLY}		--	5	--	µs
UVP Trip Threshold	V_{UVP}	UVP detect	--	60	--	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	µs
Discharge Resistance						
Discharge Resistance	R_{DIS}	BUCK5_DIS[1:0] = 00, Hi-Z	1.5	--	--	kΩ
		BUCK5_DIS[1:0] = 01	--	100	--	Ω
		BUCK5_DIS[1:0] = 10	--	200	--	Ω
		BUCK5_DIS[1:0] = 11	--	500	--	Ω
GATE1 ---V1P8_SW (1.8V, I_{MAX} = 500mA)						
Supply Voltage						
Supply Voltage			1.6	1.8	V_{CC} – 2V	V
ON-State Resistance and Soft-Start						
ON-State Resistance	$R_{DS(ON)}$	V_{IN} = 1.8V, I_{OUT} = 300mA	--	60	--	mΩ
Soft-Start Time	t_{SS}		--	0.3	--	ms
Dropout Voltage						
Dropout Voltage	V_{DROP}	I_{OUT} = 300mA	--	18	--	mV
Current Limit						
Current limit	I_{LIM}		0.7	1.2	--	A
Protections						
UVP Trip Threshold	V_{UVP}	UVP detect	--	60	--	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	µs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VTT LDO --- I_{MAX} = 500mA						
VTT Output Tolerance	V_{VTTTOL}	V_{DDQ} = $V_{DD_LDO_IN}$ = 1.1V/1.2V/1.35V, I_{VTT} = 0A	–20	--	20	mV
		V_{DDQ} = $V_{DD_LDO_IN}$ = 1.1V/1.2V/1.35V, I_{VTT} = 0.5A	–30	--	30	mV
		V_{DDQ} = $V_{DD_LDO_IN}$ = 1.1V/1.2V/1.35V, I_{VTT} = 1A	–30	--	30	mV
Current Limit						
VTT Source Current limit	I_{VTT_LIMsr}	VTT = 0V	--	1.6	--	A
VTT Sink Current limit	I_{VTT_LIMsk}	VTT = VDDQ	--	1.6	--	A
Leakage Current						
VTT Leakage Current	I_{VTTLK}	$\overline{SLP_S4}$ = 3.3V, $\overline{SLP_S3}$ = 0V, VTT = (V_{VDDQ}/2)	–10	--	10	µA
VTTSNS Leakage Current	$I_{VTTSNSLK}$	I_{SINK} = 1mA	–1	--	1	µA
Discharge Resistance						
Discharge Resistance	R_{DIS}	$\overline{SLP_S4}$ = 0V, $\overline{SLP_S3}$ = 0V	--	15	--	Ω
Buck6 ---VDDQ (1.1V, 1.2V, 1.35V Controller)						
Output Voltage	V_{OUT}	DDR_SEL = high	1.3365	1.35	1.3635	V
		DDR_SEL = low	1.188	1.2	1.212	
		DDR_SEL = floating	1.089	1.1	1.111	
Soft-Start Time	t_{SS}	VDDQ 10% to 90%	--	0.8	--	ms
Current Limit						
Current Limit Setting Current	I_{OCSET}		45	50	55	µA
Current Limit Setting Voltage	V_{OCSET}	I_{OCSET} x R_{OCSET}	0.4	--	3	V
Current Limit		GND – PHASE = V_{OCSET} / 12	–6	0	6	mV
Current Limit Temperature Coefficient			--	4700	--	ppm/°C
Switching Frequency and Minimum Off Timer						
Switching Frequency Accuracy	f_{SW}		510	600	690	kHz
Minimum Off-Time	t_{OFF_MIN}		--	400	--	ns
Minimum On-Time	t_{ON_MIN}		--	50	--	ns
Protections						
OVP Trip Threshold	V_{OVP}	OVP detect	--	135	--	%
OVP Propagation Delay	t_{OVPDLY}		--	5	--	µs
UVP Trip Threshold	V_{UVP}		--	60	--	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	µs
Zero Current Crossing Threshold	V_{PHASE_ZC}		–4	--	4	mV

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Discharge Resistance							
Discharge Resistance		R_{DIS}	BUCK6_DIS[1:0] = 00, Hi-Z	1.5	--	--	kΩ
			BUCK6_DIS[1:0] = 01	--	100	--	Ω
			BUCK6_DIS[1:0] = 10	--	200	--	Ω
			BUCK6_DIS[1:0] = 11	--	500	--	Ω
PWM Driving Capability							
PWM Source Resistor		R_{PWMsr}		--	30	--	Ω
PWM Sink Resistor		R_{PWMsk}		--	10	--	Ω
I^2C Interface							
SDA, SCL Input Voltage	High			--	---	1.2	V
	Low			0.6	--	--	
SDA, SCL Operate Frequency				--	--	1.2	MHz
Buck1 ---VNN (0.5V to 1.45V, Controller)							
Output Voltage Default		V_{OUT}		1.0395	1.05	1.0605	V
Output Voltage Accuracy		V_{OUT}	VID = 0.75V to 1.45V	–1%	--	1%	% of VID
			VID = 0.5V to 0.74V	–9	--	9	mV
DC Output Voltage Programmable Step		V_{STEP}		--	10	--	mV
Dynamic Voltage Scale Slew Rate		SR_{DVS}		2.5	3.125	--	mV/μs
Current Limit							
Current Limit Setting Current		I_{OCSET}		42.5	50	57.5	μA
Current Limit Setting Voltage		V_{OCSET}	$I_{OCSET} \times R_{OCSET}$	0.4	--	3	V
Current Limit			GND – PHASE = V_{OCSET} / 12	–6	0	6	mV
Current Limit Temperature Coefficient				--	4700	--	ppm/°C
Switching Frequency Accuracy		f_{SW}	V_{BUCK1_VID} = 1V	--	750	--	kHz
Minimum Off-Time		t_{OFF_MIN}		--	400	--	ns
Minimum On-Time		t_{ON_MIN}		--	50	--	ns

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protections						
OVP Trip Threshold	V_{OVP}	VID ≥ 0.8V	--	135	--	%
		VID < 0.8V	--	1.65	--	V
OVP Propagation Delay	t_{OVPDLY}		--	5	--	µs
UVP Trip Threshold	V_{UVP}	For VID from 0.5V to 1.45V	--	60	--	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	µs
Zero Current Crossing Threshold	V_{PHASE_ZC}		–4	--	4	mV
Discharge Resistance						
Discharge Resistance	R_{DIS}	BUCK1_DIS[1:0] = 00, Hi-Z	1.5	--	--	kΩ
		BUCK1_DIS[1:0] = 01	--	100	--	Ω
		BUCK1_DIS[1:0] = 10	--	200	--	Ω
		BUCK1_DIS[1:0] = 11	--	500	--	Ω
PWM Driving Capability						
PWM Source Resistor	R_{PWMsr}		--	30	--	Ω
PWM Sink Resistor	R_{PWMsk}		--	10	--	Ω
Buck2 ---VCCGI (0.5V to 1.45V, Controller)						
Output Voltage Default	V_{OUT}		0.99	1	1.01	V
Output Voltage Accuracy	V_{OUT}	VID = 0.75V to 1.45V	–1%	--	1%	% of VID
		VID = 0.5V to 0.74V	–9	--	9	mV
DC Output Voltage Programmable Step	V_{STEP}		--	10	--	mV
Dynamic Voltage Scale Slew Rate	SR_{DVS}		2.5	3.125	--	mV/µs
Current Limit						
Current Limit Setting Current	I_{OCSET}		42.5	50	57.5	µA
Current Limit Setting Voltage	V_{OCSET}	$I_{OCSET} \times R_{OCSET}$	0.4	--	3	V
Current Limit		GND – PHASE = V_{OCSET} / 12	–6	0	6	mV
Current Limit Temperature Coefficient			--	4700	--	ppm/°C
Switching Frequency Accuracy	f_{SW}	$V_{_BUCK1_VID}$=1V	--	750	--	kHz
Minimum Off-Time	t_{OFF_MIN}		--	400	--	ns
Minimum On-Time	t_{ON_MIN}		--	50	--	ns
Protections						
OVP Trip Threshold	V_{OVP}	VID ≥ 0.8V	--	135	--	%
		VID < 0.8V	--	1.65	--	V
OVP Propagation Delay	t_{OVPDLY}		--	5	--	µs
UVP Trip Threshold	V_{UVP}	UVP detect	--	60	--	%

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Propagation Delay	t_{UVPDLY}		--	5	--	μs
Zero Current Crossing Threshold	V_{PHASE_ZC}		−4	--	4	mV
Discharge Resistance						
Discharge Resistance	R_{DIS}	BUCK2_DIS[1:0] = 00, Hi-Z	1.5	--	--	kΩ
		BUCK2_DIS[1:0] = 01	--	100	--	Ω
		BUCK2_DIS[1:0] = 10	--	200	--	Ω
		BUCK2_DIS[1:0] = 11	--	500	--	Ω
PWM Driving Capability						
PWM Source Resistor	R_{PWMsr}		--	--	30	Ω
PWM Sink Resistor	R_{PWMsk}		--	--	10	Ω
Pin Disable Threshold (For Buck 3/4/5)						
VOUT Pin Disable Threshold	$V_{O_Dis_th}$	V_{CC} = 5V	3.9	4.2	--	V
Pin Disable Threshold (For Buck 1/2/6)						
Disable Threshold	OCSETx Pin	$V_{OCSET_Dis_th}$	V_{CC} = 5V	3.9	4.2	--	V

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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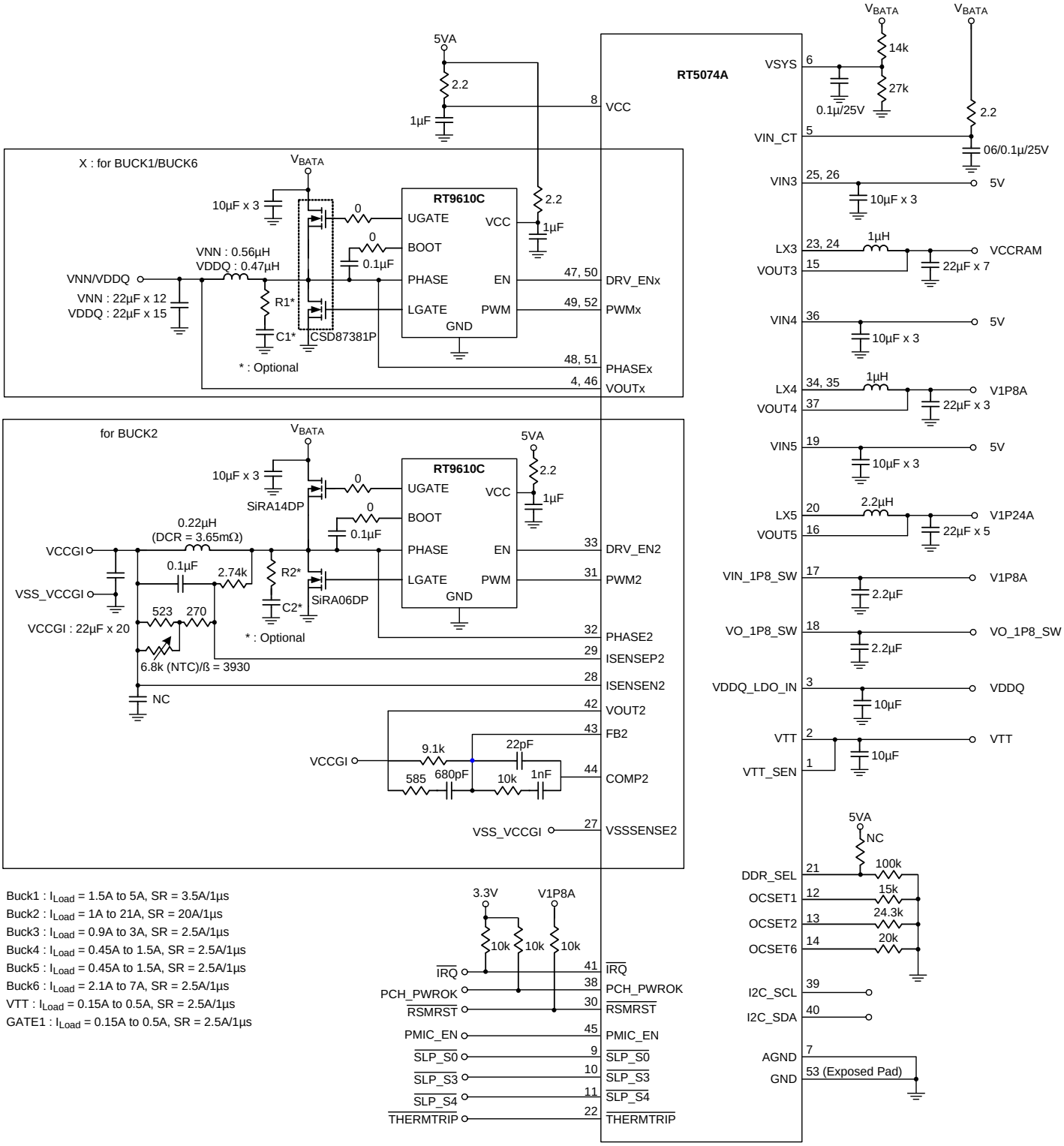
Typical Application Circuit



Buck1 : I_{Load} = 1.5A to 5A, SR = 3.5A/1µs
Buck2 : I_{Load} = 1A to 21A, SR = 20A/1µs
Buck3 : I_{Load} = 0.9A to 3A, SR = 2.5A/1µs
Buck4 : I_{Load} = 0.45A to 1.5A, SR = 2.5A/1µs
Buck5 : I_{Load} = 0.45A to 1.5A, SR = 2.5A/1µs
Buck6 : I_{Load} = 2.1A to 7A, SR = 2.5A/1µs
VTT : I_{Load} = 0.15A to 0.5A, SR = 2.5A/1µs
GATE1 : I_{Load} = 0.15A to 0.5A, SR = 2.5A/1µs

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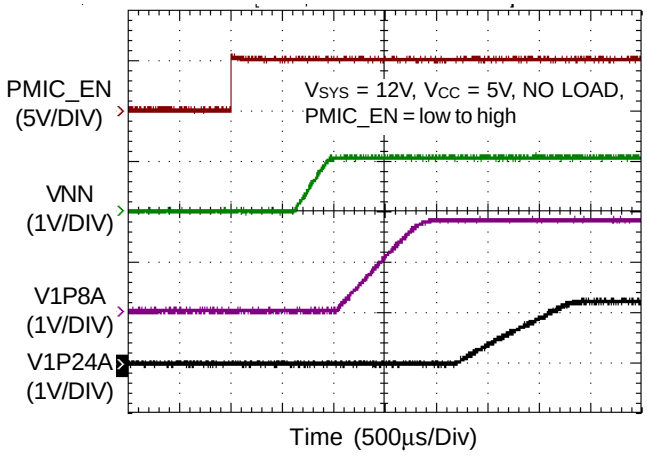
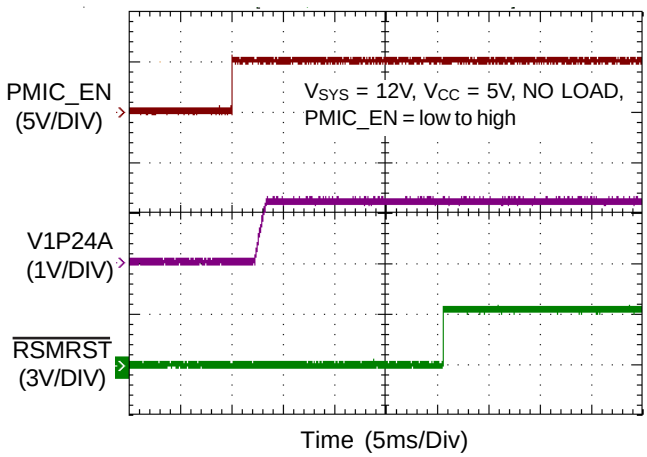
Typical Operating Characteristics

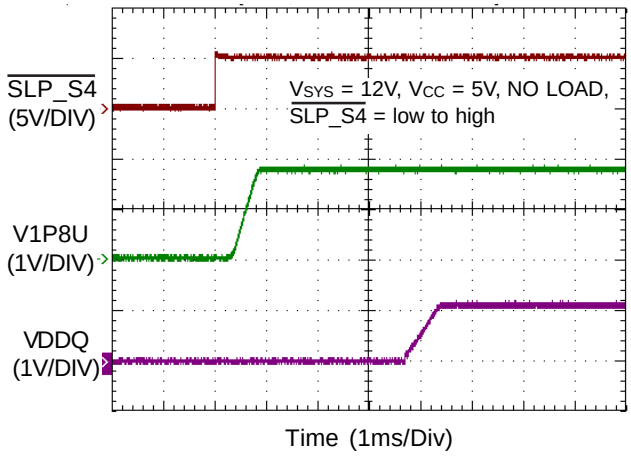
Power On from PMIC_EN to S4/S5



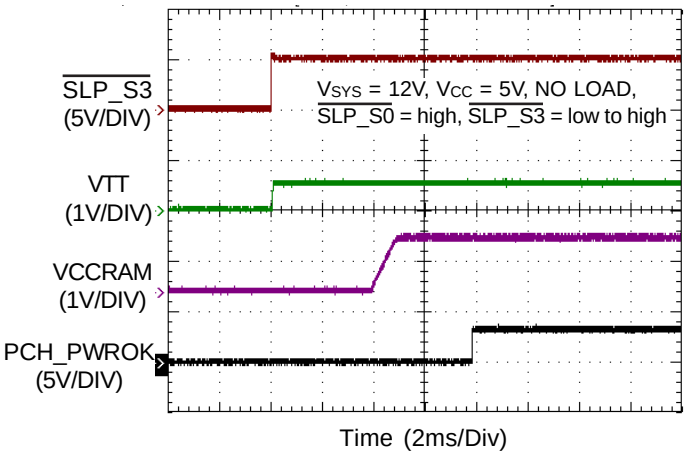
Power On from PMIC_EN to S4/S5



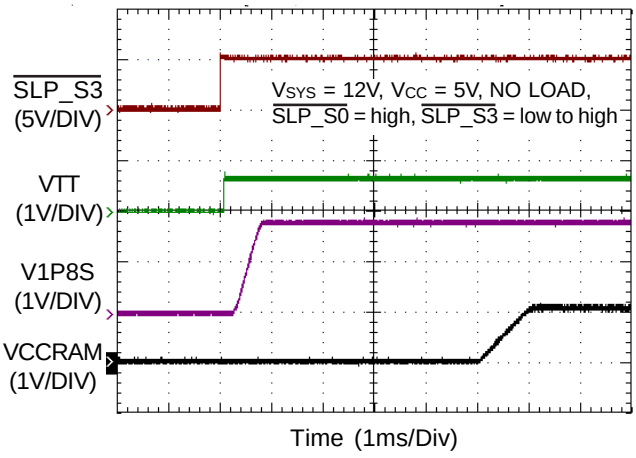
Power On from S4/S5 to S3



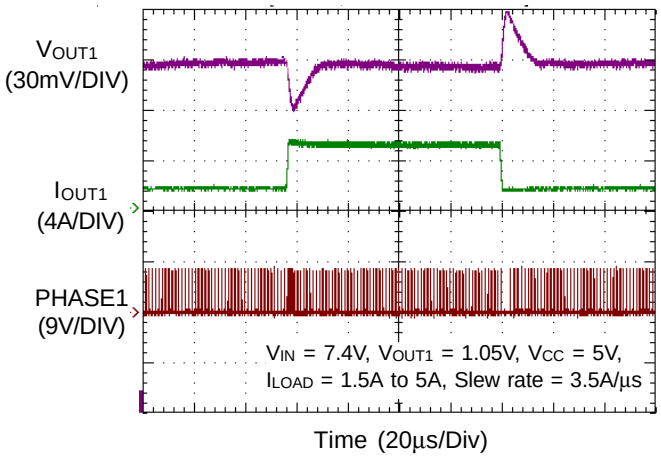
Power On from S3 to S0



Power On from S3 to S0



VNN Load Transient Response



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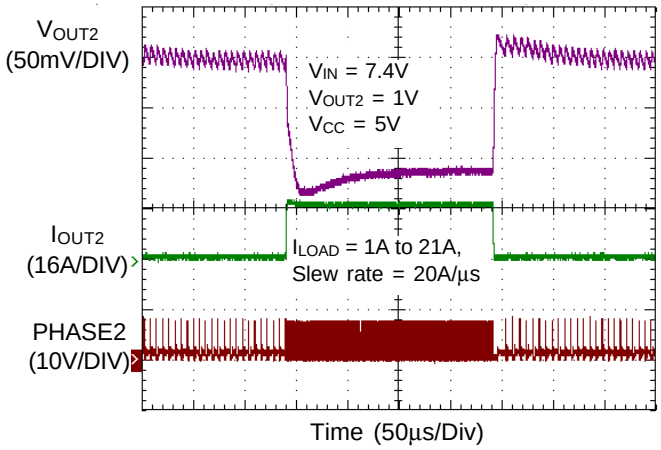
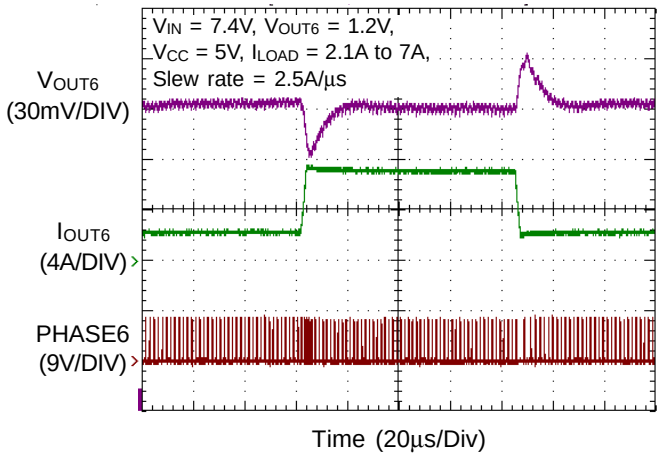
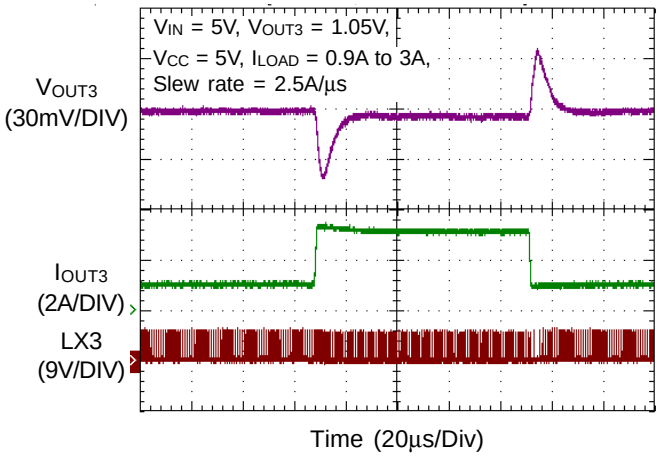
VCCGI Load Transient Response



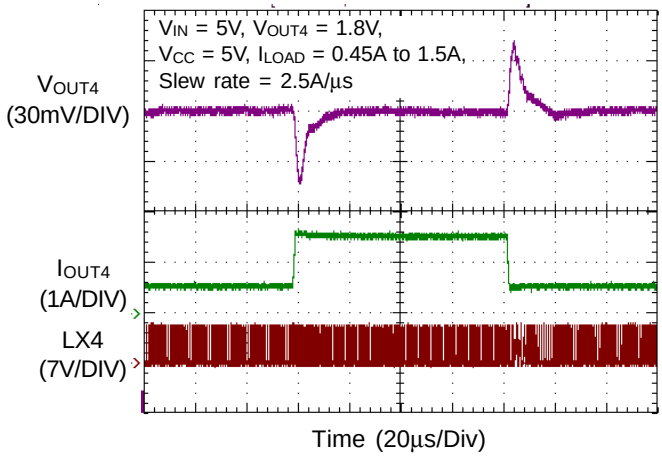
VDDQ Load Transient Response



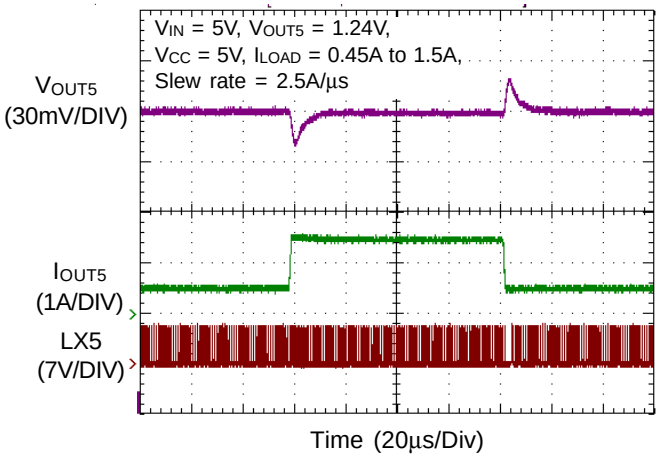
VCCRAM Load Transient Response



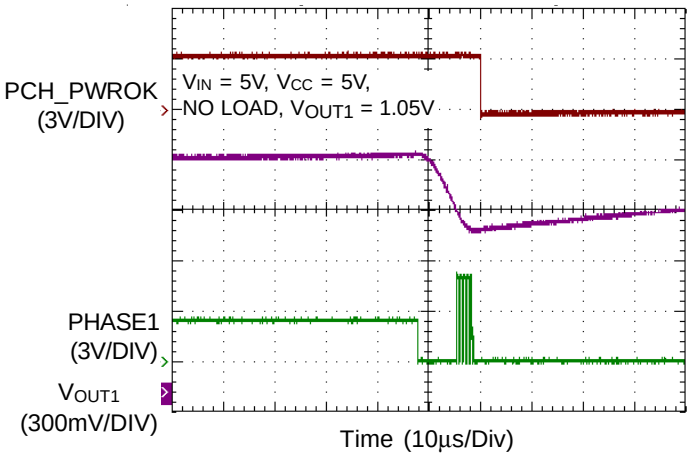
V1P8A Load Transient Response



V1P24A Load Transient Response



VNN Over-Voltage Protection



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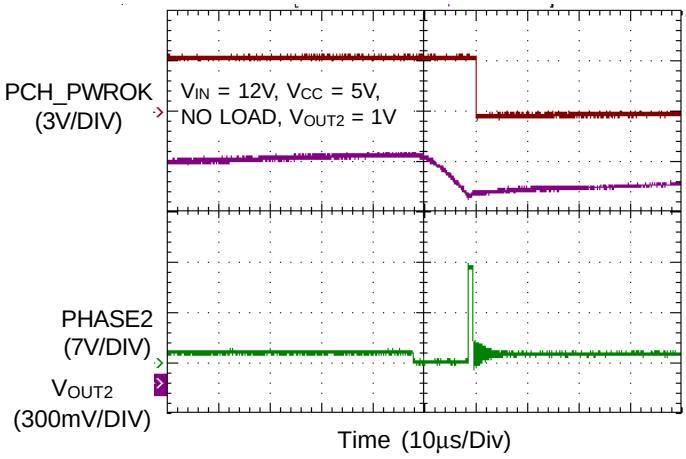
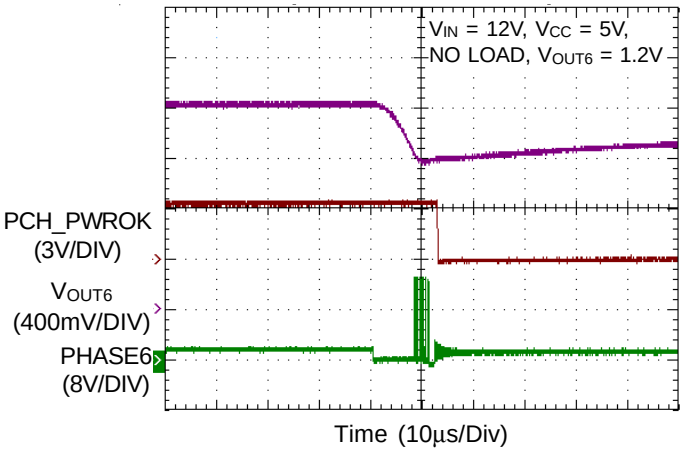
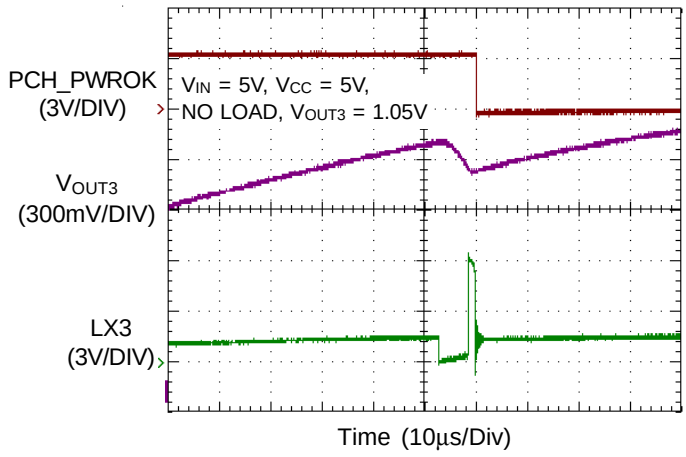
VCCGI Over-Voltage Protection



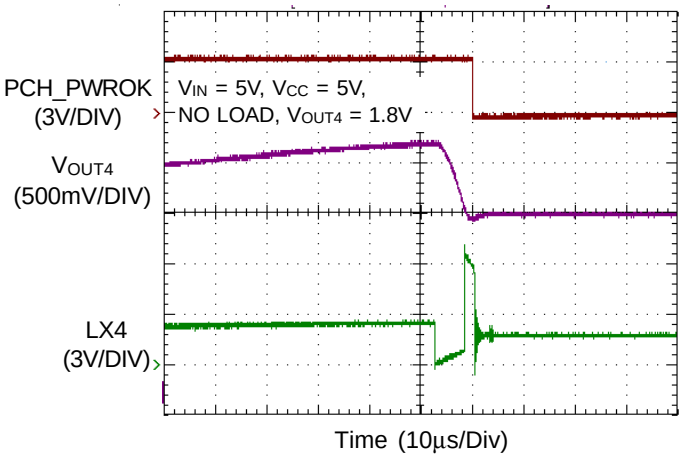
VDDQ Over-Voltage Protection



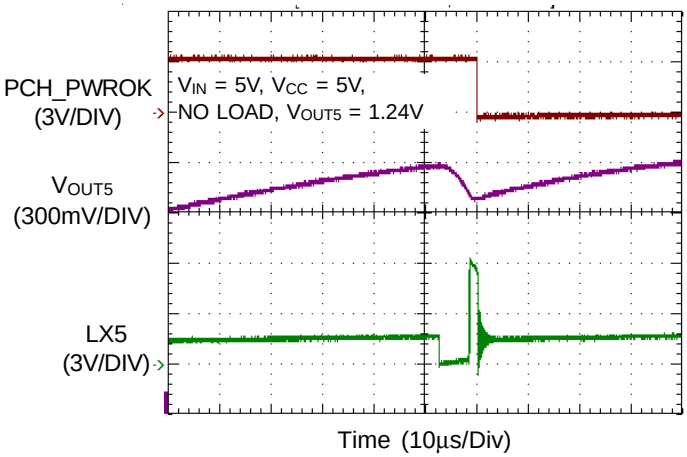
VCCRAM Over-Voltage Protection



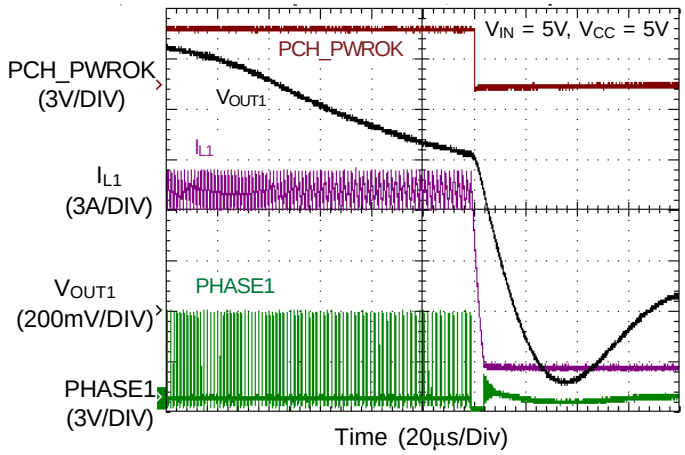
V1P8A Over-Voltage Protection



V1P24A Over-Voltage Protection



VNN Over-Current Limit



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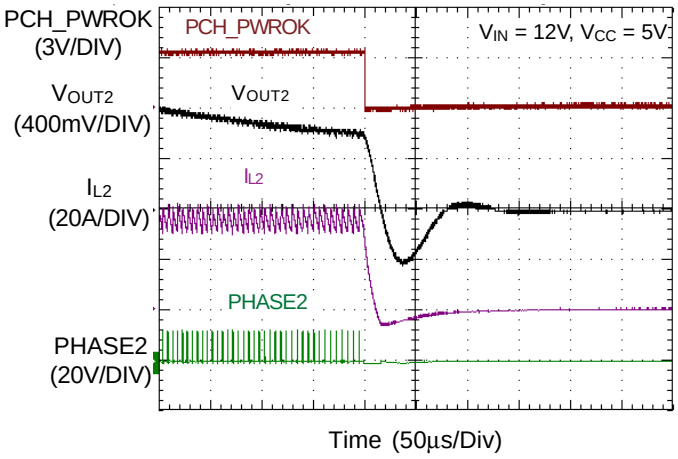
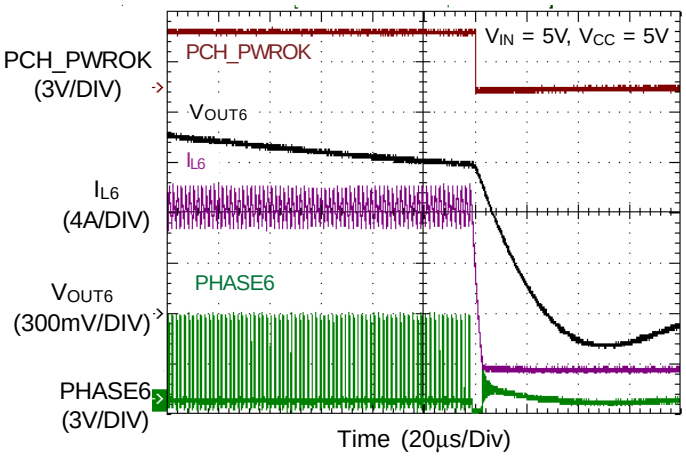
VCCGI Over-Current Limit



VDDQ Over-Current Limit



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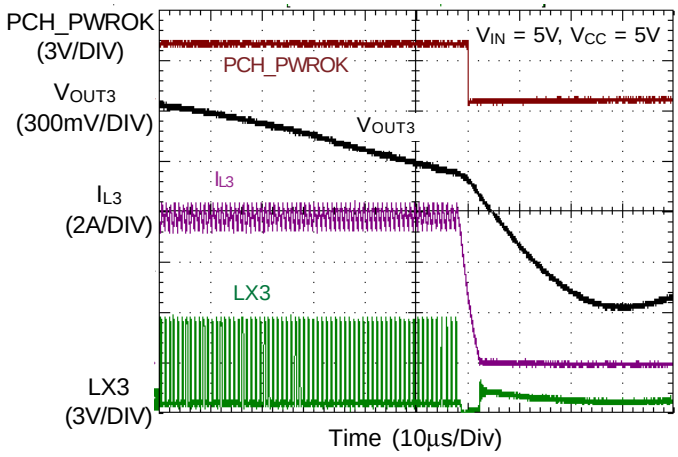
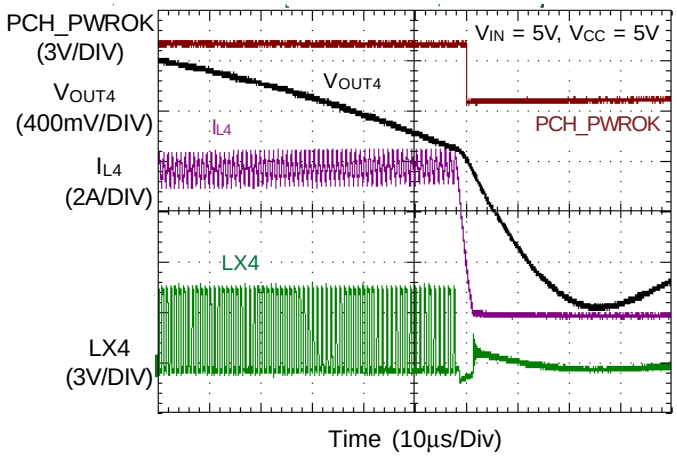
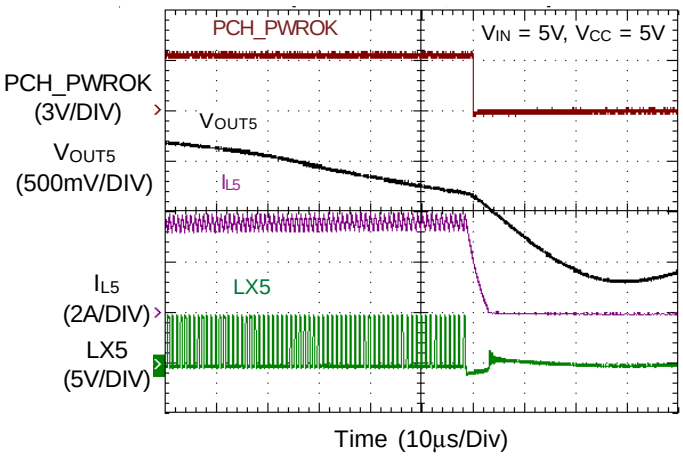


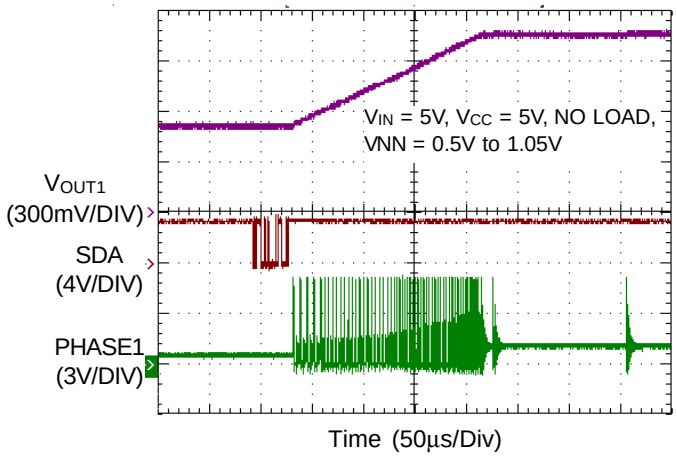
V1P8A Over-Current Limit



V1P24A Over-Current Limit



VNN DVID Up



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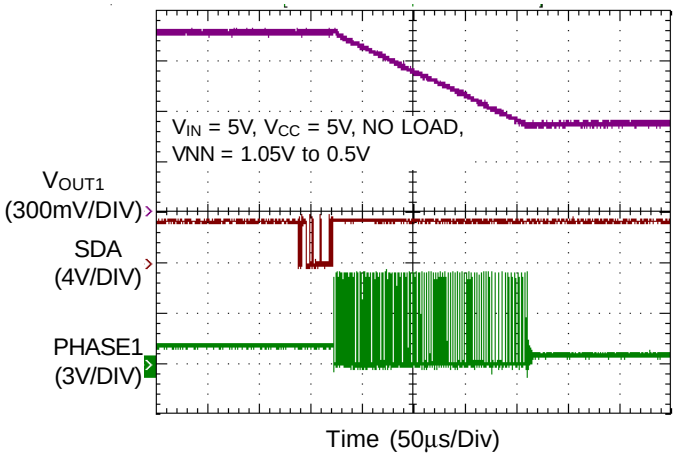
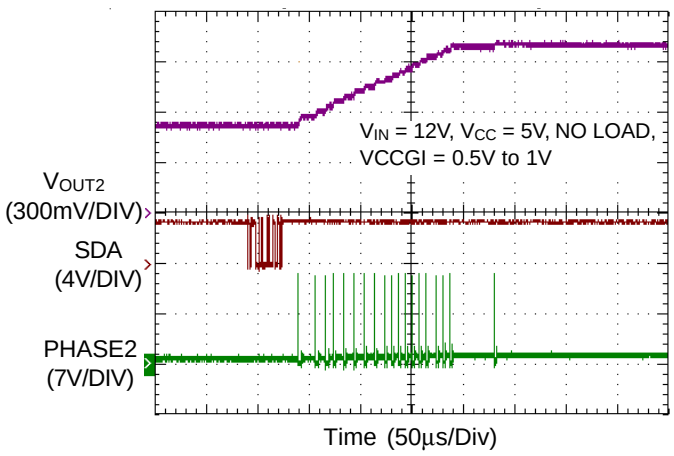
VNN DVID Down



VCCGI DVID Up



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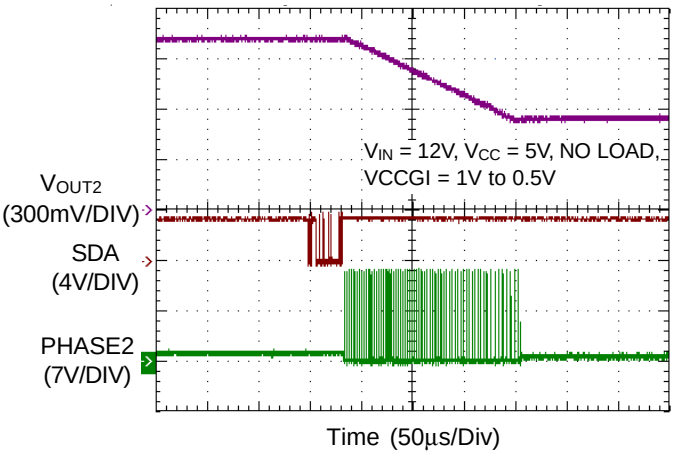
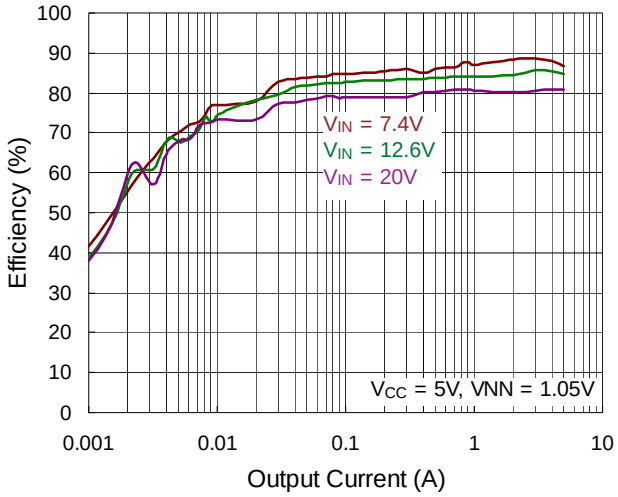
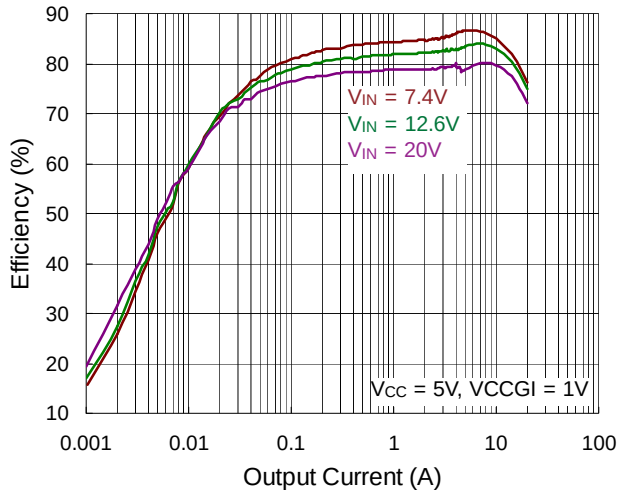


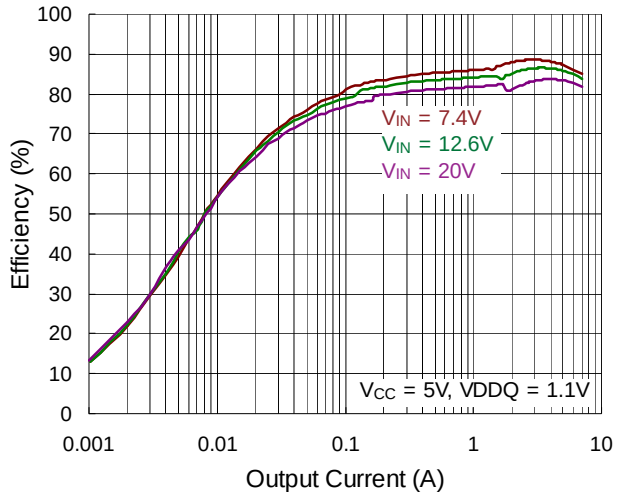
VNN Efficiency vs. Output Current



VCCGI Efficiency vs. Output Current



VDDQ Efficiency vs. Output Current



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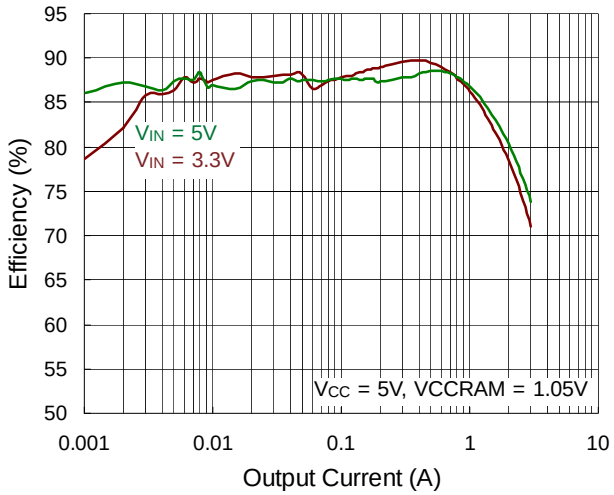
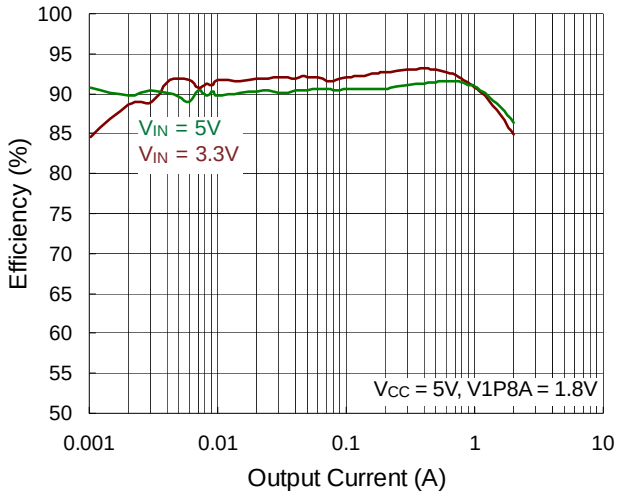
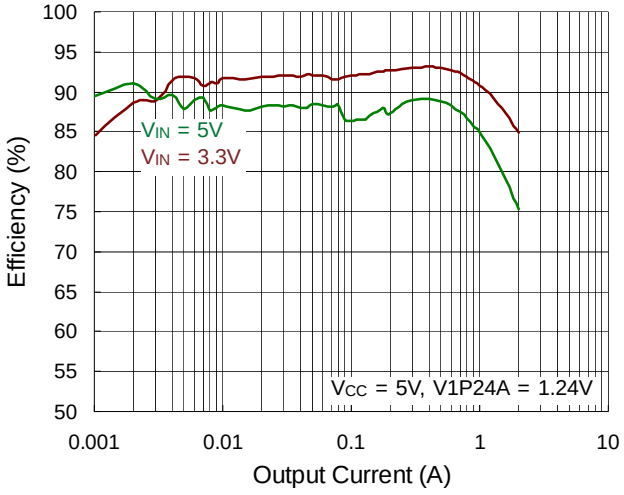
VCCRAM Efficiency vs. Output Current



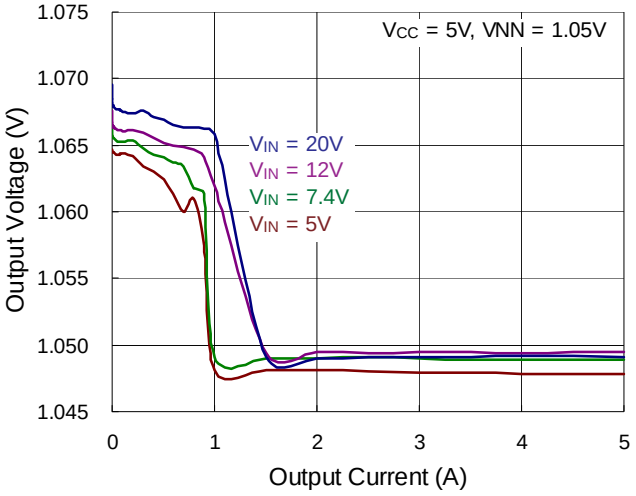
V1P8A Efficiency vs. Output Current



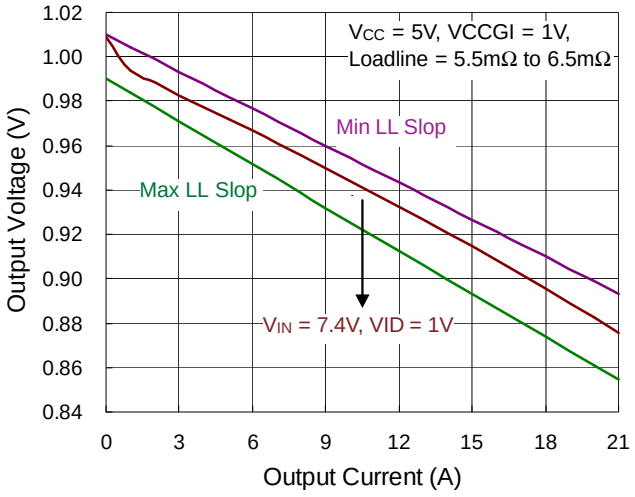
V1P24A Efficiency vs. Output Current



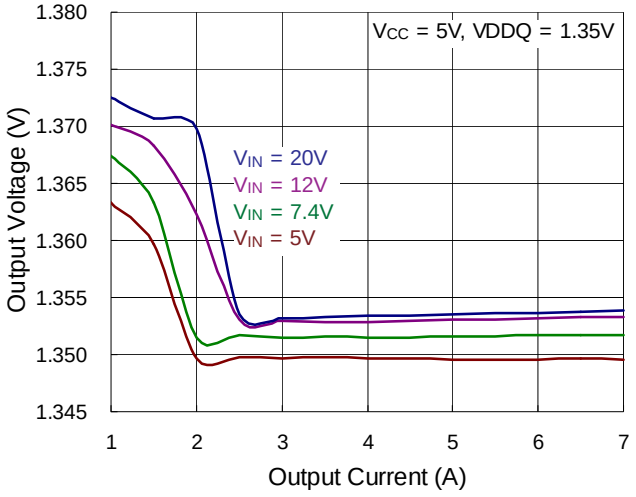
VNN Output Voltage vs. Output Current



VCCGI Output Voltage vs. Output Current



VDDQ Output Voltage vs. Output Current



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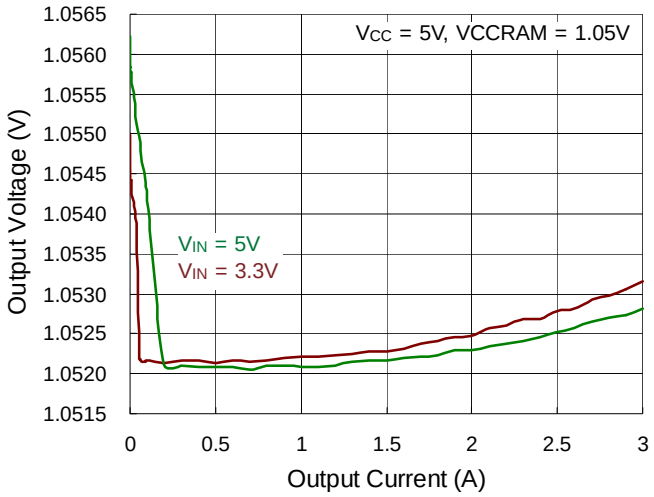
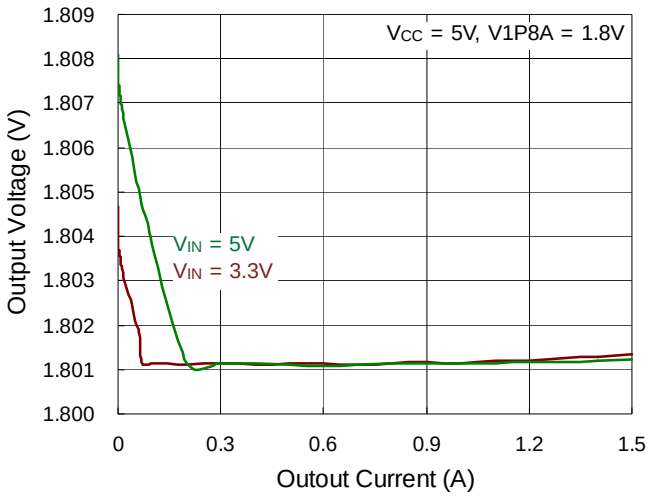
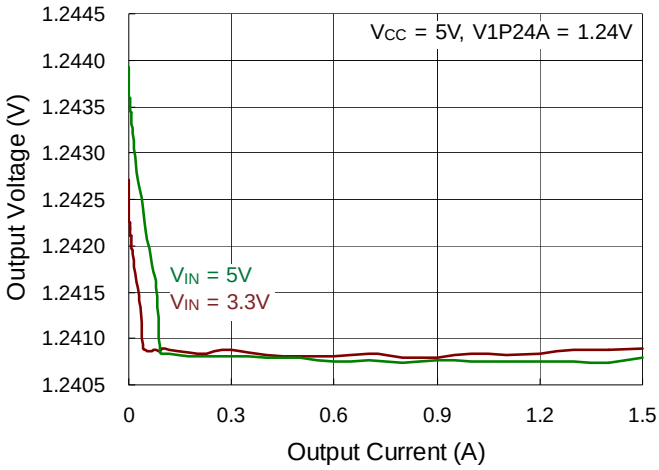
VCCRAM Output Voltage vs. Output Current



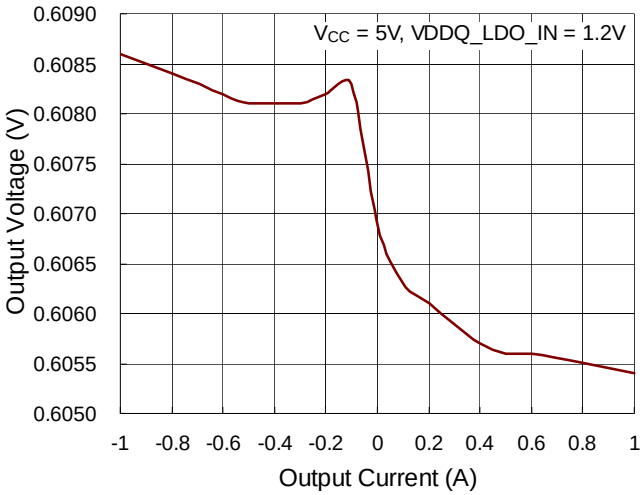
V1P8A Output Voltage vs. Output Current



V1P24A Output Voltage vs. Output Current



VTT Output Voltage vs. Output Current



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VID Register Table

Table 1. VID Table

0000000 = 0.00V	0100000 = 0.81V	1000000 = 1.13V	1100000 = 1.45V
0000001 = 0.50V	0100001 = 0.82V	1000001 = 1.14V	1100001 = RSVD
0000010 = 0.51V	0100010 = 0.83V	1000010 = 1.15V	1100010 = RSVD
0000011 = 0.52V	0100011 = 0.84V	1000011 = 1.16V	1100011 = RSVD
0000100 = 0.53V	0100100 = 0.85V	1000100 = 1.17V	1100100 = RSVD
0000101 = 0.54V	0100101 = 0.86V	1000101 = 1.18V	1100101 = RSVD
0000110 = 0.55V	0100110 = 0.87V	1000110 = 1.19V	1100110 = RSVD
0000111 = 0.56V	0100111 = 0.88V	1000111 = 1.20V	1100111 = RSVD
0001000 = 0.57V	0101000 = 0.89V	1001000 = 1.21V	1101000 = RSVD
0001001 = 0.58V	0101001 = 0.90V	1001001 = 1.22V	1101001 = RSVD
0001010 = 0.59V	0101010 = 0.91V	1001010 = 1.23V	1101010 = RSVD
0001011 = 0.60V	0101011 = 0.92V	1001011 = 1.24V	1101011 = RSVD
0001100 = 0.61V	0101100 = 0.93V	1001100 = 1.25V	1101100 = RSVD
0001101 = 0.62V	0101101 = 0.94V	1001101 = 1.26V	1101101 = RSVD
0001110 = 0.63V	0101110 = 0.95V	1001110 = 1.27V	1101110 = RSVD
0001111 = 0.64V	0101111 = 0.96V	1001111 = 1.28V	1101111 = RSVD
0010000 = 0.65V	0110000 = 0.97V	1010000 = 1.29V	1110000 = RSVD
0010001 = 0.66V	0110001 = 0.98V	1010001 = 1.30V	1110001 = RSVD
0010010 = 0.67V	0110010 = 0.99V	1010010 = 1.31V	1110010 = RSVD
0010011 = 0.68V	0110011 = 1.00V	1010011 = 1.32V	1110011 = RSVD
0010100 = 0.69V	0110100 = 1.01V	1010100 = 1.33V	1110100 = RSVD
0010101 = 0.70V	0110101 = 1.02V	1010101 = 1.34V	1110101 = RSVD
0010110 = 0.71V	0110110 = 1.03V	1010110 = 1.35V	1110110 = RSVD
0010111 = 0.72V	0110111 = 1.04V	1010111 = 1.36V	1110111 = RSVD
0011000 = 0.73V	0111000 = 1.05V	1011000 = 1.37V	1111000 = RSVD
0011001 = 0.74V	0111001 = 1.06V	1011001 = 1.38V	1111001 = RSVD
0011010 = 0.75V	0111010 = 1.07V	1011010 = 1.39V	1111010 = RSVD
0011011 = 0.76V	0111011 = 1.08V	1011011 = 1.40V	1111011 = RSVD
0011100 = 0.77V	0111100 = 1.09V	1011100 = 1.41V	1111100 = RSVD
0011101 = 0.78V	0111101 = 1.10V	1011101 = 1.42V	1111101 = RSVD
0011110 = 0.79V	0111110 = 1.11V	1011110 = 1.43V	1111110 = RSVD
0011111 = 0.80V	0111111 = 1.12V	1011111 = 1.44V	1111111 = RSVD

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Application Information

The RT5074A is a PMIC (Power Management Integrated Circuit) of the APL Platform focused on power solution integration to minimize system board area.

Power Path

The RT5074A is an integrated power solution for the APL platform. It includes three DC-DC Buck Controllers, three DC-DC Buck converters, one Linear Dropout regulators and one power switch. Expect System 3V/5V power, the RT5074A package the rest power paths into one.

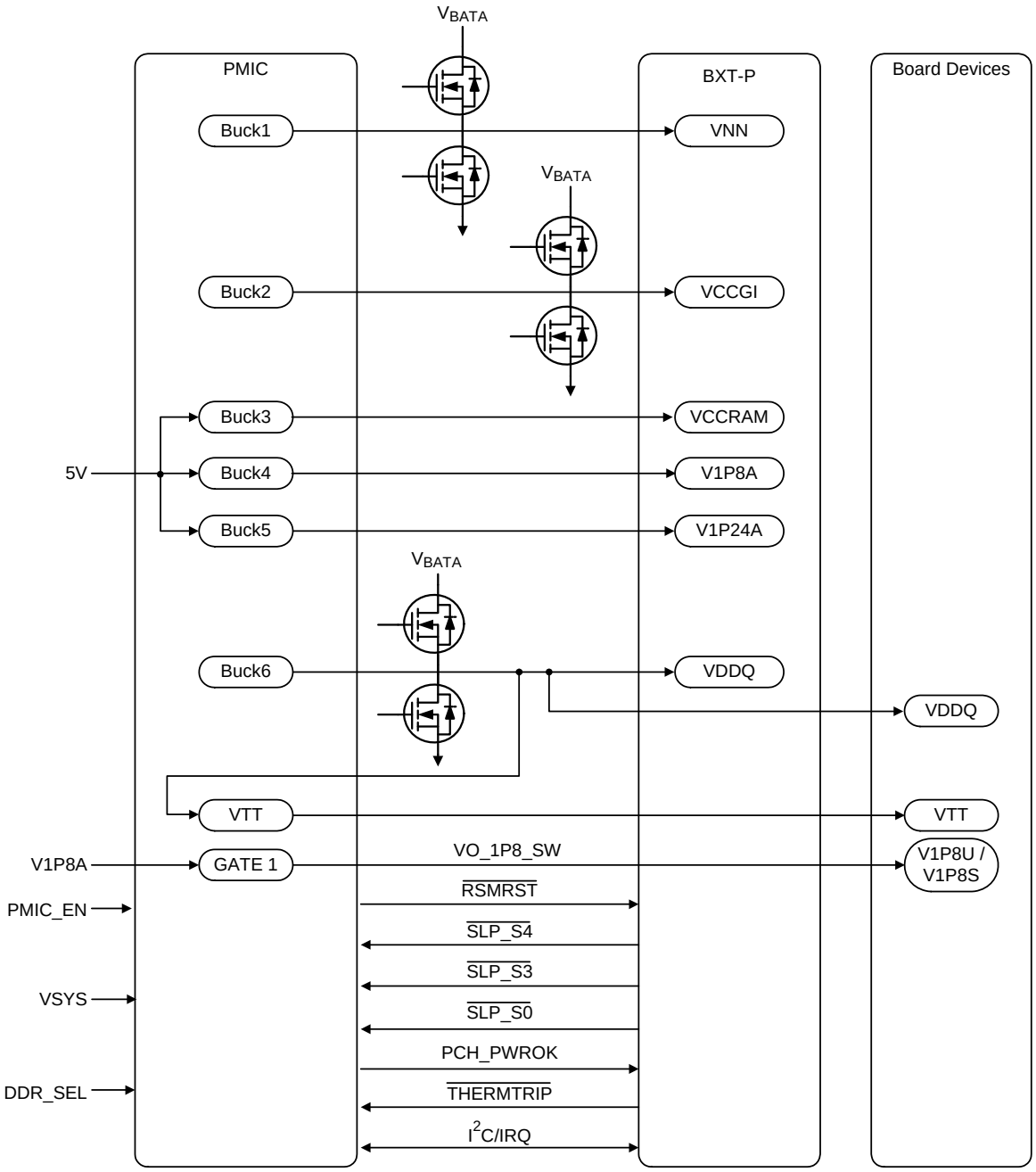

Figure 1. Simplified PMIC Power Map

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Buck Regulators

The RT5074A is a highly integrated multi-channel power management solution, including 3 step-down controllers and 3 step-down converters.

Buck 1 and Buck 6 of the RT5074A are high-performance controllers, the control scheme is based on an Advanced Constant On-Time (ACOT™) control architecture that provides stable operation for ceramic output capacitors without complicated external compensation, among other benefits. In ACOT™ architecture, it measures real switching frequency from phase pin and modifies on-time through a feedback loop to keep switching frequency constant. Furthermore, in order to get good stability with using low-ESR multi-layer ceramic capacitors (MLCC), internal circuitry creates a virtual inductor current ramp (work at switching frequency) to replace traditional ramp sensed from ESR resistance of output capacitor. So, it could improve stability and reduce jitter and variation with ACOT™ topology.

VCCGI Regulator

COMPCOT Control Scheme

The Buck2 adopt COMPCOT control scheme, which is a Flexible Constant On Time (F-COT™) with TYPE III compensator. It is a fixed frequency constant on time topology.

For stability when using pure MLCC in output capacitor, ramp compensation is necessary. In order to obtain further excellent noise immunity for jitter, increase the slope of ramp but it will bring about double poles with high Q(Quality factor) in low frequency and that is bound to attack load transient performance(with ring back and poor undershoot). So a TYPE III compensator is adopted to improve load transient performance.

Figure 2 is the COMPCOT control scheme.In order to strengthen load transient response, the COMPCOT scheme comparison V_{COMP} and V_{tON} to determine on time.

The Figure 3 shows the COMPCOT behavior in load transient.

Figure 3(a) shows the behavior of COMPCOT control scheme. In steady state, when V_{COMP} is reached V_{OUT}, that will generates PWM begin, and the end of PWM is depending on V_{tON} reached V_{COMP}. When load step up, V_{COMP} will thrown up, V_{tON} reach V_{COMP} delayed that will bring about PWM on time larger to improve undershoot. Figure 3(b) shows load step down behavior. When load step down, the PWM on time will smaller to improved overshoot. With the control scheme will improved greatly load transient performance.

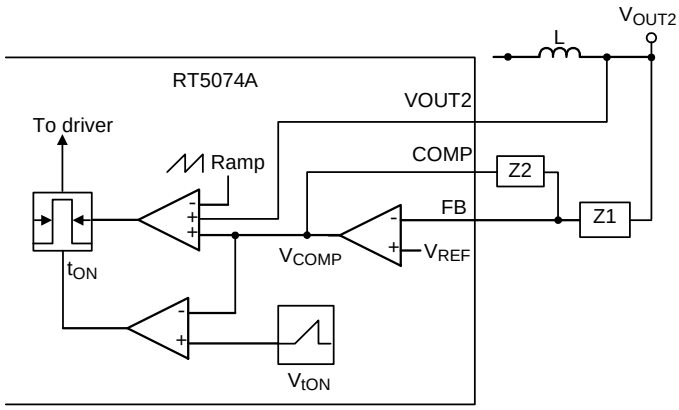

Figure 2. COMPCOT Control Scheme Circuit

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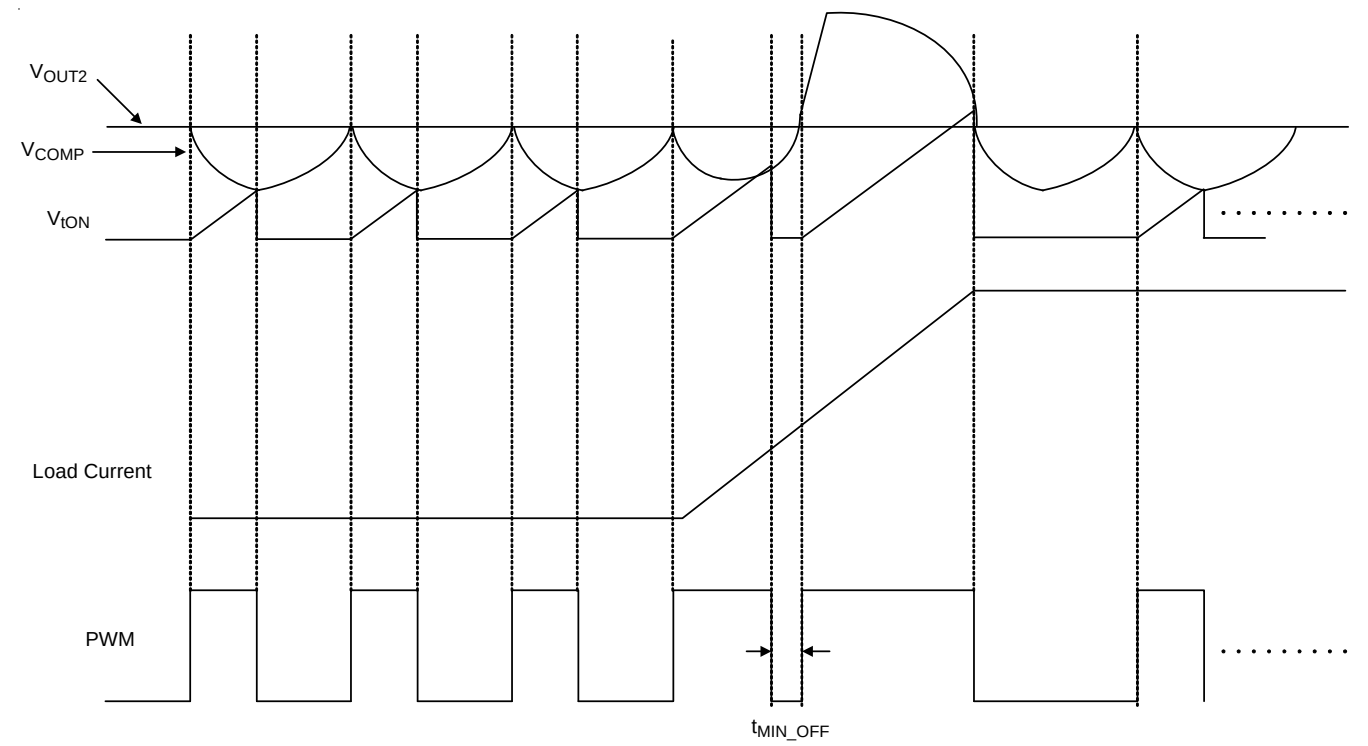

Figure 3(a). COMPCOT Behavior Waveforms in Load Step Up

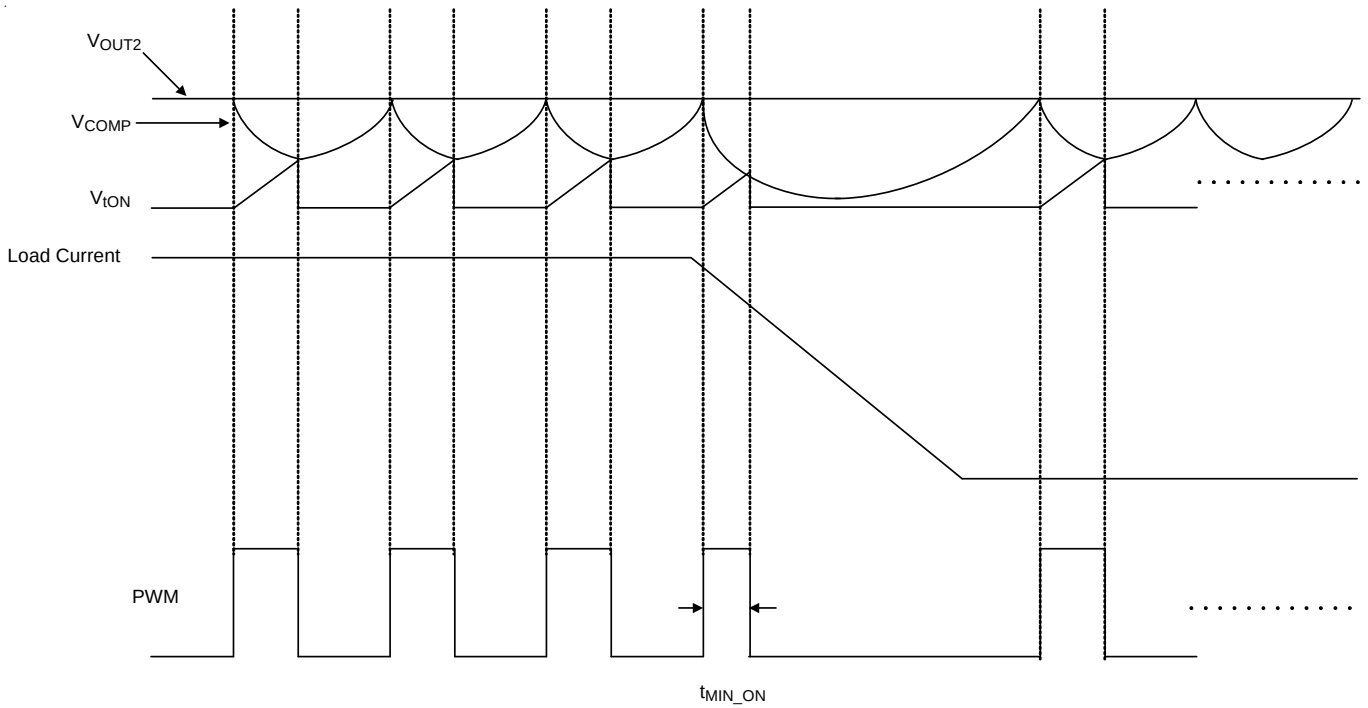

Figure3 (b). COMPCOT Behavior Waveforms in Load Step Down

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TYPE III Compensator

Due to one pair of double pole local at low frequency, a TYPE III compensator is adopted. The TYPE III compensator can bring 2 zeros, 3poles that can compensate loop gain. The TYPE III compensator is shown as Figure 4.

For TYPE III compensator calculation, Richtek provide design tool for customer in order to simplify design.

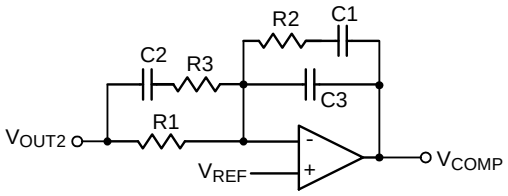

Figure 4. TYPE III Compensator

Droop Setting and Thermal Compensation

The Buck2 also provide droop setting via DCR network as Figure 5.

But due to the cooper wire of inductor has a positive temperature coefficient.

And hence, temperature compensation is necessary for the lossless inductor current sense. For thermal compensation, an NTC Thermistor is put in the current sense network and it can be used to compensation DCR variation due to temperature is changed.

The DCR network equation is as follows :

$$V_{ISENSEP2-ISENSEN2} = I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \times \frac{1 + \frac{L}{DCR}s}{1 + \frac{R_X \times R_{EQ} \times C}{R_X + R_{EQ}}s}$$

Let $R_{EQ} = R_S + \frac{R_P \times R_{NTC}}{R_P + R_{NTC}}$

According to current sense network, the corresponding equation is represented as follows :

$$\frac{L}{DCR} = \frac{R_X \times R_{EQ} \times C}{R_X + R_{EQ}},$$

$$\text{then } V_{ISENSEP2-ISENSEN2} = I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}}$$

If DCR network time constant matches inductor time constant, L/DCR, an expected load transient waveform can be designed.

The droop set equation as follows :

$$V_{DROOP} = \left(I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \right) \times 8$$

$$R_{DCLL} = \frac{V_{DROOP}}{I_L} = DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \times 8$$

Where, 8 is internal parameter of the RT5074A.

For detail DCR network calculation, Richtek provide design for customer in order to simplify design.

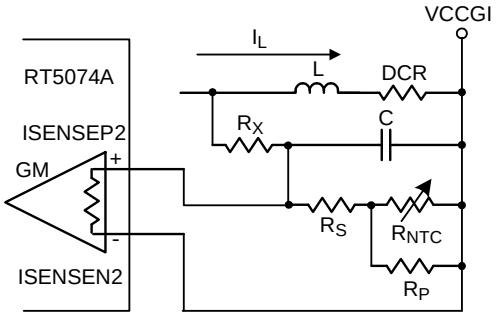

Figure 5. DCR Sense Circuit and Thermal Compensation

For Buck3, Buck4 and Buck5 of the RT5074A, the control scheme is based on current mode constant-on-time (COT) architecture, which has fast transient response and minimizes external components. Based on the internal current ramp information, it also can used multi-layer ceramic capacitors as the output capacitors without high-ESR bulk or virtual ESR network required for the loop stability.

With I^2C interface, Buck regulators can program output voltage, change the discharge resistance, VID slew down or decay down and control the on/off state. Even PWM can switch to forced PWM mode or auto pulse skip mode.

All the Buck controllers and converters of the RT5074A applies Power-Saving feature by automatic enabling diode emulation mode (DEM) as load decrease.

Buck Enable and Disable

Buck1 to Buck6 can be enabled or disabled through pin strapping. At PMIC_EN rising edge, the RT5074A detects whether the voltages of OCSETx pins for Buck1, 2 and 6 and VOUTx pins for Buck 3, 4 and 5 are higher than "VCC – 0.8V" respectively to decide which buck should be active. For example, by connecting OCSET1 pin and VOUT4 pin to VCC, the buck1 and Buck4 are disabled. When the

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bucks are disabled, the power good of the bucks are masked (high) and the system sequences as expected.

Buck6 (VDDQ) Voltage Selection

The output voltage of Buck6 can be set by DDR_SEL pin at the rising edge of PMIC_EN. If DDR_SEL pin is pulled below 0.4V, the output voltage of Buck6 will set to be 1.2V. If DDR_SEL pin is pulled up > 2.5V, the output voltage of Buck6 will set to be 1.35V. If the DDR_SEL pin is floating, the output voltage of Buck 6 will set to be 1.1V. In order to specification VOUT6, a 10kΩ resistance is connected from internal FB to GND. So we can' t use VOUT6 to resistor divider.

Table 2. Buck6 Voltage selection

DDR_SEL Pin State	Buck6 Nominal Output Voltage	DDR Technology
H	1.35V	DDR3L
Floating	1.1V	LPDDR4
L	1.2V	LPDDR3

Buck Over-Current Limit

The OCP is implemented using a cycle-by-cycle "valley" current detected control circuit, Figure 6 The switch current is monitored by measuring the low-side voltage between the LX/PHASE pin and GND. The voltage is proportional to the switch current and the on-resistance of the low-side MOSFET.

When high-side MOSFET turn-on (t_{ON}), the high-side switch current increases at a linear rate and determines by V_{IN}, V_{OUT}, t_{ON} and inductance. And when low-side MOSFET turn-on (t_{OFF}), the low-side switch current decreases linearly. The average value of the switch current is the output load curre nt. If the sensing voltage of the low-side MOSFET is above the voltage proportional to the current limit, the converter keeps the low-side turn on until the sensing voltage falls below the voltage proportional to the current limit threshold and start a new switching cycle.

For Buck1, Buck2 and Buck6, current limit threshold can be set by a resistor (R_{OCSET}) between OCSETx pin and GND. Once VCC exceeds the POR threshold and chip is enabled, an internal current source I_{OCSET} flows through R_{OCSET}. The voltage across R_{OCSET} is the current-limit protection threshold V_{OCSET}. R_{OCSET} can be determined using the following Equation (1).

$$R_{OCSET} = \frac{(R_{LG,DS(ON)} \times I_{VALLEY}) \times 12}{I_{OCSET}} \quad (1)$$

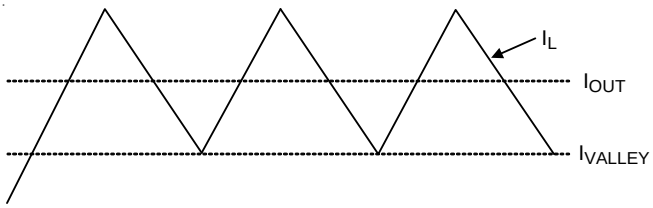

Figure 6. Cycle-By-Cycle "Valley" Current Detected Control

Where I_{VALLEY} represents the desired inductor limit current (valley inductor current) and I_{OCSET} is current limit setting current (50μA) which has a temperature coefficient to compensate the temperature dependency of the $R_{LG, DS(ON)}$.

For Buck3, Buck 4 and Buck5, the low-side MOSFET are embedded and current limit threshold has defined in electrical characteristics.

Negative Current Limit

The RT5074A supports cycle-by-cycle negative current limiting. If negative inductor current is rising to trigger negative current limit, the low-side MOSFET will be turned off and the current will flow to input side through the body diode of the high-side MOSFET. At this time, output voltage tends to rise or the DVID down slew rate tends to decrease because this protection limits current to discharge the output capacitor. In order to prevent shutdown because of over-voltage protection, the low-side MOSFET is turned on again 400ns after it is turned off. If the device hits the negative current limit threshold again before output voltage is discharged to the target level, the low-side MOSFET is turned off and process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output is discharged to the target level before negative current threshold is reached, the low-side MOSFET is turned off, the high-side MOSFET is then turned on, and the device keeps normal operation.

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Buck Under-Voltage Protection

When the over-current limit is active, the output voltage falls. If the output voltage falls under 60% of the reference voltage, the UVP comparator signal goes high and an internal UVP counter start to count. If the counted timing is over the UVP deglitch time, the high-side and low-side MOSFET will turn off and latched. The RT5074A is latched once UVP is triggered and can only be released by toggling enable or cycling VCC.

Buck Over-Voltage Protection

When the output voltage exceeds 135% of the reference voltage, the OVP comparator signal goes high and an internal OVP counter start to count. If the counted timing is over the OVP deglitch time, the low-side MOSFET will continue to turn on 10μs to discharge the output capacitor then the high-side and low-side MOSFET will turn off and latched. The RT5074A is latched once OVP is triggered and can only be released by toggling enable or cycling VCC.

Buck Over-Temperature Protection

The over-temperature protection function of the RT5074A is built inside the PMIC to prevent overheat damage. If the die temperature is over 150°C, the OTP circuit acts and makes all power rails of RT5074A shutdown. They recover back with power-up sequence when the temperature is low to 125°C.

VTT Regulator

The RT5074A includes one high performance linear dropout regulators(VTT). The VTT of the RT5074A have soft-start function. An internal current source charges an internal capacitor to make the soft-start ramp voltage. When VTT power up, the output voltage will track the internal ramp voltage during soft-start interval to prevent inrush current.

When PMIC_EN signals go low to let VTT shutdown mode occur, or the output under-voltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

The VTT contains an independent current-limit and under-voltage protection circuit to prevent unexpected applications. The current limit circuit monitors the current of the path from input to output by a current sensing circuit and controls the path transistor's gate voltage. When the path current is over the current limit, the current limit circuit fixes the gate voltage to limit the output current. And if the output voltage is less than 60% of VOUT, the UVP circuit will shut down the VTT and latched. Re-enable the RT5074A device to disable the latched status.

Power Switch

There is also power switch within the RT5074A. SW_V1P8 is a N-Channel power switch MOSFET (60mΩ) with an internal charge pump designed to provide the gate drive. Power switch of the RT5074A have soft-start function, too. An internal current source charges an internal capacitor to make the soft-start ramp voltage. When power switch turn on, the output voltage will track the internal ramp voltage during soft-start interval to prevent inrush current.

When PMIC_EN or $\overline{\text{SLP_SX}}$ goes low to let power switch shutdown mode occur, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND. The switch also apply current-limit protection and under-voltage protection function. The current limit circuitry prevents damage to the power switch MOSFET and the backend device but can deliver load current up to the current limit threshold.

Interrupt ($\overline{\text{IRQ}}$ pin)

If any interrupt event defined in interrupt status register occurs, related bits or flags are set to 1 and the RT5074A will pull $\overline{\text{IRQ}}$ pin low. When master received the Interrupt by $\overline{\text{IRQ}}$ pin pulled to low, master will perform an I^2C read cycle to read the interrupt status register and figure out the interrupt event which caused the interrupt and service it.

These bits or flags are only cleared by software writing a 1 to the appropriate bit locations and the RT5074A will reset the $\overline{\text{IRQ}}$ to high.

$\overline{\text{THERMTRIP}}$ Emergency Shutdown

PMIC shall support an emergency shutdown sequence at the assertion of the $\overline{\text{THERMTRIP}}$ (H to L) signal from the SoC. The PMIC is to take the following actions at the

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assertion of $\overline{\text{THERMTRIP}}$:

1. Immediately assert $\overline{\text{RSMRST}}$
2. Immediately de-assert PCH_PWROK
3. Shuts down all regulators and power gates after the assertion of $\overline{\text{RSMRST}}$ and de-assertion of PCH_PWROK.

PMIC Sequencing

Power-Up Sequence

During start-up, the RT5074A will detect the voltage input pins : VCC, VSYS pins. When VCC > 4.1V, VSYS > 2.7V, the RT5074A will recognize the power state of system to be ready.

The power on sequence will be :

1. PMIC_EN signal asserted.
2. VNN→1.05V, V1P8A→1.8V , V1P24A→1.24V.
3. 18ms delay.
4. $\overline{\text{RSMRST}}$ power good signal goes high.
5. $\overline{\text{SLP_S4}}$ signal asserted.
6. If DDR_SEL = Low or Floating, SW_V1P8 → 1.8V, VDDQ →1.2V or 1.1V
7. $\overline{\text{SLP_S3}}$ signal asserted, if DDR_SEL = High, SW_V1P8→1.8V, VDDQ→1.35V.
8. $\overline{\text{SLP_S0}}$ signal asserted.
9. VTT→ VDDQ/2, VCCRAM→1.05V
10. PCH_PWROK power good signals go high.
11. Set VCCGI VID → BOOT VID.

Important Notes :

1. When the PMIC is first enabled, $\overline{\text{SLP_S4}}$ and $\overline{\text{SLP_S3}}$ are to be treated as if they are low (actual state of signal ignored) until the de-assertion of $\overline{\text{RSMRST}}$. The PMIC must honor the state of $\overline{\text{SLP_S4}}$ and $\overline{\text{SLP_S3}}$ after the de-assertion of $\overline{\text{RSMRST}}$.
2. When the PMIC is first enabled, $\overline{\text{SLP_S0}}$ is to be treated as if it is high (actual state of signal ignored) until the first assertion of PCH_PWROK. The PMIC must honor the state of $\overline{\text{SLP_S0}}$ in all power states after the first assertion of PCH_PWROK.
3. $\overline{\text{THERMTRIP}}$ is to be treated as if it is high (ignored) until the de-assertion of $\overline{\text{RSMRST}}$.

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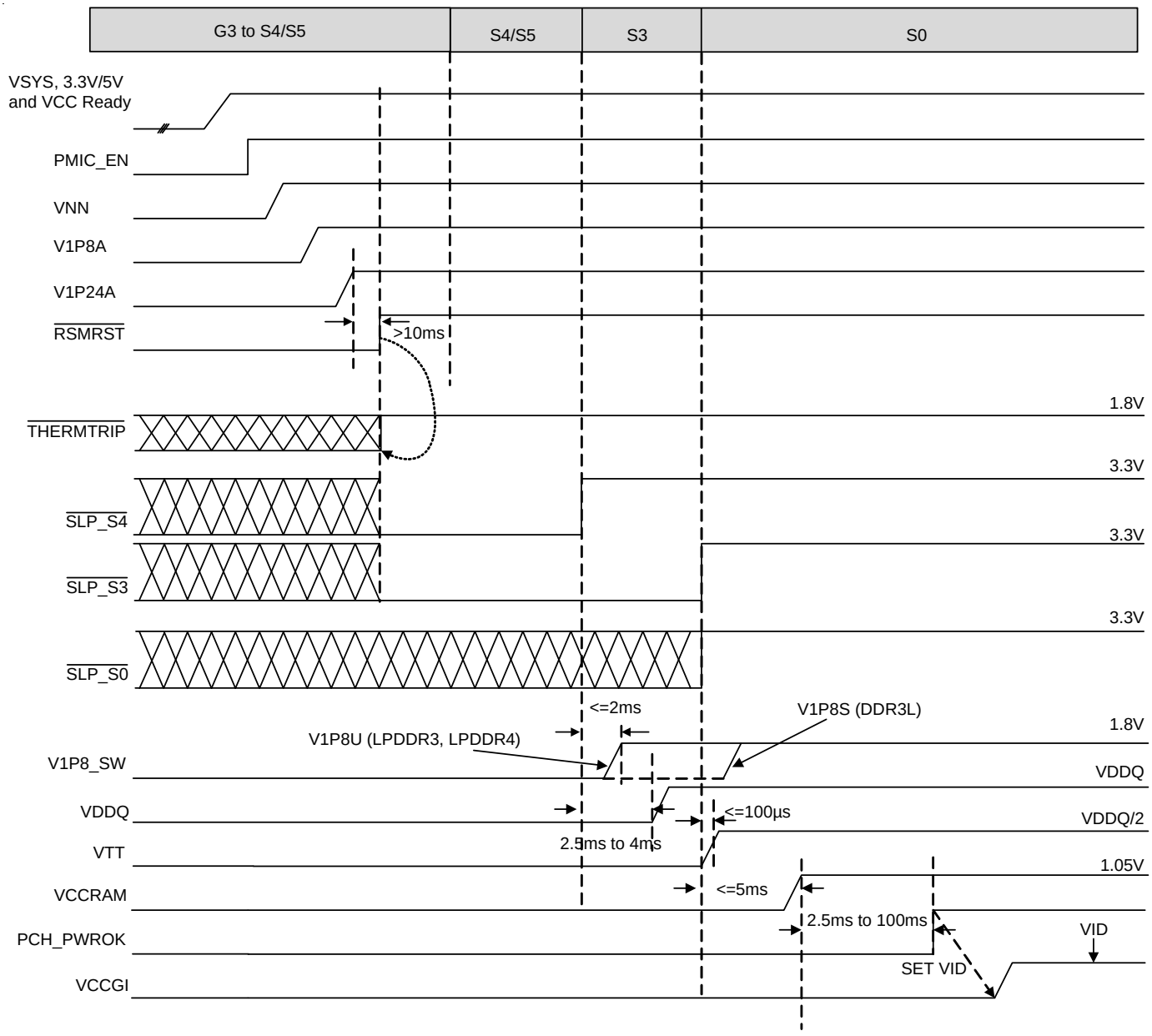

Figure 7. Power on Sequence

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S0iX Entry and Exit Power Sequences

$\overline{SLP_S0}$ to control the voltage rails to meet the power saving requirement of the sleep mode on the APL platform. From S0 mode to S0iX mode, $\overline{SLP_S0}$ goes low, VTT, VNN VCCRAM and VCCGI rails power off, at the same time, PCHPWROK is still keep high.

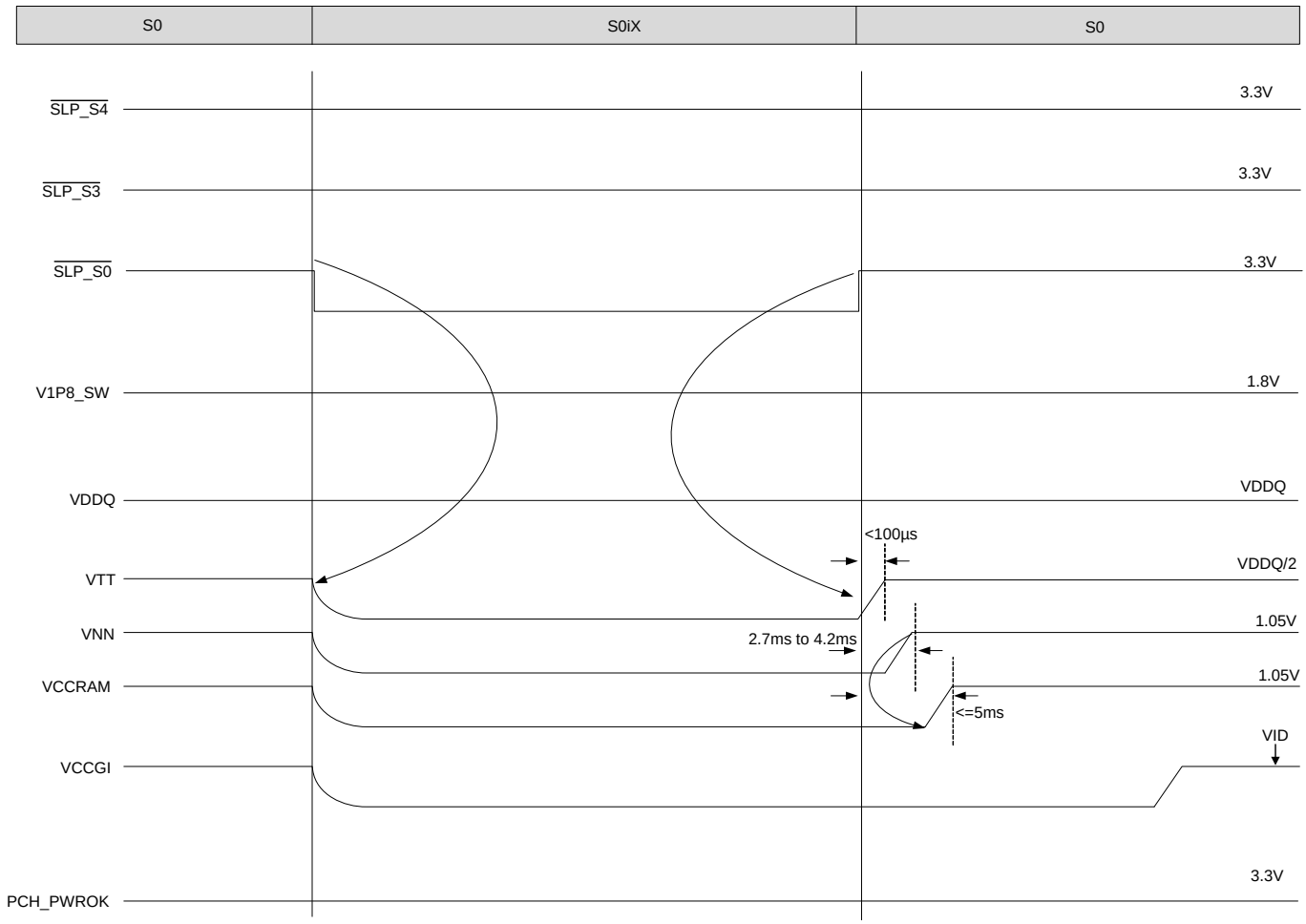

Figure 8. S0 to S0iX to S0 Sequence

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S4/S5 to S0 Entry and Exit Power Sequences

The RT5074A has three SLP enable signals $\overline{\text{SLP_S0}}$, $\overline{\text{SLP_S3}}$ and $\overline{\text{SLP_S4}}$ to control the voltage rails respectively to meet the power saving requirement of the sleep mode on the APL platform. From S0 mode to S3 mode, $\overline{\text{SLP_S3}}$ goes low from S3 to S4/S5 mode, $\overline{\text{SLP_S4}}$ go low.

From S0 to S3 mode, when $\overline{\text{SLP_S3}}$ signal goes low, VTT, VNN , VCCRAM and VCCGI rails power off. Also, if DDR_SEL = High, V1PS power off. At the same time PCH_PWROK pull low to gnd. VNN, VCCRAM and VCCGI discharge to sleep voltage set by BUCKx_RDIS register.

From S3 to S4/S5 mode, when $\overline{\text{SLP_S4}}$ signal goes low, VDDQ power off, And then if DDR_SEL = Low or Floating, V1P8U decay to zero.

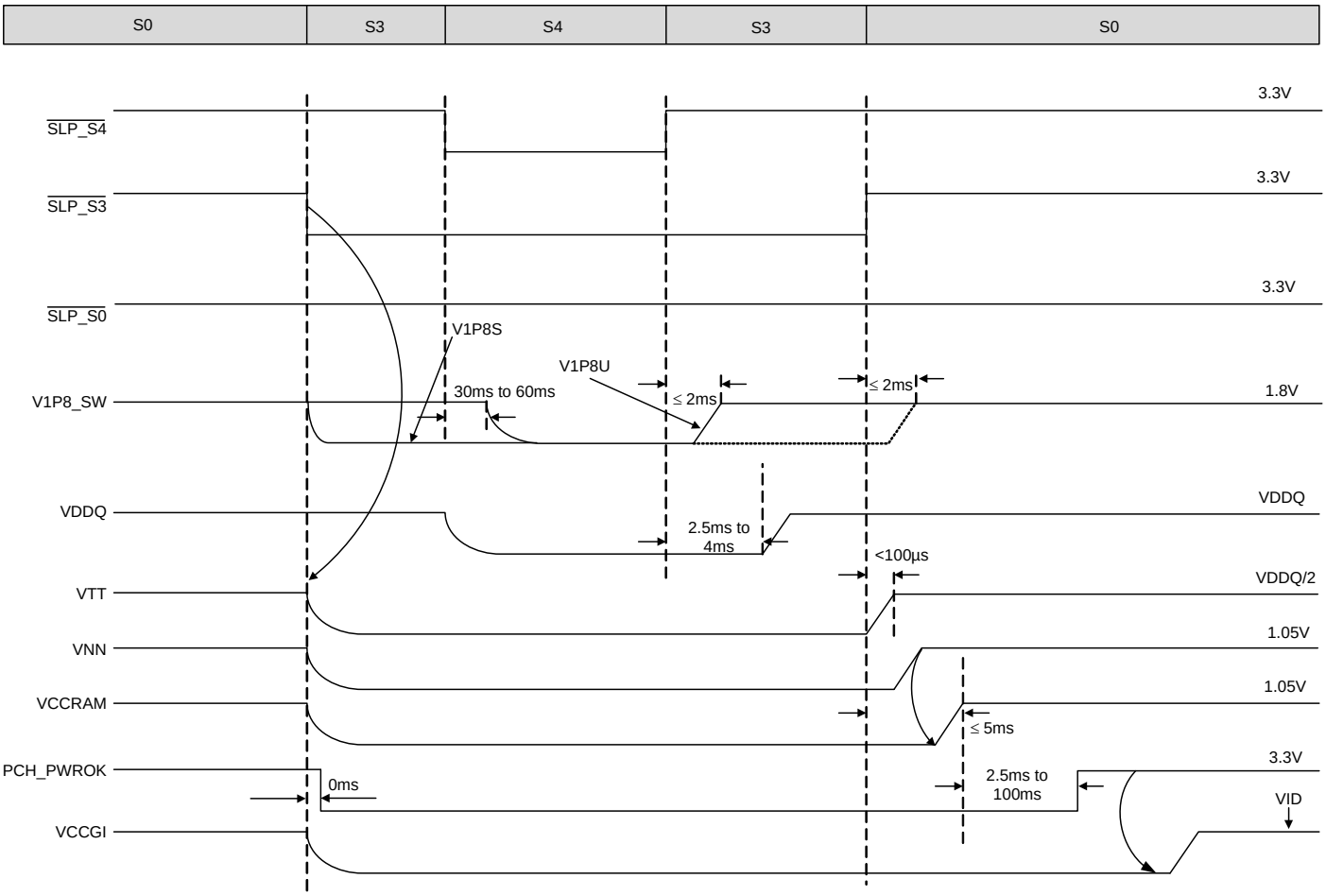

Figure 9. S0 to S4/S5 to S0 Sequence

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The VR power states and related signals are summarized as the Table 3.

Table 3. PMIC Power States

Power State / En&SLP	G3	S4/S5	S3	S0iX	S0
PMIC_EN	L	H	H	H	H
$\overline{\text{SLP_S4}}$	L	L	H	H	H
$\overline{\text{SLP_S3}}$	L	L	L	H	H
$\overline{\text{SLP_S0}}$	L	H	H	L	H
$\overline{\text{THERMTRIP}}$	L	H	H	H	H
Voltage Rails	G3	S4/S5	S3	S0iX	S0
VNN(BUCK1)	OFF	OFF	OFF	OFF	ON
VCCGI(BUCK2)	OFF	OFF	OFF	OFF	ON
VCCRAM(BUCK3)	OFF	OFF	OFF	OFF	ON
V1P8A(BUCK4)	OFF	ON	ON	ON	ON
V1P24A(BUCK5)	OFF	ON	ON	ON	ON
VDDQ(BUCK6)	OFF	OFF	ON	ON	ON
VTT	OFF	OFF	OFF	OFF	ON
GATE1, (DDR_SEL = Low or Floating)	OFF	OFF	ON	ON	ON
GATE1, (DDR_SEL = High)	OFF	OFF	OFF	ON	ON
PGOOD	G3	S4/S5	S3	S0iX	S0
$\overline{\text{RSMRST}}$	L	H	H	H	H
PCH_PWROK	L	L	L	H	H

Note : The VNN is designed as first power on when cold boot from G3. After enter S0 state, the power state of VNN should follow the table above.

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Power-Off Sequence

There are two conditions can make all power rails of the RT5074A go to off mode. One is using SLP signals and PMIC_EN signal to disable the RT5074A, all the output signals and power rails will be off sequentially. Figure 10 shows the normal power off Sequence.

When use PMIC_EN to disable the RT5074A only, all the output signals and power rails will be off at the same time.

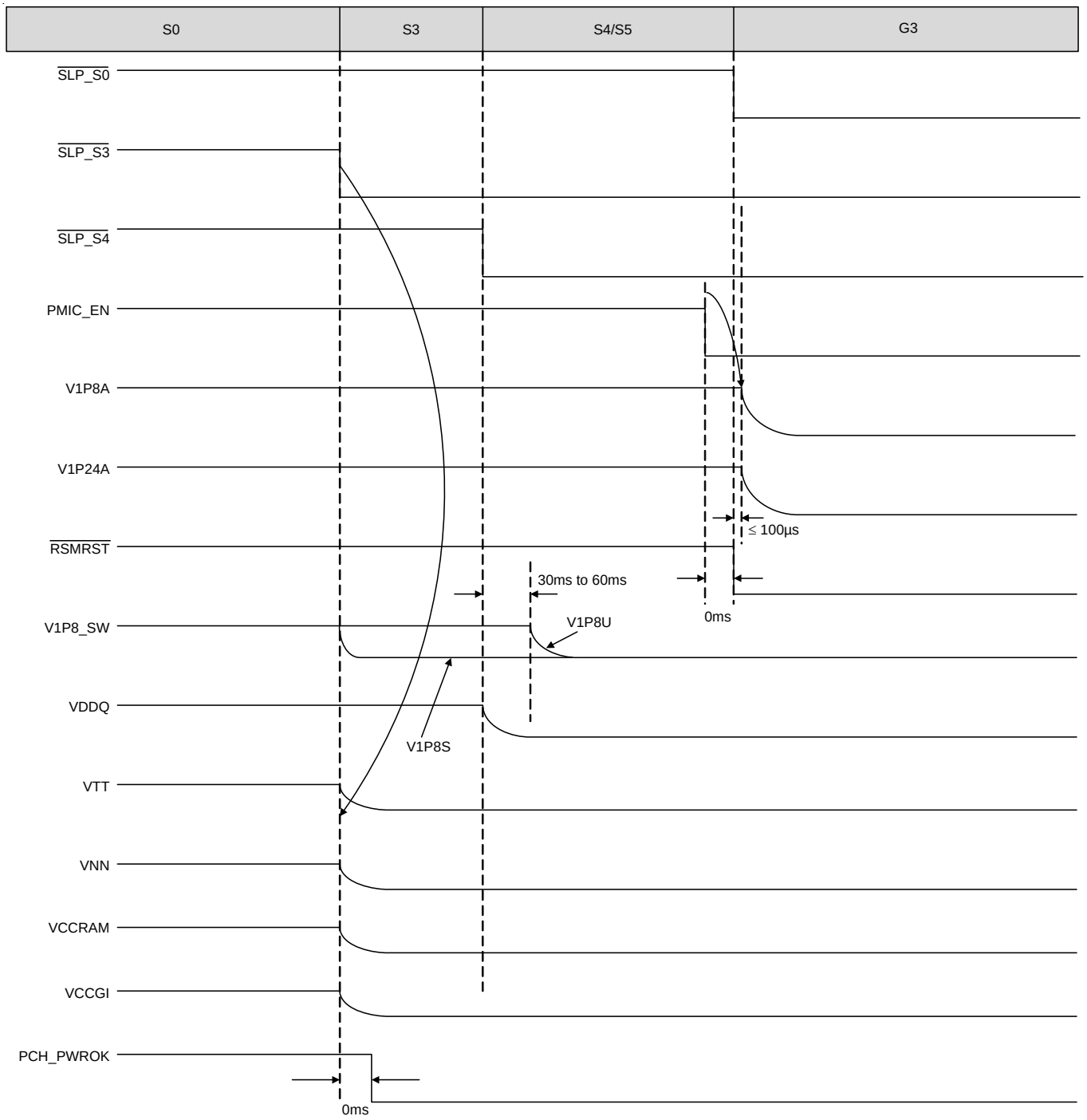

Figure 10. Power Off Sequence

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I²C Interface

An I²C Interface is used to communicate with the RT5074A and the address for the RT5074A is 0x5E. Figure 11 shows the I²C format employed by the RT5074A.

The bus provides read and write access to the internal performance registers for setting and reading of operating parameters and operates up to 1MHz. The Operating parameters that can be adjusted through the I²C interface.

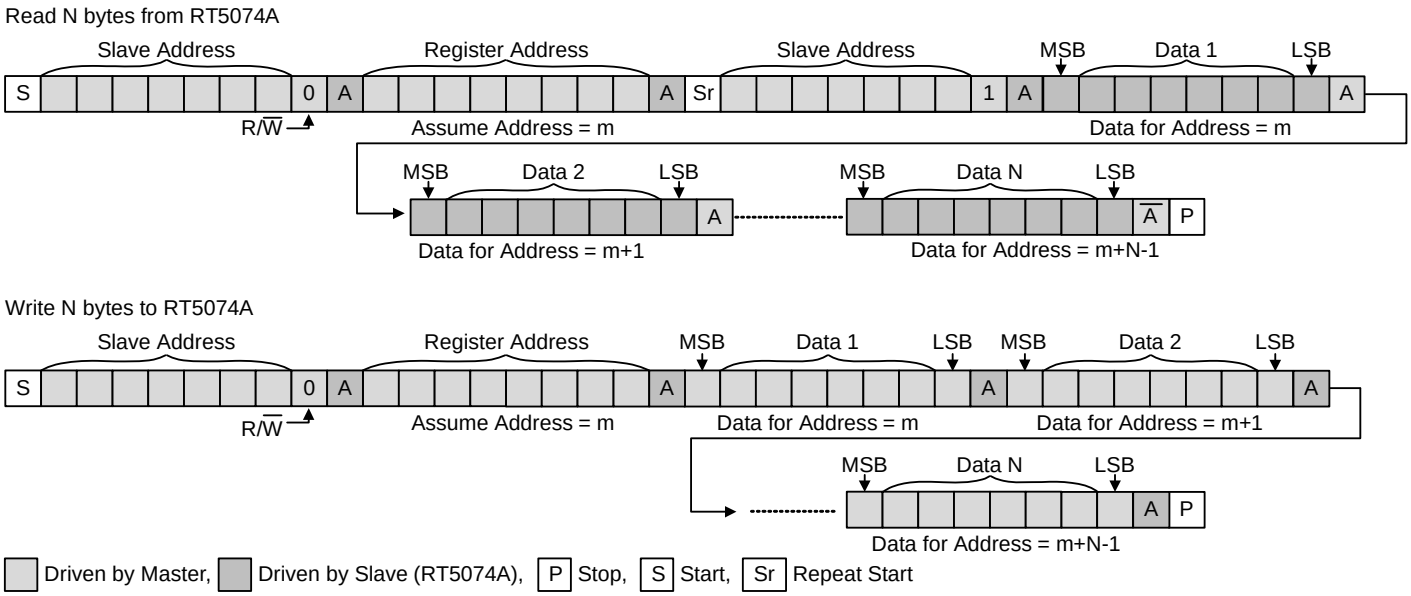

Figure 11. I²C Format

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Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-52L 6x6 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (26.5°C/W) = 3.77W for a WQFN-52L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 12 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

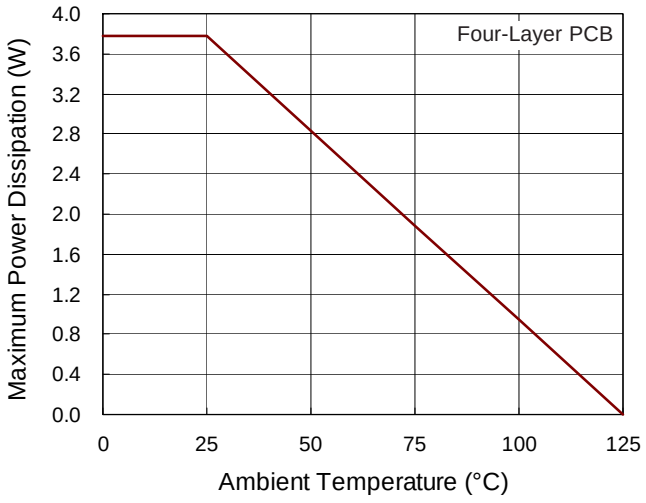

Figure 12. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout.

- Power components should be placed on the same side of board, with power traces routed on the same layer. If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths and use multiple vias for interconnection. When vias are used to connect PCB layers in the high current loop, multiple vias should be used to minimize via impedance. Certain points must be considered before starting a layout using the RT5074A.
- Make the traces of the main current paths as short and wide as possible.
- Place input decoupling capacitors as close as possible as to VIN3 (VCCRAM), VIN4 (V1P8A) and VIN5(V1P24A) pins. This cap provide the instant current into this pin when the internal MOSFET switching. It is preferable to connect the decoupling capacitors directly to the pins without using vias.
- Place the inductors close LX3 (LX_VCCRAM), LX4 (LX_1P8A) and LX5 (LX_V1P24A) to minimize the radiation noise, and the copper area should be minimized. However, the copper area is provided a heat sink to the internal MOSFET. Don't make the area of the node small by using narrow traces, using wide and short traces instead.
- For feedback signals VOUT1 to VOUT6 and VTT_SEN, the sensing point which detects the output voltage must be connected after output capacitor and keep the trace far away from the switching node or inductor.
- Place the bypass capacitor close to VDDQ_LDO_IN, VIN_1P8_SW .
- Place the filter capacitor close to place the output capacitor close to sense point or loading to increase load transient response performance.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection, and the exposed pad should have twelve 0.3mm diameter thermal vias in this pad at least. All the

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vias should be connected to the internal ground plan to minimize the electrical and thermal impedance.

- An example of PCB layout guide is shown in Figure 13. for reference.

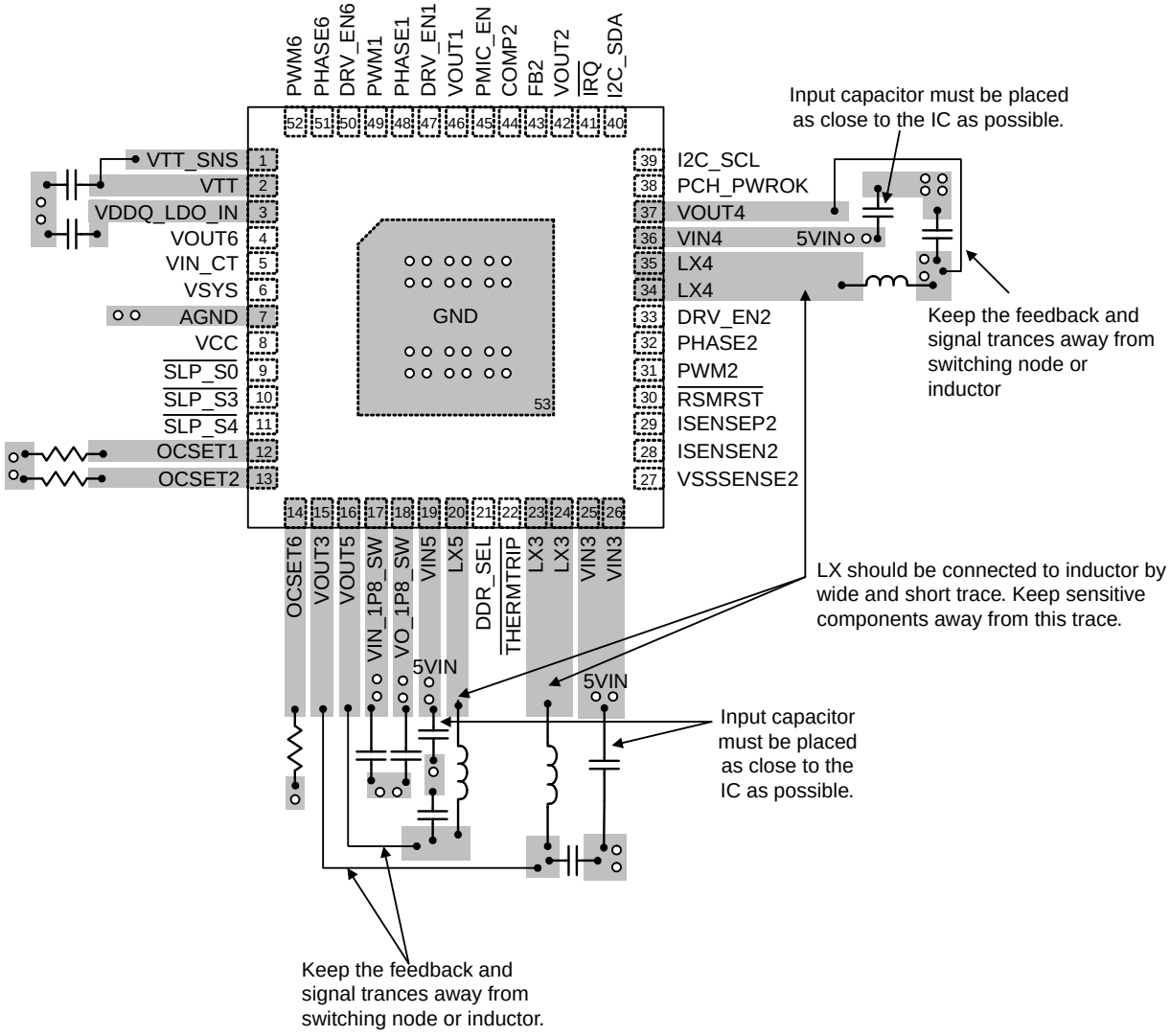

Figure 13. PCB Layout Guide

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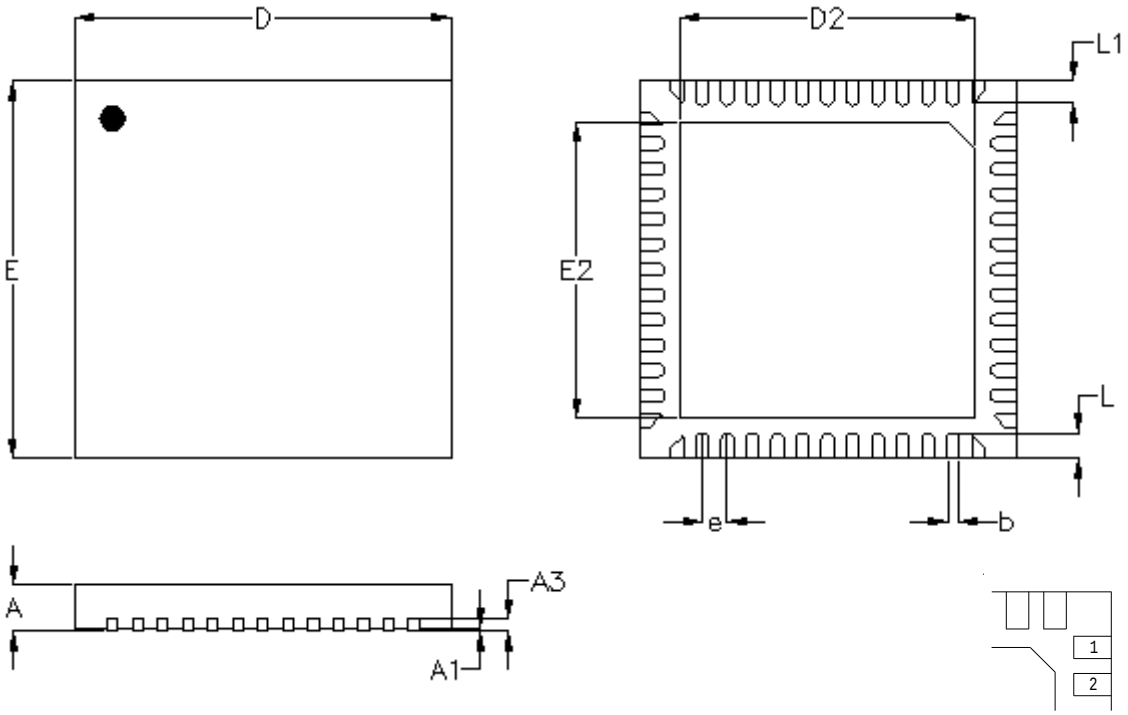
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

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