Integrated PMIC with 8-Channel LDOs and 3 GPOs for Camera Module Applications

General Description

The RT5133A is a highly-integrated power management IC, which includes 8 LDOs for camera sensor applications, including 2-Ch DVDD, 4-Ch AVDD, 1-Ch VIO, 1-Ch VAF and 3 GPOs for portable devices.

The output voltages, soft-start time and protections of regulators can be controlled by writing the registers through I^2C.

The LDO1 can be used to supply power to IO (VIO). The LDO2 can be used to supply power to auto focus unit (VAF). The LDO3 to LDO6 can be used to supply power to AVDD. The LDO7 and LDO8 can be used to supply power to DVDD.

3 GPO output pins can control external device or be reused for another purpose.

The RT5133A is available in a WL-CSP-25B 1.84x1.84 (BSC) package.

Ordering Information

RT5133A □

└Package Type
WSC : WL-CSP-25B 1.84x1.84 (BSC)

Note :

The products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

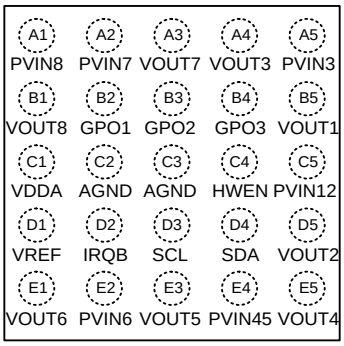
- Cellular Telephones
- Personal Information Appliances
- Tablet PCs
- Portable Instruments

Features

- **Top**
  - **Hardware Enable Pin**
  - **I^2C Controlled Interface**
  - **Programmable Channel Power On/Off**
  - **IRQB Output for Indication**
  - **Input Under-Voltage Protection**
  - **Over-Temperature Protection**
- **LDO**
  - **LDO1/2**
    - **2 Low Dropout Regulators for VIO18 and auto Focus Application**
    - **Wide 2.8V to 5V Operating Input Range**
    - **Programmable Output Voltage by I^2C**
    - **High PSRR : 70dB @ 1KHz**
    - **300mA Low Dropout Voltage Regulators**
  - **LDO3/4/5/6**
    - **4 Low Dropout Regulators for AVDD application**
    - **Wide 2.8V to 5V Operating Input Range**
    - **Programmable Output Voltage by I^2C**
    - **High PSRR : 85dB @ 1KHz**
    - **300mA Low Dropout Voltage Regulators**
  - **LDO7/8**
    - **2 Low Dropout Regulators for DVDD application**
    - **Wide 1.1V to 5V Operating Input Range**
    - **Programmable Output Voltage by I^2C**
    - **High PSRR : 75dB @ 1KHz**
    - **600mA/1000mA Low Dropout Voltage Regulators**
- **GPO**
  - **3 GPO Pins to Control a Single Regulator**

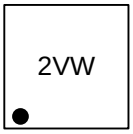
Pin Configuration

(TOP VIEW)



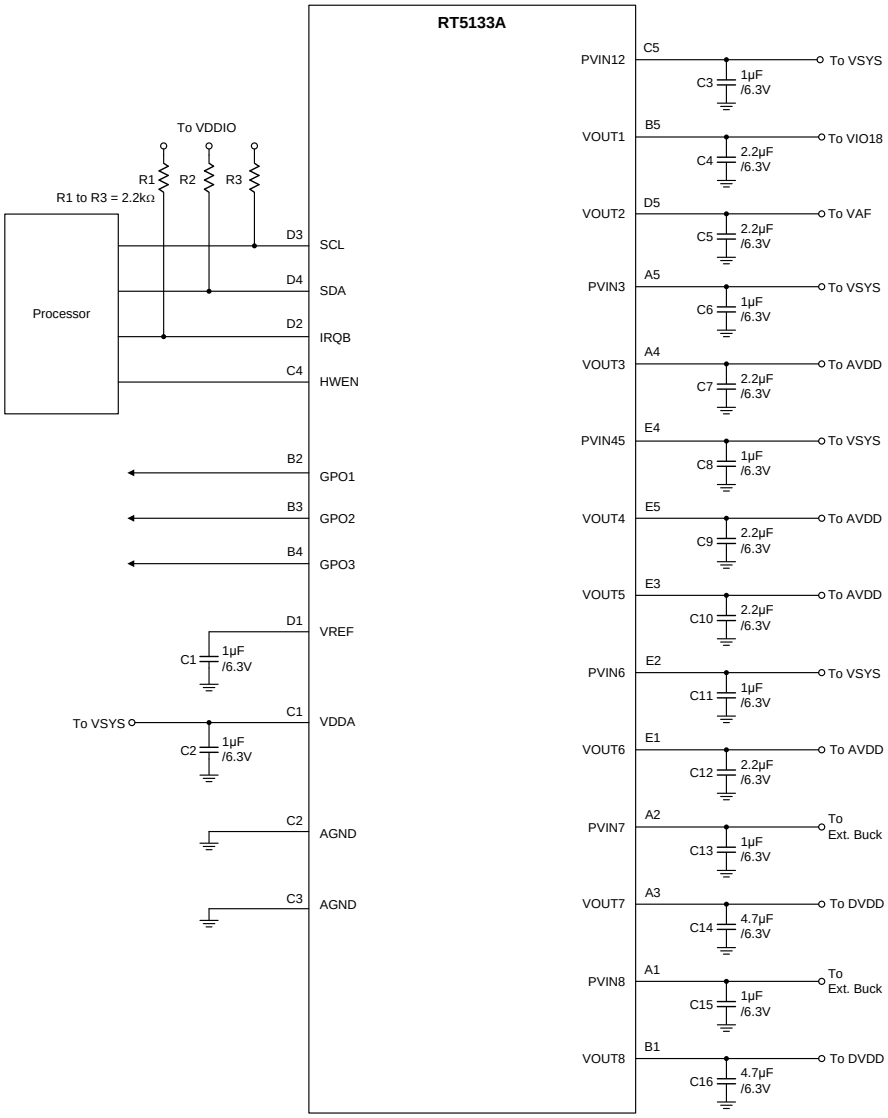
WL-CSP-25B 1.84x1.84 (BSC)

Marking Information



2V : Product Code
W : Date Code

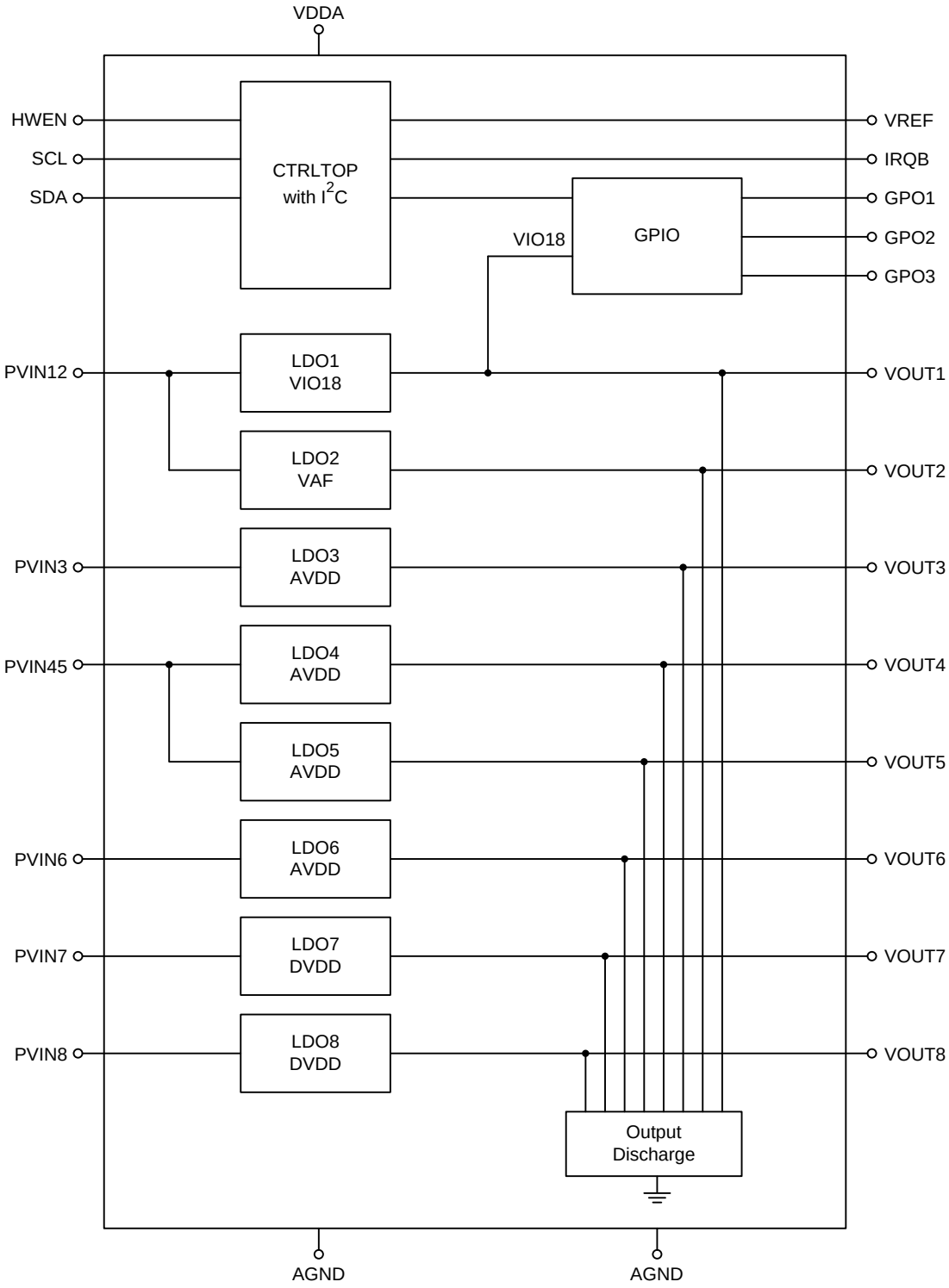
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Description
A1	PVIN8	Power supply of LDO8.
A2	PVIN7	Power supply of LDO7.
A3	VOUT7	LDO7 regulator output.
A4	VOUT3	LDO3 regulator output.
A5	PVIN3	Power supply of LDO3.
B1	VOUT8	LDO8 regulator output.
B2	GPO1	General Purpose output control 1 for external device.
B3	GPO2	General Purpose output control 2 for external device.
B4	GPO3	General Purpose output control 3 for external device.
B5	VOUT1	LDO1 regulator output.
C1	VDDA	Regulated power input for an internal analog base. Connect a 1μF ceramic capacitor between VDDA and ground.
C2, C3	AGND	Analog ground. Tie AGND and ground on the PCB.
C4	HWEN	Enable input pin to turn on/off device.
C5	PVIN12	Power supply of LDO1 to 2.
D1	VREF	Internal reference output. It requires a 1μF decouple ceramic capacitor.
D2	IRQB	Active-low open-drain interrupt output. It requests the processor to read the registers.
D3	SCL	I^2C clock signal input.
D4	SDA	I^2C data signal input/output (Open-drain).
D5	VOUT2	LDO2 regulator output.
E1	VOUT6	LDO6 regulator output.
E2	PVIN6	Power supply of LDO6.
E3	VOUT5	LDO5 regulator output.
E4	PVIN45	Power supply of LDO4 to 5.
E5	VOUT4	LDO4 regulator output.

Functional Block Diagram



Operation

Control Pin Description

Part	Pin Name	Pin Description	Pin Type	I²C Controlled	Pin Connection Suggestion when Unused
Top	SDA	I²C interface serial data input/output. Open-drain. An external pull-up resistor is required.	Input/Output/ Open-drain	Yes	
	SCL	I²C interface serial clock input. Open-drain. An external pull-up resistor is required.	Input/Open-drain	Yes	
	IRQB	Interrupt output, active-low open-drain, to request the processor to read the registers.	Output/Open-drain	No	Floating
	HWEN	Enable input	Input/Active-high	No	Tie to GPIO
	GPO1	General purpose output control	Output/Push-pull	Yes	Floating
	GPO2	General purpose output control	Output/Push-pull	Yes	Floating
	GPO3	General purpose output control	Output/Push-pull	Yes	Floating

If a channel is unused, follow the setting instructions as below

Unused Part	Unused Function	Unused Pin Name	Pin Connection (Short to Ground/Floating/Others)
LDO	LDO1	VOUT1	Floating
	LDO2	VOUT2	Floating
	LDO3	VOUT3	Floating
	LDO4	VOUT4	Floating
	LDO5	VOUT5	Floating
	LDO6	VOUT6	Floating
	LDO7	VOUT7	Floating
	LDO8	VOUT8	Floating

BOM List

Reference	Q'ty	Part Number	Description	Package	Manufacturer
C14, C16	2	GRM155R60J475ME47	4.7μF/0402/6.3V/X5R	0402	MURATA
C4, C5, C7, C9, C10, C12	4	GRM033R60J225ME47D	2.2μF/0201/6.3V/X5R	0201	MURATA
C1, C2, C3, C6, C8, C11, C13, C15	8	GRM033R60J105ME11D	1μF/0201/6.3V/X5R	0201	MURATA
R1, R2, R3	3	RM02FTN2201	2.2k/0201/1%	0201	TA-I

Protection List

Part	Protection Type	Threshold (Typical Value)	Deglitch Time	Protection Method	Reset Method
TOP	VDDA UVLO	VDDA < 2.6V	1ms	All LDOs shut down	VSYS > 2.8V
	OTP	Temperature > 150°C	1ms	OTP shut down selection by (0x0A, bit[4])	Temperature < 110°C
LDO1	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO1 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO1 shut down	Re-power on
LDO2	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO2 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO2 shut down	Re-power on
LDO3	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO3 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO3 shut down	Re-power on
LDO4	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO4 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO4 shut down	Re-power on
LDO5	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO5 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO5 shut down	Re-power on
LDO6	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO6 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO6 shut down	Re-power on
LDO7	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO7 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO7 shut down	Re-power on
LDO8	Over-Current	1.2 x Imax to 3 x Imax	5ms	LDO8 shut down	Re-power on
	Power Good	VOUT < Target x 70%	400μs	LDO8 shut down	Re-power on

Absolute Maximum Ratings (Note 1)

- All Pins ---------- –0.5V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-25B 1.84 x 1.84 (BSC) ---------- 2.07W
- Package Thermal Resistance (Note 2)
  WL-CSP-25B 1.84 x 1.84 (BSC), θ_{JA} ---------- 48.3°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VDDA Supply Input Voltage (VDDA = PVIN > VOUT + Dropout) ---------- 2.8V to 5V
- PVIN12/3/45/6 (VDDA = PVIN > VOUT + Dropout) ---------- 2.8V to 5V
- PVIN7/8 ---------- 1.1V to 5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DDA} = VSYS = PVINx = 4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PMIC Quiescent Current and OTP						
Shut Down Current	I_{SHDN}	On VDDA pin, with all channels shut down, V_{DDA} = 4V, HWEN = L	--	1	2	μA
Standby-Mode Current	$I_{Standby}$	On VDDA pin, with all channels shut down, V_{DDA} = 4V, HWEN = H	--	50	70	μA
Over-Temperature Protection Threshold	T_{OTP}	Thermal shut down threshold temperature	--	150	--	°C
Over-Temperature Protection Accuracy	T_{OTP_ACC}	Thermal shut down temperature accuracy	–15	--	15	°C
Over-Temperature Protection Recover	$T_{OTP\_RECOVER}$	Thermal shut down recover temperature	95	110	125	°C
Control I/O Pin, VDDA and VSYS						
Logic-High Threshold Voltage for GPO Outputs	V_{OH}	I_{DS} = 10mA	1.35	--	--	V
Logic-Low Threshold Voltage for All Open-Drain Outputs	V_{OL}	I_{DS} = 10mA	--	--	0.45	V
Logic-High Threshold Voltage for All Inputs	V_{IH}	Logic high threshold	1.2	--	--	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic-Low Threshold Voltage for All Inputs	V_{IL}	Logic low threshold	--	--	0.4	V
VDDA Under-Voltage Protection Rising Threshold	$V_{DDA\_UVP\_RISE}$	V_{DDA} rising	2.7	2.8	2.9	V
VDDA Under-Voltage Protection Hysteresis	$V_{DDA\_UVP\_HYS}$	V_{DDA} falling	--	0.2	--	V
Pull-Down Ability on HWEN	I_{PD_HWEN}		--	1	--	μA
Pull-Down Ability on GPO1/2/3	I_{PD_GPO}		--	1	--	μA
LDO1 to 8 (LDO1 : VIO / LDO2 : VAF / LDO3/4/5/6 : AVDD / LDO7/8 : DVDD)						
Input Voltage Range	$V_{LDO\_PVIN12/3/45/6}$	VDDA ≥ PVIN	2.8	--	5	V
	$V_{LDO\_PVIN7/8}$	LDO7 = 1.8V/10mA LDO8 = 1.71V/10mA	2	--	5	
	$V_{LDO\_PVIN7/8}$		1.1	--	2	
Output Voltage Accuracy	$\Delta V_{OUT\_LDO1/2}$	V_{OUT} = 1.8V, I_{OUT} = 300mA	–1	--	1	%
	$\Delta V_{OUT\_LDO3/4/5/6}$	V_{OUT} = 2.8V, I_{OUT} = 300mA	–1	--	1	
	ΔV_{OUT_LDO7}	V_{OUT} = 1.1V, I_{OUT} = 600mA	–1	--	1	
	ΔV_{OUT_LDO8}	V_{OUT} = 1.09V, I_{OUT} = 1000mA	–1	--	1	
Output Current Limit	$I_{oc\_LDO1/2}$		360	--	900	mA
	$I_{oc\_LDO3/4/5/6}$		360	--	900	
	I_{oc_LDO7}		720	--	1800	
	I_{oc_LDO8}		1200	--	3000	
Output Short Current limit	$I_{SHORTLIM\_LDO1/2}$	LDO1/2_OCFB_EN = 1	60	--	300	mA
	$I_{SHORTLIM\_LDO3/4/5/6}$	LDO3/4/5/6_OCFB_EN = 1	60	--	300	
	$I_{SHORTLIM\_LDO7}$	LDO7_OCFB_EN = 1	120	--	600	
	$I_{SHORTLIM\_LDO8}$	LDO8_OCFB_EN = 1	200	--	1000	
Dropout Voltage	$V_{DROP\_LDO1/2/3/4/5/6}$	I_LOAD1/2/3/4/5/6 = 300mA	--	--	350	mV
	V_{DROP_LDO7}	I_LOAD7 = 600mA	--	--	200	
	V_{DROP_LDO8}	I_LOAD8 = 1000mA	--	--	200	
Rated Load Current (I_rated)	$I_{\_LDO1/2/3/4/5/6}$	I_rated ≤ 300mA	--	--	300	mA
	$I_{\_LDO7}$	I_rated ≤ 600mA	--	--	600	
	$I_{\_LDO8}$	I_rated ≤ 1000mA	--	--	1000	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Rejection Ratio (Note 5)	$PSRR_{LDO1/2}$	1. PVIN = 3.8V 2. V_{OUT} = 1.8V/50mA 3. Freq = 1kHz	--	70	--	dB
		1. PVIN = 3.8V 2. V_{OUT} = 1.8V/50mA 3. Freq = 10kHz	--	60	--	
		1. PVIN = 3.8V 2. V_{OUT} = 1.8V/50mA 3. Freq = 100kHz	--	40	--	
		1. PVIN = 3.8V 2. V_{OUT} = 1.8V/50mA 3. Freq = 1MHz	--	25	--	
	$PSRR_{LDO3/4/5/6}$	1. PVIN = 3.8V 2. V_{OUT} = 2.8V/60mA 3. Freq = 1kHz	--	85	--	
		1. PVIN = 3.8V 2. V_{OUT} = 2.8V/60mA 3. Freq = 10kHz	--	75	--	
		1. PVIN = 3.8V 2. V_{OUT} = 2.8V/60mA 3. Freq = 100kHz	--	64	--	
		1. PVIN = 3.8V 2. V_{OUT} = 2.8V/60mA 3. Freq = 1MHz	--	41	--	
	$PSRR_{LDO7/8}$	1. PVIN = 1.35V 2. V_{OUT} = 1.1V/150mA 3. Freq = 1kHz	--	78	--	
		1. PVIN = 1.35V 2. V_{OUT} = 1.1V/150mA 3. Freq = 10kHz	--	68	--	
		1. PVIN = 1.35V 2. V_{OUT} = 1.1V/150mA 3. Freq = 100kHz	--	47	--	
		1. PVIN = 1.35V 2. V_{OUT} = 1.1V/150mA 3. Freq = 1MHz	--	32	--	
Soft-Start Time	$t_{SS\_LDO1/2}$	V_{OUT_LDO} = 90% of V_{OUT_LDO} C_{OUT} < 10µF	--	--	1000	µs
	$t_{SS\_LDO3/4/5/6/7/8}$	V_{OUT_LDO} = 90% of V_{OUT_LDO} C_{OUT} < 10µF	--	--	1000	
Power Off Time	$t_{SS\_LDO1/2}$	V_{OUT_LDO} = 10% of V_{OUT_LDO} C_{OUT} < 10µF	--	--	2000	µs
	$t_{SS\_LDO3/4/5/6/7/8}$	V_{OUT_LDO} = 10% of V_{OUT_LDO} C_{OUT} < 10µF	--	--	2000	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Current	$I_{IQ\_LDO1/2}$	VDDA = PVIN > VOUT + Dropout I_{LOAD} = 0mA and not include base Iq.	--	30	45	μA
	$I_{IQ\_LDO3/4/5/6}$	VDDA = PVIN > VOUT + Dropout I_{LOAD} = 0mA and not include base Iq.	--	55	65	
	$I_{IQ\_LDO7/8}$	PVIN > VOUT + Dropout I_{LOAD} = 0mA, LDO7 & LDO8 are turned on	--	220	320	
Output Noise Voltage (Note 5)	$Noise_{LDO1/2}$	V_{OUT} = 1.8V/150mA	--	45	--	μVrms
	$Noise_{LDO3/4/5/6}$	V_{OUT} = 2.8V/150mA	--	50	--	
	$Noise_{LDO7/8}$	V_{OUT} = 1.1V/300mA	--	75	--	
I^2C characteristics						
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}	VDD = 1.8V to 5V	1.2	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}	VDD = 1.8V to 5V	--	--	0.4	V
SCL Clock Frequency	f_{CLK}	Fast-mode	--	--	400	kHz
		High-speed mode Cb = 100pF	--	--	3.4	MHz
Bus Free Time between Stop and Start Condition	t_{BUF}	Fast-mode	1.3	--	--	μs
(Repeated) Start Hold Time	$t_{HD;STA}$	Fast-mode	0.6	--	--	μs
		High-speed mode Cb = 100pF	160	--	--	ns
(Repeated) Start Setup Time	$t_{SU;STA}$	Fast-mode	0.6	--	--	μs
		High-speed mode Cb = 100 pF	160	--	--	ns
STOP Condition Setup Time	$t_{SU;STO}$	Fast-mode	0.6	--	--	μs
		High-speed mode Cb = 100pF	160	--	--	ns
SDA Data Hold Time	$t_{HD;DAT}$	Fast-mode	0	--	--	ns
		High-speed mode Cb = 100pF	0	--	70	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Fast-mode	--	--	0.9	μs
SDA Setup Time	$t_{SU;DAT}$	Fast-mode	100	--	--	ns
		High-speed mode Cb = 100pF	10	--	--	
SCL Clock Low Time	t_{LOW}	Fast-mode	1.3	--	--	μs
		High-speed mode Cb = 100pF	160	--	--	ns
SCL Clock High Time	t_{HIGH}	Fast-mode	0.6	--	--	μs
		High-speed mode Cb = 100pF	60	--	--	ns

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

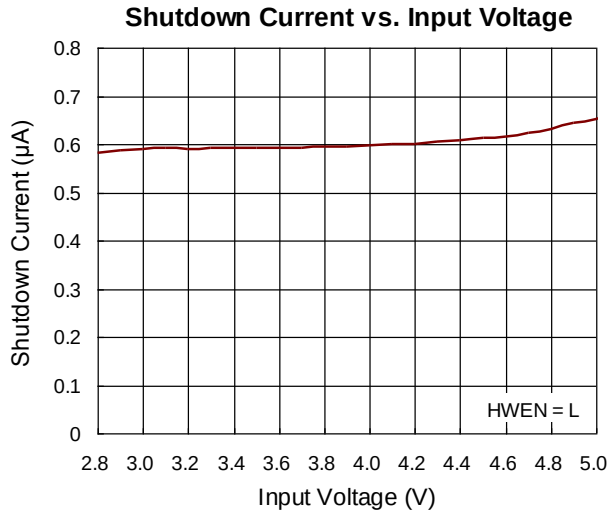
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

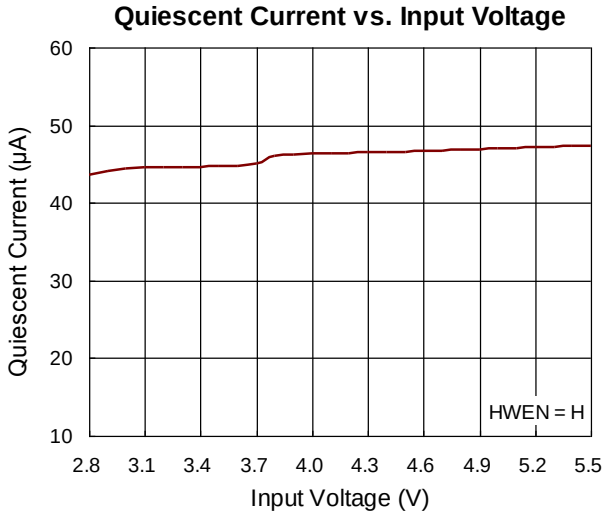
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

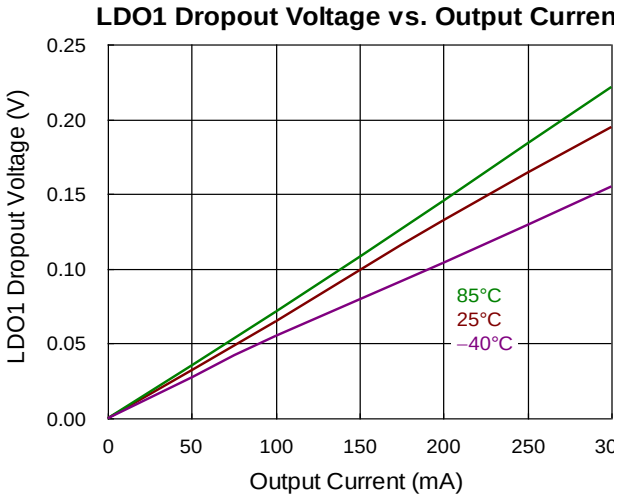
Note 4. The device is not guaranteed to function outside its operating conditions.

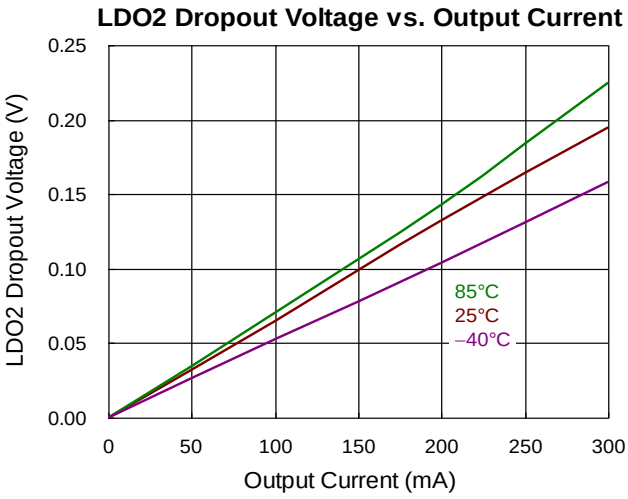
Note 5. This specification is guaranteed by design.

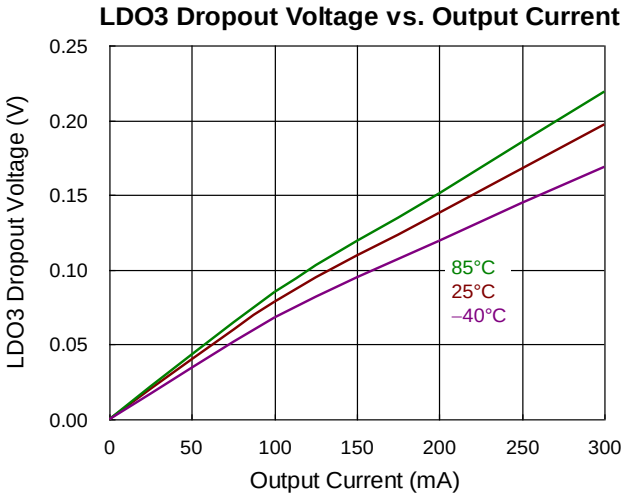
Typical Operating Characteristics

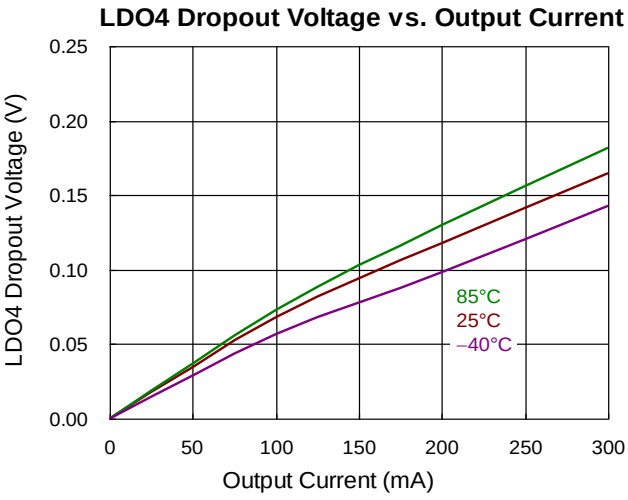




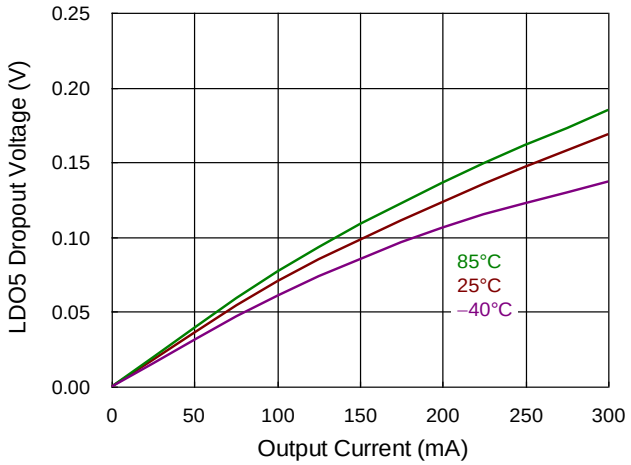




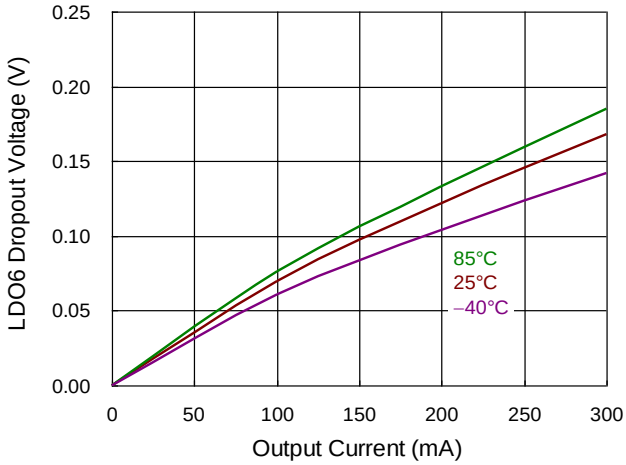




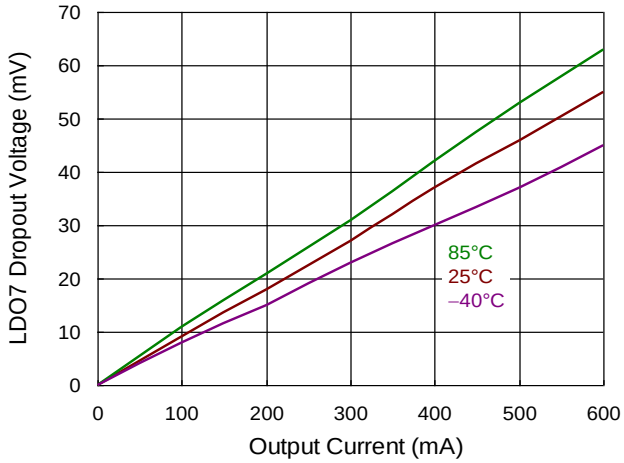
LDO5 Dropout Voltage vs. Output Current



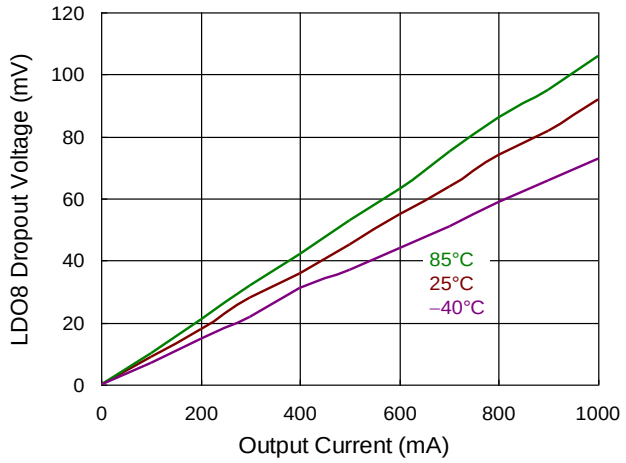
LDO6 Dropout Voltage vs. Output Current



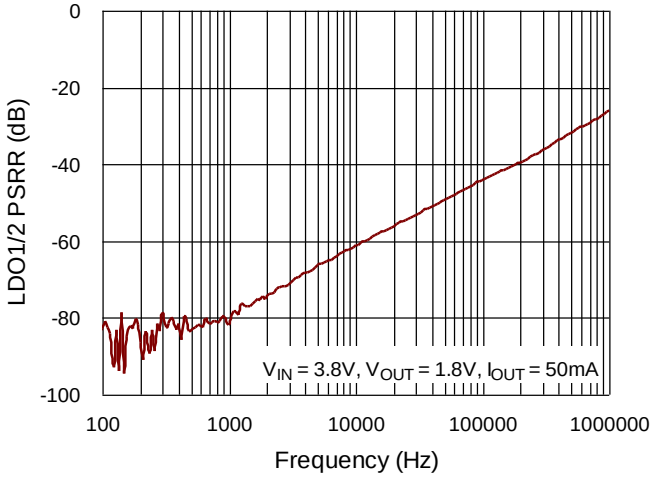
LDO7 Dropout Voltage vs. Output Current



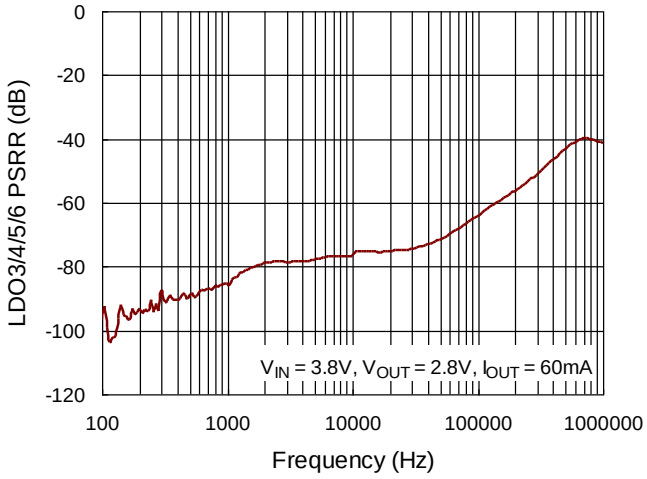
LDO8 Dropout Voltage vs. Output Current

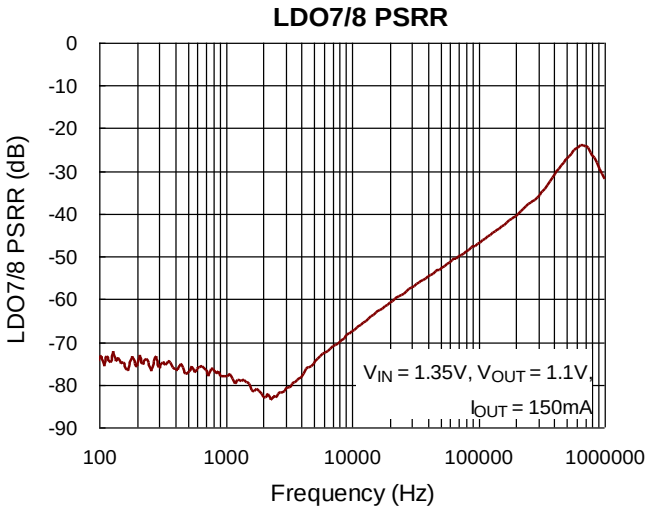


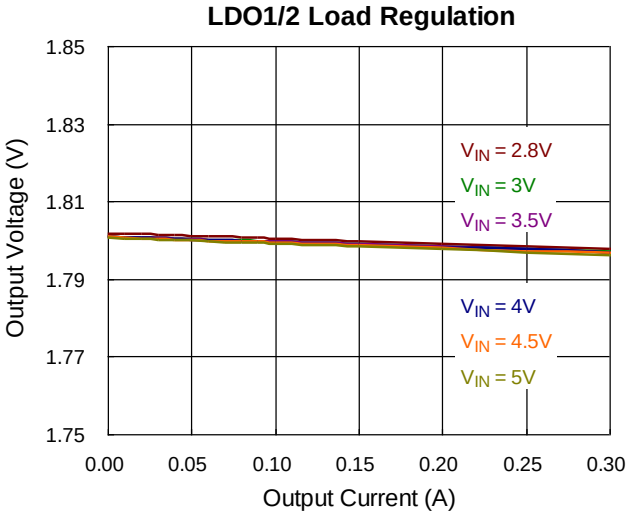
LDO1/2 PSRR

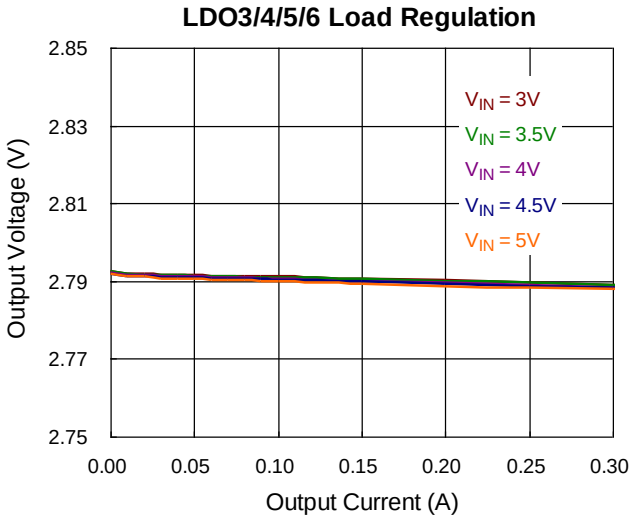


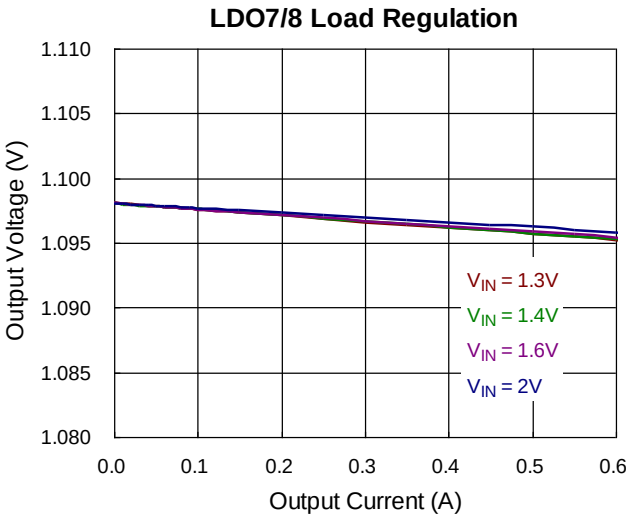
LDO3/4/5/6 PSRR











Application Information

The RT5133A is a highly-integrated power management IC, which includes 8 LDOs, 3 GPO for portable camera module. There are 2 ways to power on/off for each regulator.

1. It can be set at the registers 0x1A for power on and 0x1B for power off. When the HWEN pin toggles from low to high, it will force all 8 LDO regulators power on. The HWEN pin toggles from high to low, it will force all 8 LDO regulators to power off. The device also provides delay time selection by EN_TD bit. Because LDO7/8 PVIN is from external Buck, the external Buck needs to be powered on first before LDO7/8 operates.
2. Individual on/off control by LDOx_EN bit.

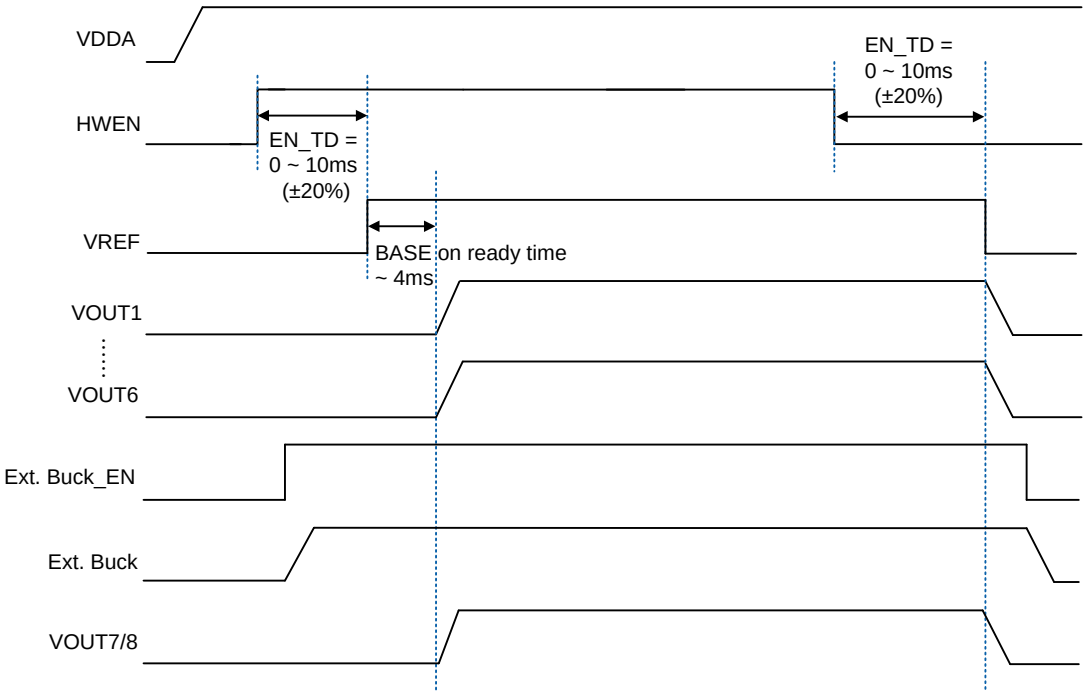


Figure 1. Power ON/OFF Control

Over-Temperature Protection

The RT5133A also features over-temperature protection (OTP), and has three sensors of OTP0, OTP1 and OTP2. They can be enabled in the registers (0x0A[7:5]).

The OTP can be triggered to shut down the device if the junction temperature exceeds T_{OTP}, 150°C typically. The channels which will be turned off can be selected by register (0x0A[4]).

If the junction temperature drops to $T_{OTP\_RECOVER}$, 110°C typically, the device can be reactivated.

VDDA

The VDDA power is from the VSYS directly and the operating input voltage range is from 2.8V to 5V. It is also a power input for an internal analog base circuit and it needs to connect a 1μF ceramic capacitor between VDDA and ground.

The device provides a VDDA Under-Voltage Protection (UVP) once the input voltage drop below 2.6V typically, the UVP function is started and all channels will be turned off after 1ms.

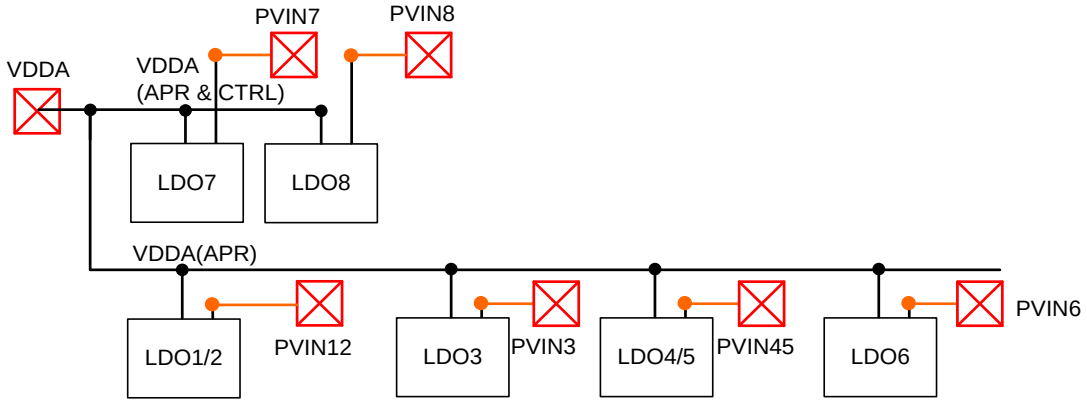


Figure 2. VDDA Power Plan

Interrupt

The RT5133A reports status to host (CPU, MCU, EC, or etc.) by the IRQB (interrupt command to host) pin, which is an open-drain output. The IRQB pin goes low when any fault occurs. It will be automatically reset when all the fault events are cleared.

The IRQB pin is used to indicate whether the RT5133A has any events. If an application processor (AP) detects a falling edge on the IRQB pin, the AP will start to read the IRQB registers 0x10 through 0x12 sequentially.

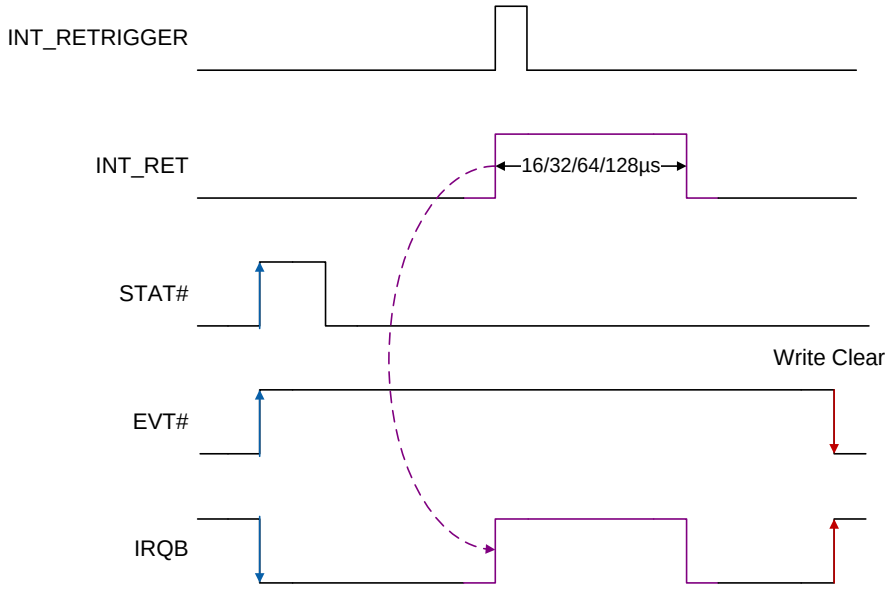


Figure 3. IRQB Pin Diagram

Table 1. LDO Types and Brief Specifications

LDO Name	Input Power Domain	Controller Power Domain	Output Voltage (V)	Imax (mA)	Application
LDO1	VSYS	VSYS	1.8/2.5/2.7/2.8/2.9/3/3.1/3.2	300mA	VIO18
LDO2	VSYS	VSYS	1.8/2.5/2.7/2.8/2.9/3/3.1/3.2	300mA	VAF
LDO3	VSYS	VSYS	1.7/1.8/1.9/2.5/2.7/2.8/2.9/3	300mA	AVDD
LDO4	VSYS	VSYS	1.7/1.8/1.9/2.5/2.7/2.8/2.9/3	300mA	AVDD
LDO5	VSYS	VSYS	1.7/1.8/1.9/2.5/2.7/2.8/2.9/3	300mA	AVDD
LDO6	VSYS	VSYS	1.7/1.8/1.9/2.5/2.7/2.8/2.9/3	300mA	AVDD
LDO7	External Buck	VSYS	0.9/0.95/1/1.05/1.1/1.15/1.2	600mA	DVDD
LDO8	External Buck	VSYS	0.855/0.9/0.95/1/1.04/1.09/1.14	1000mA	DVDD
LDO7/8	VSYS	VSYS	1.8/1.71	10mA	Ext. EN

Over-Current Protection

All of LDOs have protection behavior when over-current protection of the channel is triggered. When LDO triggered OCP that channel will shut down after 5ms de-bouncing time. The channel also provides fold-back feature when over-current protection is triggered and it can be disabled by LDOx_OCFB_EN bit.

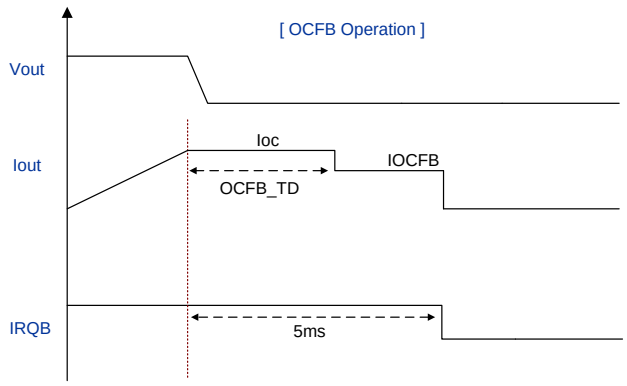


Figure 4. OCFB Operation Diagrams

Output Discharge

Set LDOx_NDIS_EN bit to select output discharge function, “0” : Disable. “1” : Enable.

Channel	Discharge Resistance (Typ. Value)
LDO1 to 6	45Ω
LDO7 to 8	25Ω

GPO Pin

The device provides 3 GPO pin to control external device. The pin can be used as an enable input for any of regulators or sequence group, and the usage is defined by register. Because VOUT1_VIO18 is also a pull-up voltage for GPO, the VOUT1 needs to power on first before GPO operates.

I²C Interface

The following table shows the RT5133A unique address to AP, respectively.

Slave Address			
MSB	LSB	R/W Bit	R/W
001100	0	1/0	31/30

The I²C interface bus must be connect a resistor 2.2kΩ to power node and independent connection to processor, individually. The I²C interface also supports High-Speed (HS) mode for data transfer rate up to 3.4Mbits. The I²C timing diagrams are listed below.

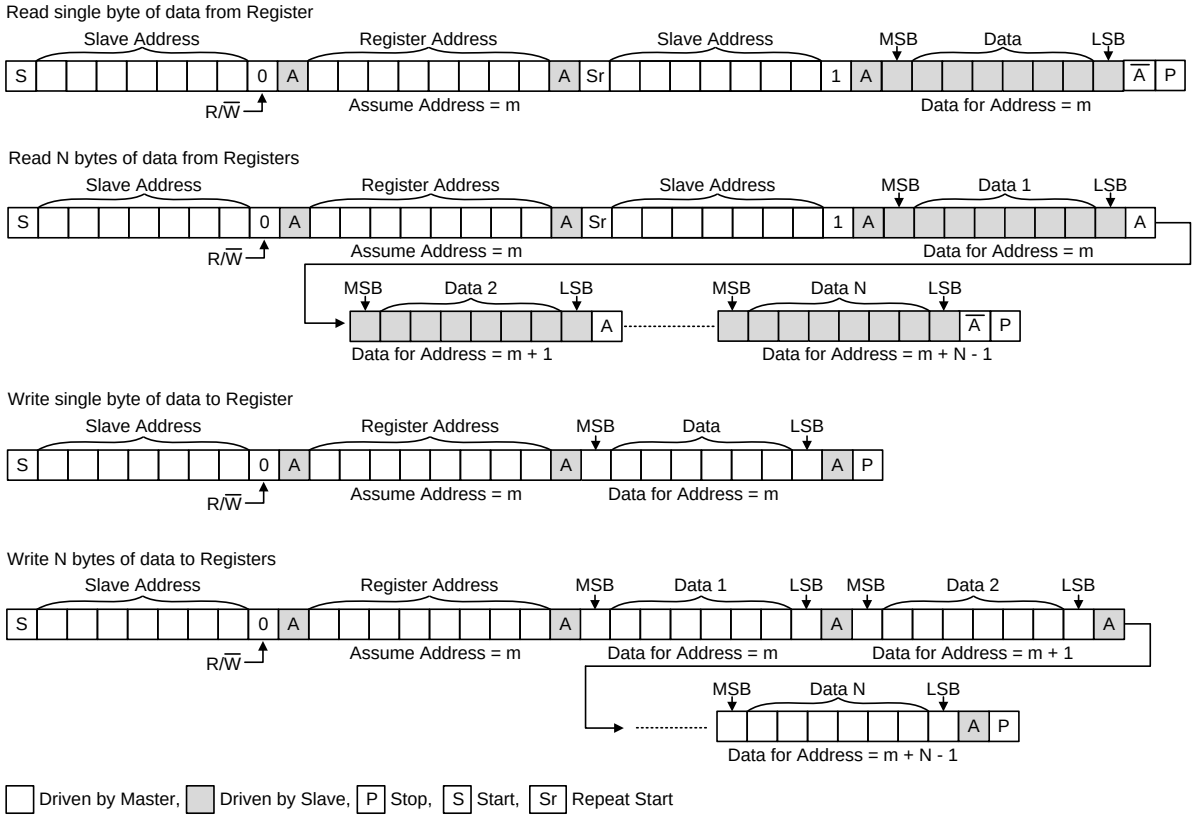


Figure 5. I²C Timing Diagrams

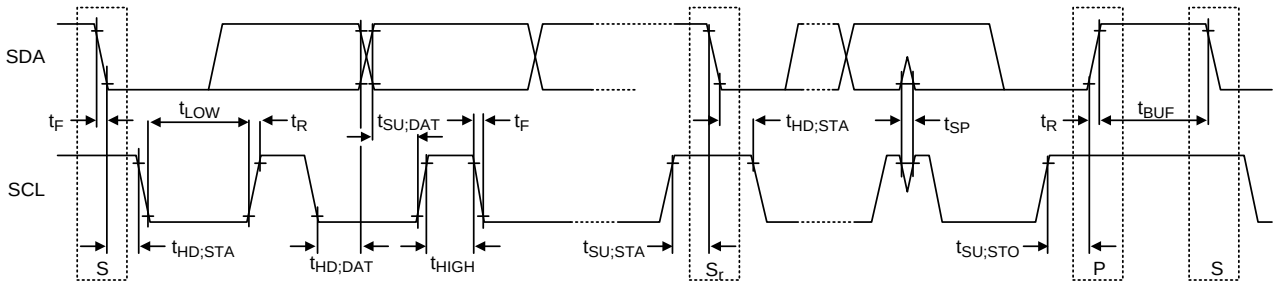


Figure 6. I²C Waveform Information

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-25B 1.84 x 1.84 (BSC) package, the thermal resistance, θ_{JA}, is 48.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (48.3°C/W) = 2.07W for a WL-CSP-25B 1.84 x 1.84 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

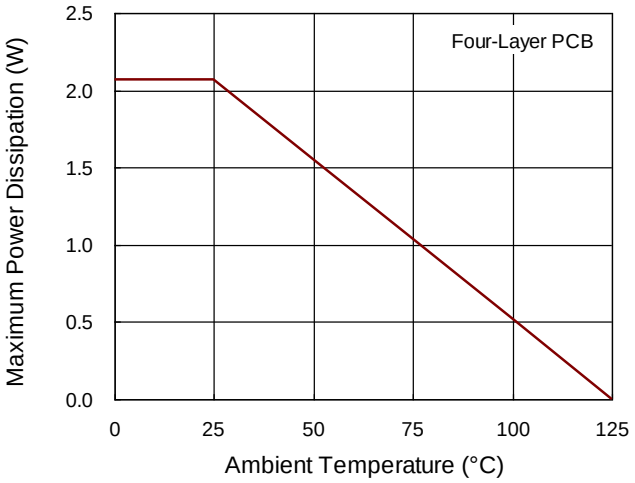


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT5133A. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues or worsened efficiency. For the best performance of the RT5133A, the following PCB layout guidelines must be strictly followed.

- Keep the main power traces as wide, short as possible.
- Place input capacitor as close as possible to input pin and AGND pin connections, and use shortest copper trace connection or AGND plane.
- Put output capacitor near to the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or AGND plane.
- The via size and number should be enough for a given current path.

Register Map

Register Detailed Description

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x00	CHIP_INFO	7:4	VENDOR_ID	1000	RO	Vendor Identification
		3:0	CHIP_REV	0001	RO	Chip Revision : 0001 : 1st Version 0010 : 2nd Version ... 1111 : 15th Version
0x06	RST_CTRL	7:4	RST_PAS_CODE	0000	RW	RESET Passcode Set REG 0x06[7:4] = 1011, then unlock REG0x06[0] ALL_RST To erase RST_PAS_CODE, ALL_RST cannot work.
		3:1	EN_TD	010	RW	Deglitch time of EN 000 : 0ms (Sync only) 001 : 0.5ms 010 : 1ms (default) 011 : 2ms 100 : 4ms 101 : 6ms 110 : 8ms 111 : 10ms
		0	ALL_RST	0	RWC	Reset bit of ALL register and logic 0 : No reset (default) 1 : Reset all registers and logic Note : After reset procedure, this bit is cleared to '0'
0x07	TM_PAS_CODE1	7	INT_RETRIGGER	0	RWC	Interrupt Re-Trigger control 0 : Disabled (default) 1 : Re-Trigger IRQB Note: After re-trigger, this bit is cleared to '0'
		6:5	INT_RET	00	RW	Pulse width of re-trigger interrupt 00 : 16μs (default) 01 : 32μs 10 : 64μs 11 : 128μs
		4:0	Reserved	00000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x08	I2C_CTRL	7	I2CSTMR_RST_EN	1	RW	Enable control of I^2C Safe Timer : Check SDA keeps low for 32ms → I^2C reset 0 : Disable 1 : Enable (default)
		6	I2C_MODE	1	RW	I^2C mode selection 0 : 400kHz 1 : 3.4MHz (default)
		5	Reserved	1	RW	
		4:3	Reserved	10	RW	
		2:0	SDA_DRVSRSEL	111	RW	SDA pull low slew rate 000 : Fastest … 111 : Slowest (default)
0x09	BASE_CTRL	7	VDDAUV_SHDN_SEL	1	RW	VDDAUV Shut down Protection 0 : Interrupt only 1 : Shut down all LDOs (default)
		6	Reserved	0	RW	
		5:4	VDDAUV_TD	11	RW	Deglitch time of VDDAUV 00 : 64μs 01 : 128μs 10 : 256μs 11 : 1024μs (default)
		3:2	Reserved	00	RW	
		1	FOFF_BASE	0	RW	Force-off BASE circuit 0 : Normal work 1 : Force-off
		0	Reserved	0	RW	
0x0A	OTP_CTRL	7	OTP0_EN	1	RW	Enable control of OTP0 0 : Disable 1 : Enable (default)
		6	OTP1_EN	1	RW	Enable control of OTP1 0 : Disable 1 : Enable (default)
		5	OTP2_EN	1	RW	Enable control of OTP2 0 : Disable 1 : Enable (default)
		4	OTP_SHDN_SEL	1	RW	OTP shut down protection 0 : Interrupt Only 1 : Shut down all LDOs (default)
		3:0	Reserved	0000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x0B	GPO_CTRL	7	GPO1_EN	0	RW	Enable control of GPO1 0 : Disable (default) 1 : Enable
		6	GPO2_EN	0	RW	Enable control of GPO2 0 : Disable (default) 1 : Enable
		5	GPO3_EN	0	RW	Enable control of GPO3 0 : Disable (default) 1 : Enable
		4	Reserved	0	RW	
		3	GPO1_TX	0	RW	GPO1 output signal 0 : Low (default) 1 : High
		2	GPO2_TX	0	RW	GPO2 output signal 0 : Low (default) 1 : High
		1	GPO3_TX	0	RW	GPO3 output signal 0 : Low (default) 1 : High
		0	Reserved	0	RW	Reserved
0x10	IRQ_MASK (IRQ Source Indicator Mask)	7	VDDAUV_EVT	0	WC	VDDAUV Event 0 : No event 1 : Event occurred
		6	VREF_EVT	0	WC	BASE VREF Event 0 : No event 1 : Event occurred
		5:3	Reserved	000	WC	
		2	OTP2_EVT	0	WC	OTP2 Event 0 : No event 1 : Event occurred
		1	OTP1_EVT	0	WC	OTP1 Event 0 : No event 1 : Event occurred
		0	OTP0_EVT	0	WC	OTP0 Event 0 : No event 1 : Event occurred

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x11	LDO_OC_EVT	7	LDO8_OC_EVT	0	WC	LDO8 OC Event 0 : No event 1 : Event occurred
		6	LDO7_OC_EVT	0	WC	LDO7 OC Event 0 : No event 1 : Event occurred
		5	LDO6_OC_EVT	0	WC	LDO6 OC Event 0 : No event 1 : Event occurred
		4	LDO5_OC_EVT	0	WC	LDO5 OC Event 0 : No event 1 : Event occurred
		3	LDO4_OC_EVT	0	WC	LDO4 OC Event 0 : No event 1 : Event occurred
		2	LDO3_OC_EVT	0	WC	LDO3 OC Event 0 : No event 1 : Event occurred
		1	LDO2_OC_EVT	0	WC	LDO2 OC Event 0 : No event 1 : Event occurred
		0	LDO1_OC_EVT	0	WC	LDO1 OC Event 0 : No event 1 : Event occurred
0x12	LDO_PGB_EVT	7	LDO8_PGB_EVT	0	WC	LDO8 PG Fault Event 0 : No event 1 : Event occurred
		6	LDO7_PGB_EVT	0	WC	LDO7 PG Fault Event 0 : No event 1 : Event occurred
		5	LDO6_PGB_EVT	0	WC	LDO6 PG Fault Event 0 : No event 1 : Event occurred
		4	LDO5_PGB_EVT	0	WC	LDO5 PG Fault Event 0 : No event 1 : Event occurred
		3	LDO4_PGB_EVT	0	WC	LDO4 PG Fault Event 0 : No event 1 : Event occurred
		2	LDO3_PGB_EVT	0	WC	LDO3 PG Fault Event 0 : No event 1 : Event occurred
		1	LDO2_PGB_EVT	0	WC	LDO2 PG Fault Event 0 : No event 1 : Event occurred
		0	LDO1_PGB_EVT	0	WC	LDO1 PG Fault Event 0 : No event 1 : Event occurred

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x13	BASE_STAT	7	VDDAUV_STAT	0	RO	VDDAUV status 0 : VDDAUV doesn't occur 1 : VDDAUV occurs
		6	VREF_STAT	0	RO	BASE VREF status 0 : BASE VREF doesn't occur 1 : BASE VREF occurs
		5:3	Reserved	000	RO	
		2	OTP2_STAT	0	RO	OTP2 detection status 0 : Temperature is normal 1 : Temperature is over threshold
		1	OTP1_STAT	0	RO	OTP1 detection status 0 : Temperature is normal 1 : Temperature is over threshold
		0	OTP0_STAT	0	RO	OTP0 detection status 0 : Temperature is normal 1 : Temperature is over threshold

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x14	LDO_OC_STAT	7	LDO8_OC_STAT	0	RO	LDO8 over-current status 0 : LDO OC doesn't occur or LDO is disabled 1 : LDO OC occurs
		6	LDO7_OC_STAT	0	RO	LDO7 over-current status 0 : LDO OC doesn't occur or LDO is disabled 1 : LDO OC occurs
		5	LDO6_OC_STAT	0	RO	LDO6 over-current status 0 : LDO OC doesn't occur or LDO is disabled 1 : LDO OC occurs
		4	LDO5_OC_STAT	0	RO	LDO5 over-current status 0 : LDO OC doesn't occur or LDO is disabled 1 : LDO OC occurs
		3	LDO4_OC_STAT	0	RO	LDO4 over-current status 0 : LDO OC doesn't occur or LDO is disabled 1 : LDO OC occurs
		2	LDO3_OC_STAT	0	RO	LDO3 over-current status 0 : LDO OC doesn't occur or LDO disabled 1 : LDO OC occurs
		1	LDO2_OC_STAT	0	RO	LDO2 over-current status 0 : LDO OC doesn't occur or LDO is disabled 1 : LDO OC occurs
		0	LDO1_OC_STAT	0	RO	LDO1 over-current status 0 : LDO OC doesn't occur or LDO is disabled 1 : LDO OC occurs

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x15	LDO_PG_STAT	7	LDO8_PGB_STAT	0	RO	LDO8 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs
		6	LDO7_PGB_STAT	0	RO	LDO7 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs
		5	LDO6_PGB_STAT	0	RO	LDO6 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs
		4	LDO5_PGB_STAT	0	RO	LDO5 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs
		3	LDO4_PGB_STAT	0	RO	LDO4 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs
		2	LDO3_PGB_STAT	0	RO	LDO3 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs
		1	LDO2_PGB_STAT	0	RO	LDO2 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs
		0	LDO1_PGB_STAT	0	RO	LDO1 power good fault status 0 : LDO PGB doesn't occur or LDO is disabled 1 : LDO PGB occurs

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x16	BASE_MASK	7	VDDAUV_MASK	0	RW	VDDAUV mask 0 : Interrupt is not masked (default) 1 : Interrupt is masked
		6	VREF_MASK	1	RW	BASE VREF mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		5:3	Reserved	111	RW	
		2	OTP2_MASK	1	RW	OTP2 mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		1	OTP1_MASK	1	RW	OTP1 mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		0	OTP0_MASK	1	RW	OTP0 mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x17	LDO_OC_MASK	7	LDO8_OC_MASK	1	RW	LDO8 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		6	LDO7_OC_MASK	1	RW	LDO7 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		5	LDO6_OC_MASK	1	RW	LDO6 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		4	LDO5_OC_MASK	1	RW	LDO5 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		3	LDO4_OC_MASK	1	RW	LDO4 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		2	LDO3_OC_MASK	1	RW	LDO3 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		1	LDO2_OC_MASK	1	RW	LDO2 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		0	LDO1_OC_MASK	1	RW	LDO1 over-current mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x18	LDO_PG_MASK	7	LDO8_PGB_MASK	1	RW	LDO8 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		6	LDO7_PGB_MASK	1	RW	LDO7 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		5	LDO6_PGB_MASK	1	RW	LDO6 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		4	LDO5_PGB_MASK	1	RW	LDO5 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		3	LDO4_PGB_MASK	1	RW	LDO4 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		2	LDO3_PGB_MASK	1	RW	LDO3 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		1	LDO2_PGB_MASK	1	RW	LDO2 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
		0	LDO1_PGB_MASK	1	RW	LDO1 PG Fault Mask 0 : Interrupt is not masked 1 : Interrupt is masked (default)
0x19	LDO_SHDN	7	LDO_OC_SHDN_ALL	0	RW	Anyone of LDO OC state, shut down all LDO channels 0 : LDO OC only shut down itself (default) 1 : LDO OC shut down all channels
		6	LDO_PGB_SHDN_ALL	0	RW	Anyone of LDO PGB state, shut down all LDO channels 0 : LDO PGB only shut down itself (default) 1 : LDO PGB shut down all channels
		5:0	Reserved	000000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x1A	LDO_ON	7	LDO8_ON	0	WC	LDO8 enable control 0 : No function 1 : Enable LDO, and then clear this bit to '0'
		6	LDO7_ON	0	WC	LDO7 enable control 0 : No function 1 : Enable LDO, and then clear this bit to '0'
		5	LDO6_ON	0	WC	LDO6 enable control 0 : No function 1 : Enable LDO, and then clear this bit to '0'
		4	LDO5_ON	0	WC	LDO5 enable control 0 : No function 1 : Enable LDO, and then clear this bit to '0'
		3	LDO4_ON	0	WC	LDO4 Enable Control 0 : No function 1 : Enable LDO, and then clear this bit to '0'
		2	LDO3_ON	0	WC	LDO3 enable control 0 : No function 1 : Enable LDO, and then clear this bit to '0'
		1	LDO2_ON	0	WC	LDO2 enable control 0 : No function 1 : Enable LDO, and then clear this bit to '0'
		0	LDO1_ON	0	WC	LDO1 enable control 0 : No function 1 : Enable LDO, and then clear this bit to '0'

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x1B	LDO_OFF	7	LDO8_OFF	0	WC	LDO8 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'
		6	LDO7_OFF	0	WC	LDO7 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'
		5	LDO6_OFF	0	WC	LDO6 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'
		4	LDO5_OFF	0	WC	LDO5 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'
		3	LDO4_OFF	0	WC	LDO4 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'
		2	LDO3_OFF	0	WC	LDO3 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'
		1	LDO2_OFF	0	WC	LDO2 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'
		0	LDO1_OFF	0	WC	LDO1 disable control 0 : No function 1 : Disable LDO, and then clear this bit to '0'

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x20	LDO1_CTRL1	7	LDO1_EN	0	RWC	Enable control of LDO1 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO1_STCD_TD	00	RW	LDO1 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO1_STBTD	01	RW	Soft-start time of LDO1 control 00 : 0ms (Sync) 01 : 1ms (default) 10 : 2ms 11 : 4ms
0x21	LDO1_CTRL2	7:5	LDO1_VOSEL	000	RW	LDO1 VOUT selection 000 : 1.8V (default) 001 : 2.5V 010 : 2.7V 011 : 2.8V 100 : 2.9V 101 : 3.0V 110 : 3.1V 111 : 3.2V
		4:0	Reserved	00000	RW	
0x22	LDO1_CTRL3	7	Reserved	0	RW	
		6	LDO1_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO1_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO1_NDIS_EN	1	RW	Enable control of LDO1 Output Discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x23	LDO1_CTRL4	7:0	Reserved	00000000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x24	LDO2_CTRL1	7	LDO2_EN	0	RWC	Enable control of LDO2 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO2_STCD_TD	00	RW	LDO2 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO2_STBTD	01	RW	Soft-start time of LDO2 control 00 : 0ms (Sync) 01 : 1ms (default) 10 : 2ms 11 : 4ms
0x25	LDO2_CTRL2	7:5	LDO2_VOSEL	011	RW	LDO2 VOUT selection 000 : 1.8V 001 : 2.5V 010 : 2.7V 011 : 2.8V (default) 100 : 2.9V 101 : 3.0V 110 : 3.1V 111 : 3.2V
		4:0	Reserved	00000	RW	
0x26	LDO2_CTRL3	7	Reserved	0	RW	
		6	LDO2_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO2_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO2_NDIS_EN	1	RW	Enable control of LDO2 Output Discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x27	LDO2_CTRL4	7:0	Reserved	00000000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x28	LDO3_CTRL1	7	LDO3_EN	0	RWC	Enable control of LDO3 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO3_STCD_TD	00	RW	LDO3 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO3_STBTD	01	RW	Soft-start time of LDO3 control 00: 0ms (Sync) 01: 1ms (default) 10: 2ms 11: 4ms
0x29	LDO3_CTRL2	7:5	LDO3_VOSEL	101	RW	LDO3 VOUT selection 000 : 1.7V 001 : 1.8V 010 : 1.9V 011 : 2.5V 100 : 2.7V 101 : 2.8V (default) 110 : 2.9V 111 : 3.0V
		4:0	Reserved	00000	RW	
0x2A	LDO3_CTRL3	7	Reserved	0	RW	
		6	LDO3_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO3_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO3_NDIS_EN	1	RW	Enable control of LDO3 Output Discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x2B	LDO3_CTRL4	7:0	Reserved	00000000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x2C	LDO4_CTRL1	7	LDO4_EN	0	RWC	Enable control of LDO4 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO4_STCD_TD	00	RW	LDO4 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO4_STBTD	01	RW	Soft-start time of LDO4 control 00 : 0ms (Sync) 01 : 1ms (default) 10 : 2ms 11 : 4ms
0x2D	LDO4_CTRL2	7:5	LDO4_VOSEL	101	RW	LDO4 VOUT selection 000 : 1.7V 001 : 1.8V 010 : 1.9V 011 : 2.5V 100 : 2.7V 101 : 2.8V (default) 110 : 2.9V 111 : 3.0V
		4:0	Reserved	00000	RW	
0x2E	LDO4_CTRL3	7	Reserved	0	RW	
		6	LDO4_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO4_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO4_NDIS_EN	1	RW	Enable control of LDO4 output discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x2F	LDO4_CTRL4	7:0	Reserved	00000000	RW	

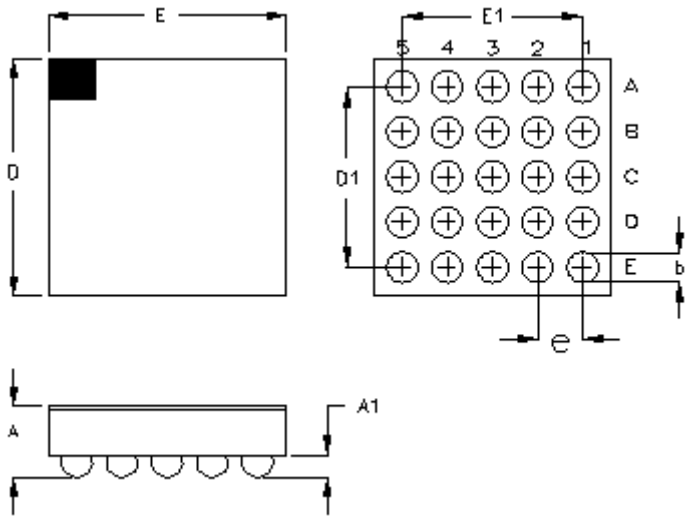
Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x30	LDO5_CTRL1	7	LDO5_EN	0	RWC	Enable control of LDO5 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO5_STCD_TD	00	RW	LDO5 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO5_STBTD	01	RW	Soft-start time of LDO5 control 00 : 0ms (Sync) 01 : 1ms (default) 10 : 2ms 11 : 4ms
0x31	LDO5_CTRL2	7:5	LDO5_VOSEL	101	RW	LDO5 VOUT selection 000 : 1.7V 001 : 1.8V 010 : 1.9V 011 : 2.5V 100 : 2.7V 101 : 2.8V (default) 110 : 2.9V 111 : 3.0V
		4:0	Reserved	00000	RW	
0x32	LDO5_CTRL3	7	Reserved	0	RW	
		6	LDO5_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO5_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO5_NDIS_EN	1	RW	Enable control of LDO5 Output Discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x33	LDO5_CTRL4	7:0	Reserved	00000000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x34	LDO6_CTRL1	7	LDO6_EN	0	RWC	Enable control of LDO6 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO6_STCD_TD	00	RW	LDO6 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO6_STBTD	01	RW	Soft-start time of LDO6 control 00 : 0ms (Sync) 01 : 1ms (default) 10 : 2ms 11 : 4ms
0x35	LDO6_CTRL2	7:5	LDO6_VOSEL	101	RW	LDO6 VOUT selection 000 : 1.7V 001 : 1.8V 010 : 1.9V 011 : 2.5V 100 : 2.7V 101 : 2.8V (default) 110 : 2.9V 111 : 3.0V
		4:0	Reserved	00000	RW	
0x36	LDO6_CTRL3	7	Reserved	0	RW	
		6	LDO6_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO6_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO6_NDIS_EN	1	RW	Enable control of LDO6 Output Discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x37	LDO6_CTRL4	7:0	Reserved	00000000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x38	LDO7_CTRL1	7	LDO7_EN	0	RWC	Enable control of LDO7 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO7_STCD_TD	00	RW	LDO7 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO7_STBTD	01	RW	Soft-start time of LDO7 control 00 : 0ms (Sync) 01 : 1ms (default) 10 : 2ms 11 : 4ms
0x39	LDO7_CTRL2	7:5	LDO7_VOSEL	100	RW	LDO7 VOUT selection 000 : 0.90V 001 : 0.95V 010 : 1.00V 011 : 1.05V 100 : 1.10V (default) 101 : 1.15V 110 : 1.20V 111 : 1.80V
		4:0	Reserved	00000	RW	
0x3A	LDO7_CTRL3	7	Reserved	0	RW	
		6	LDO7_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO7_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO7_NDIS_EN	1	RW	Enable control of LDO7 Output Discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x3B	LDO7_CTRL4	7:0	Reserved	00000000	RW	

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x3C	LDO8_CTRL1	7	LDO8_EN	0	RWC	Enable control of LDO8 0 : Disable (default) 1 : Enable Note : Clear by VDDAUV/OT/OC/PGB event
		6	Reserved	0	RW	
		5	Reserved	1	RW	
		4	Reserved	1	RW	
		3:2	LDO8_STCD_TD	00	RW	LDO8 soft-start count down 00 : 1ms (default) 01 : 2ms 10 : 4ms 11 : 8ms
		1:0	LDO8_STBTD	01	RW	Soft-start time of LDO8 control 00 : 0ms (Sync) 01 : 1ms (default) 10 : 2ms 11 : 4ms
0x3D	LDO8_CTRL2	7:5	LDO8_VOSEL	100	RW	LDO8 VOUT selection 000 : 0.855V 001 : 0.9V 010 : 0.95V 011 : 1V 100 : 1.04V (default) 101 : 1.09V 110 : 1.14V 111 : 1.71V
		4:0	Reserved	00000	RW	
0x3E	LDO8_CTRL3	7	Reserved	0	RW	
		6	LDO8_OCFB_EN	1	RW	Enable control of OCFB function 0 : Disable 1 : Enable (default)
		5:4	LDO8_OCFB_TD	10	RW	Deglitch time of OCFB 00 : 10μs 01 : 15μs 10 : 60μs (default) 11 : 100μs
		3	Reserved	0	RW	
		2	LDO8_NDIS_EN	1	RW	Enable control of LDO8 Output Discharge 0 : Disable 1 : Enable (default)
		1:0	Reserved	00	RW	
0x3F	LDO8_CTRL4	7:0	Reserved	00000000	RW	

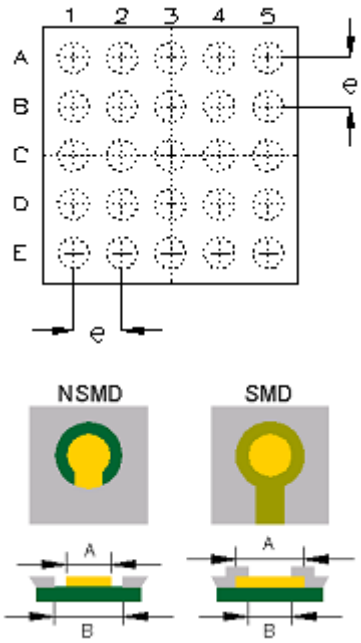
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.140	0.200	0.006	0.008
b	0.210	0.270	0.008	0.011
E	1.800	1.880	0.071	0.074
E1	1.400		0.055	
D	1.800	1.880	0.071	0.074
D1	1.400		0.055	
e	0.350		0.014	

25B WL-CSP 1.84x1.84 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.84x1.84-25(BSC)	25	NSMD	0.350	0.220	0.320	±0.025
		SMD		0.250	0.220	

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