Power Management Unit Total Power Solution for SSD

General Description

The RT5142 offers highly-integrated multi-channel system power management solutions to meet the performance, efficiency, and feature requirements.

The RT5142 incorporates four buck regulators and two LDOs that deliver several output voltages. This provides flexibility to support applications of different VIDs with a configurable power-on sequence.

The RT5142 supplies 8 configurable GPIOs for system hardware control requirements. These GPIOs can be configured for multiple purposes, such as, PWRDIS/ Sleep/ Deep Sleep settings for PMIC state machine control, Buck1/2 Enable/Disable setting, Buck3/4 VID control setting, POR_RST_N pin for monitoring PMIC power good and can also be configured as two sets External_EN and External_PG signals. In addition, the GPIOs also support three-state through I^2C interface configuration when the RT5142 works in the normal mode.

Applications

- SSD

Marking Information

2ZXXYY CCC-RRR YMDNN ●	2Z: Product Code XXYY: Wafer ID with Check Sum CCC-RRR: IC Coordinate (X, Y) YMDNN: Date Code

Features

- **Input Supply Voltage Range: 2.7V to 3.7V.**
- **Highly Efficient Programmable Regulators**
  - **BUCK 1: 1.7V to 2.9V, 20mV per step; 4A**
  - **BUCK 2: 0.9V to 2.0V, 10mV per step; 2A**
  - **BUCK 3: 0.5V to 1.3V, 10mV per step; 4A**
  - **BUCK 4: 0.9V to 2.0V, 10mV per step; 2A**
  - **LDO 1: 1.0V to 2.7V, 50mV per step; 400mA**
  - **LDO 2: 1.0V to 2.7V, 50mV per step; 400mA**
- **Configurable Outputs**
  - **±1.5% Feedback Voltage Accuracy for Full Temperature Range (–40°C to 125°C)**
  - **DVID Change for all Bucks Via I^2C Interface**
  - **Enable Time for All VRs**
  - **Soft-start Time for All VRs**
  - **Selectable Switching Frequency for Every Buck Rail**
- **Input OV/UV Warning Indication and Fault Protection**
- **Outputs OV/UV/OC Fault Protection**
- **Thermal Shutdown Protection**
- **Diode Emulation Mode for Light-Load, High Efficiency Operation**
- **Non-Volatile Register Configurability**
- **I^2C Interface 400kHz/1MHz/3.4MHz**
- **8 GPIOs Multi-functions for Control and Command unit**
  - **POR_RST_N for ASIC to RESET PMIC**
  - **IRQ_N Interrupt Flag**
  - **PWRDIS, SLEEP, Deep SLEEP**
  - **Buck1/2 Enable/Disable**
  - **2 Sets EXT_EN_I and EXT_EN_O**
  - **Buck1/2/3/4 and LDO1/2 Selection by GPIOx**
- **Ambient Temperature Range: –40°C to 85°C**
- **Junction Temperature Range: –40°C to 125°C**

Ordering Information

RT5142□-05

- Trim Version
- Package Type
  WSC : WL-CSP-36B 2.66x2.70 (BSC)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020

Pin Configuration

(TOP VIEW)

A1 SW_B1	A2 SW_B1	A3 PGND12	A4 SW_B2	A5 VIN_B2	A6 VIN_LDO1
B1 VIN_B1	B2 VIN_B1	B3 PGND12	B4 PGND12	B5 FB_B2	B6 LDO1
C1 GPIO3	C2 GPIO7	C3 FB_B1	C4 AGND	C5 GPIO6	C6 LDO2
D1 GPIO2	D2 SCL	D3 SDA	D4 GPIO5	D5 FB_B3	D6 AVIN
E1 FB_B4	E2 GPIO8	E3 GPIO1	E4 PGND34	E5 GPIO4	E6 VIN_B3
F1 VIN_B4	F2 SW_B4	F3 PGND34	F4 PGND34	F5 SW_B3	F6 SW_B3

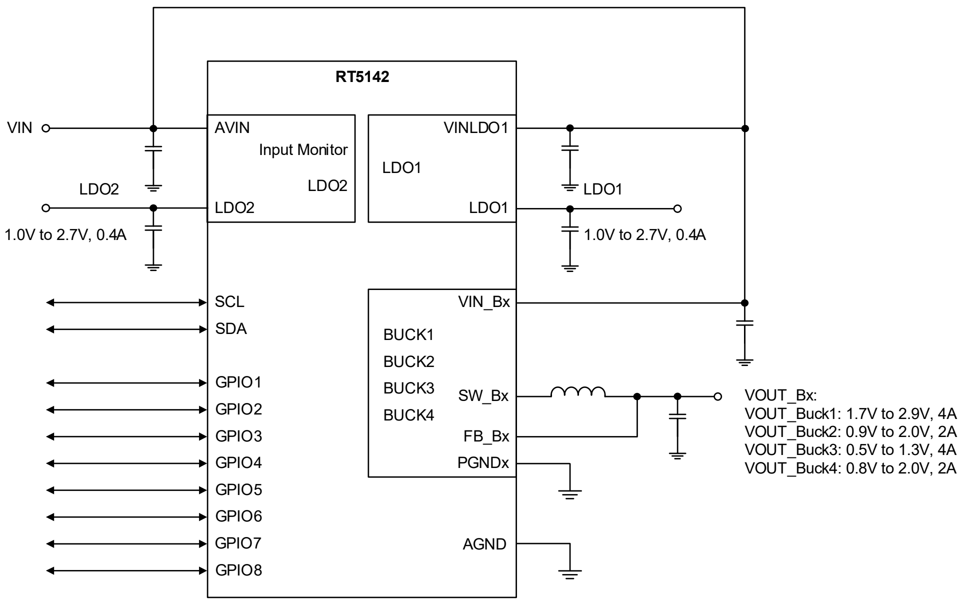
WL-CSP-36B 2.66x2.70 (BSC)

Part Number Version Table

Part Number	Status	VIN (V)	VOUT (V)						
			BUCK1 (B1)	BUCK2 (B2)	BUCK3 (B3)		BUCK4 (B4)	LDO1 (L1)	LDO2 (L2)
					Normal	Sleep			
RT5142WSC-05	H	3.3	PLSW	BUCK = 1.2	BUCK = 0.83	BUCK = 0.83	BUCK = 1.1	LDO = 1.8	LDO = 1.8
	Hi-Z	3.3	BUCK = 2.5	BUCK = 1.2	BUCK = 0.8	BUCK = 0.75	LDO = 1.8	PLSW	X
	L	3.3	BUCK = 2.9	BUCK = 1.2	BUCK = 0.85	BUCK = 0.73	BUCK = 1.2	LDO = 1.8	PLSW

Note: The status "H" is the corresponding GPIO2/3/4/6 high level voltage, "Hi-Z" is floating, and "L" is low level voltage. PLSW is P-type Load Switch

Simplified Application Circuit

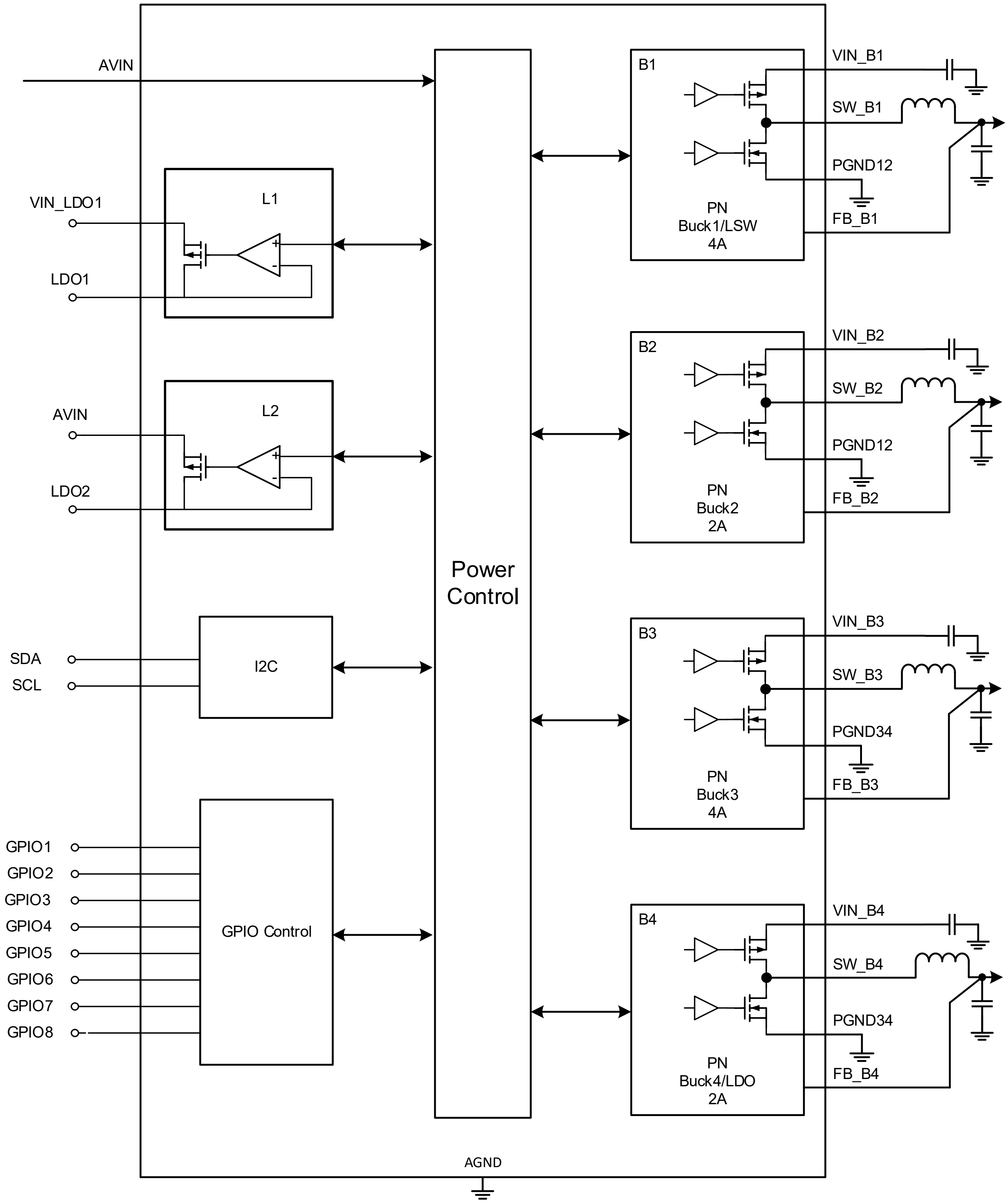


Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, A2	SW_B1	Switch node of Buck1. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
A3, B3, B4	PGND12	Power Stage Power Ground for Buck1 and Buck2. Ground return from low-side power MOSFET and driver of Buck1/2. Directly soldering to a large PCB PGND plane and connecting thermal vias under PGND pin are required to minimize the parasitic impedance and thermal resistance.
A4	SW_B2	Switch node of Buck2. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
A5	VIN_B2	Buck2 Input voltage pins. It is internally connected to the source terminal of Buck2 high-side MOSFET. And connecting the ceramic capacitor (C = 10μF/0603) as close as possible from VIN_B2 pin to PGND12 pin is necessary.
A6	VIN_LDO1	LDO1 input supply. Connecting the ceramic capacitor (C = 2.2μF/0402) as close as possible from VIN_LDO1 pin to PGND pin is necessary.
B1, B2	VIN_B1	Buck1 Input voltage pins. It is internally connected to the source terminal of Buck1 high-side MOSFET. And connecting the ceramic capacitor (C = 10μF/0603) as close as possible from VIN_B1 pin to PGND12 pin is necessary.
B5	FB_B2	Buck2 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power Good of Buck2. And connect to the Buck2 Output Capacitor.
B6	LDO1	LDO1 output. To ensure stability of the LDO, it is recommended to Connecting the ceramic capacitor (C = 2.2μF/0402)
C1	GPIO3	The default function of GPIO3 is General GPIO1(as EXT_EN1_O) output pin with an Open Drain type, requiring an external pull-up resistor. Once the AVIN exceeds the UVLO threshold, the user can select GPIO3 to perform one of the other nine available functions.
C2	GPIO7	The default function of GPIO7 is PWRDIS (Power Disable) input pin with an Open Drain type, requiring an external pull-up resistor. Once the AVIN exceeds the UVLO threshold, the user can select GPIO6 to perform one of the other nine available functions.
C3	FB_B1	Buck1 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power Good of Buck1. And connect to the Buck1 Output Capacitor.
C4	AGND	Ground of internal analog circuitry. AGND must be connected to the PGND plane through a single point.
C5	GPIO6	The default function of GPIO6 is General GPIO1(as EXT_EN1_O) output pin with an Open Drain type, requiring an external pull-up resistor. Once the AVIN exceeds the UVLO threshold, the user can select GPIO6 to perform one of the other nine available functions.
C6	LDO2	LDO2 output. To ensure stability of the LDO, it is recommended to Connecting the ceramic capacitor(C = 2.2μF/0402).
D1	GPIO2	The default function of GPIO2 is General GPIO1(as EXT_EN1_O) output pin with an Open Drain type, requiring an external pull-up resistor. Once the AVIN exceeds the UVLO threshold, the user can select GPIO2 to perform one of the other nine available functions.
D2	SCL	I^2C clock pin. This pin is the input of serial bus clock signal.
D3	SDA	I^2C data pin. This pin is the input and output of serial bus data signal.

Pin No.	Pin Name	Pin Function
D4	GPIO5	The default function of GPIO5 is nIRQ (Negative Interrupt Request) output pin with an Open Drain type, requiring an external pull-up resistor. Once the AVIN exceeds the UVLO threshold, the user can select GPIO5 to perform one of the other nine available functions.
D5	FB_B3	Buck3 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power Good of Buck3. And connect to the Buck3 Output Capacitor.
D6	AVIN	Input voltage pin of internal analog circuitry. Connecting the ceramic capacitor (C = 2.2μF/0402) as close as possible from AVIN pin to AGND pin is necessary. It is also used to detect input voltage status for VIN OV and UV.
E1	FB_B4	Buck4 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power Good of Buck4. And connect to the Buck4 Output Capacitor.
E2	GPIO8	The default function of GPIO8 is Sleep Mode 2 (Deeper Sleep Mode, PS4) input pin with an Open Drain type, requiring an external pull-up resistor. Once the AVIN exceeds the UVLO threshold, the user can select GPIO4 to perform one of the other nine available functions.
E3	GPIO1	GPIO1 is output pin and is fixed to nRESET (POR_RST_N) signal. After Buck1 power-up sequence, nRESET = H indicates PMIC Power Good (PG), while nRESET = L indicates Power Bad (PBAD).
E4, F3, F4	PGND34	Power Stage Power Ground for Buck3 and Buck4. Ground return from low-side power MOSFET and driver of Buck3/4. Directly soldering to a large PCB PGND plane and connecting thermal vias under PGND pin are required to minimize the parasitic impedance and thermal resistance.
E5	GPIO4	The default function of GPIO4 is General GPIO1(as EXT_EN1_O) output pin with an Open Drain type, requiring an external pull-up resistor. Once the AVIN exceeds the UVLO threshold, the user can select GPIO4 to perform one of the other nine available functions.
E6	VIN_B3	Buck3 Input voltage pins. It is internally connected to the source terminal of Buck3 high-side MOSFET. And connecting the ceramic capacitor (C = 10μF/0603) as close as possible from VIN_B3 pin to PGND34 pin is necessary.
F1	VIN_B4	Buck4 Input voltage pins. It is internally connected to the source terminal of Buck4 high-side MOSFET. And connecting the ceramic capacitor (C = 10μF/0603) as close as possible from VIN_B4 pin to PGND34 pin is necessary.
F2	SW_B4	Switch node of Buck4. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
F5, F6	SW_B3	Switch node of Buck3. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN -- –0.3V to 6V
- VIN_B1, VIN_B2, VIN_B3, VIN_B4, AVIN, VIN_LDO1 -------------------------- –0.3V to 6V
- SWx to PGNDx (DC) -- –0.3V to 6V
- SWx to PGNDx (<100ns) -- –0.3V to 6.5V
- SWx to PGNDx (<10ns) --- –2.5V to 9.0V
- PGNDx to AGNDx --- –0.3V to 0.3V
- Other Pins to AGNDx -- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-36B 2.66x2.70 (BSC) --- 3.5W
- Package Thermal Resistance (Note 2)

  WL-CSP-36B 2.66x2.70 (BSC), θ_{JA} -------------------------------- 28.56°C/W
- Lead Temperature (Soldering, 10 sec) ------------------------------------- 260°C
- Junction Temperature --- 150°C
- Storage Temperature Range -- –65°C to 150°C
- ESD Susceptibility (Note3)

  HBM (Human Body Model) --- ±2kV

  CDM (Charge Device Model) -- ±500V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage --- 2.7V to 3.7V
- Other Pins --- 0V to 5.5V
- Ambient Temperature Range -- –40°C to 85°C
- Junction Temperature Range --- –40°C to 125°C

Electrical Characteristics

(VIN_B1 = VIN_B2 = VIN_B3 = VIN_B4 = AVIN = VIN_LDO1 = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Inputs Voltage Range						
VIN_B1 to PGND12 VIN_B2 to PGND12 VIN_B3 to PGND34 VIN_B4 to PGND34	V_{VIN_Bx}	Input voltage range	2.7	--	3.7	V
VIN_LDO1 to AGND	V_{VIN_LDO1}	LDO Mode	1.62	--	5.5	V
	$V_{VIN\_LDO1\_NLSW}$	NLSW Mode	0.4	--	3.6	V
	$V_{VIN\_LDO1\_PLSW}$	PLSW Mode	1.62	--	AVIN	V
AVIN UVLO	$V_{AVIN\_UV\_F\_TH}$	Falling Threshold	2.4	2.5	2.6	V
	$V_{AVIN\_UVLO\_HYS}$	Hysteresis	--	100	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AVIN OV	$V_{AVIN\_OV\_R\_TH}$	Rising Threshold	3.8	3.9	4	V
	$V_{AVIN\_OV\_HYS}$	Hysteresis	--	300	--	mV
AVIN POK OV	$V_{AVIN\_POK\_R\_TH}$	REG_0x10_bit 7 = 0b, Rising Threshold	3.38	3.5	3.62	V
		REG_0x10_bit 7 = 1b, Rising Threshold	3.66	3.8	3.93	V
	$V_{AVIN\_POK\_HYS}$	Hysteresis	100	200	300	mV
	$t_{AVIN\_POK\_R\_DEG}$	Deglitch Time	--	10	--	μs
Operating Supply Current						
AVIN Supply Current	I_{AVIN_Q}	All Rails Off	--	30	--	μA
VIN_LDO1	$I_{VIN\_LDO1\_Q}$	Normal Mode	--	31	--	μA
	$I_{VIN\_LDO1\_LPM\_Q}$	Low Power Mode, LPM	--	15	--	μA
VIN_Bx	$I_{VIN\_Bx\_Q}$	Normal Mode	--	25	35	μA
	$I_{VIN\_Bx\_LPM\_Q}$	Low Power Mode	--	15	25	μA
System Monitor/Warning						
SYSMON Rising Threshold	$V_{SYSMON\_R\_TH}$	25mV Step	2.725	--	3.1	V
SYSMON Accuracy			–3.5	--	3.5	%
SYSWARN Rising Threshold	$V_{SYSWARN\_R\_TH}$	25mV Step	2.755	--	3.15	V
SYSWARN Accuracy			–3.5	--	3.5	%
Input Deglitch Time						
AVIN UV	$t_{AVIN\_UV\_R\_EXIT}$		--	20	--	μs
AVIN OV	$t_{AVIN\_OV\_R\_TH}$		--	10	--	μs
Others						
Thermal Shutdown	$T_{Critical\_SD}$	Temperature for Critical Shutdown	--	150	--	°C
	$T_{Recovery\_HYS}$	Hysteresis for Thermal Recovery	--	25	--	°C
	$T_{Interrupt\_TH}$	Interrupt Flag Threshold	--	110	--	°C
OV/UV Retry Time	$t_{Recovery\_Dwell\_Time}$	VIN = 3.3V, Power Rails OV or UV	--	200	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Bx Startup Delay		Bx_ON_DLY_Bits = 000b	--	0	--	ms
		Bx_ON_DLY_Bits = 001b	--	0.25	--	ms
		Bx_ON_DLY_Bits = 010b	--	0.5	--	ms
		Bx_ON_DLY_Bits = 011b	--	0.75	--	ms
		Bx_ON_DLY_Bits = 100b	--	1	--	ms
		Bx_ON_DLY_Bits = 101b	--	2	--	ms
		Bx_ON_DLY_Bits = 110b	--	4	--	ms
		Bx_ON_DLY_Bits = 111b	--	8	--	ms
Bx Turn Off Delay		Bx_OFF_DLY_Bits = 000b	--	0	--	ms
		Bx_OFF_DLY_Bits = 001b	--	0.25	--	ms
		Bx_OFF_DLY_Bits = 010b	--	0.5	--	ms
		Bx_OFF_DLY_Bits = 011b	--	0.75	--	ms
		Bx_OFF_DLY_Bits = 100b	--	1	--	ms
		Bx_OFF_DLY_Bits = 101b	--	2	--	ms
		Bx_OFF_DLY_Bits = 110b	--	4	--	ms
		Bx_OFF_DLY_Bits = 111b	--	8	--	ms
EXT_EN Delay		EXT_EN1_DLY_Bits = 0000b	--	0	--	ms
		EXT_EN1_DLY_Bits = 0001b	--	0.25	--	ms
		EXT_EN1_DLY_Bits = 0010b	--	0.5	--	ms
		EXT_EN1_DLY_Bits = 0011b	--	0.75	--	ms
		EXT_EN1_DLY_Bits = 0100b	--	1	--	ms
		EXT_EN1_DLY_Bits = 0101b	--	1.25	--	ms
		EXT_EN1_DLY_Bits = 0110b	--	1.5	--	ms
		EXT_EN1_DLY_Bits = 0111b	--	1.75	--	ms
		EXT_EN1_DLY_Bits = 1000b	--	2	--	ms
		EXT_EN1_DLY_Bits = 1001b	--	2.25	--	ms
		EXT_EN1_DLY_Bits = 1010b	--	2.5	--	ms
		EXT_EN1_DLY_Bits = 1011b	--	2.75	--	ms
		EXT_EN1_DLY_Bits = 1100b	--	3	--	ms
		EXT_EN1_DLY_Bits = 1101b	--	3.25	--	ms
		EXT_EN1_DLY_Bits = 1110b	--	3.5	--	ms
		EXT_EN1_DLY_Bits = 1111b	--	3.75	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
nRESET		POR_DLY_TIME_Bits = 000b	--	0.5	--	ms
		POR_DLY_TIME_Bits = 001b	--	1	--	ms
		POR_DLY_TIME_Bits = 010b	--	2	--	ms
		POR_DLY_TIME_Bits = 011b	--	4	--	ms
		POR_DLY_TIME_Bits = 100b	--	8	--	ms
		POR_DLY_TIME_Bits = 101b	--	16	--	ms
		POR_DLY_TIME_Bits = 110b	--	32	--	ms
		POR_DLY_TIME_Bits = 111b	--	64	--	ms
Buck1 Converter						
Output Voltage Range	V_{B1_VOUT}	B1 (Buck1) VID Range	1.7	--	2.9	V
	$V_{B1\_Per\_Step}$	B1 Programmable Step	--	20	--	mV
Standby Current	$I_{Standby\_B1}$	Enable, no Switching	--	25	35	μA
		Enable, no Switching, LPM	--	15	25	μA
Output voltage Accuracy	V_{B1_Error}	GPIO2 = Hi-Z	2.475	2.5	2.525	V
		GPIO2 = L	2.871	2.9	2.929	
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		I_{OUT} = 0 to Max Rating	--	0.5	--	%/A
Transient Load Regulation	$V_{B1\_TLR\_Error}$	VIN_B1 = 3.3V, FB1 = 2.5V, L = 0.47μH, C_{OUT} = 22μF x 2. 1. Load = 1A to 2A @ 0.2A/μs 2. Load = 50mA to 1A @ 0.2A/μs	–75 (–3%)	--	100 (4%)	mV
PG Threshold (Low Level)	$V_{B1\_PGL\_R\_0b}$	VOUT_B1 rises from 0V to PG Rising (EFUSE_UVSEL = 0b, Default)	90	93	96	%
	$V_{B1\_PGL\_R\_1b}$	VOUT_B1 rises from 0V to PG Rising (EFUSE_UVSEL = 1b)	82	85	88	%
	$V_{B1\_PGL\_HYS}$	VOUT_B1 falls from VID to PG Falling	--	3	--	%
PG Threshold (High Level)	$V_{B1\_PGH\_F}$	VOUT_B1 rises from VID to PG Falling	107	110	113	%
	$V_{B1\_PGH\_HYS}$	VOUT_B1 falls from VID to PG Rising	--	3	--	%
Switching Frequency	f_{SW_B1}	REG_0x1B[3:1] = 101b	1.8	2	2.2	MHz
Min Off-Time	$t_{B1\_OFF\_MIN}$		--	120	160	ns
Soft-Start Time	$t_{B1\_Soft\_Start}$	REG_0x19[7:6] = 00b	--	125	200	μs
		REG_0x19[7:6] = 01b (Default)	--	250	400	μs
		REG_0x19[7:6] = 10b	--	500	800	μs
		REG_0x19[7:6] = 11b	--	750	1200	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit	I_{B1_CL}	Valley Current, REG_0x1B[7:6] = 00b	3.5	4	--	A
		Valley Current, REG_0x1B[7:6] = 01b	4.5	5	--	A
		Valley Current, REG_0x1B[7:6] = 10b	5.5	6	--	A
		Valley Current, REG_0x1B[7:6] = 11b	6.5	7	--	A
PMOS On-Resistance	$R_{DS(ON)\_B1\_P}$	PVIN = 3.3V	--	60	--	mΩ
NMOS On-Resistance	$R_{DS(ON)\_B1\_N}$	PVIN = 3.3V	--	35	--	mΩ
Output Discharge Resistance	R_{DISCH_B1}		--	4.4	--	Ω
Efficiency	Eff_{B1}	PVIN = 3.3V, FB_B1 = 2.5V, I_{OUT} = 10mA	85	--	--	%
		PVIN = 3.3V, FB_B1 = 2.5V, I_{OUT} = 1A	90	--	--	%
Buck1 Bypass Mode						
Input Voltage Range	$V_{VIN\_B1\_BYP}$	GPIO2 = H	2.7	3.3	3.7	V
PMOS On-Resistance	$R_{DS(ON)\_B1\_BYP\_P}$	I_{SW} = –1A, VIN_B1 = 3.3V	--	60	--	mΩ
Internal PMOS Shutdown Current	$I_{B1\_BYP\_OC\_OFF}$	REG_0x1B[7:6] = xxb, all registers code (00~11) are same OC value	4.5	5	--	A
Internal PMOS Shutdown Current Off Time	$t_{B1\_BYP\_OC\_OFF}$		--	14	--	ms
Internal PMOS Soft-Start Time	$t_{B1\_BYP\_SStart}$	PVIN = 3.3V	--	250	--	μs
OV Threshold	$V_{B1\_BYP\_OV\_TH}$		--	3.8	--	V
OV Deglitch Time	$t_{B1\_BYP\_OV\_DEG}$		--	20	--	μs
Buck2 Converter						
Output Voltage Range	V_{B2_VOUT}	B2 (Buck2) VID Range	0.9	--	2.0	V
	$V_{B2\_Per\_Step}$	B2 Programmable Step	--	10	--	mV
Standby Current	$I_{Standby\_B2}$	Enable, no Switching	--	25	35	μA
		Enable, no Switching, LPM	--	15	25	μA
Output voltage Accuracy	V_{B2_Error}	Valley Accuracy	1.188	1.2	1.212	V
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		I_{OUT} = 0 to Max Rating	--	0.5	--	%/A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transient Load Regulation	$V_{B2\_TLR\_Error}$	VIN_B2 = 3.3V, FB2 = 1.2V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 1A to 2A @ 0.2A/μs 2. Load = 50mA to 1A @ 0.2A/μs	–36 (–3%)	--	48 (4%)	mV
PG Threshold (Low Level)	$V_{B2\_PGL\_R\_0b}$	VOUT_B2 rises from 0V to PG Rising (EFUSE_UVSEL = 0b, Default)	90	93	96	%
	$V_{B2\_PGL\_R\_1b}$	VOUT_B2 rises from 0V to PG Rising (EFUSE_UVSEL = 1b)	82	85	88	%
	$V_{B2\_PGL\_HYS}$	VOUT_B2 falls from VID to PG Falling	--	3	--	%
PG Threshold (High Level)	$V_{B2\_PGH\_F}$	VOUT_B2 rises from VID to PG Falling	107	110	113	%
	$V_{B2\_PGH\_HYS}$	VOUT_B2 falls from VID to PG Rising	--	3	--	%
Switching Frequency	f_{SW_B2}	REG_0x1D[3:1] = 101b	1.8	2	2.2	MHz
Soft-Start Time	$t_{B2\_Soft\_Start}$	REG_0x19[5:4] = 00b	--	125	200	μs
		REG_0x19[5:4] = 01b (Default)	--	250	400	μs
		REG_0x19[5:4] = 10b	--	500	800	μs
		REG_0x19[5:4] = 11b	--	750	1200	us
Current Limit	I_{B2_CL}	Valley Current, REG_0x1D[7:6] = 00b	1.5	2	--	A
		Valley Current, REG_0x1D[7:6] = 01b	2.5	3	--	A
		Valley Current, REG_0x1D[7:6] = 10b	3.5	4	--	A
		Valley Current, REG_0x1D[7:6] = 11b	4.5	5	--	A
PMOS On-Resistance	$R_{DS(ON)\_B2\_P}$	PVIN = 3.3V	--	65	--	mΩ
NMOS On-Resistance	$R_{DS(ON)\_B2\_N}$	PVIN = 3.3V	--	30	--	mΩ
Output Discharge Resistance	R_{DISCH_B2}		--	9.4	--	Ω
Efficiency	Eff_{B2}	PVIN = 3.3V, FB_B1 = 1.2V, I_{OUT} = 10mA	85	--	--	%
		PVIN = 3.3V, FB_B1 = 1.2V, I_{OUT} = 1A	85	--	--	%
Buck3 Converter						
Output Voltage Range	V_{B3_VOUT}	B3 (Buck3) VID Range	0.5	--	1.3	V
	$V_{B3\_Per\_Step}$	B3 Programmable Step	--	10	--	mV
Standby Current	$I_{Standby\_B3}$	Enable, no Switching	--	25	35	μA
		Enable, no Switching, LPM	--	15	25	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output voltage Accuracy	V_{B3_Error}	GPIO3 = H	0.8217	0.83	0.8383	V
		GPIO3 = Hi-Z	0.792	0.8	0.808	
		GPIO3 = L	0.8415	0.85	0.8585	
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		I_{OUT} = 0 to Max Rating	--	0.5	--	%/A
Transient Load Regulation	$V_{B3\_TLR\_Error}$	VIN_B3 = 3.3V, FB3 = 0.8V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 2A to 4A @ 0.2A/μs 2. Load = 50mA to 2A @ 0.2A/μs	–28 (–3.5%)	--	32 (4%)	mV
PG Threshold (Low Level)	$V_{B3\_PGL\_R\_0b}$	VOUT_B3 rises from 0V to PG Rising (EFUSE_UVSEL = 0b, Default)	90	93	96	%
	$V_{B3\_PGL\_R\_1b}$	VOUT_B3 rises from 0V to PG Rising (EFUSE_UVSEL = 1b)	82	85	88	%
	$V_{B3\_PGL\_HYS}$	VOUT_B3 falls from VID to PG Falling	--	3	--	%
PG Threshold (High Level)	$V_{B3\_PGH\_F}$	VOUT_B3 rises from VID to PG Falling	107	110	113	%
	$V_{B3\_PGH\_HYS}$	VOUT_B3 falls from VID to PG Rising	--	3	--	%
Switching Frequency	f_{SW_B3}	REG_0x1F[3:1] = 101b	1.8	2	2.2	MHz
Soft-Start Time	$t_{B3\_Soft\_Start}$	REG_0x19[3:2] = 00b	--	125	200	μs
		REG_0x19[3:2] = 01b (Default)	--	250	400	μs
		REG_0x19[3:2] = 10b	--	500	800	μs
		REG_0x19[3:2] = 11b	--	750	1200	μs
Current Limit	I_{B3_CL}	Valley Current, REG_0x1F[7:6] = 00b	3.5	4	--	A
		Valley Current, REG_0x1F[7:6] = 01b	4.5	5	--	A
		Valley Current, REG_0x1F[7:6] = 10b	5.5	6	--	A
		Valley Current, REG_0x1F[7:6] = 11b	6.5	7	--	A
PMOS On-Resistance	$R_{DS(ON)\_B3\_P}$	PVIN = 3.3V	--	55	--	mΩ
NMOS On-Resistance	$R_{DS(ON)\_B3\_N}$	PVIN = 3.3V	--	25	--	mΩ
Dynamic Voltage Scaling Rate	$V_{DVID\_UP\_B3}$	REG_0x1F[5:4] = 00b	--	20	--	mV/μs
		REG_0x1F[5:4] = 01b	--	15	--	mV/μs
		REG_0x1F[5:4] = 10b	--	10	--	mV/μs
		REG_0x1F[5:4] = 11b	--	5	--	mV/μs
Output Discharge Resistance	R_{DISCH_B3}		--	9.4	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Efficiency	Eff_{B3}	PVIN = 3.3V, FB_B3 = 0.8V, I_{OUT}= 1mA, LPM	80	--	--	%
		PVIN = 3.3V, FB_B3 = 0.8V, I_{OUT} = 1A	85	--	--	%
Buck4 Converter						
Output Voltage Range	V_{B4_VOUT}	B4 (Buck4) VID Range	0.9	--	2.0	V
	$V_{B4\_Per\_Step}$	B4 Programmable Step	--	10	--	mV
Standby Current	$I_{Standbyt\_B4}$	Enable, no Switching	--	25	35	μA
		Enable, no Switching, LPM	--	15	25	μA
Output voltage Accuracy	V_{B4_Error}	GPIO4 = ~~High~~ or L	1.188	1.2	1.212	V
Line Regulation		VIN = 2.7V to 3.7V	--	0.5	--	%/V
Load Regulation		IOUT = 0 to Max Rating	--	0.5	--	%/A
Transient Load Regulation	$V_{B4\_TLR\_Error}$	VIN_B4 = 3.3V, FB4 = 1.2V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 1A to 2A @ 0.2A/μs 2. Load = 50mA to 1A @ 0.2A/μs	–36 (–3%)	--	48 (4%)	mV
		VIN_B4 = 3.3V, FB4 = 1.8V, L = 0.47μH, C_{OUT} = 22μF. 1. Load = 1A to 2A @ 0.2A/μs 2. Load = 50mA to 1A @ 0.2A/μs	–54 (–3%)	--	72 (4%)	mV
PG Threshold (Low Level)	$V_{B4\_PGL\_R\_0b}$	VOUT_B4 rises from 0V to PG Rising (EFUSE_UVSEL = 0b, Default)	90	93	96	%
	$V_{B4\_PGL\_R\_1b}$	VOUT_B4 rises from 0V to PG Rising (EFUSE_UVSEL = 1b)	82	85	88	%
	$V_{B4\_PGL\_HYS}$	VOUT_B4 falls from VID to PG Falling	--	3	--	%
PG Threshold (High Level)	$V_{B4\_PGH\_F}$	VOUT_B4 rises from VID to PG Falling	107	110	113	%
	$V_{B4\_PGH\_HYS}$	VOUT_B4 falls from VID to PG Rising	--	3	--	%
Switching Frequency	f_{SW_B4}	REG_0x22[3:1] = 101b	1.8	2	2.2	MHz
Soft-Start Time	$t_{B4\_Soft\_Start}$	REG_0x19[1:0] = 00b	--	125	200	μs
		REG_0x19[1:0] = 01b (Default)	--	250	400	μs
		REG_0x19[1:0] = 10b	--	500	800	μs
		REG_0x19[1:0] = 11b	--	750	1200	μs
Current Limit	I_{B4_CL}	Valley Current, REG_0x22[7:6] = 00b	1.5	2	--	A
		Valley Current, REG_0x22[7:6] = 01b	2.5	3	--	A
		Valley Current, REG_0x22[7:6] = 10b	3.5	4	--	A
		Valley Current, REG_0x22[7:6] = 11b	4.5	5	--	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PMOS On-Resistance	$R_{DS(ON)\_B4\_P}$	PVIN = 3.3V	--	70	--	mΩ
NMOS On-Resistance	$R_{DS(ON)\_B4\_N}$	PVIN = 3.3V	--	40	--	mΩ
Output Discharge Resistance	R_{DISCH_B4}		--	9.4	--	Ω
Efficiency	Eff_{B3}	PVIN = 3.3V, FB_B4 = 1.2V, I_{OUT} = 10mA, LPM	85	--	--	%
		PVIN = 3.3V, FB_B4 = 1.2V, I_{OUT} = 1A	85	--	--	%
B4_LDO Mode						
Output Voltage Range	$V_{B4\_LDO\_VOUT}$	GPIO4 = Hi-Z	0.9	1.8	2.0	V
Output voltage range	$V_{B4\_LDO\_Per\_Step}$	B4_LDO Programmable Step	--	10	--	mV
Standby Current	$I_{Standby\_B4\_LDO}$	Enabled, No Load, Low Power Mode	--	15	--	μA
		Enabled, No Load	--	31	--	μA
Output voltage Accuracy	$V_{B4\_LDO\_Error}$	AVIN > B4_LDO + 0.4V @ Normal, VNOM = 1.8V (25°C)	-1	--	1	%
		AVIN > B4_LDO + 0.4V@ Normal, VNOM = 1.8V (-40~125°C)	–1.5	--	1.5	%
Line Regulation (GBD) (Note 5)		AVIN = 2.7V to 3.3V, B4_LDO Load 5mA @ Normal, VNOM = 1.8V	--	0.5	--	%/V
Load Regulation (GBD)		AVIN > B4_LDO + 0.4V, Load = 1mA to 390mA @ Normal VNOM = 1.8V	--	0.5	--	%/A
Transient Load Regulation (GBD)	$V_{B4\_LDO\_TLR\_Err}$	AVIN > B4_LDO + 0.4V VNOM = 1.8V, C_{OUT} = 2.2μF 1. Load= 5mA to 50mA @ 0.2A/μs 2. Load= 50mA to 100mA @ 0.2A/μs	–3.5	--	+3.5	%
PG Threshold (Low Level)	$V_{B4\_LDO\_PGL\_R\_0b}$	VOUT_B4_LDO rises from 0V to PG Rising (EFUSE_UVSEL = 0b, Default)	90	93	96	%
	$V_{B4\_LDO\_PGL\_R\_1b}$	VOUT_B4_LDO rises from 0V to PG Rising (EFUSE_UVSEL = 1b)	82	85	88	%
	$V_{B4\_LDO\_PGL\_HYS}$	VOUT_B4_LDO falls from VID to PG Falling	--	3	--	%
PG Threshold (High Level)	$V_{B4\_LDO\_PGH\_F}$	VOUT_B4_LDO rises from VID to PG Falling	107	110	113	%
	$V_{B4\_LDO\_PGH\_HYS}$	VOUT_B4_LDO falls from VID to PG Rising	--	3	--	%
Soft-Start Time	$t_{B4\_LDO\_Soft\_Start}$	B4_LDO = 10% to 90% of VNOM, REG_0x19[0] = 0b	--	250	--	μs
		B4_LDO = 10% to 90% of VNOM, REG_0x19[0] = 1b	--	500	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dropout Voltage	$V_{B4\_LDO\_DROP}$	AVIN = 2.7V, B4_LDO = 2.6V, Load = 200mA @ Normal	--	--	200	mV
		AVIN = 2.7V, B4_LDO = 2.5V, Load = 400mA @ Normal	--	--	400	mV
Discharge Resistance	$R_{DISCH\_B4\_LDO}$		--	9.4	--	Ω
Overcurrent Limit	$I_{B4\_LOD\_CL}$	AVIN > B4_LDO + 0.4V @ Normal, REG_0x22[6] = 0b	300	400	--	mA
		AVIN > B4_LDO + 0.4V @ Normal, REG_0x22[6] = 1b (Default)	400	500	--	mA
PG/OV Deglitch Time (GBD)	$t_{B4\_LDO\_PG/OV\_DEG}$		--	20	--	μs
LDO1						
Output Voltage Range	V_{LDO1_VOUT}	LDO1 VID Range, GPIO4 = L	1	1.8	2.7	V
Output Voltage Programmable Step	$V_{LDO1\_Per\_Step}$	LDO1 Programmable Step	--	50	--	mV
Standby Current	$I_{Standby\_LDO1}$	Enabled, No Load, Low Power Mode	--	15	--	μA
		Enabled, No Load	--	31	--	μA
Output voltage Accuracy	V_{LDO1_Error}	AVIN = VIN_LDO1 > LDO1 + 0.4V @ Normal, VNOM = 2.5V (25°C)	−1	--	1	%
		AVIN = VIN_LDO1 > LDO1 + 0.4V@ Normal, VNOM = 2.5V (-40~125°C)	−1.5	--	1.5	%
Line Regulation (GBD)		AVIN = VIN_LDO1 = 2.7V to 3.3V, LDO1 Load 5mA @ Normal, VNOM = 2.5V.	--	0.5	--	%/V
Load Regulation (GBD)		AVIN = VIN_LDO1 > LDO1 + 0.4V, LDO1 Load = 1mA to 390mA @ Normal, VNOM = 2.5V.	--	0.5	--	%/A
Transient Load Regulation (GBD)	$V_{LDO1\_TLR\_Err}$	AVIN = VIN_LDO1 > LDO1 + 0.4V, VNOM = 2.5V, C_{OUT} = 2.2μF 1. Load= 5mA to 50mA @ 0.2A/μs 2. Load= 50mA to 100mA @ 0.2A/μs	−3.5	--	3.5	%
PG Threshold (Low Level)	$V_{LDO1\_PGL\_R}$	V_{LDO1} rises from 0V to PG Rising	81	84	88	%
	$V_{LDO1\_PGL\_HYS}$	V_{LDO1} falls from VID to PG Falling	--	4	--	%
PG Threshold (High Level)	$V_{LDO1\_PGH\_F}$	V_{LDO1} rises from VID to PG Falling	111	114	118	%
	$V_{LDO1\_PGH\_HYS}$	V_{LDO1} falls from OV to PG Rising	--	8	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft-Start Time	$t_{LDO1\_Soft\_Start}$	LDO1 = 10% to 90% of VNOM, REG_0x1A[7] = 0b (Default)	--	180	--	μs
		LDO1 = 10% to 90% of VNOM, REG_0x1A[7] = 1b	--	360	--	μs
Dropout Voltage	V_{LDO1_DROP}	AVIN = VIN_LDO1 = 2.7V, LDO1 = 2.6V, Load = 200mA @ Normal	--	--	200	mV
		AVIN = VIN_LDO1 = 2.7V, LDO1 = 2.5V, Load = 400mA @ Normal	--	--	400	mV
Discharge Resistance	R_{DISCH_LDO1}	Discharged Path Enabled When LDO1 Disabled.	--	20	--	Ω
Overcurrent Limit	I_{LOD1_CL}	AVIN = VIN_LDO1 > LDO1 + 0.4V @ Normal, EFUSE_LDO1_LIM = 0b	300	400	--	mA
		AVIN = VIN_LDO1 > LDO1 + 0.4V @ Normal, EFUSE_LDO1_LIM = 1b	400	500	--	mA
LDO1_LSW Mode (Load Switch)						
Operating Voltage Range	$V_{LDO1\_SW\_VIN}$	NLSW Mode, EFUSE_LDO1_LSW_SEL = 0b	0.4	--	AVIN −1	V
		PLSW Mode (default), EFUSE_LDO1_LSW_SEL = 1b	--	AVIN	--	V
Load Switch On-Resistance	$R_{LDO1\_NSW\_ON}$	NLSW Mode, AVIN = 3.3V, VIN_LDO1 = 0.4V, Load = 100mA	--	50	--	mΩ
	$R_{LDO1\_PSW\_ON}$	PLSW Mode, VIN_LDO1 = 3.3V, Load = 100mA	--	200	--	mΩ
Load Switch Standby Current	$I_{Standby\_LDO1\_SW}$	NLSW Mode, Enabled, No Load, LPM	--	10	--	μA
		NLSW Mode, Enabled, No Load.	--	22	--	μA
		PLSW Mode, Enabled, No Load	--	12	--	μA
Soft-Start Time	$t_{LDO1\_SW\_Soft\_Start}$	NLSW Mode, VIN_LDO1 = 0.8V, LDO1_LSW = 10% to 90%	--	200	--	μs
		PLSW Mode, Enable Soft-Start Current Limit	--	n/a	--	μs
Output Current Limit	$I_{LDO1\_SW\_OC}$	NLSW Mode, EFUSE_LDO1_LIM = 0b (default)	0.45	0.6	--	A
		NLSW Mode, EFUSE_LDO1_LIM = 1b	0.9	1.2	--	A
		PLSW Mode, EFUSE_LDO1_LIM = 0b (default)	0.3	0.4	--	A
		PLSW Mode, EFUSE_LDO1_LIM = 1b	0.4	0.5	--	A
OV Protection Threshold	$V_{LDO1\_SW\_OV}$		--	3.8	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OV Deglitch Time	$t_{LDO1\_SW\_DEG}$		--	20	--	μs
LDO2						
Output Voltage Range	V_{LDO2_VOUT}	LDO2 VID Range, GPIO6 = H	1	1.8	2.7	V
Output Voltage Programmable Step	$V_{LDO2\_Per\_Step}$	LDO1 Programmable Step	--	50	--	mV
Standby Current	$I_{Standby\_LDO2}$	Enabled, No Load, Low Power Mode	--	15	--	μA
		Enabled, No Load	--	31	--	μA
Output voltage Accuracy	V_{LDO2_Error}	AVIN > LDO2 + 0.4V @ Normal, VNOM = 1.8V (25°C)	−1	--	1	%
		AVIN > LDO2 + 0.4V@ Normal, VNOM = 1.8V (−40 to125°C)	−1.5	--	1.5	%
Line Regulation (GBD)		AVIN = 2.7V to 3.3V, LDO2 = 5mA @ Normal, VNOM = 1.8V.	--	0.5	--	%/V
Load Regulation (GBD)		AVIN = LDO2 + 0.4V, LDO2 = 1mA to 390mA @ Normal, VNOM = 1.8V.	--	0.5	--	%/A
Transient Load Regulation (GBD)	$V_{LDO2\_TLR\_Err}$	AVIN > LDO2 + 0.4V, VNOM = 1.8V, C_{OUT} = 2.2μF 1. Load= 5mA to 50mA @ 0.2A/μs 2. Load= 50mA to 100mA @ 0.2A/μs	−3.5	--	+3.5	%
PG Threshold (Low Level)	$V_{LDO2\_PGL\_R}$	V_{LDO2} rises from 0V to PG Rising	81	84	88	%
	$V_{LDO2\_PGL\_HYS}$	V_{LDO2} falls from VID to PG Falling	--	4	--	%
PG Threshold (High Level)	$V_{LDO2\_PGH\_F}$	V_{LDO2} rises from VID to PG Falling	111	114	118	%
	$V_{LDO2\_PGH\_HYS}$	V_{LDO2} falls from OV to PG Rising	--	8	--	%
Soft-Start Time	$t_{LDO2\_Soft\_Start}$	LDO2 = 10% to 90% of VNOM, REG_0x1A[6] = 0b (Default)	--	180	--	μs
		LDO2 = 10% to 90% of VNOM, REG_0x1A[6] = 1b	--	360	--	μs
Dropout Voltage	V_{LDO1_DROP}	AVIN = 2.7V, LDO1 = 2.6V, Load = 200mA @ Normal	--	--	200	mV
		AVIN = 2.7V, LDO1 = 2.5V, Load = 400mA @ Normal	--	--	400	mV
Discharge Resistance	R_{DISCH_LDO2}		--	20	--	Ω
Overcurrent Limit	I_{LOD2_CL}	AVIN > LDO2 + 0.4V @ Normal, EFUSE_LDO2_LIM = 0b. (default)	300	400	--	mA
		AVIN > LDO2 + 0.4V @ Normal, EFUSE_LDO2_LIM = 1b.	400	500	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO2_LSW Mode (Load Switch)						
Operating Voltage Range	$V_{LDO2\_SW\_VIN}$	GPIO6 = L	--	AVIN	--	V
PMOS On-Resistance	$R_{LDO1\_PSW\_ON}$		--	200	--	mΩ
Load Switch Standby Current	$I_{Standby\_LDO2\_SW}$	PLSW Mode, Enabled, No Load	--	12	--	μA
Soft-Start Time	$t_{LDO2\_SW\_Soft\_Start}$	PLSW Mode, Enable Soft-Start Current Limit	--	n/a	--	μs
Output Current Limit	$I_{LDO2\_SW\_OC}$	EFUSE_LDO2_LIM = 0b (default)	0.3	0.4	--	A
		EFUSE_LDO2_LIM = 1b	0.4	0.5	--	A
OV Protection Threshold	$V_{LDO2\_SW\_OV}$		--	3.8	--	V
OV Deglitch Time	$t_{LDO2\_SW\_DEG}$		--	20	--	μs
Digital I/O						
GPIOs Output Low (Open Drain)	V_{GPIOx_L}		--	--	0.55	V
GPIO1/5/6/7/8 Input High	$V_{GPIO1\_5\text{-}8\_VIN\_H}$		1.1	--	--	V
GPIO1/5/6/7/8 Input Low	$V_{GPIO1\_508\_VIN\_L}$		--	--	0.55	V
GPIO2/3/4 Input High	$V_{GPIO2\text{-}4\_VIN\_H}$		2.3	--	--	V
GPIO2/3/4 Input High-Z	$V_{GPIO2\text{-}4\_VIN\_Hi\text{-}Z}$		--	1.35	--	V
GPIO2/3/4 Input Low	$V_{GPIO2\text{-}4\_VIN\_L}$		--	--	0.55	V
I^2C for Fast Mode						
SDA, SCL Input Voltage High			1.2	--	--	V
SDA, SCL Input Voltage Low			--	--	0.4	V
SCL Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time for a Repeated START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	0.6	--	--	μs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Set Up Time For a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	μs
Data Set Up Time	$t_{SU;DAT}$		100	--	--	ns
Set Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between a STOP and a START Condition	t_{BUF}		1.3	--	--	μs
Rising Time of Both SDA/SCL Signals	t_R		20	--	300	ns
Falling Time of Both SDA/SCL Signals	t_F		20	--	300	ns
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

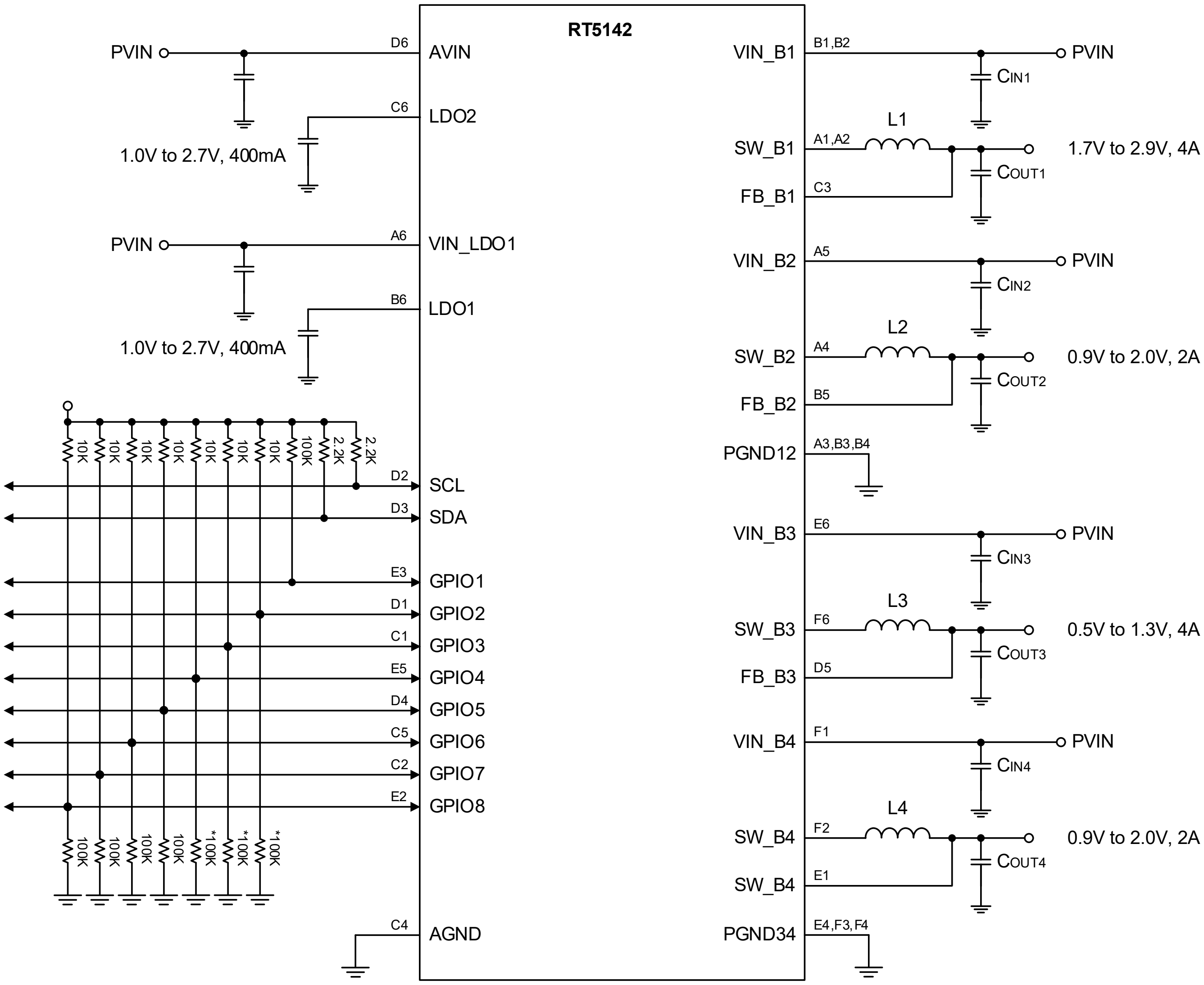
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-9 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

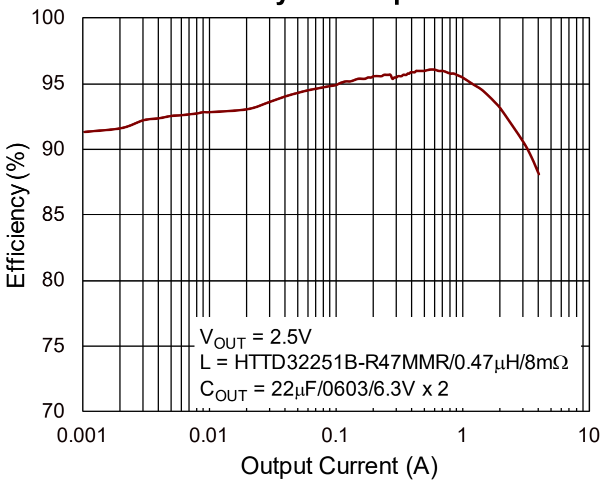
Typical Application Circuit



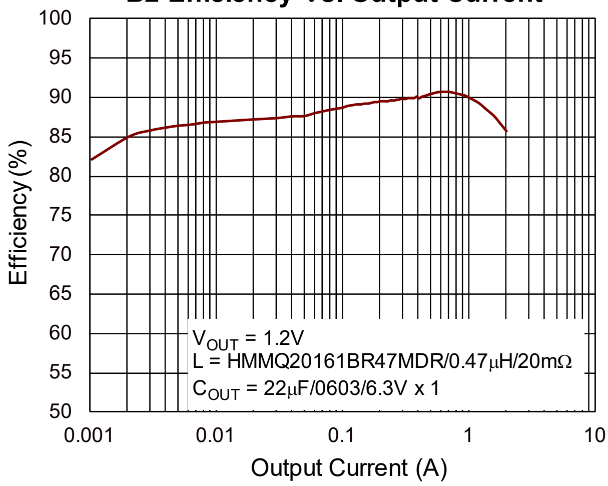
Note: *:If GPIOx is set to High-Z, 100k should be removed.

Typical Operating Characteristics

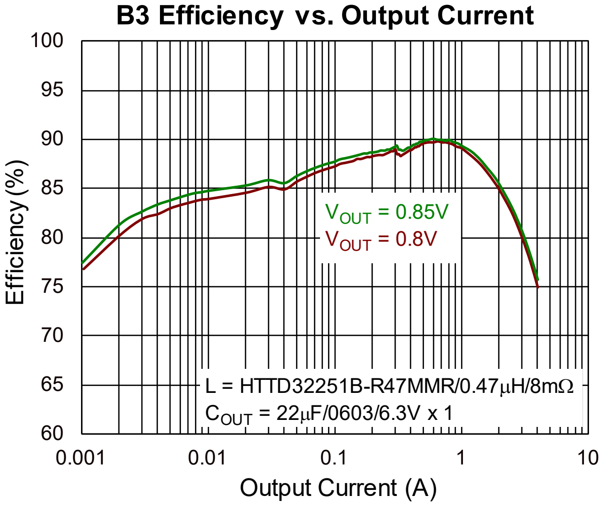
B1 Efficiency vs. Output Current



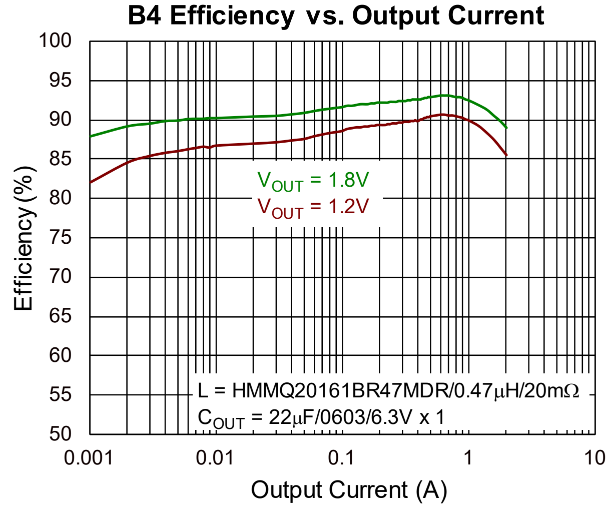
B2 Efficiency vs. Output Current



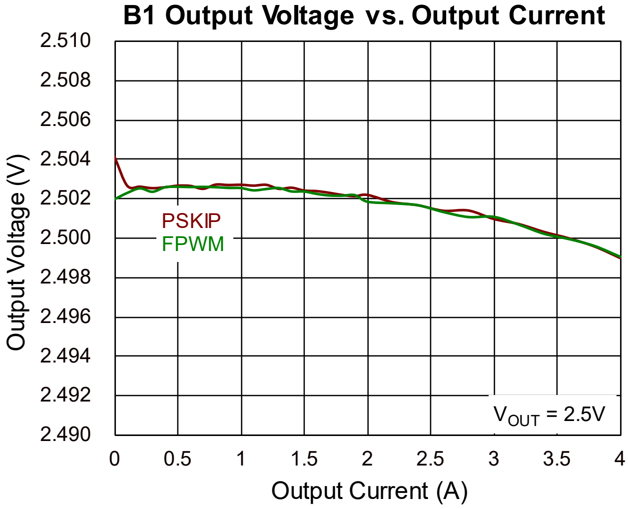
B3 Efficiency vs. Output Current



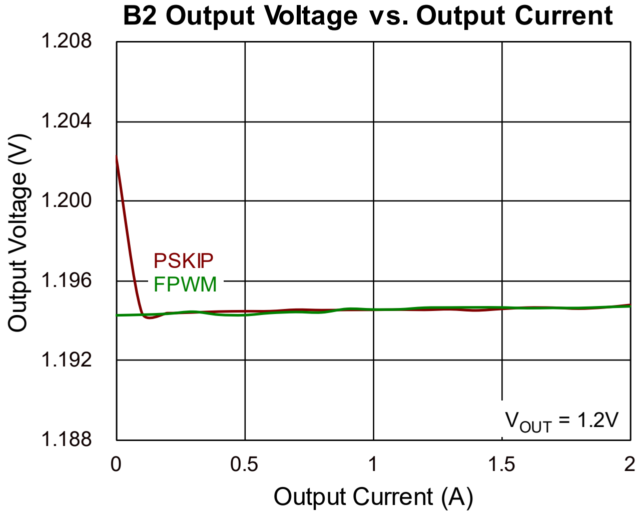
B4 Efficiency vs. Output Current



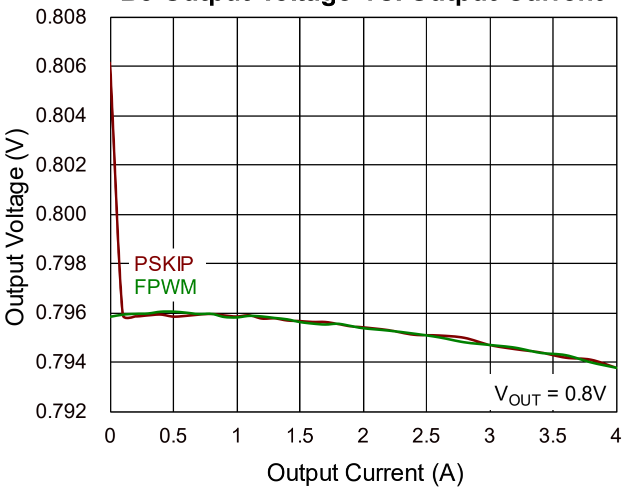
B1 Output Voltage vs. Output Current



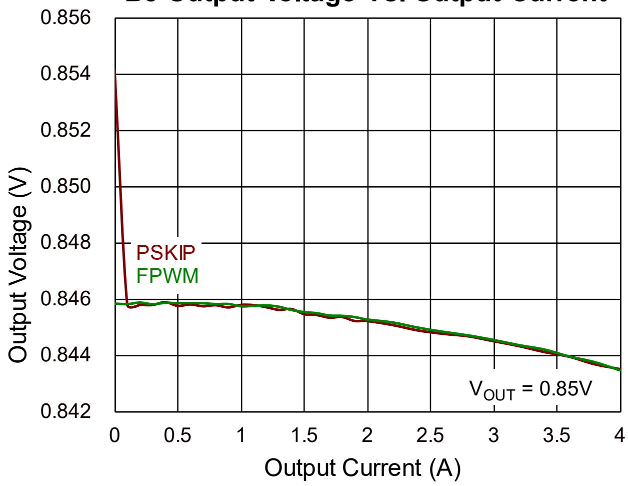
B2 Output Voltage vs. Output Current



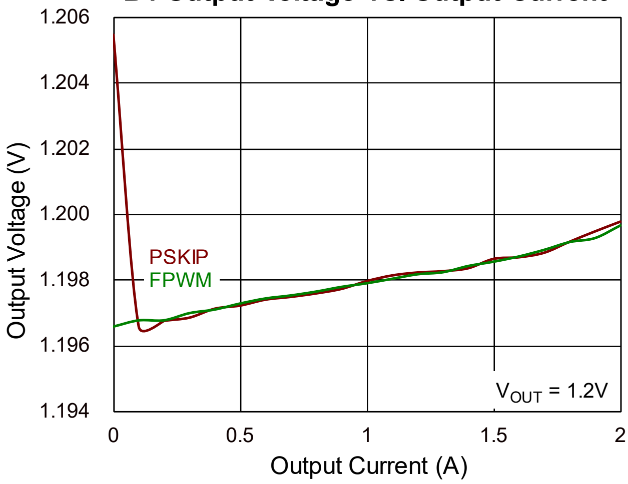
B3 Output Voltage vs. Output Current



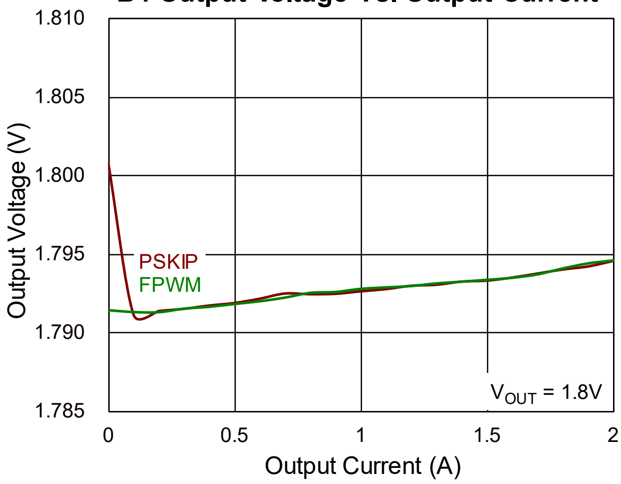
B3 Output Voltage vs. Output Current



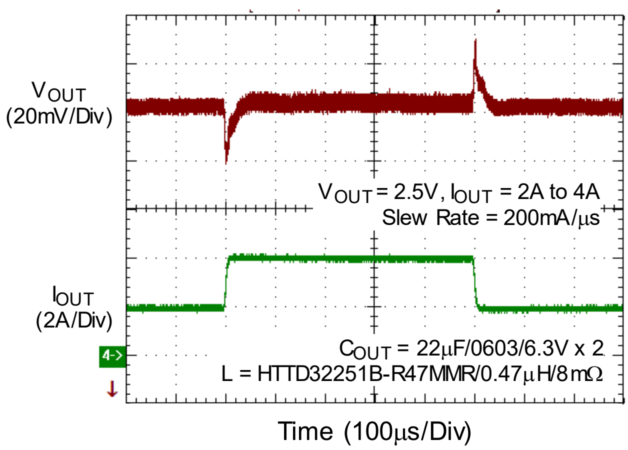
B4 Output Voltage vs. Output Current



B4 Output Voltage vs. Output Current



B1 Load Transient Response



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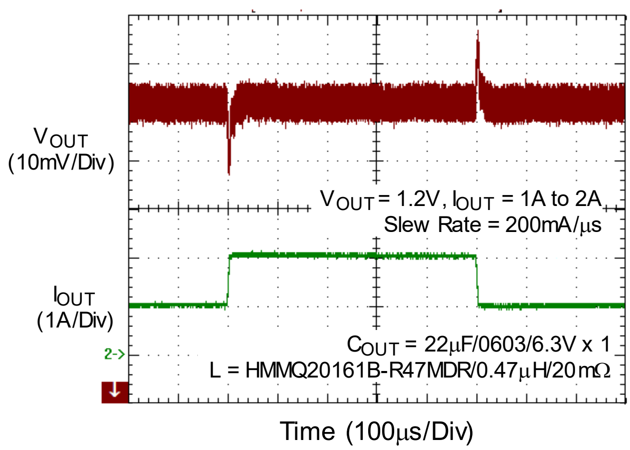
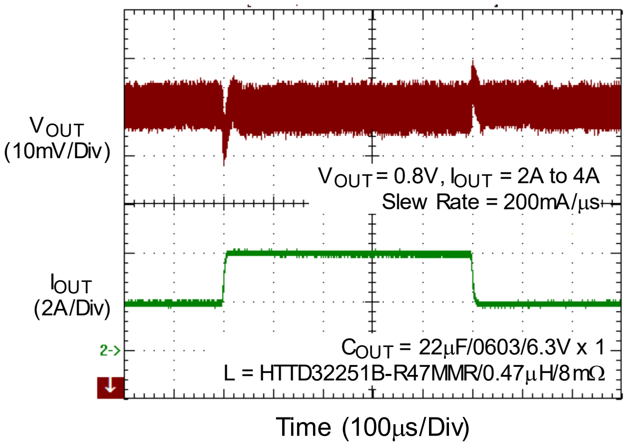


B3 Load Transient Response



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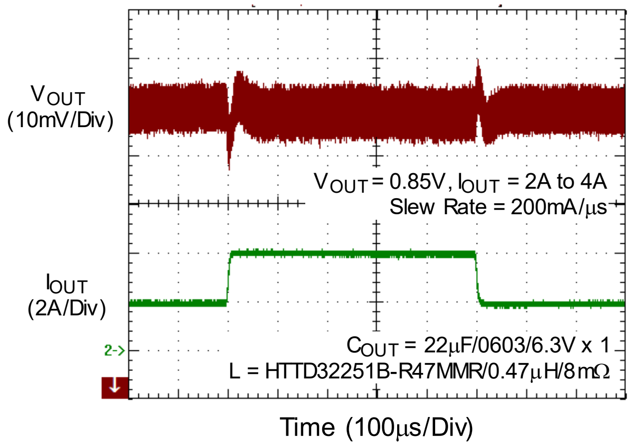

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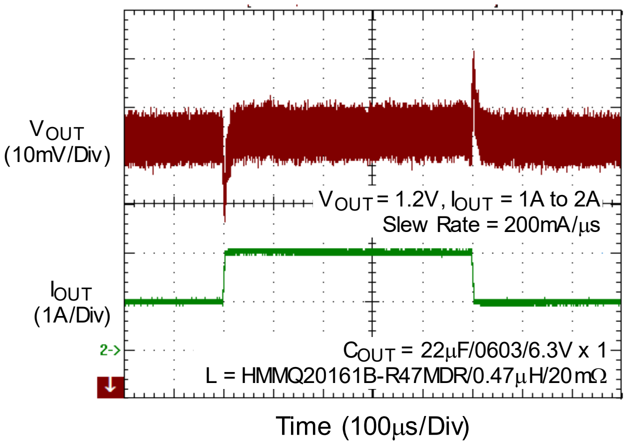

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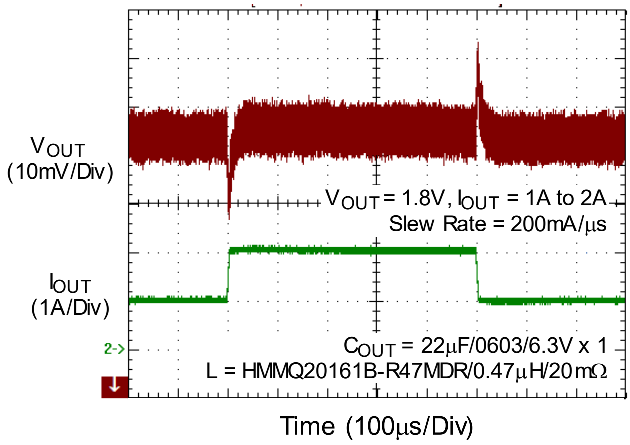
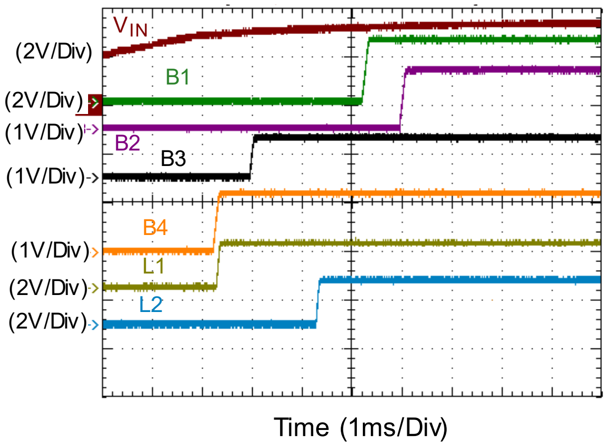
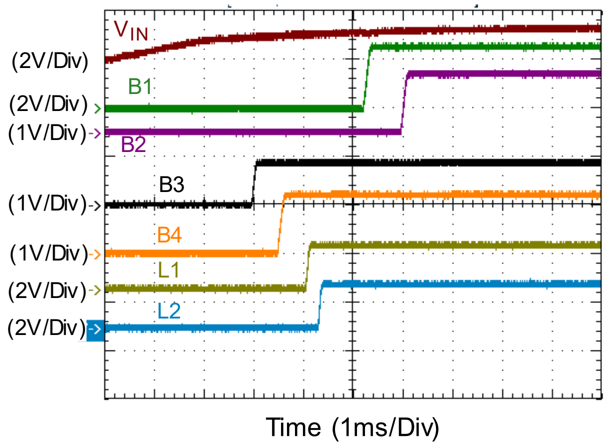


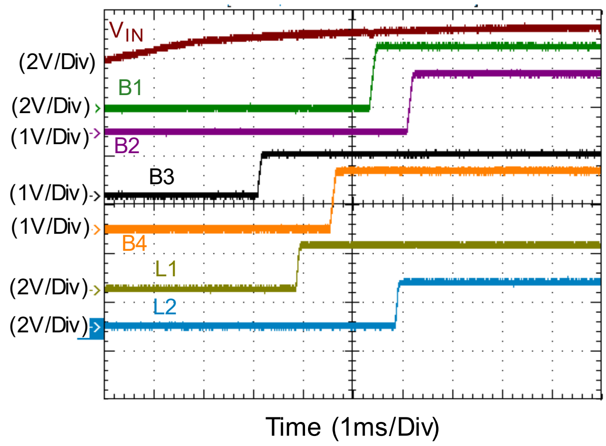
Power Up Sequence for GPIO3 = Hz



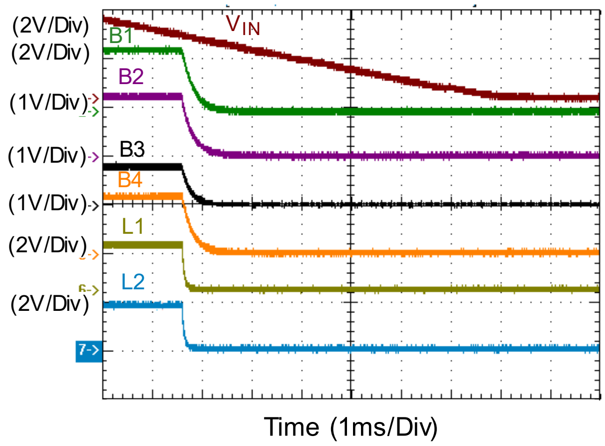
Power Up Sequence for GPIO3 = L



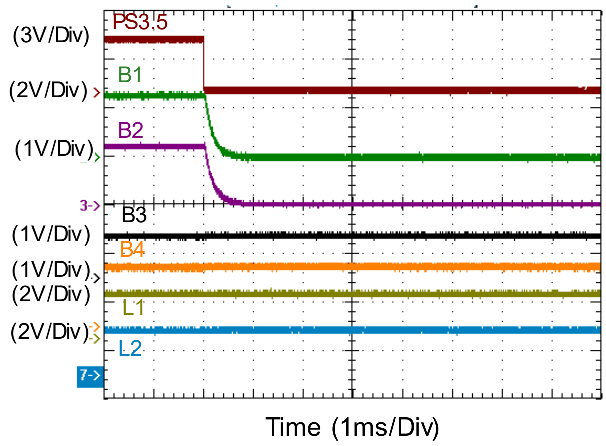
Power Up Sequence for GPIO3 = H



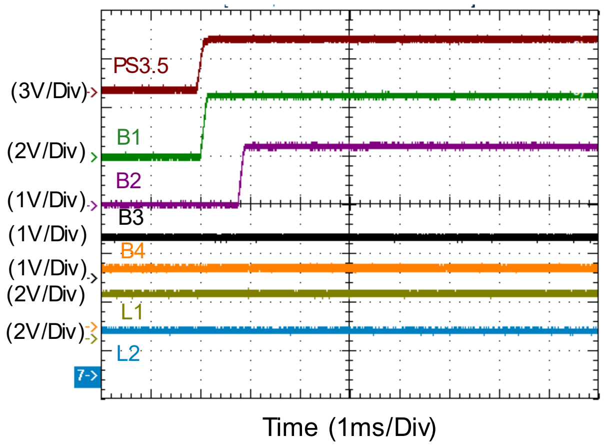
Power Off Sequence



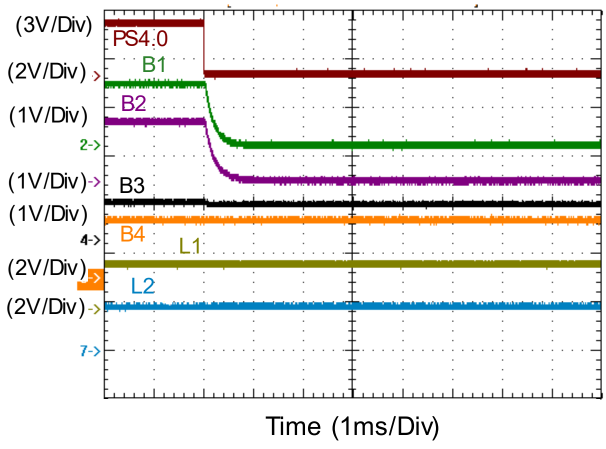
PS3.5 Power Off Sequence



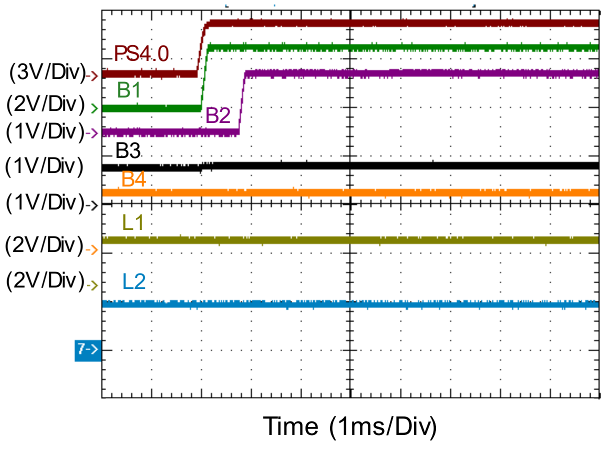
PS3.5 Power Up Sequence



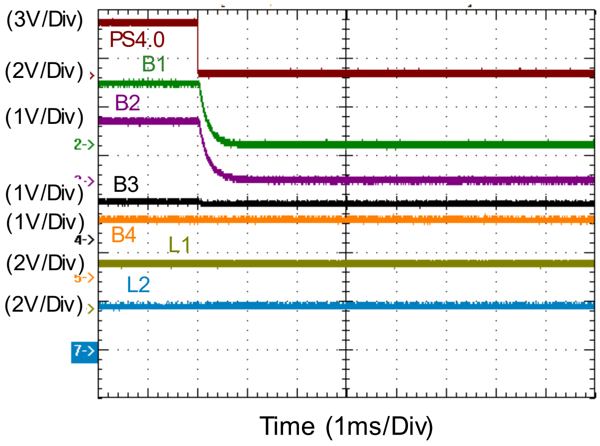
PS4.0 Power Off Sequence for GPIO3 = Hz



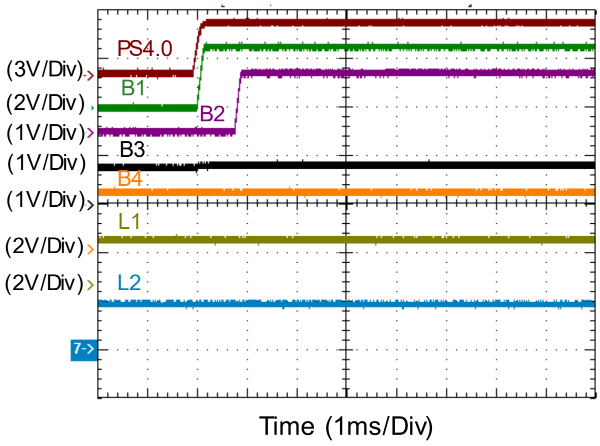
PS4.0 Power Up Sequence for GPIO3 = Hz



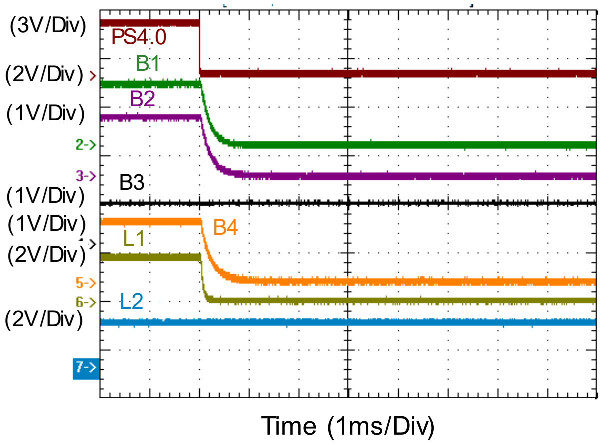
PS4.0 Power Off Sequence for GPIO3 = L



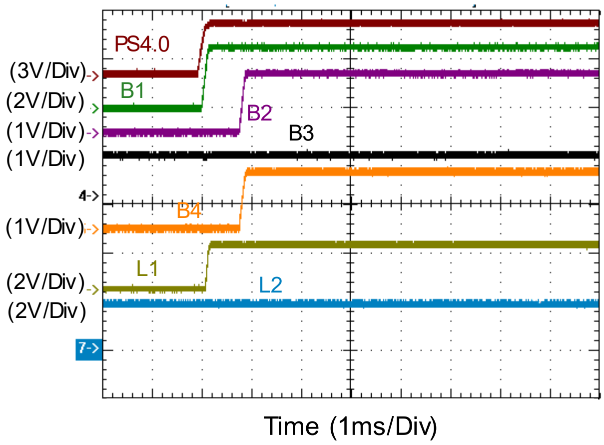
PS4.0 Power Up Sequence for GPIO3 = L



PS4.0 Power Off Sequence for GPIO3 = H



PS4.0 Power Up Sequence for GPIO3 = H



Operation

The RT5142 provides four high-efficiency synchronous buck converters and two LDO regulators for the power system of SSD.

Buck Converter

The RT5142 incorporates four high-efficiency synchronous switching buck converters that deliver programmable output voltages. They feature advance constant-on-time voltage mode (ACOT®) for low output voltage, quick transient response, and low quiescent current. These buck converters are also built with standard protections, such as OVP, UVP and OCL.

Buck Overcurrent Limiter (OCL)

The current limited architecture of all rails is designed to detect valley current. When Low-Side turns on, inductor current will be sensed from $R_{DS(ON)}$ of Low-Side by internal ZC/OC circuit. If the voltage on Low-Side $R_{DS(ON)}$ is over V_{OC} (overcurrent voltage) which is defined by register OC_CFG_*, the OC circuit will force to keep Low-Side turn on to lower down the inductor current. The Low-Side will not turn off until the inductor current is lower than OC level. Once inductor current is under OC level, the rail will be back to normal operation.

Buck Undervoltage Protection (UVP)

The UVP is a level detection. If the output voltage falls below −7% or -15% (selected by register) of the reference voltage, undervoltage protection will be triggered and both the high-side and low-side MOSFET will be turned off immediately. The UVP circuit will be blocked during soft-start time and DVID duration.

Buck Overvoltage Protection (OVP)

The OVP is a level detection. If the output voltage exceeds +10% of the reference voltage, overvoltage protection will be triggered and both the high-side and low-side MOSFET will be turned off immediately. The OVP circuit will be blocked during soft-start time and DVID duration.

Linear Dropout Regulator (LDO)

The RT5142 includes two linear dropout regulators. The LDOs contains an independent current limit and both overvoltage and undervoltage protection circuits to prevent unexpected applications. When the path current is above the current-limit threshold, the current limit circuit adjusts the gate voltage of power stage to limit the output current. If the output voltage is lower than −16% of reference voltage, the LDO will be shut off by the UVP circuit immediately. If the output voltage is higher than +8% of reference voltage, the OVP circuit will also shut off LDO immediately.

Over-Temperature Protection (OTP)

If the chip temperature is higher than 150°C, the OTP circuit will shut down all power rails. The PMIC will reboot with power- up sequence after the chip temperature is down to 125°C.

GPIO1

GPIO1 is fixed to nRESET signal. After power-up sequence, nRESET = H indicates PMIC Power Good (PG), while nRESET = L indicates Power Bad (PBAD).

The n_RESET_MASK_REG provides the function to mask any output PBAD event, VIN_OV event and OT event. By setting the corresponding bits to “1b” in the nRESET_MASK_REG register, nRESET will ignore any PBAD events on the rail. Any PBAD events on an un-masked rail will cause nRESET to go low. In addition, the Power Good delay time from the rising edge of the Buck3 PG flag to the rising edge of the nRESET can be set in the GPIO1_REG.POR_DELAY_TIME.

GPIO2

GPIO2 has a default function, B1/B2 VSEL, before nRESET = H. Once AVIN voltage > “UVLO+HYS” voltage, the selected default values of the B1/B2 VSEL functions will be recorded into the relative register values, such as B1 VR structure, B1_SEL and B2_SEL, immediately. Please see Table 1 for the description of B1/B2 VSEL.

Table 1. GPIO2 Function

B1/B2 VSEL			
GPIO2 Status	**High**	**High-Z**	**Low**
B1 Status	B1 = LSW	B1 = Buck/ 2.5V	B1 = Buck/ 2.9V
B2 Status	B1 = 1.2V	B1 = 1.2V	B1 = 1.2V

After power-up sequence and nRESET going to high level, the GPIO2 function can be changed to other function (see Table 5.) by configuring GPIO2_REG.GPIO2_FUNC_SEL. The setting of GPIO3, 4 and 6 are the same as the GPIO2. They all have the internal default functions before nRESET = H and can be changed to other functions after nRESET = H.

Set GPIO2/3/4/6_FUNC_EN = 0b to disable the function set in GPIO2/3/4/6_FUNC_SEL and GPIO2/3/4/6 will keep the internal default function.

GPIO3

GPIO3 has a default function, B3 VSEL, before nRESET = H. Once AVIN voltage > “UVLO+HYS” voltage, the selected default value of the B3 VSEL function will be recorded into the relative register value, such as B3_SEL and some delay time of other rails, immediately. In addition, if PMIC enters Deeper Sleep Mode (PS4), B3 VSEL will be Dynamic Voltage Scaling (DVS) mode, such as B3_DVS. Please see Table 2. for the description of B3 VSEL.

Table 2. GPIO3 Function

B3 VSEL			
GPIO3 Status	**High**	**High-Z**	**Low**
B3 Status	B3_SEL = 0.83V B3_DVS = 0.83V	B3_SEL = 0.8V B3_DVS = 0.75V	B3_SEL = 0.85V B3_DVS = 0.73V
Power Up Delay Time for B4/ L1/ L2	B4 = +2.25ms L1 = + 1.5ms L2 = + 3.5ms	L1 = 0ms L2 = + 2.0ms	B4 = +1.25ms L1 = + 1.75ms L2 = + 2.0ms

Note: The default power up sequence of the die code configuring (no loaded from EFUSE) will be: B4, L1, L2 power up at 0ms → B3 power up at 0.75ms → B1 power up at 3.0ms → B2 power up at 3.75ms.

GPIO4

GPIO4 has a default function, L1/B4 VSEL, before nRESET = H. Once AVIN voltage > “UVLO+HYS” voltage, the selected default values of the L1/B4 VSEL functions will be recorded into the relative register values, such as L1 VR structure, L1_SEL, B4 VR structure and B4_SEL, immediately. Please see Table 3. for the description of L1/B4 VSEL.

Please note only GPIO2, GPIO3 and GPIO4 have the High-z state setting.

Table 3. GPIO4 Function

L1/B4 VSEL			
GPIO4 Status	**High**	**High-Z**	**Low**
L1 Status	L1 = LDO/ 1.8V	L1 = PLSW	L1 = LDO/ 1.8V
B4 Status	B4 = Buck/ 1.1V	B4 = LDO/ 1.8V	B4 = Buck/ 1.2V

GPIO6

GPIO6 has a default function used to select LDO2 regulator mode. The other GPIO2/3/4 signals will check their self-voltage level to confirm the rails' mode and voltage at VIN > UVLO + HYS voltage, but only GPIO6 will check its self-voltage level to get the regulator mode and its output voltage of LDO2 before LDO2 ramping up. Please see Table 4. for the description of LDO2 MODE.

Table 4. GPIO6 Function

LDO2 MODE			
GPIO6 Status	**High**	**High-Z**	**Low**
L2 Status	L2 = LDO/ 1.8V	--	L2 = PLSW

GPIO5/7/8

The default function of the GPIO5/7/8 is decided by the default register value of GPIO5/7/8_FUNC_SEL, the RT5142 applies these functions, which can be assigned into GPIO5/7/8 pins. The GPIO5/7/8 will be as the enable/disable controlled signal of the selected function shown in Table 5. And the default function of GPIO1 to GPIO8 is shown in Table 6. GPIO1~8 Default Function.

In addition, GPIO2/3/4/6 can also be adjusted to the function shown in Table 5, after nRESET = H.

Table 5. GPIO2 - 8 Function

GPIOx_FUNC_SEL	I/O	FUNC_NAME	Function Descriptions
0x00	O	General GPIO1 (as EXT_EN1_O)	General Purpose I/O1 is as the EXT_EN1_O for external enable signal.
0x01	O	General GPIO2 (as EXT_EN2_O)	General Purpose I/O2 is as the EXT_EN2_O for external enable signal.
0x02	O	nIRQ	As Internal signal, nIRQ, output.
0x03	I	Sleep Mode 1 (Sleep Mode, PS3.5)	As the input controlled signal for Sleep1. High = Wake up from Sleep Mode 1 Low = Enable Sleep Mode 1
0x04	I	Sleep Mode 2 (Deeper Sleep Mode, PS4)	As the input controlled signal for Sleep2. High = Wake up from Sleep Mode 2 Low = Enable Sleep Mode 2
0x05	I	B1/B2 EN/DIS	As the enable/disable signal for controlling B1/B2. The priority of this function is lower than Sleep1 and Sleep2. High = Enable B1/B2 Low = Disable B1/B2
0x06	I	PWRDIS	As the Power Disable signal for controlling

GPIOx_FUNC_SEL	I/O	FUNC_NAME	Function Descriptions
			RT5142. High = Disable RT5142 Low = Enable RT5142
0x07	I	EXT_EN1_I function. No use for GPIO2/3/4	Input Triggered Signal for EXT_EN1_O. High = EXT_EN1/2_O will go high with the configured delay time. Low = No action.
0x08	I	EXT_EN2_I function. No use for GPIO2/3/4	
0x09	O	SYSMON Output	Only GPIO5 can output SYSMON. High = VIN > SYSMON Low = VIN < SYSMON

Table 6. GPIO1 - 8 Default Function

GPIOx	GPIOx_FUNC_SEL			I/O	FUNC_NAME
	H	Hi-Z	L		
GPIO1	X			O	nRST(nRESET)
GPIO2	0x00			O	General GPIO1 (as EXT_EN1_O)
GPIO3	0x00			O	General GPIO1 (as EXT_EN1_O)
GPIO4	0x00			O	General GPIO1 (as EXT_EN1_O)
GPIO5	0x03	0x02	0x02	I/O	Sleep Mode 1 (PS3.5) input by GPIO3 = H nIRQ output by GPIO3 = Hi-Z or L
GPIO6	0x00			O	General GPIO1 (as EXT_EN1_O)
GPIO7	0x06			I	PWRDIS
GPIO8	0x04			I	Sleep Mode 2 (Deeper Sleep Mode, PS4)

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The RT5142 provides four synchronous buck regulators and two LDOs to satisfy requirements of entire power system of the client SSD. This device can communicate with processors through I^2C interface for programming the output voltages of the rails, monitoring the status of the rails, or entering sleep mode for power saving. Table 7 lists the information of the power rails provided by the RT5142.

Table 7. Detail of Power Rails

Resource Name	Type	Voltage Range	Current Rating
BUCK1	Buck Converter/LSW	1.7V to 2.9V with 20mV/step	4000mA
BUCK2	Buck Converter	0.9V to 2.0V with 10mV/step	2000mA
BUCK3	Buck Converter	0.5V to 1.3V with 10mV/step	4000mA
BUCK4	Buck Converter/LDO	0.9V to 2.0V with 10mV/step	2000mA
LDO1	LDO/PLSW or NLSW	1.0V to 2.7V with 50mV/step	400mA
LDO2	LDO/LSW	1.0V to 2.7V with 50mV/step	400mA

Bucker Converter

The RT5142 incorporates four high-efficiency, ACOT® based synchronous buck converters that deliver various voltages via I^2C interface. The buck converter can own the fast transient feature with the ACOT® typology.

Every switching regulator is specially designed for very low quiescent (< 35μA), high-efficiency operation during the current rating range. With high switching frequency operation, the external LC filter can be small and keep very low output voltage ripple.

Additional features of these buck converters include soft-start, discharge resistance, undervoltage protection, overvoltage protection, overcurrent limited and thermal shutdown protection. Please note that the RT5142 will be latched when any power rail is operated at undervoltage protection or overvoltage protection. If the die temperature of the RT5142 is higher than 150°C, the thermal protection will be enabled. The thermal protection will make all the rails go to discharge mode and keep off. The RT5142 will recover to power up the rails again when the temperature is lower than 125°C.

With I^2C interface, every buck converter can program output voltage, adjust slew rate of the DVID, change the PWM frequency, and control the on/off state. Even a PWM controller can switch to forced PWM mode, PSKIP mode or LPM mode (for more less quiescent < 25μA).

Inductor Selection

For given input voltage (V_{IN}), output voltage (V_{OUT}), and operation frequency (f_{SW}), the inductor value (L) determines the inductor ripple current (ΔI_L) as shown in equation below:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times L \times V_{IN}}$$

Having a lower ripple inductor current not only reduces the power losses on the ESR of the output capacitors, but also the output voltage ripple. A reasonable starting point for selecting the ripple current is ΔI_L = 0.3 x I_{MAX} to 0.4 x I_{MAX}. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{f_{SW} \times \Delta I_L \times V_{IN(MAX)}}$$

And the current rating of the inductor must be large enough and will not saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

C_{IN} and C_{SYS} Selection

The input capacitance of every rail, C_{IN}, needs to filter the trapezoidal current at the source of the high-side MOSFET. For preventing a large ripple voltage, a low ESR input capacitor for the maximum current should be used. The relation between C_{IN} ripple voltage and current ripple is shown in Figure 1.

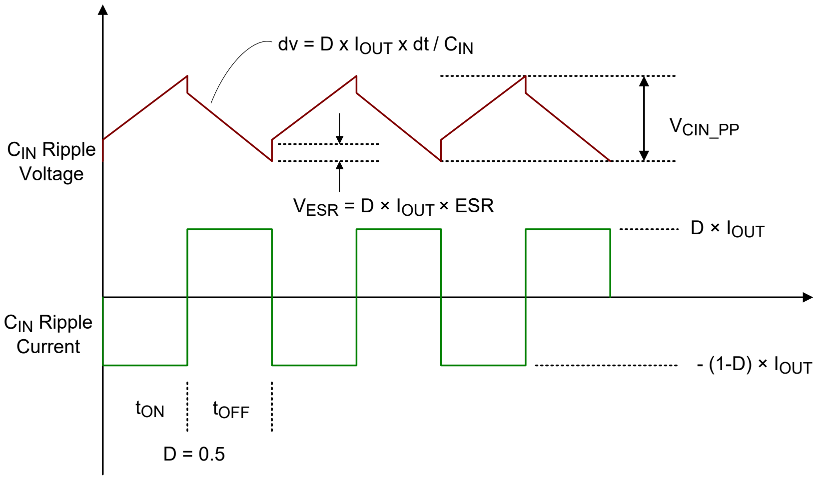


Figure 1. Relationship of C_{IN} Voltage Ripple and Current Ripple (Assuming D = 0.5)

The C_{IN} voltage ripple can be determined by the below equations when a rail works at the f_{SW} of CCM mode.

$$V_{CIN\_PP} = D \times I_{OUT(MAX)} \times (ESR + \frac{(1-D)}{C_{IN} \times f_{SW}})$$

where D = V_{OUT}/V_{IN}. If MLCC is used as the input capacitors, the ESR is almost equal to zero, and the minimum input capacitance requirement can be estimated as below:

$$C_{IN(MIN)} = I_{OUT(MAX)} \times \frac{D \times (1-D)}{V_{CIN\_PP(MAX)} \times f_{SW}}$$

Next, it also needs to consider the input bulk capacitance, C_{SYS}, to ensure a stable input voltage during all rails do the large load transient. Basically, the input host power source cannot provide enough instant input current to respond to a fast and large load current transient of the converters. The insufficient energy during load transient will be provided by the input bulk capacitors until the host power supply fills the input current requirement. Please refer to Figure 2 to better understand the above description.

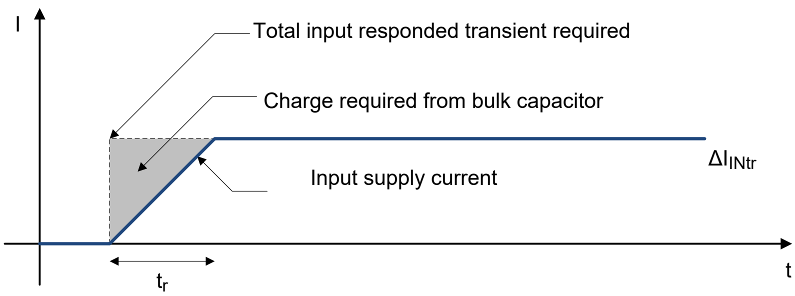


Figure 2. Charge Required from Input Bulk Capacitors during Load Transient

Figure 3 shows the diagram of every power rail of the RT5142 sharing a single bank of input bulk capacitors. The total input transient current required due to load currents of the converters can be calculated by using the following equation:

$$\Delta I_{INtr} = \sum_{n=1}^{4} \frac{V_{OUTn} \times \Delta I_{OUTn(MAX)}}{V_{IN} \times \eta_n}$$

where ΔI_{INtr} is the required total input transient current. ΔI_{OUT} is the maximum output transient current. η is the efficiency of the buck at $I_{OUT(MAX)}$.

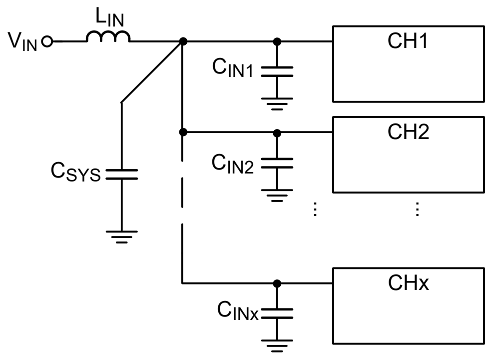


Figure 3. The Location of Input Bulk Capacitors Diagram

When ΔI_{Intr} is confirmed, the input bulk capacitance, C_{SYS}, can be decided by the following equation:

$$C_{SYS(MIN)} \cong \frac{1.21 \times \Delta I_{INtr}^2 \times L_{IN}}{\Delta V_{INPP(MAX)}^2}$$

where $\Delta V_{INPP(MAX)}$ is the maximum dropout voltage allowable and L_{IN} is the input series filter inductance. If L_{IN} is not used, put a reasonable parasitic value of 50nH for the PCB layout.

C_{OUT} Selection

The output capacitors and the inductor form a low pass filter in the buck topology. In steady state condition, the inductor ripple current flowing in-to/out-from the output capacitors will result in output ripple voltage. The peak-to-peak of output ripple voltage (ΔV_{OUTPP}) can be calculated by the following equation:

$$\Delta V_{OUTPP} = \Delta I_L \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right)$$

The output capacitors can be equivalent to a series of ESR, Capacitance and ESL circuit. When the load transient occurs, the output capacitors supply the instant load current before the inductor current catches up the output current and the response from the controller. Therefore, the output voltage under-shoot/over-shoot can be combined by the ESR voltage, ESL induced voltage and the delta voltage which is caused by the delta electric quantity coming from or charging to the capacitors. The ESR voltage (ΔV_{ESR}) can be calculated by the following equation:

$$\Delta V_{ESR} = ESR \times \Delta I_{LOAD}$$

Another parameter that can affect the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in $\Delta I_{LOAD}/\Delta t_T$ during transient, where $\Delta I_{LOAD}/\Delta t_T$ is the transient slew rate. The ESL induced voltage (ΔV_{ESL}) can be calculated by the following equation:

$$\Delta V_{ESR} = ESL \times \frac{\Delta I_{LOAD}}{\Delta t_T}$$

Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR. Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. All the buck converters of the RT5142 can operate stably with the MLCC output capacitors.

Overcurrent Limit (OCL)

The buck converters provide overcurrent limit. The current limit architecture of the buck converter uses the low-side MOSFET turn-on resistance to detect the inductor current. If the low-side sensed voltage is over the configuring V_{OC} voltage, the low-side will continue tuning on to pull the inductor current down. Once the inductor current across low-side is lower than V_{OC}, the controlled loop will be from OC loop back to normal loop. The RT5142 applies 4 overcurrent levels for each buck converter. Please see the register tables for the OCL values setting on each rail.

As for LDO, it provides overcurrent protection by continuously monitoring the load current. If the sensed current is over the current-limit threshold, the OCL will be triggered. When OCL is tripped, the rail will force to keep the overcurrent threshold level until the overcurrent condition is removed.

Undervoltage Protection (UVP)

All the rails of the RT5142 are continuously monitored for undervoltage protection.

UVP threshold:

1. BUCK1 to BUCK4: the output voltage falls below 93% or 85% (by the register configuring) of reference.
2. LDO1 and LDO2: the output voltages fall below 84% of the reference.

If the output voltage falls below UVP threshold, the UVP circuit will turn off all rails and be latched, and the POR will go low. The only way to remove the latched behavior is to make the AVIN of the RT5142 lower than UVLO voltage and then higher than POR voltage.

Overvoltage Protection (OVP)

All the rails of the RT5142 are continuously monitored for overvoltage protection.

OVP threshold:

1. BUCK1 to BUCK4: the output voltage falls below 110% of reference.
2. LDO1 and LDO2: the output voltages fall below 114% of the reference.

If the output voltage exceeds OVP threshold, the OVP circuit will turn off all rails and be latched, and the POR will go low. The only way to remove the latched behavior is to make the AVIN of the RT5142 lower than UVLO voltage and then higher than (UVLO + HYS) voltage.

AVIN Overvoltage Protection (AVIN OVP)

If the AVIN is over 3.8V, the AVIN OVP circuit acts and makes all power rails shutdown, and the POR will go low. They recover back with power-up sequence when the AVIN drops to 3.5V (3.8V – HYS).

AVIN Undervoltage Lockout (AVIN UVLO)

If the AVIN voltage exceeds the UVLO falling threshold voltage + 100mV, the PMIC is working at standby mode and all register values are re-load from the EFUSEs. The rails do not power up at this standby mode. The rails will not do the power up sequence until AVIN is over SYSMON voltage. If AVIN voltage falls below the UVLO falling threshold voltage, all power rails will stop operation immediately and the digital controller will also not work. The PMIC resets all register codes and enter the standby mode when AVIN voltage is higher than the UVLO falling threshold voltage + 100mV again. There is a hysteresis voltage about 100mV between the UVLO rising and falling threshold voltage to prevent the noise that causes reset.

Over-Temperature Protection (OTP)

If the temperature of the IC is over 150°C, the OTP circuit acts and makes all power rails shutdown (include LSW), and the POR will go low. They recover back with power-up sequence when the temperature of PMIC drops to 125°C.

Protection Functions

The RT5142 applies several types of protection functions to avoid the unexpected events in applications. The details of the protection functions are shown in Table 8, when any event occurs. The table also highlights 6 events that causes PMIC to generate nRESET signal go low command. For remaining the Overcurrent Limit (OCL) event, that does not trigger the rail shutdown command, the PMIC continues to operate as normal.

Table 8. Details of the Protection Functions

Fault Events	Shutdown Rails	Fault Responses	nRESET Behaviors	Register Value
OCL (Buck and LDO)	None	N/A	Keep high	Keep
UVP (Buck and LDO)	Buck B1/2/3/4, LDO1/2	Hiccup	Go low	Keep
OVP (Buck and LDO)	Buck B1/2/3/4, LDO1/2	Hiccup	Go low	Keep
AVIN OVP	Buck B1/2/3/4, LDO1/2	Non-Latch	Go low	Keep
AVIN UVLO	Buck B1/2/3/4, LDO1/2	Non-Latch	Go low	Reset
OTP	Buck B1/2/3/4, LDO1/2	Non-Latch	Go low	Keep

Rails Configuration

Any of the four rails, Buck1, Buck4, LDO1 and LDO2 can change to the other type of a regulator via the GPIO2/4/6 setting. The Buck1, LDO1 and LDO2 can be configured as the PLSW (PMOS type load switch). When the rails become to PLSWs, they keep the overvoltage and overcurrent limit but no undervoltage protection. Please take care to use the rails when they are modified as the load switches. LDO1 can also become NLSW (NMOS type load switch) for lower input voltage and higher output current use. Because the max voltage inside RT5142, AVIN (range: 2.5V – 3.8V), will be as the NMOS gate driver voltage, the higher input voltage as the NLSW input source will cause the larger delta voltage between input and output.

The Buck4 can be configured as the LDO. The LDO has the all set protections which are overvoltage, undervoltage and overcurrent limit. If the delta voltage between input voltage and output voltage is small, using the Buck4 as the LDO will get better efficiency than as the Buck4 converter.

Note that if the original rail become to the other type regulator, their rails' on/off sequence and their current rating setting will be different. Please see the Electrical Characteristics Section for the more detailed SPEC.

I^2C Interface

A general-purpose serial interface to control and monitor the configuration registers is provided in the RT5142 and its I^2C slave address is 0x25. This serial interface supports the I^2C protocol 2.1 with standard slave mode (100Kbps), fast mode (400Kbps) and high speed mode (3.4Mbps). A multiple bytes reading or writing over the I^2C interface of the RT5142 can also be done with standard slave mode (100Kbps) and fast mode (400Kbps). When performing a multiple byte read or write, the RT5142 will automatically increase to the next address for subsequence byte (see Figure 4).

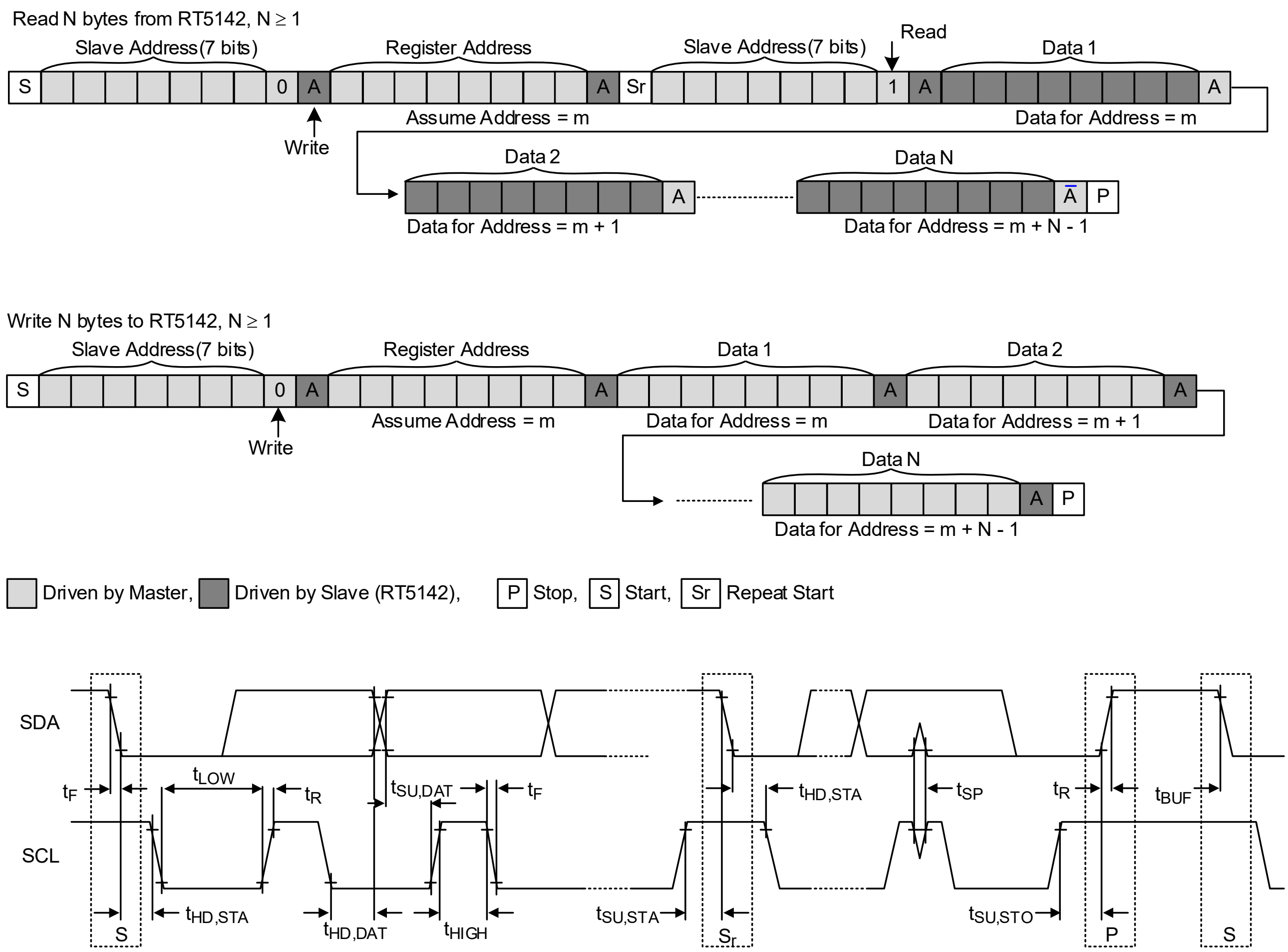


Figure 4. I^2C Read/Write Stream and Timing Diagram

The user can modify the output voltage, fault threshold, interrupt masks, etc..., via the I^2C interface. There are two types of the registers as the following descriptions:

Volatile Registers – These include R/W (Read and Write), RO (Read only) and W1C (Write 1b to clear this bit). After the AVIN > (UVLO + 100mV) = 2.6V, the user can modify the R/W register values to change the register functions. The RO registers are used to provide the rails' status and RT5142 information such as various ID numbers. W1C type means that writing a 1b into the bit will clear itself and become to 0b. Any changes to these volatile registers are lost when AVIN is under 2.5V. The default values are fixed and cannot be modified.

Non-Volatile Registers – These include R/W and RO. After the AVIN > (UVLO + 100mV) = 2.6V, the user can modify the R/W register values to change the register functions. The RO registers are used to provide the rails' status and RT5142 information such as various ID numbers. Any changes to these volatile registers are lost when AVIN is under 2.5V. The default values can be modified at the factory to optimize IC functionality for specific applications. Please contact RichTek for custom configurations to meet the system requirement.

State Machine

The RT5142 contains an internal state machine which has six states. The definition of the states described as below are related to various signals such as, AVIN, POWER_DIS, Sleep1, Sleep2 and some related register settings. The followings are the classifications about the states.

- **Off State**

If AVIN goes to under "UVLO + HYS" voltage from 0V, all the internal circuits of RT5142 do not work at this status.

- **Standby State**

If AVIN is between "UVLO + HYS" voltage and SYSMON voltage or AVIN is over AVIN_OV voltage, the internal digital controller of RT5142 starts to work. Once the digital core is alive, it will process the step of reloading register values from the EFUSEs configuration. After completed the reload step, any register function value still can be modified via the I^2C interface. In addition, RT5142 also stays in the "Standby State" when AVIN range is in the normal operation with PWRDIS = H.

The only way for the register values of RT5142 reloaded from the EFUSE is the state machine changing from Off State to Standby State. Please also note that RT5142 only downloads the EFUSE codes configuration, form the level status of the GPIO2/3/4/6's, into the corresponding register addresses when the digital core is from off state to on state.

- **Normal State**

If AVIN is in the range between SYSMON voltage and VIN OVP voltage and POWER_DIS = L, the rails will follow their GPIOs' setting and their internal configurations of the time slot functions (X_TIME_SLOT), turn-on delay functions (X_ON_DLY) and the soft-start time functions (X_SST_SEL) to do power up sequence. Once the GPIO1 signal, as nRESET, raises up to high level, the RT5142 gets the power good flags and stays in the Normal State. The above description occurs from standby state to normal state.

At Normal State, a rail can be controlled to ON/OFF with configuring the X_EN register function. If the rail power up via setting X_EN from b0 to b1, it will just follow X_SST_SEL function setting to do soft-start immediately with ignoring any configured delay time. Please note if the rails' X_TIME_SLOT = b00 (disabled setting), the rail will always keep off with ignoring any configuring signal.

- **Sleep1/Sleep2 State**

When RT5142 works at Normal State, it will go to "Sleep State" if one of the following conditions is satisfied:

- A GPIOx which is set to SLEEP1 function goes from high voltage to low voltage. The state machine of the RT5142 will go to Sleep1 State.
- A GPIOx which is set to SLEEP2 function goes from high voltage to low voltage. The state machine of the RT5142 will go to Sleep2 State. Please note the priority of the rail's off state in the Sleep1 function and Sleep2 function are higher. If one of the rail's off state in the Sleep1 function or in the Sleep2 function gets

real, the rail will power off with PMIC changing to Sleep1/2 State.

- Besides external hardware signal controlling the sleep mode, RT5142 also applies the software control via I^2C interface to enable sleep mode. If set SLEEP1_EN/SLEEP2_EN function to b1, the PMIC will go to sleep mode.

When RT5142 changes from normal mode to sleep mode, the rails will follow SLEEP1/2_REG setting to do power off. Especially, only the Buck3 can change its voltage from B3_SEL to B3_DVS_SEL, if Buck3 keeps alive with entering sleep mode. All the alive rails will disable some internal circuit to enter low power mode to reduce the VIN supply current for power saving when RT5142 is at Sleep State.

RT5142 can easily go back to normal state from sleep state with disabling the sleep mode condition. For back to normal state, the disabled rails will follow their X_ON_DLY function, X_WAKEUP_DELAY function and X_SST_SEL function to do their wake up sequence.

- **Thermal Recovery State**

When the die temperature of RT5142 hits critical over-temperature event (~150°C), all the rails force to do power off but the digital controller keeps alive. The PMIC stays at the Thermal Recovery State. The PMIC will go back to normal state when the die temperature is lower than 125°C.

- **Recovery State**

If any rail gets the fault flag of overvoltage event or undervoltage event, the fault rail will open its power stage and the others will do power discharge at the same time. After power off the rails, RT5142 will hiccup all rails and the I^2C still works. Users can read back the fault information via the I^2C interface to understand which rail gets the fault flag.

RT5142 will continue to retry. Once RT5142 is no longer in fault events, each rail will return to normal state according to the power up sequence. If AVIN is under UVLO falling threshold, RT5142 will go to OFF State.

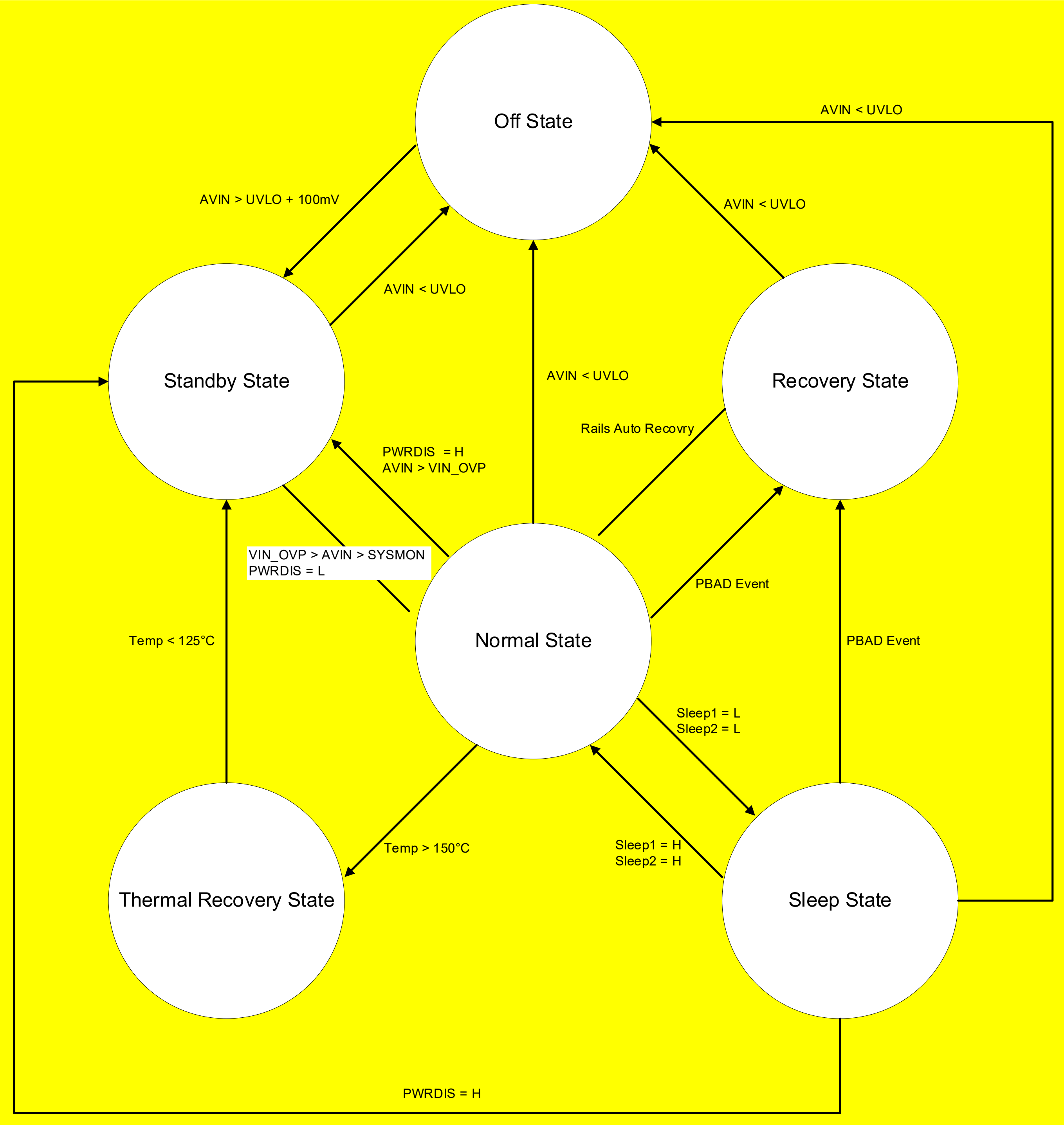


Figure 5. RT5142 State Machine

Sequence Diagram

The RT5142 starts a power up sequence when AVIN > SYSMON threshold voltage, and the device shuts down with VIN < UVLO falling threshold voltage. The RT5142 applies sleep mode to power off some rails, lower down the buck3 output voltage and turn the alive rail to low power mode for saving power consumption. All the rails will be back to normal operation when RT5142 goes to normal state from the sleep state. The power on/off sequence and sleep off/wake up sequence of all rails in the RT5142 are shown in Figure 6, Figure 7 and Figure 8.

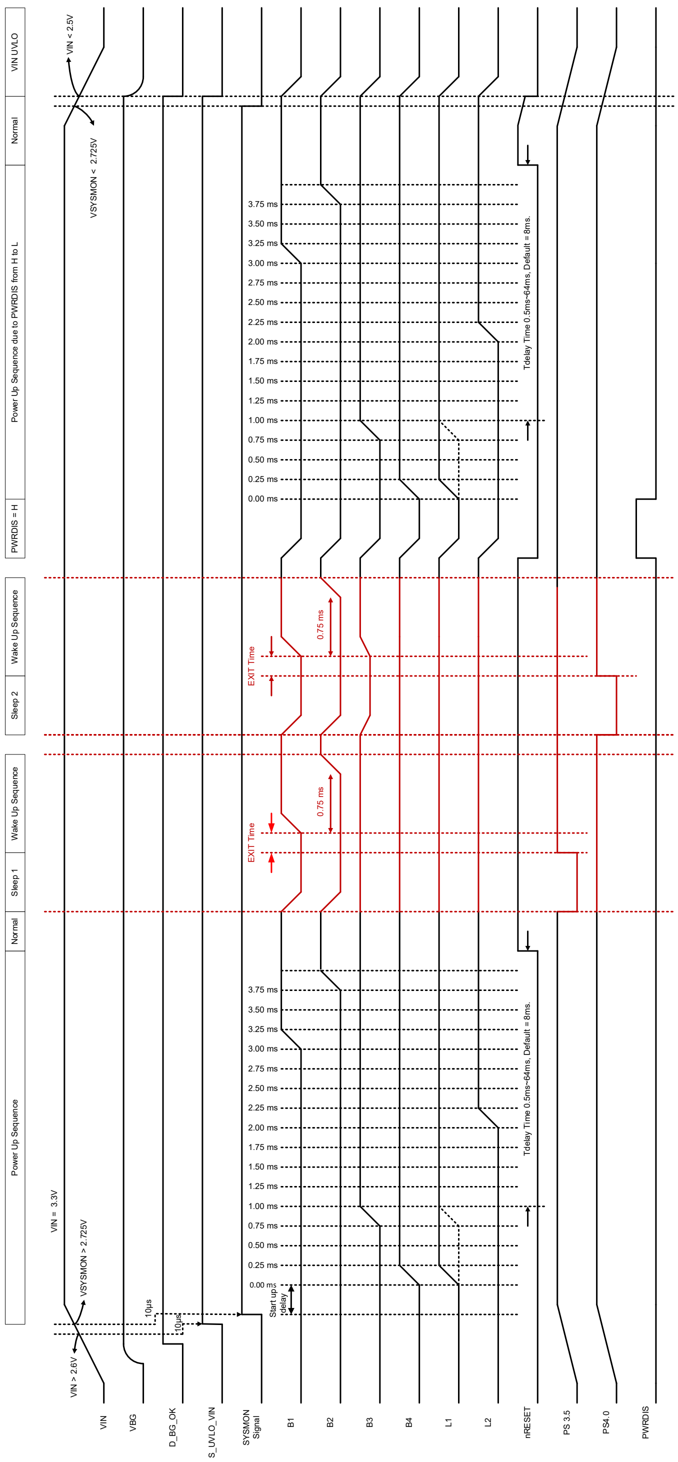


Figure 6. Power Up/Off Sequence and Sleep Off/Wake Up Sequence for GPIO3 = Hi-Z.

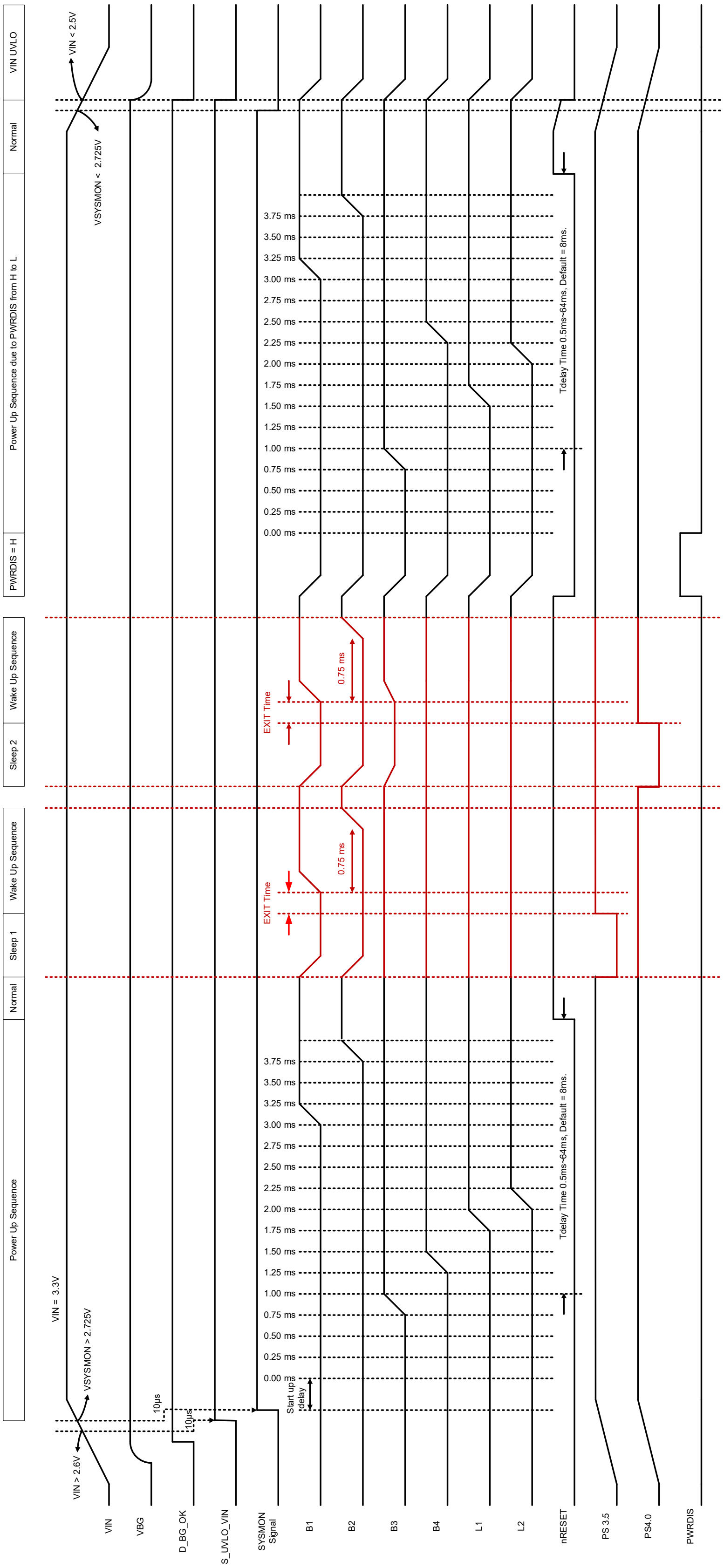


Figure 7. Power Up/Off Sequence and Sleep Off/Wake Up Sequence for GPIO3 = L.

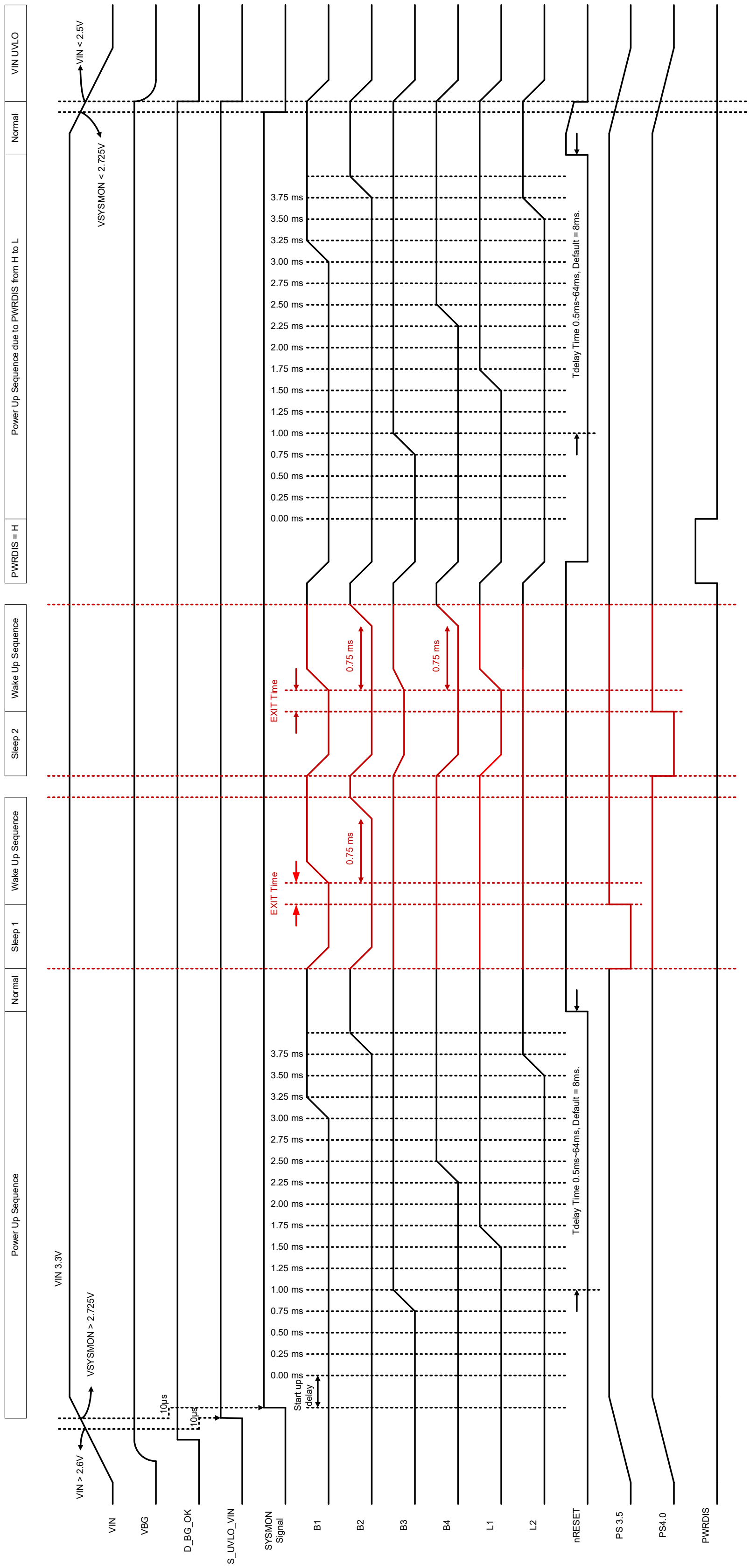


Figure 8. Power Up/Off Sequence and Sleep Off/Wake Up Sequence for GPIO3 = H.

TIME_SLOT, ON_DLY, WAKE_UP_DLY and OFF_DLY

RT5142 embeds four timers to build the power up sequence, sleep off sequence and wake up sequence for every rail. These four timers are TIME_SLOT, WAKE_UP_DLY, ON_DLY and OFF_DLY. All their functions are described below:

1. TIME_SLOT timer: This timer is used to design the enable delay time of the buck converter or the LDO with discrete regulated duration during the power up sequence. The time slot applies the enable delay time from 0ms to 3.75ms with 0.25ms step resolution. The enable delay time = 0ms is counted from AVIN = SYSMON with the additional delay of "10μs and Start Up Delay" and the Start Up Delay is 380μs. Please note that if set the Time_Slot register of a rail to 0x00, the rail will never power up with any sequence. The register of the Time_Slot for enable delay time = 0ms should be 0x01.
2. WAKE_UP_DLY timer: This timer is used to design the enable delay time of a regulator during the wake up sequence. The options of the WAKE_UP_DLY function are planned as 0μs, 250μs, 500μs, 750μs, 1000μs, 2000μs, 4000μs and 8000μs. The wake up delay time = 0μs is counted from the rising edge of the Sleep1/2 signal with the additional delay of "EXIT TIME" and the EXIT TIME is less than 1μs. Without wake up delay time setting to all regulators, they will raise up at the same time during wake up sequence.
3. ON_DLY: The ON_DLY timer is used for the additional delay time to a rail's enable signal from 0 to 1 during the power up sequence and the wake up sequence. It means that the total delay time of a rail in the power up sequence is "TIME_SLOT + ON_DLY"; the total delay time of a rail in the wake up sequence is "WAKE_UP_DLY + ON_DLY".
4. OFF_DLY: The OFF_DLY timer is only used for the delay time to a rail's enable signal from 1 to 0 during sleep off sequence. All rails without OFF_DLY setting will power off at the same time during the sleep off sequence.

All the rails in the power-off sequence, when AVIN < UVLO or PWR_DIS = L, always do discharge off at the same time. The OFF_DLY will not apply the delay time to the regulator in the power-off sequence. Please see Table 9 for the functions of the four timers to all the sequences:

Table 9. The Delay Time Contributions of the Timer Register Functions to the Sequences.

Sequence	TIME_SLOT	WAKE_UP_DLY	ON_DLY	OFF_DLY
Power up	Yes	--	Yes	--
Sleep off	--	--	--	Yes
Wake up	--	Yes	Yes	--
Power off	--	--	--	--

B1/B2_EN

The priority of B1/B2_EN signals, compared with Sleep1 and Sleep2, is the lowest. If B1/B2_EN = H before AVIN > SYSMON, the Buck1 and Buck2 will follow the delay time configured from the time slot function and on delay time function to power up. If B1/B2_EN keeps L after AVIN > SYSMON, the Buck1 and Buck2 will stay at off during the power up sequence. And then the Buck1 and Buck2 will follow the delay time configured from the wake up delay time and on delay time to power up when setting B1/B2_EN to H at normal operation status.

VOUT_LOW

The RT5142 provides the VOUT_LOW function to prevent the error power up sequence due to the higher residue voltage on the larger output capacitors. Without VOUT_LOW function, RT5142 has the opportunity to do the power down sequence and then power up sequence in a very short time by following the low short-pulse from AVIN or the high short-pulse from PMIC_DIS signal. It will cause the following fact that all the outputs still keep higher residue voltages to do the power up sequence, because there is no enough time to discharge their output voltages. The result of the above will make the system stop working due to the wrong rails' power up sequence.

The VOUT_LOW function can be enabled by configuring VOUTLOW_MASK_BIT in the TOP_CTRL_REG into b0. If enabling the VOUT_LOW function, RT5142 will not enable the power up sequence with any rail of RT5142 being higher than 200mV. Through this function, it can make sure that RT5142 provides the right power up sequence to the system.

EXT_ENx_O

RT5142 provides additional two external enable signals to control the external converters for supporting larger current rating or expanding more rails to use. Any of the GPIO2 ~ GPIO8 can be configured as the output signal, EXT_EN1_O or EXT_EN2_O. The GPIOx as the EXT_ENx_O can join the power up sequence or use manual operation to power up via I^2C Interface or sending input triggered signal to another GPIOx. The EXT_ENx_O_INPUT_SEL function apply four selections to trigger EXT_ENx_O to issue enable signal and the EXT_ENx_O_TIME_SLOT function and EXT_ENx_DELAY function contribute the delay time to meet the power up sequence. Please see the following descriptions for more detail about the configuration of the EXT_ENx_O:

1. EXT_ENx_O_INPUT_SEL = Rail's POK and its delay time is affected by EXT_ENx_DELAY.

   The EXT_ENx_O will follow the selected rail's power good configured by EXT_ENx_POK_SEL function to issue the enable signal after a delay time. Please note there is always an offset delay time about 250μs when the Rail's POK is set as the input triggered signal to EXT_ENx_O.

1. EXT_ENx_O_INPUT_SEL = EXT_ENx_I and its delay time is affected by EXT_ENx_DELAY.

   The EXT_ENx_O will follow an external high level signal received by the GPIO5/6/7/8, configured by EXT_ENx_POK_SEL function and EXT_ENx_I_SEL function, to issue its enable signal after a delay time. Please make sure that the configurations of EXT_ENx_O and EXT_ENx_I are assigned to different GPIOx.

2. EXT_ENx_O_INPUT_SEL = the command from the I2C interface and there is no delay time.

   The EXT_ENx_O can set to follow the command from the I^2C interface. The register address for the command is located at GPIOx_GENERAL_CTRL function. Write 00b to pull down EXT_ENx_O as low level signal and 01b to pull high EXT_ENx_O as high level signal.

3. EXT_ENx_O_INPUT_SEL = EXT_ENx_O_Time_Slot and its delay time just come from the time slot setting.

   The EXT_ENx_O will follow the delay time configured by EXT_ENx_O_Time_Slot function to issue the enable signal during the power up sequence of RT5142. Please note there is always an offset delay time about 400μs when EXT_ENx_O sets to follow its time slot.

EXT_ENx_O will just power up with the above descriptions, and it does not go low until RT5142 is forced to process the power down sequence which is caused by the protection, such as VIN OV, OT, PWR_DIS = H, and output rails suffering OV and UV. After the PMIC finishes the power up sequence, the only way for controlling EXT_ENx_O to low level signal at normal operation is to configure EXT_ENx_O to follow the I^2C command.

SYSMON, SYSWARN and POK_OV

SYSMON is the configurable threshold voltage for monitoring AVIN and the threshold can be configured from 2725mV to 3100mV with the 25mV step resolution. When the AVIN is over the SYSMON Vth, RT5142 can enable the rail's power up sequence.

SYSWARN is the warning signal to alarm that the AVIN voltage is lower than SYSWARN monitored voltage. The SYSWARN alarmed voltage can be configured from 2775mV to 3150mV with the 25mV step resolution. Same as SYSWARN, POK_OV is also the warning signal to alarm that the AVIN voltage is higher than POK_OV monitored voltage. The POK_OV monitored voltage has two selections, 3.5V and 3.8V. The system can monitor AVIN as the input source power good by the two signals, SYSWARN and POK_OV.

The indication bits for SYSMON, SYSWARN and POK_OV are listed in the TOP_STATUS_REG. These three bits are designed as real time reaction. Their corresponding bits will show real status when the AVIN voltage is over their setting threshold voltage. It means that if POK_OV bit in the TOP_STATUS_REG shows b1, the AVIN is over POK_OV monitored voltage. It should keep the POK_OV bit = b0 to keep the AVIN in the correct operational range. For SYSMON and SYSWARN indication signals, they will show b0 when the AVIN is lower than their configured monitored voltage. Please keep the indication signals of SYSMON and SYSWARN to b1 for normal operation.

AVIN_OV and AVIN UVLO

Once the AVIN is over the SYSMON voltage, the PMIC starts to work. SYSWARN and POK_OV can be used to monitor the AVIN voltage. If the AVIN is under SYSWARN or over POK_OV, the fault status can be sent by nIRQ signal to warn the system. When AVIN is under than SYSWARN (even under than SYSMON) or over than POK_OV, the PMIC still work with the warning status. But if the AVIN continues getting worse to be under AVIN UVLO or be over AVIN OV, the PMIC will force to shut down to protect itself and the backend circuits. Please refer to "State Machine" section for more details.

Status and Flag

The monitored AVIN Status, OT, nRESET and nIRQ in the TOP_STATUS_REG and the monitored Outputs' POK Status in the RAIL_STATUS_REG are all real-time-reaction signal. They are designed as level-triggered signals. When the signal is real (equal to 1), the corresponding bit will also show high level. On the other hand, the bit equal to low level will indicate that the false status is in the corresponding monitored function.

The status of the Outputs' PBAD flags in the RAIL_FLAGx are used to record that the PBAD events issued once. They are designed as edge-triggered signals. If a fault of a rail happens, the related PBAD bit will record the real status at the same time. And then the corresponding PBAD bit will lock the issued PBAD signal even the rail's fault is removed. Read the bit will make the I^2C interface from the "Master Bus" get the real state, but RT5142 will clear the bit to false state (equal to b0) if the PBAD event is removed.

TOP_STATUS_REG, RAIL_STATUS_REG and RAIL_FLAG_REG are the fault codes system used to record what happen in the present. When the power system of the SSD application gets a problem, reading back the register values from the fault codes system can help the user easily understand what is/was going on.

nIRQ (Negative Interrupt Request)

The nIRQ system also belongs to the fault codes system. All the faults happen under RT5142 operation will be recorded by the corresponding internal register functions. The nIRQ system can decide which fault to be exported to SSD system.

There are two embedded register functions, nIRQ_CLEAR and nIRQ_MASK, in the nIRQ system. The nIRQ_CLEAR has two functions:

- One is used to record the fault flag from the TOP_STATUS, RAIL_STATUS and RAIL_FLAGx register.

- The other is designed to write a b1 into self to clear the record of the fault flag from the first function description.

The record function is designed to edge-trigger and lock-out behavior. Once the bit is recorded to b1, the bit will remain locked until it is cleared following step 2 or AVIN is under UVLO voltage.

The nIRQ_MASK function is used to decide that nIRQ output (active low) will monitor the fault built in the nIRQ_CLEAR. If the fault is recorded but masked by the nIRQ system, nIRQ output will ignore the record fault. If the fault is recorded and un-masked, the GPIOx as the nIRQ will output low-level signal (see Figure 9).

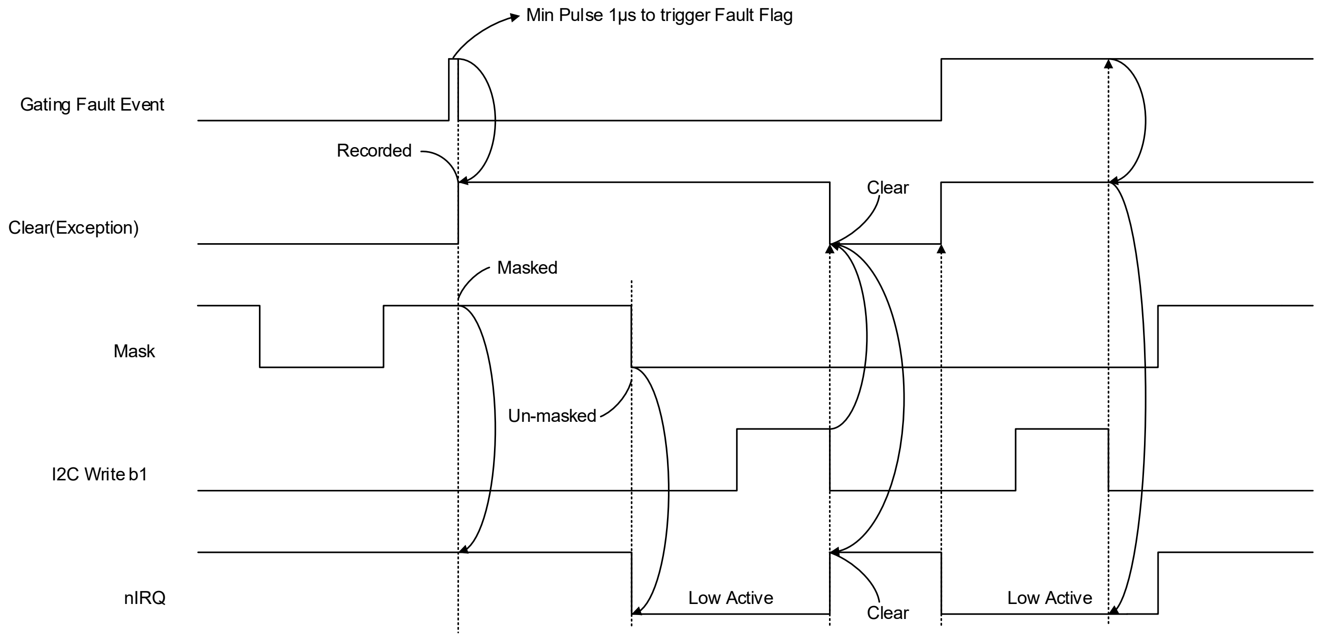


Figure 9. The Relation Chart for nIRQ, Clear and Mask

Power Disable (PWRDIS)

PWRDIS is the main on/off signal to the power down/up sequence of the RT5142. However, it will not enable the behavior of the register values re-loaded from the EFUSE with PWRDIS = H to L. PWRDIS_DELAY_TIME function can delay the PWRDIS signal to the power-off sequence of the RT5142. When PWRDIS = L with AVIN in the normal range, RT5142 will enable the power up sequence immediately. The power off delay time can be set as 0ms, 0.5ms, 1ms, 2ms, 4ms, 8ms and 16ms. If users want to disable this function, please set PWRDIS_DELAY_TIME = 0x7 to make RT5142 ignore PWRDIS function.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-36B 2.66x2.70 (BSC) package, the thermal resistance, θ_{JA}, is 28.56°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C − 25°C)/(28.56°C/W) = 3.5W for a WL-CSP-36B 2.66x2.70 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

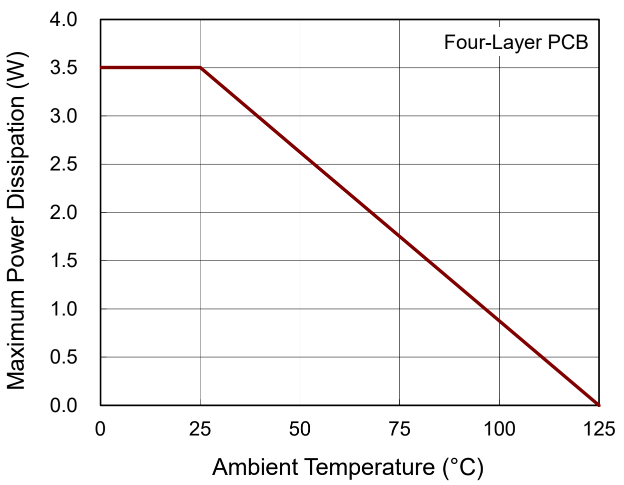


Figure 10. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout.

Power components should be placed on the same side of board, with power traces routed on the same layer. If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths and use multiple vias for interconnection. When vias are used to connect PCB layers in the high current loop, it should have enough vias to reduce the path impedance as possible. The width of power trace is decided by the maximum current passing through. With enough width and vias, the resistance of the entire power trace can be minimized to improve the performance of the converter. Below are some other layout guidelines which should be considered:

- Place the input decoupling capacitors as close as possible to VIN pins (i.e. AVIN, VINLDO1, VIN_B1, VIN_B2, VIN_B3, VIN_B4). Input capacitor can provide instant current to the converter when high-side turns on. It is better to connect the input capacitors to VIN pins directly with a trace on the same layer. It is preferable to connect the decoupling capacitors directly to the pins without using vias.
- Place the inductors close to LX pins (i.e. SW_B1, SW_B2, SW_B3 and SW_B4) and the power trace between them should be wide and short. Using the wide and short trace to minimize the ESR will gain better efficiency. Additionally, this trace copper area provides a heat sink of the inductor and the internal MOSFETs. Do not make the area of the node small by using narrow traces, keep the area as wide as possible without affecting other paths. However, the largest voltage and current variation also happen on the trace of SW_Bx, it should keep any sensitive trace far away from this node.
- For feedback signals FB_B1, FB_B2, FB_B3 and FB_B4, the sensing point which detects the output

voltage must be connected after output capacitor, and keep the trace far away from the switching node or inductor. In addition, the current through the FB_Bx trace should be very small. Please place the feedback network as close to the chip as possible.

- Place the output capacitors close to LDO1, LDO2 and the output side of the Bx inductor to minimize trace inductance.
- The GND pins should be connected to a strong ground plane for heat sinking and noise protection.

Suggested Inductors for Typical Application Circuit

Component Supplier	Part No.	Inductance (μH)	Dimensions (mm)	Note
Cyntec	HTTD32251B-R47MMR	0.47	3.2 x 2.5 x 1.2	L1, L3
Cyntec	HMMQ20161B-R47MDR	0.47	2 x 1.6 x 1.2	L2, L4

Recommended Component Selection for Typical Application Circuit

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM155R60J225ME01	2.2	0402
MURATA	GRM188R60J106ME47	10	0603
MURATA	GRM188R60J226ME15	22	0603

Functional Register Table

The following Table 10 is a summary of registers. It shows the register default value of PMIC when the AVIN is over UVLO rising threshold but under VSYSMON. Certain default values of register address are from EFUSE. When AVIN is over UVLO, thes status of some registers will be decided by the three states (H, Hi-Z, L) of GPIO#.

Table 10. Register Summary

Address	Register Name	Default Value (Hex.)			Type	EFUSE	Control by GPIO#
		H	Hi-Z	L			
0x00	TOP_STATUS_REG	00	00	00	RO	--	--
0x01	RAIL_FLAG_REG0	00	00	00	RO	--	--
0x02	RAIL_FLAG_REG1	00	00	00	RO	--	--
0x03	RAIL_STATUS_REG	00	00	00	RO	--	--
0x04	RAIL_FALG_REG2	00	00	00	RO	--	--
0x05	GPIO1_REG	04	04	04	RW	Bits[7:0]	--
0x06	GPIO2_REG	00	00	00	RW	Bits[6:3]	--
0x07	GPIO3_REG	00	00	00	RW	Bits[6:3]	--
0x08	GPIO4_REG	00	00	00	RW	Bits[6:3]	--
0x09	GPIO5_REG	18	10	10	RW	Bits[6:3]	GPIO3
0x0A	GPIO6_REG	00	00	00	RW	Bits[6:3]	--
0x0B	GPIO7_REG	30	30	30	RW	Bits[6:3]	GPIO3
0x0C	GPIO8_REG	20	20	20	RW	Bits[6:3]	GPIO3
0x0D	GPIO3_DELAY_REG0	25	00	15	RW	Bits[7:0]	GPIO3
0x0E	GPIO3_DELAY_REG1	8E	08	C8	RW	Bits[7:0]	GPIO3
0x0F	WARN_VTH_REG0	00	00	00	RW	--	--
0x10	WARN_VTH_REG1	00	00	00	RW	--	--
0x11	nRESET_MASK_REG	00	00	00	RW	--	--
0x12	nIRQ_CLEAR_REG	00	00	00	W1C*1	--	--
0x13	nIRQ_MASK_REG	00	00	00	RW	--	--
0x14	EXT_EN1_TIME	07	07	07	RW	Bits[7:0]	--
0x15	EXT_EN2_TIME	07	07	07	RW	Bits[7:0]	--
0x16	EXT_EN_PG_1	C0	C0	C0	RW	--	--
0x17	EXT_EN_PG_2	C0	C0	C0	RW	--	--
0x18	EXT_EN_DELAY	00	00	00	RW	--	--
0x19	SST_REG0	55	55	55	RW	Bits[7:0]	--
0x1A	SST_REG1	00	00	00	RW	Bits[7:0]	--
0x1B	B1_CFG_REG	6A	6A	6A	RW	Bits[3:1]	--
0x1C	B1_SEL_REG	A0	A0	F0	RW	Bits[7:2]	GPIO2
0x1D	B2_CFG_REG	6A	6A	6A	RW	--	--

Address	Register Name	Default Value (Hex.)			Type	EFUSE	Control by GPIO#
		H	Hi-Z	L			
0x1E	B2_SEL_REG	3C	3C	3C	RW	Bits[7:1]	GPIO2
0x1F	B3_CFG_REG	6A	6A	6A	RW	Bits[3:1]	--
0x20	B3_SEL_REG	42	3C	46	RW	Bits[7:1]	GPIO3
0x21	B3_DVS_SEL_REG	42	32	2E	RW	Bits[7:1]	GPIO3
0x22	B4_CFG_REG	6A	6A	6A	RW	--	--
0x23	B4_SEL_REG	28	B4	3C	RW	Bits[7:1]	GPIO4
0x24	LDO1_SEL_REG	40	40	40	RW	Bits[7:2]	GPIO4
0x25	LDO2_SEL_REG	40	40	40	RW	Bits[7:2]	GPIO6
0x26	DCDCCTRL_REG0	00	00	00	RW	--	--
0x27	SLEEP_REG0	3C	3C	3C	RW	Bits[7:2]	GPIO3
0x28	SLEEP_REG1	24	3C	3C	RW	Bits[7:2]	GPIO3
0x29	DCDCCRTL_REG1	00	00	00	RW	--	--
0x2A	DISCHARGE_REG	FC	FC	FC	RW	--	--
0x2B	DCDCCTRL_REG2	00	00	00	RW	--	--
0x2C	B1_TIME_REG0	00	00	00	RW	--	--
0x2D	B1_TIME_REG1	0D	0D	0D	RW	Bits[4:0]	--
0x2E	B2_TIME_REG0	00	00	00	RW	--	--
0x2F	B2_TIME_REG1	70	70	70	RW	Bits[4:0]	--
0x30	B3_TIME_REG0	00	00	00	RW	--	--
0x31	B3_TIME_REG1	04	04	04	RW	Bits[4:0]	--
0x32	B4_TIME_REG0	00	00	00	RW	--	--
0x33	B4_TIME_REG1	61	61	61	RW	Bits[4:0]	--
0x34	MANUFACTURER_ID_REG	--	--	--	RO	Bits[7:0]	--
0x35	LDO1_TIME_REG0	00	00	00	RW	--	--
0x36	LDO1_TIME_REG1	01	01	01	RW	Bits[4:0]	--
0x37	LDO2_TIME_REG0	00	00	00	RW	--	--
0x38	LDO2_TIME_REG1	01	01	01	RW	Bits[4:0]	--
0x39	PWRDIS_REG	00	00	00	RW	Bits[2:0]	--
0x3A	PRODUCT_ID_REG	--	--	--	RO	--	--
0x3B	REVISION_NUMBER_REG	--	--	--	RO	--	--
0x3C	TOP_CTRL_REG	70	70	70	RW*2	Bit[4]	--
0x3D	B3_REAL_SEL_REG	--	--	--	RO	--	GPIO3
0x3E	RELOAD_EFUSE_REG	00	00	00	RW*2	--	--
0xF0	MODE_FLAG_REG	00	00	00	R	--	--
0xF1	PASSWORD_REG	00	00	00	RW	--	--

Note: *1: W1C means that “write 1b to clear the bit”. *2: The register read/write only in the hidden mode.

Registers Configuration

Please see below register tables for the detailed description of their functions. Some of the registers are volatile registers. Volatile registers are accessible through I^2C slave bus and are not valid while AVIN is under UVLO. Some of the registers will re-load its register values from the values fixed by the EFUSE. Table 6 shows which value of the register function can be adjusted by the factory.

Table 11. TOP_STATUS_REG

Address: 0x00
Description: Top status bit to indicate VIN and PMIC PG or PBAD.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VSYSMON	VSYSWARN	POK_OV	VIN_OV	OT_WARN	OT_PMIC	nRESET	IRQ
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	VSYSMON	Real Time bit. 1b: VIN ≥ VSYSMON 0b: VIN < VSYSMON If AVIN is above VSYSMON threshold, REG_0x00[7], VSYSMON, will become 1b with delay 10μs(Typ.).
6	VSYSWARN	Real Time bit. 1b: VIN ≥ VSYSWARN 0b: VIN < VSYSWARN If AVIN is above VSYSWARN threshold, REG_0x00[6], VSYSWARN, will become 1b with delay 10μs(Typ.).
5	POK_OV	Real Time bit. 1b: VIN ≥ POK_OV 0b: VIN < POK_OV If AVIN is above POK_OV threshold, REG_0x00[5], POK_OV, will become 1b with delay 10μs(Typ.).
4	VIN_OV	Real Time bit. 1b: VIN ≥ VIN_OV 0b: VIN < VIN_OV If AVIN is above VIN_OV threshold, REG_0x00[4], VIN_OV, will become 1b with delay 10μs(Typ.).
3	OT_WARN	Real Time bit. 1b: PMIC temperature ≥ OT_WARN 0b: PMIC temperature < OT_WARN If PMIC temperature is above OT_WARN threshold, REG_0x00[3], OT_WARN, will become 1b.
2	OT_PMIC	Real Time bit. 1b: PMIC temperature ≥ OT_PMIC 0b: PMIC temperature < OT_PMIC If PMIC temperature is above OT_PMIC threshold, REG_0x00[2], OT_PMIC, will become 1b.
1	nRESET	Real Time bit. 1b: indicates PMIC Power Good (PG) after power-up sequence 0b: indicates PMIC Power Bad (PBAD)
0	IRQ	Real Time bit. 1b: indicates triggered fault 0b: indicates non-fault

Table 12. RAIL_FLAG_REG0

Address: 0x01 **Description:** This register bit is used to record the UVP event triggered once.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_UV	B2_UV	B3_UV	B4_UV	LDO1_UV	LDO2_UV	Reserved	
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_UV	Rails' flag bit. 1b: indicates UV on B1 once 0b: normal Reading this bit will reset this bit to 0b.
6	B2_UV	Rails' flag bit. 1b: indicates UV on B2 once 0b: normal Reading this bit will reset this bit to 0b.
5	B3_UV	Rails' flag bit. 1b: indicates UV on B3 once 0b: normal Reading this bit will reset this bit to 0b.
4	B4_UV	Rails' flag bit. 1b: indicates UV on B4 once 0b: normal Reading this bit will reset this bit to 0b.
3	LDO1_UV	Rails' flag bit. 1b: indicates UV on LDO1 once 0b: normal Reading this bit will reset this bit to 0b.
2	LDO2_UV	Rails' flag bit. 1b: indicates UV on LDO2 once 0b: normal Reading this bit will reset this bit to 0b.

Table 13. RAIL_FLAG_REG1

Address: 0x02
Description: This register bit is used to record the OVP event triggered once.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_OV	B2_OV	B3_OV	B4_OV	LDO1_OV	LDO2_OV	Reserved	
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_OV	Rails' flag bit. 1b: indicates OV on B1 once 0b: normal Reading this bit will reset this bit to 0b.
6	B2_OV	Rails' flag bit. 1b: indicates OV on B2 once 0b: normal Reading this bit will reset this bit to 0b.
5	B3_OV	Rails' flag bit. 1b: indicates OV on B3 once 0b: normal Reading this bit will reset this bit to 0b.
4	B4_OV	Rails' flag bit. 1b: indicates OV on B4 once 0b: normal Reading this bit will reset this bit to 0b.
3	LDO1_OV	Rails' flag bit. 1b: indicates OV on LDO1 once 0b: normal Reading this bit will reset this bit to 0b.
2	LDO2_OV	Rails' flag bit. 1b: indicates OV on LDO2 once 0b: normal Reading this bit will reset this bit to 0b.

Table 14. RAIL_STATUS_REG

Address: 0x03 **Description:** The rail's status bit to indicate output POK.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_POK	B2_POK	B3_POK	B4_POK	LDO1_POK	LDO2_POK	Reserved	
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	B1_POK	Real time for rail's flag bit. 1b: indicates POK on B1 0b: no POK on B1
6	B2_POK	Real time for rail's flag bit. 1b: indicates POK on B2 0b: no POK on B2
5	B3_POK	Real time for rail's flag bit. 1b: indicates POK on B3 0b: no POK on B3
4	B4_POK	Real time for rail's flag bit. 1b: indicates POK on B4 0b: no POK on B4
3	LDO1_POK	Real time for rail's flag bit. 1b: indicates POK on LDO1 0b: no POK on LDO1
2	LDO2_POK	Real time for rail's flag bit. 1b: indicates POK on LDO2 0b: no POK on LDO2

Table 15. RAIL_FLAG_REG2

Address: 0x04 **Description:** This register bit is used to record the ILIM event triggered once.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ILIM	B2_ILIM	B3_ILIM	B4_ILIM	LDO1_ILIM	LDO2_ILIM	Reserved	
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	B1_ILIM	Rails' flag bit. Indicates ILIM on B1 once. 1b: indicates ILIM on B1 once 0b: normal Reading this bit will reset this bit to 0b.
6	B2_ILIM	Rails' flag bit. Indicates ILIM on B2 once. 1b: indicates ILIM on B2 once 0b: normal Reading this bit will reset this bit to 0b.
5	B3_ILIM	Rails' flag bit. Indicates ILIM on B3 once. 1b: indicates ILIM on B3 once 0b: normal Reading this bit will reset this bit to 0b.
4	B4_ILIM	Rails' flag bit. Indicates ILIM on B4 once. 1b: indicates ILIM on B4 once 0b: normal Reading this bit will reset this bit to 0b.
3	LDO1_ILIM	Rails' flag bit. Indicates ILIM on LDO1 once. 1b: indicates ILIM on LDO1 once 0b: normal Reading this bit will reset this bit to 0b.
2	LDO2_ILIM	Rails' flag bit. Indicates ILIM on LDO2 once. 1b: indicates ILIM on LDO2 once 0b: normal Reading this bit will reset this bit to 0b.

Table 16. GPIO1(POR)_REG

Address: 0x05 **Description:** GPIO1 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved					nRST_DELAY_TIME		
Read/Write	R	R	R	R	R	RW	RW	RW
Default Value	0	0	0	0	0	1	0	0

Bits	**Name**	**Description**
2:0	nRST _DELAY_TIME	The timing from the POK signal of B3 rail in the power up sequence to nRESET signal. 000b = delay 0.5ms. 001b = delay 1ms. 010b = delay 2ms. 011b = delay 4ms. 100b = delay 8ms. 101b = delay 16ms. 110b = delay 32ms. 111b = delay 64ms.

Table 17. GPIO2_REG

Address: 0x06 **Description:** GPIO2 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO2_FUNC_EN	GPIO2_FUNC_SEL				Reserved	GPIO2_GENERAL_CTRL	
Read/Write	RW	RW	RW	RW	RW	R	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GPIO2_FUNC_EN	GPIO2 has an initial function before nRESET=1. This bit can disable the function of "GPIO2_FUNC_SEL" after nRESET=1. 0b: disable 1b: enable
6:3	GPIO2_FUNC_SEL	0000b = General IO1 (as EXT_EN1_O output) 0001b = General IO2 (as EXT_EN2_O output) 0010b = nIRQ (output) 0011b = Sleep Mode (input) 0100b = Deeper Sleep Mode (input) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ no use for GPIO2/3/4 1000b = EXT_EN2_I (input)/ no use for GPIO2/3/4
1:0	GPIO2_GENERAL_CTRL	If the function selection is as "General IO1/2", these bits can control the voltage level of the General IO1/2. If GPIO2/3/4/6 is as EXT_EN1/2_O, the EXT_EN1/2_O function only can be enabled after nRESET = 1.* 00b = low level 01b = high level

NOTE: *: GPIO2/3/4/6 are used to control the VSELx of the rails before nRESET = 1. Please send out EXT_EN1/2_O signal after nRESET = 1 manually, if set GPIO2/3/4/6 as the EXT_EN1/2_O function.

Table 18. GPIO3_REG

Address: 0x07 **Description:** GPIO3 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO3_FUNC_EN	GPIO3_FUNC_SEL				Reserved	GPIO3_GENERAL_CTRL	
Read/Write	RW	RW	RW	RW	RW	R	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GPIO3_FUNC_EN	GPIO3 has an initial function before nRESET=1. This bit can disable the function of "GPIO3_FUNC_SEL" after nRESET=1. 0b: disable 1b: enable
6:3	GPIO3_FUNC_SEL	0000b = General IO1 (as EXT_EN1_O output) 0001b = General IO2 (as EXT_EN2_O output) 0010b = nIRQ (output) 0011b = Sleep Mode (input) 0100b = Deeper Sleep Mode (input) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ no use for GPIO2/3/4 1000b = EXT_EN2_I (input)/ no use for GPIO2/3/4
1:0	GPIO3_GENERAL_CTRL	If the function selection is as "General IO1/2", these bits can control the voltage level of the General IO1/2. If GPIO2/3/4/6 is as EXT_EN1/2_O, the EXT_EN1/2_O function only can be enabled after nRESET = 1. 00b = low level 01b = high level

Table 19. GPIO4_REG

Address: 0x08 **Description:** GPIO4 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO4_FUNC_EN	GPIO4_FUNC_SEL				Reserved	GPIO4_GENERAL_CTRL	
Read/Write	RW	RW	RW	RW	RW	R	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GPIO4_FUNC_EN	GPIO4 has an initial function before nRESET=1. This bit can disable the function of "GPIO4_FUNC_SEL" after nRESET=1. 0b: disable 1b: enable
6:3	GPIO4_FUNC_SEL	0000b = General IO1 (as EXT_EN1_O output) 0001b = General IO2 (as EXT_EN2_O output) 0010b = nIRQ (output) 0011b = Sleep Mode (input) 0100b = Deeper Sleep Mode (input) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ no use for GPIO2/3/4 1000b = EXT_EN2_I (input)/ no use for GPIO2/3/4
1:0	GPIO4_GENERAL_CTRL	If the function selection is as "General IO1/2", these bits can control the voltage level of the General IO1/2. If GPIO2/3/4/6 is as EXT_EN1/2_O, the EXT_EN1/2_O function only can be enabled after nRESET = 1. 00b = low level 01b = high level

Table 20. GPIO5_REG

Address: 0x09
Description: GPIO5 configuration by GPIO3 status (H, Hi-Z, L).

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		Reserved	GPIO5_FUNC_SEL				Reserved	GPIO5_GENERAL_CTRL	
Read/Write		R	RW	RW	RW	RW	R	RW	RW
Default Value	H	--	0	0	1	1	--	0	0
	Hi-Z	--	0	0	1	0	--	0	0
	L	--	0	0	1	0	--	0	0

Bits	**Name**	**Description**
6:3	GPIO5_FUNC_SEL	0000b = General IO1 (as EXT_EN1_O output) 0001b = General IO2 (as EXT_EN2_O output) 0010b = nIRQ (output) 0011b = Sleep Mode (input) 0100b = Deeper Sleep Mode (input) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ no use for GPIO2/3/4 1000b = EXT_EN2_I (input)/ no use for GPIO2/3/4 1001b = SYSMON
1:0	GPIO5_GENERAL_CTRL	If the function selection is as “General GPIO1/2”, these bits can control the voltage level of the General GPIO1/2. 00b = low level 01b = high level

Table 21. GPIO6_REG

<table>
<tr><td colspan="9">Address: 0x0A
Description: GPIO6 configuration.</td></tr>
<tr><td>Bits</td><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>Name</td><td>GPIO6_FUNC_EN</td><td colspan="4">GPIO6_FUNC_SEL</td><td>Reserved</td><td colspan="2">GPIO6_GENERAL_CTRL</td></tr>
<tr><td>Read/Write</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>R</td><td>RW</td><td>RW</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

Bits	**Name**	**Description**
7	GPIO6_FUNC_EN	GPIO6 has an initial function before nRESET=1. This bit can disable the function of “GPIO6_FUNC_SEL” after nRESET=1. 0b: disable 1b: enable
6:3	GPIO6_FUNC_SEL	0000b = General IO1 (as EXT_EN1_O output) 0001b = General IO2 (as EXT_EN2_O output) 0010b = nIRQ (output) 0011b = Sleep Mode (input) 0100b = Deeper Sleep Mode (input) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ no use for GPIO2/3/4 1000b = EXT_EN2_I (input)/ no use for GPIO2/3/4
1:0	GPIO6_GENERAL_CTRL	If the function selection is as “General IO1/2”, these bits can control the voltage level of the General IO1/2. If GPIO2/3/4/6 is as EXT_EN1/2_O, the EXT_EN1/2_O function only can be enabled after nRESET = 1. 00b = low level 01b = high level

Table 22. GPIO7_REG

Address: 0x0B **Description:** GPIO7 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	GPIO7_FUNC_SEL				Reserved	GPIO7_GENERAL_CTRL	
Read/Write	R	RW	RW	RW	RW	R	RW	RW
Default Value	0	0	1	1	0	0	0	0

Bits	Name	Description
6:3	GPIO7_FUNC_SEL	0000b = General IO1 (as EXT_EN1_O output) 0001b = General IO2 (as EXT_EN2_O output) 0010b = nIRQ (output) 0011b = Sleep Mode (input) 0100b = Deeper Sleep Mode (input) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ no use for GPIO2/3/4 1000b = EXT_EN2_I (input)/ no use for GPIO2/3/4
1:0	GPIO7_GENERAL_CTRL	If the function selection is as "General GPIO1/2", these bits can control the voltage level of the General GPIO1/2. 00b = low level 01b = high level

Table 23. GPIO8_REG

Address: 0x0C **Description:** GPIO8 configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	GPIO8_FUNC_SEL				Reserved	GPIO8_GENERAL_CTRL	
Read/Write	R	RW	RW	RW	RW	R	RW	RW
Default Value	0	0	1	0	0	0	0	0

Bits	Name	Description
6:3	GPIO8_FUNC_SEL	0000b = General IO1 (as EXT_EN1_O output) 0001b = General IO2 (as EXT_EN2_O output) 0010b = nIRQ (output) 0011b = Sleep Mode (input) 0100b = Deeper Sleep Mode (input) 0101b = B1/B2 enable/disable (input) 0110b = PWRDIS (input) 0111b = EXT_EN1_I (input)/ no use for GPIO2/3/4 1000b = EXT_EN2_I (input)/ no use for GPIO2/3/4
1:0	GPIO8_GENERAL_CTRL	If the function selection is as "General GPIO1/2", these bits can control the voltage level of the General GPIO1/2. 00b = low level 01b = high level

Table 24. GPIO3_Delay_REG0

Address: 0x0D
Description: B4 and LDO1 delay time selection during the power up sequence by GPIO3 status (H, Hi-Z, L).

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B4_DELAY_SEL						LDO1_DELAY_SEL_H	
Read/Write		RW	RW	RW	RW	RW	RW	RW	RW
Default Value	H	0	0	1	0	0	1	0	1
	Hi-Z	0	0	0	0	0	0	0	0
	L	0	0	0	1	0	1	0	1

Bits	**Name**	**Description**
7:2	B4_DELAY_SEL	Offset = 0ms Step = 0.25ms Delay time = DEC(0x0D[7:2]) x 0.25ms
1:0	LDO1_DELAY_SEL_H	LDO1_DELAY_SEL_H bits and LDO1_DELAY_SEL_L bits are combined to 4 bits. Offset = 0ms Step = 0.25ms Delay time = DEC(0x0D[1:0]) x 4 x 0.25ms

Table 25. GPIO3_Delay_REG1

Address: 0x0E
Description: LDO1 and LDO2 delay time selection during the power up sequence by GPIO3 status (H, Hi-Z, L).

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		LDO1_DELAY_SEL_L		LDO2_DELAY_SEL					
Read/Write		RW	RW	RW	RW	RW	RW	RW	RW
Default Value	H	1	0	0	0	1	1	1	0
	Hi-Z	0	0	0	0	1	0	0	0
	L	1	1	0	0	1	0	0	0

Bits	**Name**	**Description**
7:6	LDO1_DELAY_SEL_L	LDO1_DELAY_SEL_H bits and LDO1_DELAY_SEL_L bits are combined to 4 bits. Offset = 0ms Step = 0.25ms Delay time = DEC(0x0E[7:6]) x 0.25ms
5:0	LDO2_DELAY_SEL	Offset = 0ms Step = 0.25ms Delay time = DEC(0x0E[5:0]) x 0.25ms

Table 26. WARN_REG0

Address: 0x0F **Description:** SYSWARN and SYSMON Vth configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SYSWARN_SEL				SYSMON_SEL			
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	SYSWARN_SEL	Vth of the SYSWARN selection: Offset = 2775mV Step = 25mV Max = 3150mV SYSWARN threshold = 2775mV + DEC(0x0F[7:4]) x 25mV
3:0	SYSMON_SEL	Vth of the SYSMON selection Offset = 2725mV Step = 25mV Max = 3100mV SYSMON threshold = 2725mV + DEC(0x0F[3:0]) x 25mV

Table 27. WARN_REG1

Address: 0x10 **Description:** POK_OV Vth configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	POK_OV_SEL	Reserved						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	POK_OV_SEL	Vth of POK_OV warning signal selection: 0b = 3.5V 1b = 3.8V

Table 28. nRESET_MASK_REG

Address: 0x11 **Description:** Mask the protection function which will make nRESET signal active.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_PBAD_RESET_MASK	B2_PBAD_RESET_MASK	B3_PBAD_RESET_MASK	B4_PBAD_RESET_MASK	L1_PABD_RESET_MASK	L2_PBAD_RESET_MASK	VIN_OV_RESET_MASK	OT_RESET_MASK
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7	B1_PBAD_RESET_MASK	Mask the analog circuit protection behavior, but the digital fault flags still implement. 0b = Nothing. 1b = mask the analog protection behavior.
6	B2_PBAD_RESET_MASK	
5	B3_PBAD_RESET_MASK	
4	B4_PBAD_RESET_MASK	
3	L1_PBAD_RESET_MASK	
2	L2_PBAD_RESET_MASK	
1	VIN_OV_RESET_MASK	
0	OT_RESET_MASK	

Table 29. nIRQ_CLEAR_REG

Address: 0x12 **Description:** Indicates the interrupt flag and can write 1b to clear the interrupt flag of the exception bit.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_UNDER_SYSMON_CLR	VIN_UNDER_SYSWARN_CLR	VIN_OVER_POK_OV_CLR	VIN_OV_CLR	OT_WARN_CLR	OUTPUT_OVUV_CLR	Reserved	
Read/Write	W1C	W1C	W1C	W1C	W1C	W1C	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	VIN_UNDER_SYSMON_CLR	0b: nothing 1b: indicates the interrupt flag of the event Write 1b to clear the exception bit, if the event does not exist.
6	VIN_UNDER_SYSWARN_CLR	
5	VIN_OVER_POK_OV_CLR	
4	VIN_OV_CLR	
3	OT_WARN_CLR	
2	OUTPUT_OVUV_CLR	

Table 30. nIRQ_MASK_REG

Address: 0x13 **Description:** Mask the interrupt flag (nIRQ) of the event but the flag of the exception bit will still work.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_UNDER_SYSMON_MASK	VIN_UNDER_SYSWARN_MASK	VIN_OVER_POK_OV_MASK	VIN_OV_MASK	OT_WARN_MASK	OUTPUT_OVUV_MASK	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	VIN_UNDER_SYSMON_MASK	Only mask the interrupt flag (nIRQ) of the event but the flag of the exception bit will still work well. 0b: does not mask the interrupt flag of the event 1b: mask the interrupt flag of the event
6	VIN_UNDER_SYSWARN_MASK	
5	VIN_OVER_POK_OV_MASK	
4	VIN_OV_MASK	
3	OT_WARN_MASK	
2	OUTPUT_OVUV_MASK	

Table 31. EXT_EN1_O_TIME_SLOT_REG

Address: 0x14
Description: Configure the wake-up time slot of the external enable1 output (EXT_EN1_O) during the wake-up sequence. The EXT_EN1_O will issue from low to high automatically at the setting time slot.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved			EXT_EN1_O_TIME_SLOT				
Read/Write	R	R	R	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	1	1	1

Bits	Name	Description
4:0	EXT_EN1_O_TIME_SLOT	EXT_EN1_O wake-up sequence w/o external controlled signal from sleep mode 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 32. EXT_EN2_O_TIME_SLOT_REG

Address: 0x15
Description: Configure the wake-up time slot of the external enable2 output (EXT_EN2_O) during the wake-up sequence. The EXT_EN2_O will issue from low to high automatically at the setting time slot.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved			EXT_EN2_O_TIME_SLOT				
Read/Write	R	R	R	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	1	1	1

Bits	Name	Description
4:0	EXT_EN2_O_TIME_SLOT	EXT_EN2_O wake-up sequence w/o external controlled signal from sleep mode. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 33. EXT_EN1_I

Address: 0x16 **Description:** Configure the input signal to trigger EXT_EN1_O.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXT_EN1_O_INPUT_SEL		EXT_EN1_O_POK_SEL			EXT_EN1_I_SEL		Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	R
Default Value	1	1	0	0	0	0	0	0

Bits	Name	Description
7:6	EXT_EN1_O_INPUT_SEL	EXT_EN1_O follows the below selected signal and issue the high level voltage signal with a delay time. 00b = Rails' POK 01b = EXT_EN1_I 10b = I2C Interface. (as General IO1/2) 11b = EXT_EN1_O_TIME_SLOT
5:3	EXT_EN1_POK_SEL	If bits [7:6] = 00b, EXT_EN1_O will go high after the below POK signal of the rail with a delay time. 000b = B1 001b = B2 010b = B3 011b = B4 100b = L1 101b = L2 110b = nRESET 111b = VSYSMON
2:1	EXT_EN1_I_SEL	If bit[7:6] = 01b, EXT_EN1_O will go high after the below GPIOx (as EXT_EN1_I) going high with a delay time. 000b = GPIO5 001b = GPIO6 010b = GPIO7 011b = GPIO8

Table 34. EXT_EN2_I

Address: 0x17 **Description:** Configure the input signal to trigger EXT_EN2_O.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXT_EN2_O_INPUT_SEL		EXT_EN2_O_POK_SEL			EXT_EN2_I_SEL		Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	R
Default Value	1	1	0	0	0	0	0	0

Bits	Name	Description
7:6	EXT_EN2_O_INPUT_SEL	EXT_EN2_O follows the below selected signal and issue the high level voltage signal with a delay time. 00b = Rails' POK 01b = EXT_EN2_I 10b = I2C Interface. (as General IO1/2) 11b = EXT_EN2_O_TIME_SLOT
5:3	EXT_EN2_POK_SEL	If bits [7:6] = 00b, EXT_EN2_O will go high after the below POK signal of the rail with a delay time. 000b = B1 001b = B2 010b = B3 011b = B4 100b = L1 101b = L2 110b = nRESET 111b = VSYSMON
2:1	EXT_EN2_I_SEL	If bit[7:6] = 01b, EXT_EN2_O will go high after the below GPIOx (as EXT_EN2_I) going high with a delay time. 000b = GPIO5 001b = GPIO6 010b = GPIO7 011b = GPIO8

Table 35. EXT_ENx_O_DELAY

Address: 0x18 **Description:** The delay time setting for EXT_EN1 and EXT_EN2.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXT_EN1_O_DELAY				EXT_EN2_O_DELAY			
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	EXT_EN1_O_DELAY	If the following signal is Rail's POK, EXT_EN1/2_I or Time_Slot, EXT_EN1/2_O will issue from low to high with below delay time. Offset = 0ms Step = 0.25ms EXT_EN1 Delay time = DEC(0x18[7:4]) x 0.25ms EXT_EN2 Delay time = DEC(0x18[3:0]) x 0.25ms
3:0	EXT_EN2_O_DELAY	

Table 36. SST_REG0

Address: 0x19 **Description:** Rails' soft-start time configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_SST_SEL		B2_SST_SEL		B3_SST_SEL		B4_SST_SEL	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	1	0	1	0	1	0	1

Bits	Name	Description
7:6	B1_SST_SEL	Soft-start time for B1 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs
5:4	B2_SST_SEL	Soft-start time for B2 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs
3:2	B3_SST_SEL	Soft-start time for B3 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs
1:0	B4_SST_SEL	Soft-start time for B4_BUCK Mode 00b = 125μs, 01b = 250μs, 10b = 500μs, 11b = 750μs Soft-start time for B4_LDO Mode 00b = 250μs, 01b = 500μs, 10b = Reserved, 11b = Reserved.

Table 37. SST_REG1

Address: 0x1A **Description:** Rails' soft-start time configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO1_SST_SEL	LDO2_SST_SEL	Reserved					
Read/Write	RW	RW	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	LDO1_SST_SEL	Soft-start time for LDO1/2 Mode 0b = 250μs 1b = 500μs
6	LDO2_SST_SEL	

Table 38. B1_CFG_REG

Address: 0x1B **Description:** Configure OC level, soft-start slew rate, and f_{SW} of B1.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ILMAX		B1_TSTEP		B1_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	R
Default Value	0	1	1	0	1	0	1	0

Bits	**Name**	**Description**
7:6	B1_ILMAX	00b = 4A 01b = 5A(default) 10b = 6A 11b = 7A
5:4	B1_TSTEP	00b = DVID up:20mV/μs, DVID down:5mV/μs 01b = DVID up:15mV/μs, DVID down:5mV/μs 10b = DVID up:10mV/μs, DVID down:5mV/μs(default) 11b = DVID up:5mV/μs, DVID down:5mV/μs
3:1	B1_FREQ	f_{SW} supply state: 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

Table 39. B1_SEL_REG

Address: 0x1C
Description: B1 VID selection by GPIO2 status (H, Hi-Z, L).

Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B1_SEL						Reserved	
Read/Write		RW	RW	RW	RW	RW	RW	R	R
Default Value	H	1	0	1	0	0	0	0	0
	Hi-Z	1	0	1	0	0	0	0	0
	L	1	1	1	1	0	0	0	0

Bits	Name	Description
7:2	B1_SEL	B1 VOUT supply voltage: 000000b: 1.7V 000001b: 1.72V 000010b: 1.74V … 101000b: 2.5V … 111100b: 2.9V 111100b ~111111b: 2.9V

Table 40. B2_CFG_REG

Address: 0x1D
Description: Configure OC level, soft-start slew rate, and fsw of B2.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_ILMAX		B2_TSTEP		B2_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	R
Default Value	0	1	1	0	1	0	1	0

Bits	Name	Description
7:6	B2_ILMAX	00b = 2A 01b = 3A(default) 10b = 4A 11b = 5A
5:4	B2_TSTEP	00b = DVID up:20mV/µs, DVID down:5mV/µs 01b = DVID up:15mV/µs, DVID down:5mV/µs 10b = DVID up:10mV/µs, DVID down:5mV/µs(default) 11b = DVID up:5mV/µs, DVID down:5mV/µs
3:1	B2_FREQ	fsw supply state: 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

Table 41. B2_SEL_REG

Address: 0x1E Description: B2 VID selection.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_SEL							Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	R
Default Value	0	0	1	1	1	1	0	0

Bits	Name	Description
7:1	B2_SEL	B2 VOUT supply voltage: 0000000b: 0.9V 0000001b: 0.91V 0000010b: 0.92V … 0011110b: 1.2V … 1101110b:2.0V 1101110b ~1111111b: 2.0V

Table 42. B3_CFG_REG

Address: 0x1F Description: Configure OC level, soft-start slew rate, and fsw of B3.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_ILMAX		B3_TSTEP		B3_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	R
Default Value	0	1	1	0	1	0	1	0

Bits	Name	Description
7:6	B3_ILMAX	00b = 4A 01b = 5A(default) 10b = 6A 11b = 7A
5:4	B3_TSTEP	00b = DVID up:20mV/μs, DVID down:5mV/μs 01b = DVID up:15mV/μs, DVID down:5mV/μs 10b = DVID up:10mV/μs, DVID down:5mV/μs(default) 11b = DVID up:5mV/μs, DVID down:5mV/μs
3:1	B3_FREQ	fsw supply state: 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

Table 43. B3_SEL_REG

Address: 0x20 **Description:** B3 VID selection by GPIO3 status (H, Hi-Z, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B3_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	R
Default Value	H	0	1	0	0	0	0	1	0
	Hi-Z	0	0	1	1	1	1	0	0
	L	0	1	0	0	0	1	1	0

Bits	**Name**	**Description**
7:1	B3_SEL	B3 VOUT supply voltage: 0000000b: 0.5V 0000001b: 0.51V 0000010b: 0.52V … 0011110b: 0.8V … 0100001b: 0.83V … 0100011b: 0.85V … 1010000b: 1.3V 1010000b ~1111111b: 1.3V

Table 44. B3_DVS_SEL_REG

Address:0x21 **Description:** Configure the B3 voltage which will do DVID down to at the sleep mode. (by GPIO3 status (H, Hi-Z, L))									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B3_DVS_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	R
Default Value	H	0	1	0	0	0	0	1	0
	Hi-Z	0	0	1	1	0	0	1	0
	L	0	0	1	0	1	1	1	0

Bits	**Name**	**Description**
7:1	B3_DVS_SEL	B3 VOUT supply voltage at sleep mode: 0000000b: 0.5V 0000001b: 0.51V 0000010b: 0.52V … 0010111b: 0.73V … 0011001b: 0.75V … 0100001b: 0.83V … 1010000b: 1.3V 1010000b ~1111111b: 1.3V

Table 45. B4_CFG_REG

Address: 0x22
Description: Configure OC level, soft-start slew rate, and f_{SW} of B4.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B4_ILMAX		B4_TSTEP		B4_FREQ			Reserved
Read/Write	RW	RW	RW	RW	RW	RW	RW	R
Default Value	0	1	1	0	1	0	1	0

Bits	Name	Description
7:6	B4_ILMAX	Overcurrent Limit for B4_BUCK Mode 00b = 2A 01b = 3A (default) 10b = 4A 11b = 5A Overcurrent Limit for B4_LDO Mode 00b = 400mA 01b = 500mA (default) 10b = Reserved 11b = Reserved
5:4	B4_TSTEP	00b = DVID up:20mV/μs, DVID down:5mV/μs 01b = DVID up:15mV/μs, DVID down:5mV/μs 10b = DVID up:10mV/μs, DVID down:5mV/μs(default) 11b = DVID up:5mV/μs, DVID down:5mV/μs
3:1	B4_FREQ	f_{SW} supply state: 000b to 011b = 1MHz 100b = 1.5MHz 101b = 2MHz (default) 110b = 2.5MHz 111b = 3MHz

Table 46. B4_SEL_REG

Address: 0x23 **Description:** B4 VID selection by GPIO4 status (H, Hi-Z, L).									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B4_SEL							Reserved
Read/Write		RW	RW	RW	RW	RW	RW	RW	R
Default Value	H	0	0	1	0	1	0	0	0
	Hi-Z	1	0	1	1	0	1	0	0
	L	0	0	1	1	1	1	0	0

Bits	**Name**	**Description**
7:1	B4_SEL	B4 VOUT supply voltage: 0000000b: 0.9V 0000001b: 0.91V 0000010b: 0.92V … 0010100b: 1.1V … 0011110b: 1.2V … 1011010b: 1.8V (LDO mode) … 1101110b: 2.0V 1101110b ~1111111b: 2.0V

Table 47. LDO1_SEL_REG

Address: 0x24 **Description:** LDO1 VID selection.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO1_SEL						Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	R	R
Default Value	0	1	0	0	0	0	0	0

Bits	**Name**	**Description**
7:2	LDO1_SEL	LDO1 VOUT supply voltage: 000000b: 1.0V 000001b: 1.05V 000010b: 1.10V … 010000b: 1.8V … 100010b:2.7V 100010b ~111111b: 2.7V

Table 48. LDO2_SEL_REG

Address: 0x25 **Description:** LDO2 VID selection.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO2_SEL						Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	R	R
Default Value	0	1	0	0	0	0	0	0

Bits	**Name**	**Description**
7:2	LDO2_SEL	LDO2 VOUT supply voltage: 000000b: 1.0V 000001b: 1.05V 000010b: 1.10V … 010000b: 1.8V … 100010b:2.7V 100010b ~111111b: 2.7V

Table 49. DCDCCTRL_REG0

Address: 0x26 **Description:** Rails' enable signal control.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_EN	B2_EN	B3_EN	B4_EN	LDO1_EN	LDO2_EN	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	B1_EN	0b = low level ENABLE signal 1b = high level ENABLE signal For nRESET = 0, if ENABLE keeps high level which is not from low to high, the rail will follow the time slot to ramp up. For nRESET = 1, if set ENABLE from low level to high level, the rail will ramp up immediately.
6	B2_EN	
5	B3_EN	
4	B4_EN	
3	LDO1_EN	
2	LDO1_EN	

Table 50. SLEEP1_REG

Address: 0x27
Description: Configure the rail to be off or enter low power mode (LPM) in SLEEP1 (PS3.5) mode.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ALIVE_SLEEP1	B2_ALIVE_SLEEP1	B3_ALIVE_SLEEP1	B4_ALIVE_SLEEP1	LDO1_ALIVE_SLEEP1	LDO2_ALIVE_SLEEP1	Reserved	SLEEP1_ENABLE
Read/Write	RW	RW	RW	RW	RW	RW	R	RW
Default Value	0	0	1	1	1	1	0	0

Bits	Name	Description
7	B1_ALIVE_SLEEP1	0b = When PMIC is in SLEEP1 mode (PS3.5 mode), B1 turns off. 1b = When in PS3.5 mode, B1 keeps alive and enter LPM.
6	B2_ALIVE_SLEEP1	0b = When PMIC is in SLEEP1 mode (PS3.5 mode), B2 turns off. 1b = When in PS3.5 mode, B2 keeps alive and enter LPM.
5	B3_ALIVE_SLEEP1	0b = When PMIC is in SLEEP1 mode (PS3.5 mode), B3 turns off. 1b = When in PS3.5 mode, B3 keeps alive and enter LPM.
4	B4_ALIVE_SLEEP1	0b = When PMIC is in SLEEP1 mode (PS3.5 mode), B4 turns off. 1b = When in PS3.5 mode, B4 keeps alive and enter LPM.
3	LDO1_ALIVE_SLEEP1	0b = When PMIC is in SLEEP1 mode (PS3.5 mode), LDO1 turns off. 1b = When in PS3.5 mode, LDO1 keeps alive and enter LPM.
2	LDO2_ALIVE_SLEEP1	0b = When PMIC is in SLEEP1 mode (PS3.5 mode), LDO2 turns off. 1b = When in PS3.5 mode, LDO2 keeps alive and enter LPM.
1	Reserved	Reserved bit.
0	SLEEP1_ENABLE	0b = PMIC is in normal mode, if SLEEP2_ENABLE is also 0b. 1b = PMIC is in sleep mode and all rails follow the settings in this register function to ramp down or enter LPM. The priority of the rail's off state in the SLEEP1 or SLEEP2 is higher than the rail's alive state. If PMIC goes to sleep mode, the rail will follow the off state in the SLEEP1 or SLEEP2 to shutdown at first. Or, the rail will keep alive with both alive settings in the sleep register functions.

Table 51. SLEEP2_REG

Address: 0x28 **Description:** Configure the rail to be off or enter low power mode (LPM) in SLEEP2 (PS4) mode.									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		B1_ALIVE_SLEEP2	B2_ALIVE_SLEEP2	B3_ALIVE_SLEEP2	B4_ALIVE_SLEEP2	LDO1_ALIVE_SLEEP2	LDO2_ALIVE_SLEEP2	Reserved	SLEEP2_ENABLE
Read/Write		RW	RW	RW	RW	RW	RW	R	RW
Default Value	H	0	0	1	0	0	1	0	0
	Hi-Z	0	0	1	1	1	1	0	0
	L	0	0	1	1	1	1	0	0

Bits	**Name**	**Description**
7	B1_ALIVE_SLEEP2	0b = When PMIC is in SLEEP2 mode (PS4 mode), B1 turns off. 1b = When in PS4 mode, B1 keeps alive and enter LPM.
6	B2_ALIVE_SLEEP2	0b = When PMIC is in SLEEP2 mode (PS4 mode), B2 turns off. 1b = When in PS4 mode, B2 keeps alive and enter LPM.
5	B3_ALIVE_SLEEP2	0b = When PMIC is in SLEEP2 mode (PS4 mode), B3 turns off. 1b = When in PS4 mode, B3 keeps alive and enter LPM.
4	B4_ALIVE_SLEEP2	0b = When PMIC is in SLEEP2 mode (PS4 mode), B4 turns off. 1b = When in PS4 mode, B4 keeps alive and enter LPM.
3	LDO1_ALIVE_SLEEP2	0b = When PMIC is in SLEEP2 mode (PS4 mode), LDO1 turns off. 1b = When in PS4 mode, LDO1 keeps alive and enter LPM.
2	LDO2_ALIVE_SLEEP2	0b = When PMIC is in SLEEP2 mode (PS4 mode), LDO2 turns off. 1b = When in PS4 mode, LDO2 keeps alive and enter LPM.
1	Reserved	Reserved bit.
0	SLEEP2_ENABLE	0b = PMIC is in normal mode, if SLEEP1_ENABLE is also 0b. 1b = PMIC is in sleep mode and all rails follow the settings in this register function to ramp down or enter LPM. The priority of the rail's off state in the SLEEP1 or SLEEP2 is higher than the rail's alive state. If PMIC goes to sleep mode, the rail will follow the off state in the SLEEP1 or SLEEP2 to shutdown at first. Or, the rail will keep alive with both alive settings in the sleep register functions.

Table 52. DCDCCTRL_REG1

Address: 0x29
Description: Configure the rail to enter Forced PWM mode (FPWM) at normal operation.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_FPWM	B2_FPWM	B3_FPWM	B4_FPWM	Reserved			
Read/Write	RW	RW	RW	RW	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	B1_FPWM	0b = PSKIP mode 1b = Forced PWM mode
6	B2_FPWM	0b = PSKIP mode 1b = Forced PWM mode
5	B3_FPWM	0b = PSKIP mode 1b = Forced PWM mode
4	B4_FPWM	0b = PSKIP mode 1b = Forced PWM mode

Table 53. DISCHARGE_REG

Address: 0x2A
Description: Rails' discharged resistor path enable signal control.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ DISCH	B2_ DISCH	B3_ DISCH	B4_ DISCH	LDO1_ DISCH	LDO2_ DISCH	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	R	R
Default Value	1	1	1	1	1	1	0	0

Bits	**Name**	**Description**
7	B1_DISCH	0b = disable discharged resistor path 1b = enable discharged resistor path The discharged resistor path will be connected from VOUT to ground with the rail's ENABLE = low level, if the setting of the rail's discharged resistor path enable signal is 1b.
6	B2_DISCH	
5	B3_DISCH	
4	B4_DISCH	
3	LDO1_DISCH	
2	LDO1_DISCH	

Table 54. DCDCCTRL_REG2

Address: 0x2B
Description: Configure the rail to enter PSKIP mode or LPM mode at normal operation.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_LPM	B2_LPM	B3_LPM	B4_LPM	LDO1_ LPM	LDO2_ LPM	Reserved	
Read/Write	RW	RW	RW	RW	RW	RW	R	R
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7	B1_LPM	0b = PSKIP mode 1b = Low Power Mode (LPM mode)
6	B2_LPM	0b = PSKIP mode 1b = LPM mode
5	B3_LPM	0b = PSKIP mode 1b = LPM mode
4	B4_LPM	0b = PSKIP mode 1b = LPM mode
3	LDO1_LPM	0b = PSKIP mode 1b = LPM mode
2	LDO2_LPM	0b = PSKIP mode 1b = LPM mode

Table 55. B1_TIME_REG0

Address: 0x2C **Description:** Configure the turn-on delay time and sleep-off delay time of B1 rail.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B1_ON_DLY			B1_SLEEP_OFF_DLY		
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
5:3	B1_ON_DLY	B1 turns on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B1 will turn on with the setting delay time when PMIC is in the power up sequence and wake up sequence.
2:0	B1_SLEEP_OFF_DLY	B1 turns off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B1 will turn off with the setting delay time when PMIC is in the sleep off sequence.

Table 56. B1_TIME_REG1

Address: 0x2D
Description: Configure the wake-up delay time and the time slot of B1 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_WAKEUP_DELAY			B1_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	1	1	0	1

Bits	Name	Description
7:5	B1_WAKEUP_DELAY	B1 wake up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B1 will turn on with the wake up delay time when PMIC wake up from the sleep mode.
4:0	B1_TIME_SLOT	B1 time slot setting for power up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 57. B2_TIME_REG0

Address: 0x2E
Description: Configure the turn-on delay time and sleep-off delay time of B2 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B2_ON_DLY			B2_SLEEP_OFF_DLY		
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	B2_ON_DLY	B2 turns on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B2 will turn on with the setting delay time when PMIC is in the power up sequence and wake up sequence.
2:0	B2_SLEEP_OFF_DLY	B2 turns off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B2 will turn off with the setting delay time when PMIC is in the sleep off sequence.

Table 58. B2_TIME_REG1

Address: 0x2F **Description:** Configure the wake-up delay time and the time slot of B2 rail.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_WAKEUP_DELAY			B2_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	1	1	1	0	0	0	0

Bits	**Name**	**Description**
7:5	B2_WAKEUP_DELAY	B2 wake up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B2 will turn on with the wake up delay time when PMIC wake up from the sleep mode.
4:0	B2_TIME_SLOT	B2 time slot setting for power up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 59. B3_TIME_REG0

Address: 0x30
Description: Configure the turn-on delay time and sleep-off delay time of B3 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B3_ON_DLY			B3_SLEEP_OFF_DLY		
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	B3_ON_DLY	B3 turns on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B3 will turn on with the setting delay time when PMIC is in the power up sequence and wake up sequence.
2:0	B3_SLEEP_OFF_DLY	B3 turns off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B3 will turn off with the setting delay time when PMIC is in the sleep off sequence.

Table 60. B3_TIME_REG1

Address: 0x31 **Description:** Configure the wake-up delay time and the time slot of B3 rail.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_WAKEUP_DELAY			B3_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	1	0	0

Bits	Name	Description
7:5	B3_WAKEUP_DELAY	B3 wake up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B3 will turn on with the wake up delay time when PMIC wake up from the sleep mode.
4:0	B3_TIME_SLOT	B3 time slot setting for power up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 61. B4_TIME_REG0

Address: 0x32
Description: Configure the turn-on delay time and sleep-off delay time of B4 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		B4_ON_DLY			B4_SLEEP_OFF_DLY		
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
5:3	B4_ON_DLY	B4 turns on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B4 will turn on with the setting delay time when PMIC is in the power up sequence and wake up sequence.
2:0	B4_SLEEP_OFF_DLY	B4 turns off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms B4 will turn off with the setting delay time when PMIC is in the sleep off sequence.

Table 62. B4_TIME_REG1

Address: 0x33 **Description:** Configure the wake-up delay time and the time slot of B4 rail.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B4_WAKEUP_DELAY			B4_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	1	1	0	0	0	0	1

Bits	Name	Description
7:5	B4_WAKEUP_DELAY	B4 wake up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms B4 will turn on with the wake up delay time when PMIC wake up from the sleep mode.
4:0	B4_TIME_SLOT	B4 time slot setting for power up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 63. MANUFACTURE_ID_REG

Address: 0x34
Description: Show the Manufacturer ID.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MANUFACTURER_ID				EFUSE_VERSION_NUM			
Read/Write	R	R	R	R	R	R	R	R
Default Value	--	--	--	--	--	--	--	--

Bits	Name	Description
7:4	MANUFACTURER_ID	Manufacturer ID number.
3:0	EFUSE_VERSION_NUM	EFUSE revision number. [3:0] = EFUSE code version number (EFUSE number)

Table 64. LDO1_TIME_REG0

Address: 0x35
Description: Configure the turn-on delay time and sleep-off delay time of LDO1 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		LDO1_ON_DLY			LDO1_SLEEP_OFF_DLY		
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	LDO1_ON_DLY	LDO1 turns on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO1 will turn on with the setting delay time when PMIC is in the power up sequence and wake up sequence.
2:0	LDO1_SLEEP_OFF_DLY	LDO1 turns off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO1 will turn off with the setting delay time when PMIC is in the sleep off sequence.

Table 65. LDO1_TIME_REG1

Address: 0x36
Description: Configure the wake-up delay time and the time slot of LDO1 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO1_WAKEUP_DELAY			LDO1_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	1

Bits	**Name**	**Description**
7:5	LDO1_WAKEUP_DELAY	LDO1 wake up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms LDO1 will turn on with the wake up delay time when PMIC wake up from the sleep mode.
4:0	LDO1_TIME_SLOT	LDO1 time slot setting for power up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 66. LDO2_TIME_REG0

Address: 0x37 **Description:** Configure the turn-on delay time and sleep-off delay time of LDO2 rail.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved		LDO2_ON_DLY			LDO2_SLEEP_OFF_DLY		
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
5:3	LDO2_ON_DLY	LDO2 turns on delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO2 will turn on with the setting delay time when PMIC is in the power up sequence and wake up sequence.
2:0	LDO2_SLEEP_OFF_DLY	LDO2 turns off delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8.0ms LDO2 will turn off with the setting delay time when PMIC is in the sleep off sequence.

Table 67. LDO2_TIME_REG1

Address: 0x38
Description: Configure the wake-up delay time and the time slot of LDO2 rail.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDO2_WAKEUP_DELAY			LDO2_TIME_SLOT				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	1

Bits	Name	Description
7:5	LDO2_WAKEUP_DELAY	LDO2 wake up delay time. 000b = 0ms 001b = 0.25ms 010b = 0.50ms 011b = 0.75ms 100b = 1.0ms 101b = 2.0ms 110b = 4.0ms 111b = 8ms LDO2 will turn on with the wake up delay time when PMIC wake up from the sleep mode.
4:0	LDO2_TIME_SLOT	LDO2 time slot setting for power up. 0x00 = disabled 0x01 = Time Slot1 (0μs) 0x02 = Time Slot2 (250μs) 0x03 = Time Slot3 (500μs) … 0x1E = Time Slot30 (7250μs) 0x1F = Time Slot31 (7500μs)

Table 68. PWRDIS_REG

Address: 0x39 Description: Configure the delay time of the PWRDIS signal.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved					PWRDIS_DELAY_TIME		
Read/Write	R	R	R	R	R	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	Name	Description
2:0	PWRDIS_DELAY_TIME	PMIC will enter power-off sequence with the delay time after the low-level detected PWRDIS signal. 000b = 0ms 001b = 0.5ms 010b = 1.0ms 011b = 2.0ms 100b = 4.0ms 101b = 8.0ms 110b = 16ms 111b = disable PWRDIS function

Table 69. PRODUCT_ID_REG

Address: 0x3A Description: Show the PRODUCT_ID.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRODUCT_ID							
Read/Write	R	R	R	R	R	R	R	R
Default Value	--	--	--	--	--	--	--	--

Bits	Name	Description
7:0	PRODUCT_ID	Product ID number.

Table 70. REVISION_NUMBER_REG

Address: 0x3B **Description:** Show the REVISION_NUMBER.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ALL LAYER NUMBER				METAL NUMBER			
Read/Write	R	R	R	R	R	R	R	R
Default Value	--	--	--	--	--	--	--	--

Bits	Name	Description
7:4	ALL LAYER NUMBER	Record the all layer change times. 0xA = 1 time 0xB = 2 times 0xC = 3 times … 0xF = 6 times 7 times will be back to 0xA.
3:0	METAL NUMBER	Record the metal change times for the all layer change. 0x1 = 1 time 0x2 = 2 times 0x3 = 3 times …. 0xF = 15 times 16 times will be back to 0x0.

Table 71. TOP_CTRL_REG

Address: 0x3C **Description:** TOP circuit: PUSHPULL_EN, SYSMON_EN, SYSWARN_EN and VOUTLOW_MASK setting. (Read/write available only when the PMIC enters hidden mode)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PUSHPULL_EN	SYSMON_EN	SYSWARN_EN	VOUTLOW_MASK	Reserved			
Read/Write	RW	RW	RW	RW	R	R	R	R
Default Value	0	1	1	1	--	--	--	--

Bits	Name	Description
7	PUSHPULL_EN	0b = Disable. The I/Os will become open drain. 1b = Enable
6	SYSMON_EN	0b = Disable 1b = Enable
5	SYSWARN_EN	0b = Disable 1b = Enable
4	VOUTLOW_MASK	0b = Disable 1b = Enable It will not check low VOUT, if VOUTLOW_MASK = 1b.

Table 72. B3_REAL_VID_REG

Address: 0x3D
Description: Buck3 real VID selection.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_REAL_VID							Reserved
Read/Write	R	R	R	R	R	R	R	R
Default Value	--	--	--	--	--	--	--	--

Bits	**Name**	**Description**
7:1	B3_REAL_VID	Supply B3 Voltage: 0000000b = 0.5V 0000001b = 0.51V 0000010b = 0.52V 0000011b = 0.53V … … 1001111b = 1.29V 1010001b ~ 1111111b = 1.30V

Table 73. RELOAD_EFUSE_REG

Address: 0x3E
Description: Re-load EUFSE Value into all registers. (Read/write available only when the PMIC enters hidden mode)

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved							RELOAD_EFUSE
Read/Write	R	R	R	R	R	R	R	RW
Default Value	--	--	--	--	--	--	--	0

Bits	**Name**	**Description**
0	RELOAD_EFUSE	Set 1b to re-load all EFUSE values into all registers.

Table 74. MODE_FLAG_REG

Address: 0xF0
Description: The state of hidden mode.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	--	MODE_FLAG	Reserved					
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

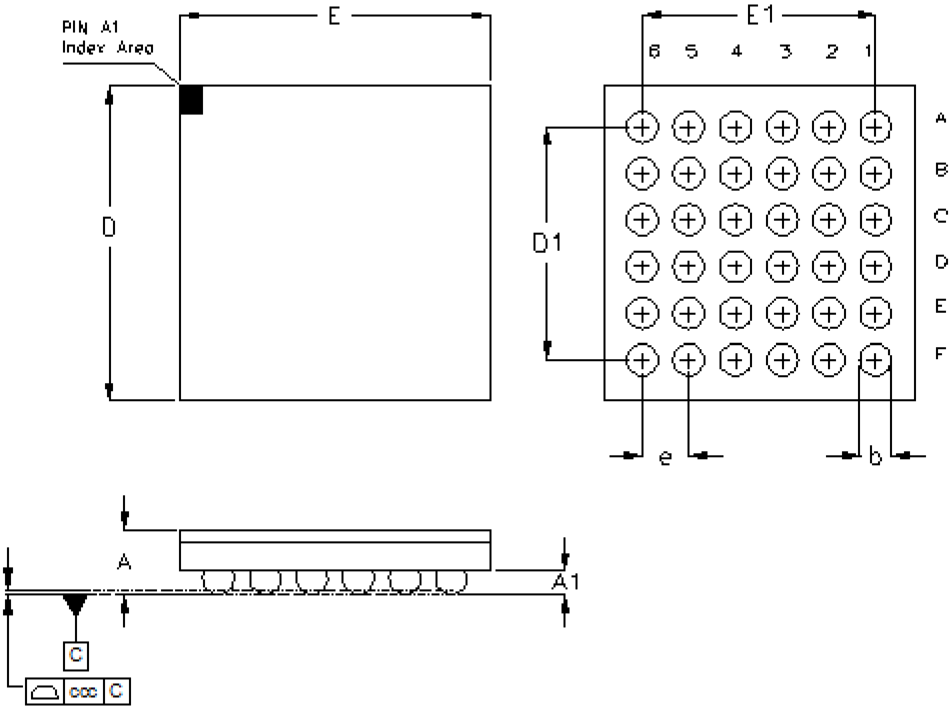
Bits	**Name**	**Description**
6	HIDDEN_MODE	Indicates HIDDEN_MODE. (Read = 1) After writing the password of the hidden mode, 0xF0[6] = 1.

Table 75. PASSWORD_REG

Address: 0xF1 **Description:** Selection of hidden mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PASSWORD							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Default Value	0	0	0	0	0	0	0	0

Bits	**Name**	**Description**
7:0	PASSWORD	1st: 0x24, 2nd: 0x54 = hidden mode First write 0x24 and then 0x54 to enter the hidden mode.

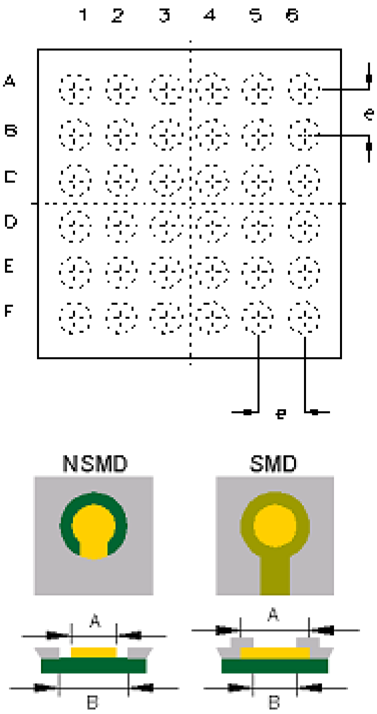
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.660	2.740	0.105	0.108
D1	2.000		0.079	
E	2.620	2.700	0.103	0.106
E1	2.000		0.079	
e	0.400		0.016	
ccc	0.020		0.001	

36B WL-CSP 2.66x2.70 Package (BSC)

Footprint Information



<table>
<tr><td rowspan="2">Package</td><td rowspan="2">Number of Pin</td><td rowspan="2">Type</td><td colspan="3">Footprint Dimension (mm)</td><td rowspan="2">Tolerance</td></tr>
<tr><td>e</td><td>A</td><td>B</td></tr>
<tr><td rowspan="2">WL-CSP2.66x2.70-36(BSC)</td><td rowspan="2">36</td><td>NSMD</td><td rowspan="2">0.400</td><td>0.240</td><td>0.340</td><td rowspan="2">±0.025</td></tr>
<tr><td>SMD</td><td>0.270</td><td>0.240</td></tr>
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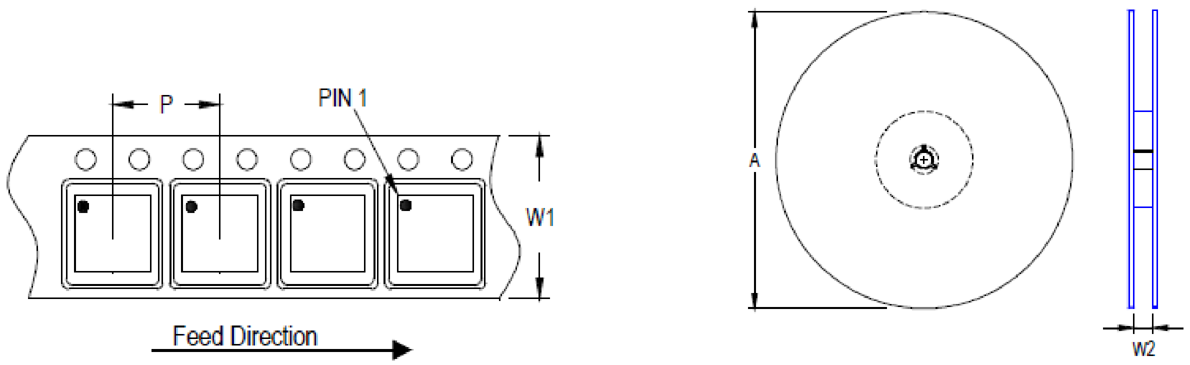
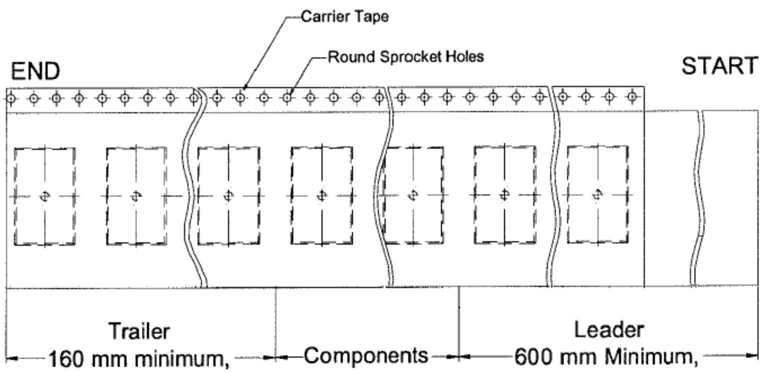
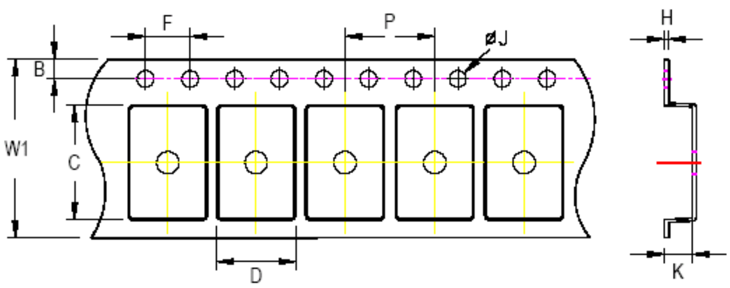
Packing Information

Tape and Reel Data





Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.66x2.70	8	4	180	7	3,000	160	600	8.4/9.9



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 2.66x2.70	7”	3,000	Box A	18.3*18.3*8.0	0.1	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	0.03	1	3,000	For Combined or Partial Reel			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/4/6	Final	
01	2023/8/23	Modify	General Description Features Marking Information Ordering Information Simplified Application Circuit Functional Pin Description Functional Block Diagram Absolute Maximum Ratings Electrical Characteristics Operation Application Information Functional Register Table