High Efficiency Single Synchronous DC-DC Step-Down Controller with 5V LDO

General Description

RT6575K is a single-channel step-down controller generating supply voltage for battery-powered systems. It includes a Pulse-Width Modulation (PWM) controller adjustable from 2V to 5.5V, and a fixed 5V linear regulator. The linear regulator provides up to 100mA output current. Other features include on-board power-up sequencing, a power-good output, internal soft-start, and soft-discharge output that prevents negative voltage during shutdown.

A constant current ripple PWM control scheme operates without sense resistors and provides 100ns response to load transient. For maximizing power efficiency, the RT6575K automatically switches to the diode-emulation mode in light load applications. The RT6575K is available in the VQFN-16L 3x3 package.

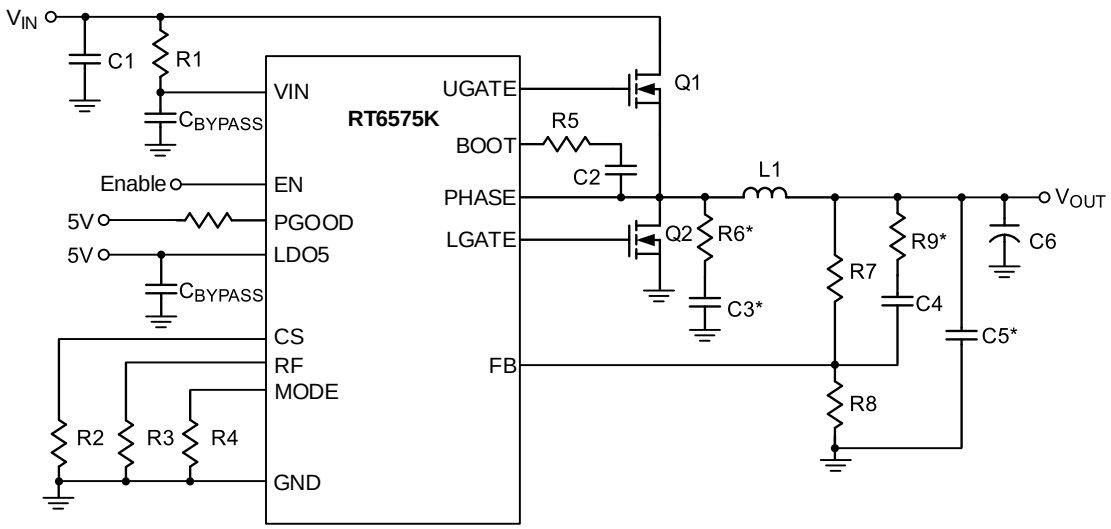
Features

- **CCRCOT Control with 100ns Load Step Response**
- **PWM Maximum Duty Ratio > 98%**
- **5V to 25V Input Voltage Range**
- **2V to 5.5V Output Voltage Range**
- **5V LDO with 100mA Output Current**
- **Two Selectable Frequency Settings**
- **Internal Soft-Start and Soft-Discharge**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing**
- **Independent Switcher Enable Control**
- **Built-in OVP/UVP/OCP/OTP**
- **Non-Latch UVLO**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook and Sub-Notebook Computers
- System Power Supplies

Simplified Application Circuit



* : is reserved for option

Ordering Information

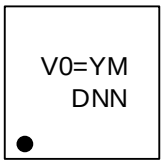
RT6575K □□□

- Pin 1 Orientation
  (2): Quadrant 2, Follow EIA-481-D
  (Empty means Pin1 orientation is Quadrant 1)
- Package Type
  QV : VQFN-16L 3x3 (V-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

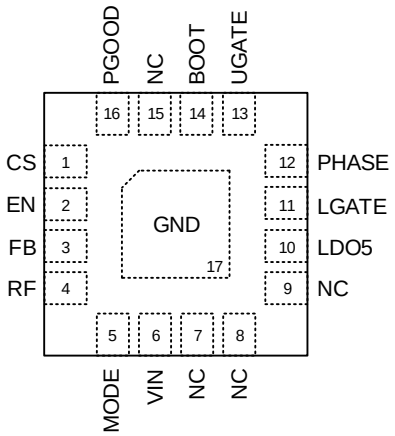
Marking Information



V0=: Product Code
YMDNN: Date Code

Pin Configuration

(TOP VIEW)



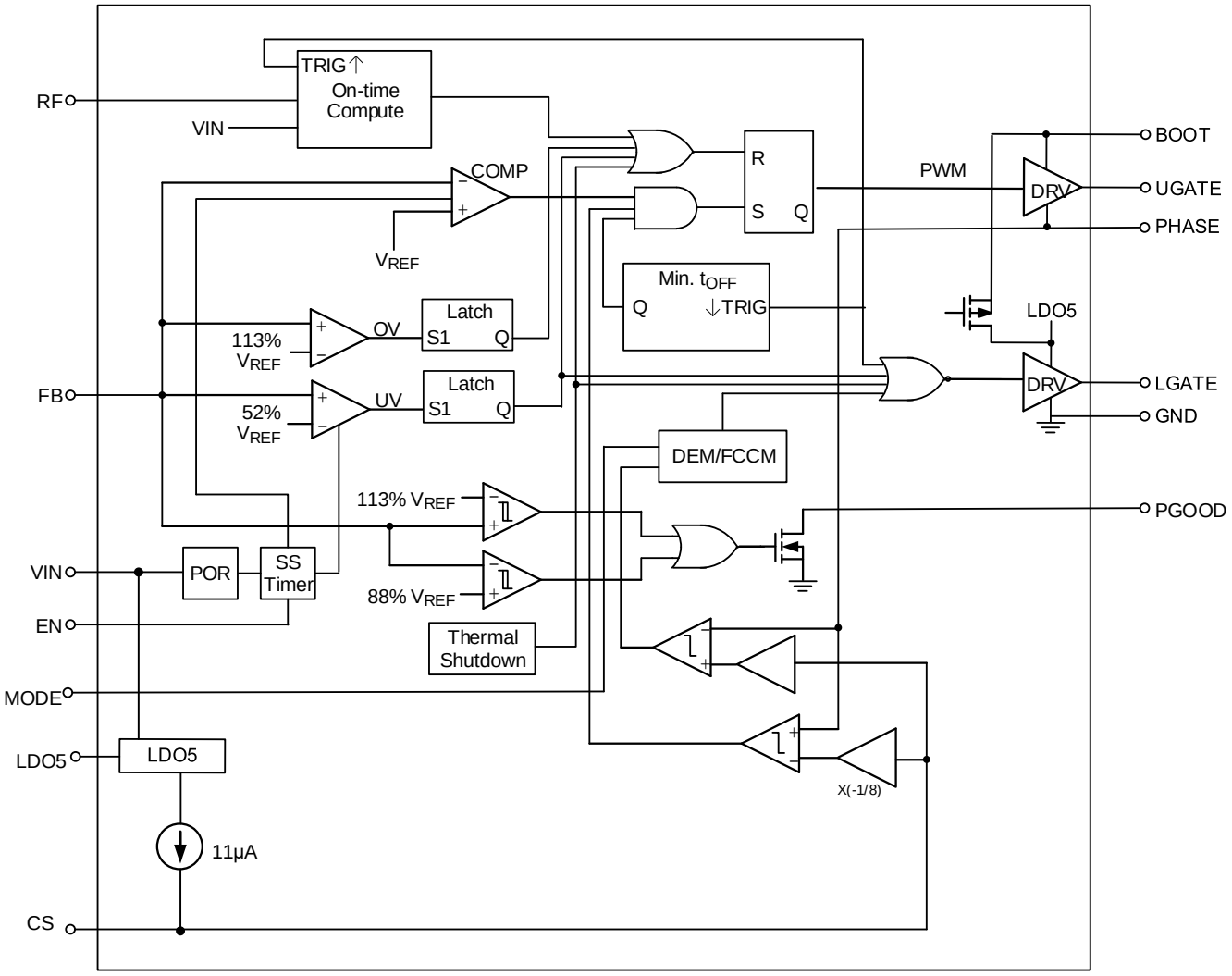
VQFN-16L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	CS	Current-limit setting. Connect a resistor to GND to set the threshold for synchronous $R_{DS(ON)}$ sense. The GND − Phase current-limit threshold is 1/8 the voltage seen at CS over a 0.2V to 2V range. There is an internal 11μA current source from LDO5 to CS.
2	EN	Enable control input. Pull low to GND to disable the PWM.
3	FB	VOUT feedback voltage input. Connect FB to a resistive voltage divider from VOUT to GND to adjust output from 2V to 5.5V.
4	RF	Switching frequency selection. Connect a resistor to select switching frequency as shown in Electrical Characteristics section. Pull down to GND with 620kΩ resistor: Switching frequency = 400kHz. Connect to 5V with 620kΩ resistor: Switching frequency = 500kHz.
5	MODE	DEM/FCCM selection. Pull down to GND with resistor: Diode Emulation Mode. Connect to PGOOD with resistor: forced CCM after PGOOD becomes high.
6	VIN	Power input for the 5V LDO regulator and buck controller.
7, 8, 9, 15	NC	No connection.
10	LDO5	5V linear regulator output. LDO5 is also the supply voltage for the low-side MOSFET and analog supply voltage for the device.
11	LGATE	Gate driver output for low side external MOSFET.
12	PHASE	External inductor connection pin for PWM converter. It behaves as the current sense comparator input for low-side MOSFET $R_{DS(ON)}$ sensing and reference voltage for on-time generation.
13	UGATE	Gate drive output for high-side external MOSFET.

Pin No.	Pin Name	Pin Function
14	BOOT	Bootstrap supply for high-side gate driver. Connect through a capacitor to the floating node (PHASE).
16	PGOOD	Open-drain power good indicator. High impedance indicates power is good.
17 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- −0.3V to 30V
- BOOT to GND
  - DC ---------- −0.3V to 36V
  - <100ns ---------- −5V to 42V
- BOOT to PHASE
  - DC ---------- −0.3V to 6V
  - <100ns ---------- −5V to 7.5V
- PHASE to GND
  - DC ---------- −5V to 30V
  - <100ns ---------- −10V to 42V
- UGATE to GND
  - DC ---------- −5V to 36V
  - <100ns ---------- −10V to 42V
- UGATE to PHASE
  - DC ---------- −0.3V to 6V
  - <100ns ---------- −5V to 7.5V
- LGATE to GND
  - DC ---------- −0.3V to 6V
  - <100ns ---------- −5V to 7.5V
- Other Pins ---------- −0.3V to 6.5V
- Power Dissipation, PD @ T_A = 25°C
  - VQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  - VQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  - VQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- −65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 5V to 25V
- Junction Temperature Range ---------- −40°C to 125°C
- Ambient Temperature Range ---------- −40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{EN}= 3.3V, V_{CS} = 2V, No Load, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Power-On Reset	V_{INPOR}	Rising threshold	--	4.6	4.9	V
		Falling threshold	3.2	3.7	--	
VIN Shutdown Current	I_{SHDN}	RT6575K buck controller off, V_{EN} = GND	--	30	40	μA
VIN Quiescent Current	I_{VIN_nosw}	Buck controller on, V_{FB} = 2.05V	--	250	400	μA
Buck Controllers Output and FB Voltage						
FB Valley Trip Voltage	V_{FB}	CCM operation	1.98	2	2.02	V
PHASE Discharge Current	I_{DCHG_LX}	V_{PHASE} = 0.5V	5	8	--	mA
Switching Frequency						
Switching Frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 5V, V_{RF} = 5V FCCM, I_{OUT} = 0A	400	500	600	kHz
Minimum Off-Time	$t_{OFF(MIN)}$	V_{FB} = 1.9V	--	200	275	ns
Soft-Start						
Soft-Start Time	t_{SS}	V_{OUT} ramp-up time	--	1.4	--	ms
Current Sense						
CS Source Current	I_{CS}	V_{CS} = 1V, V_{FB} = 1.9V	9.9	11	12.1	μA
CS Current Temperature Coefficient	TC_{ICS}	In comparison with 25°C	--	4700	--	ppm/°C
Zero-Current Threshold	V_{ZC}	V_{FB} = 2.05V, GND – PHASE	--	1	--	mV
Internal Regulator						
LDO5 Output Voltage	V_{LDO5}	V_{IN} = 12V, no load	4.9	5	5.1	V
		V_{IN} > 7V, I_{LDO5} < 100mA	4.8	5	5.1	
		V_{IN} > 5.5V, I_{LDO5} < 35mA	4.8	5	5.1	
		V_{IN} > 5V, I_{LDO5} < 20mA	4.5	4.75	5.1	
LDO5 Output Current	I_{LDO5}	V_{LDO5} = 4.5V, V_{IN} = 7.4V	100	175	--	mA
UVLO						
LDO5 UVLO Threshold	V_{UVLO5}	Rising edge	--	4.3	4.65	V
		Falling edge	3.7	3.9	4.1	
Power Good Indicator						
PGOOD Threshold	V_{PGxTH}	PGOOD Detect, V_{FBx} rising edge	85	90	95	%
		Hysteresis	--	8	--	
PGOOD Leakage Current		High state, V_{PGOOD} = 5.5V	--	--	1	μA
PGOOD Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
PGOOD Delay Time		From soft-start end to PGOOD high	--	0.92	--	ms

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Fault Detection							
OVP Trip Threshold		V_{OVP}	FB with respect to internal reference	109	113	117	%
OVP Propagation Delay				--	1	--	μs
UVP Trip Threshold		V_{UVP}	UVP detect, FB falling edge	47	52	57	%
UVP Shutdown Blanking Time		t_{SHDN_UVP}	From EN enable	--	2.6	--	ms
Thermal Shutdown							
Thermal Shutdown		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	10	--	°C
Logic Inputs							
EN Threshold Voltage	Logic-High	V_{EN_H}	SMPS on	1.6	--	--	V
	Logic-Low	V_{EN_L}	SMPS off	--	--	0.4	
MODE Threshold Voltage	Logic-High	V_{MODE_H}	FCCM operation	1.6	--	--	V
	Logic-Low	V_{MODE_L}	DEM operation	--	--	0.4	
RF Threshold Voltage	Logic-High	V_{RF_H}	500kHz	1.6	--	--	V
	Logic-Low	V_{RF_L}	400kHz	--	--	0.8	
Internal Boost Switch							
Internal Boost Switch On-Resistance		R_{BST}	LDO5 to BOOT	--	80	--	Ω
Power MOSFET Drivers							
UGATE On-Resistance		R_{UGATE}	High state, $V_{BOOT} - V_{UGATE}$ = 0.25V, $V_{BOOT} - V_{PHASE}$ = 5V	--	3	--	Ω
			Low state, $V_{UGATE} - V_{PAHSE}$ = 0.25V, $V_{BOOT} - V_{PHASE}$ = 5V	--	2	--	
LGATE On-Resistance		R_{LGATE}	High state, $V_{LDO5} - V_{LGATE}$ = 0.25V, V_{LDO5} = 5V	--	3	--	Ω
			Low state, V_{LGATE} – GND = 0.25V	--	1	--	
Dead-Time		t_D	LGATE rising	--	20	--	ns
			UGATE rising	--	30	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the case top of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

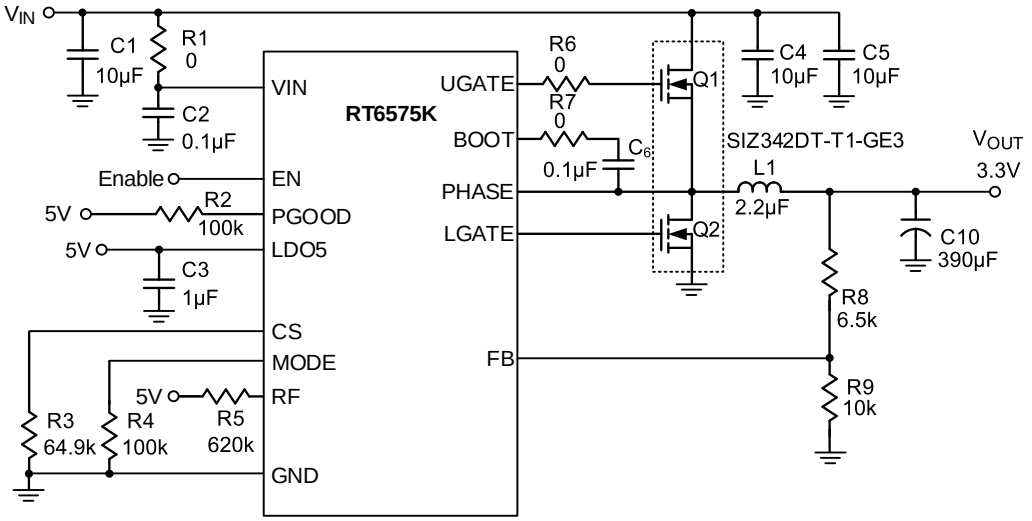


Figure 1. Typical Application Circuit for V_{OUT} = 3.3V

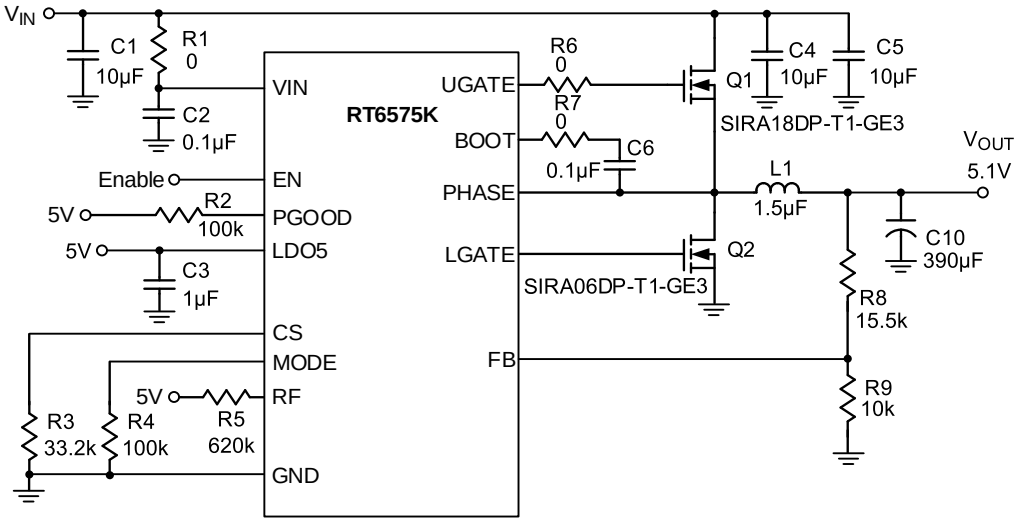


Figure 2. Typical Application Circuit for V_{OUT} = 5.1V

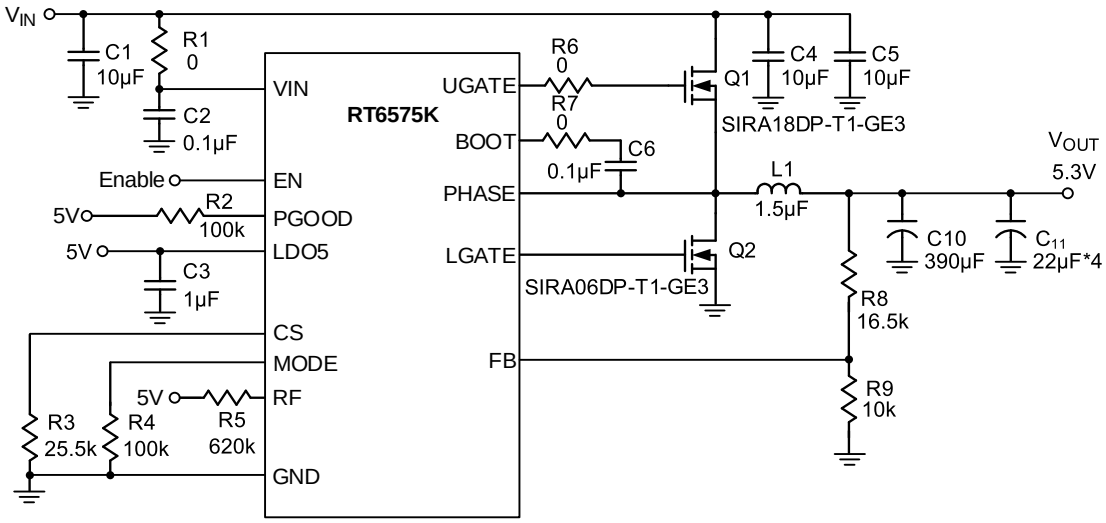
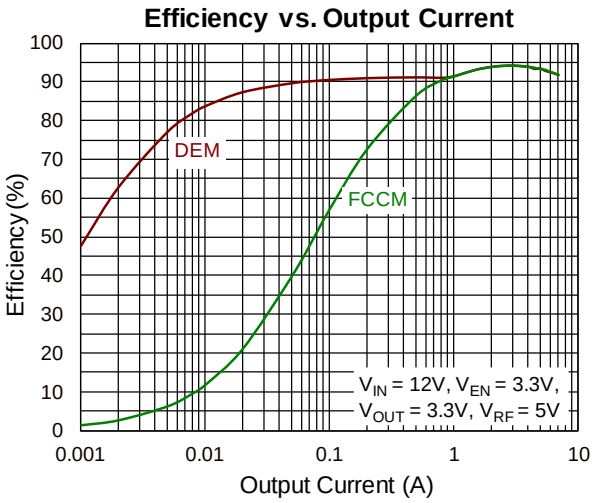
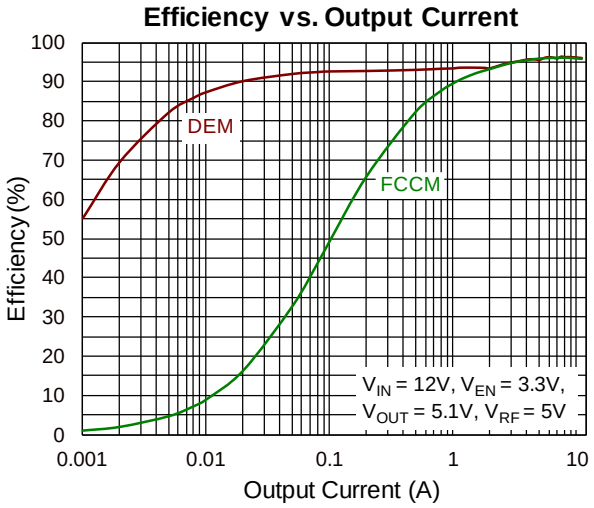
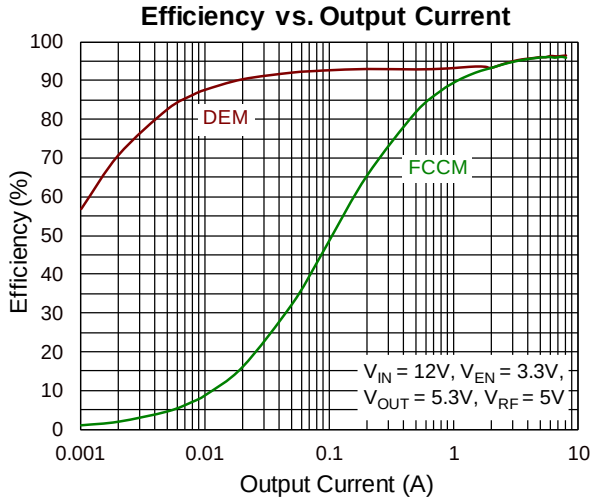


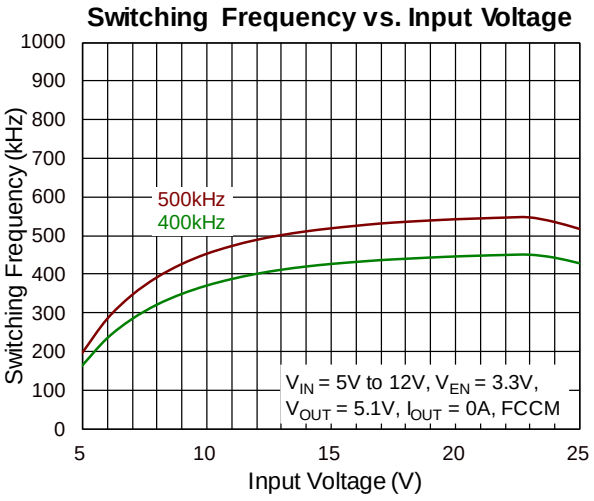
Figure 3. Typical Application Circuit for V_{OUT} = 5.3V

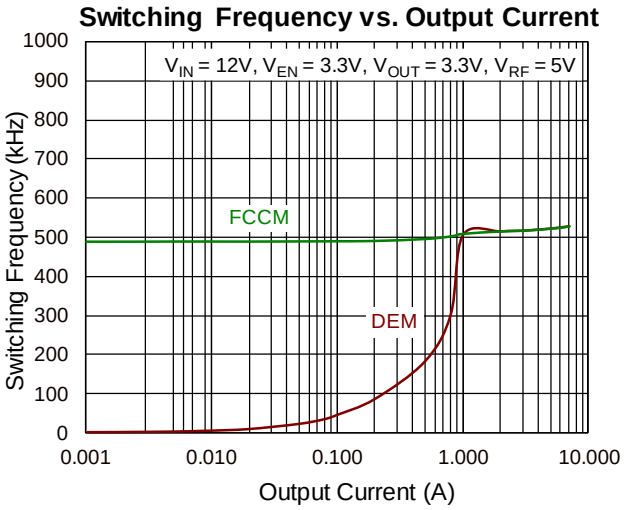
Typical Operating Characteristics

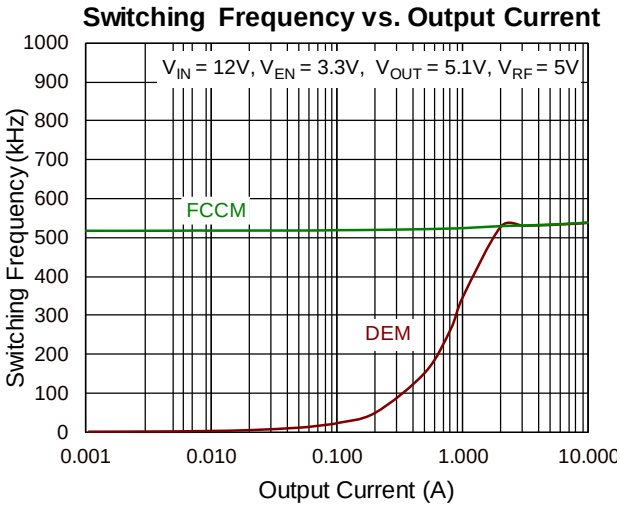


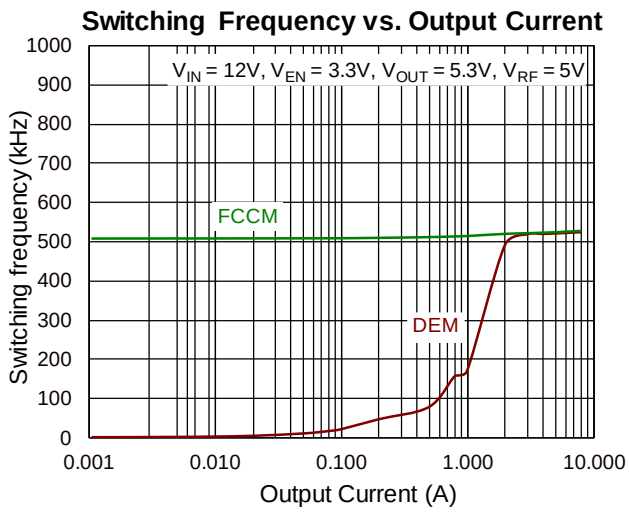


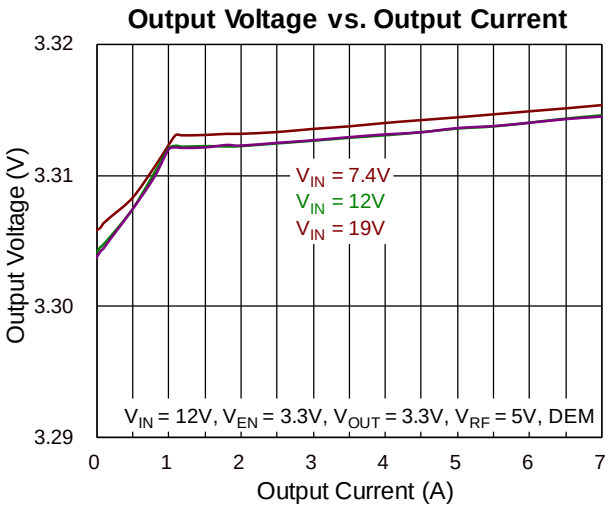


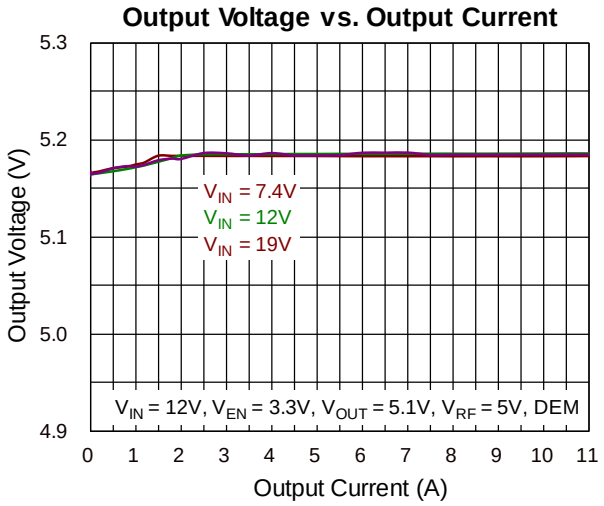


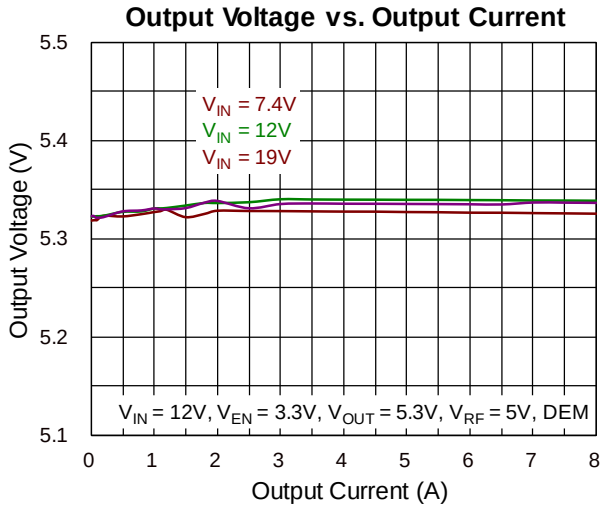


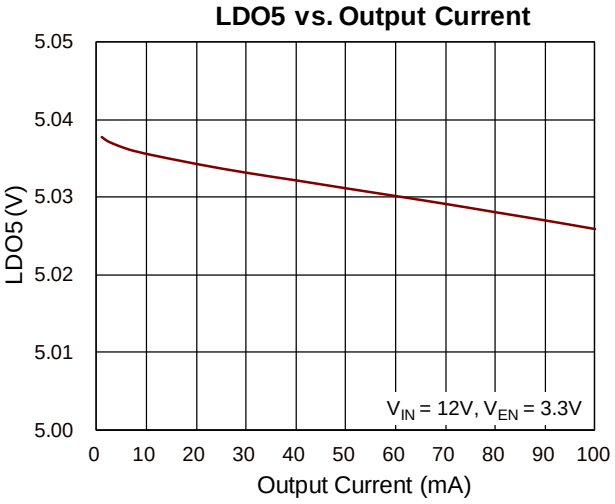


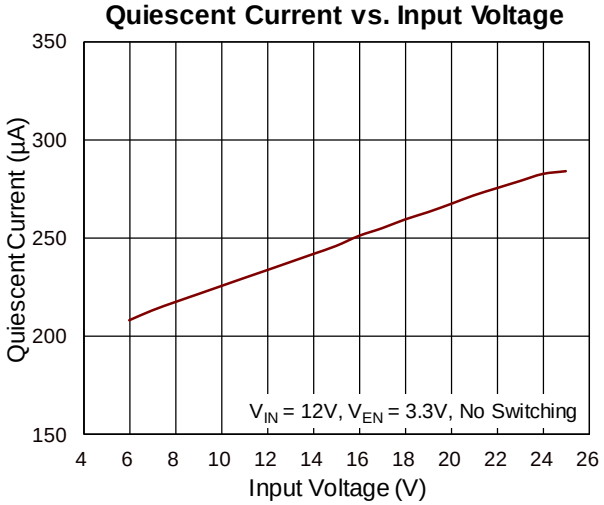




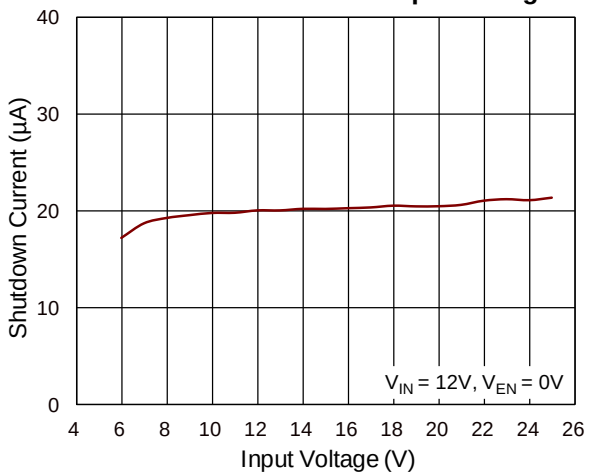




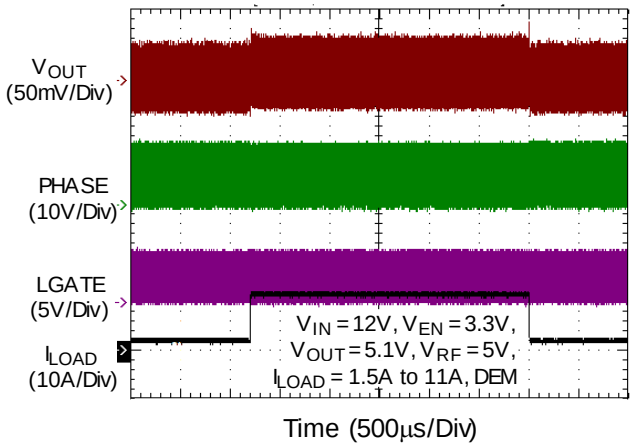




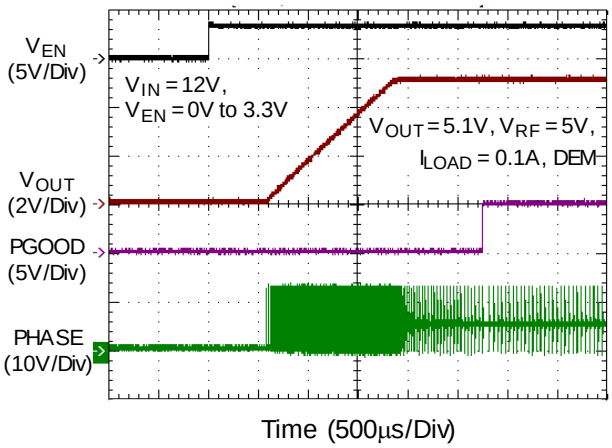
Shutdown Current vs. Input Voltage



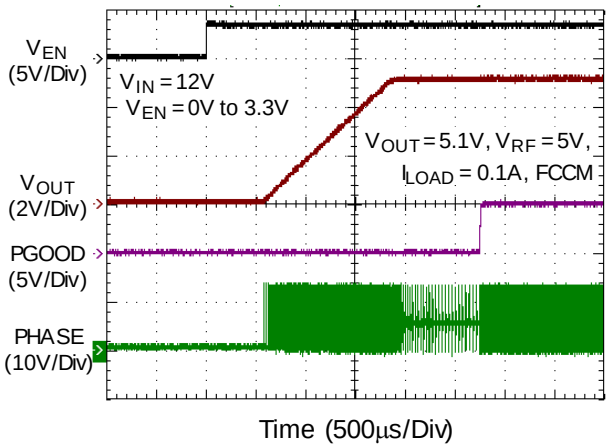
Load Transient Response



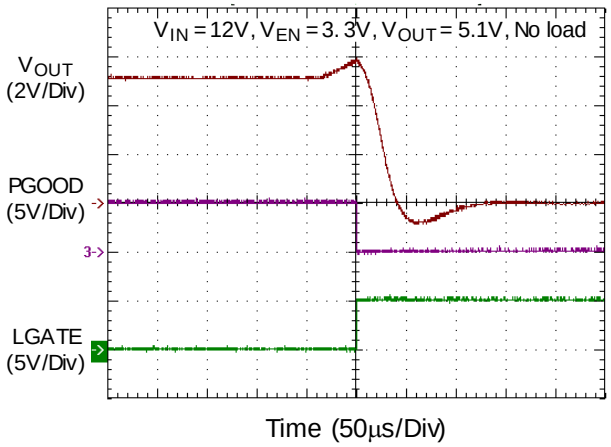
Power On from EN



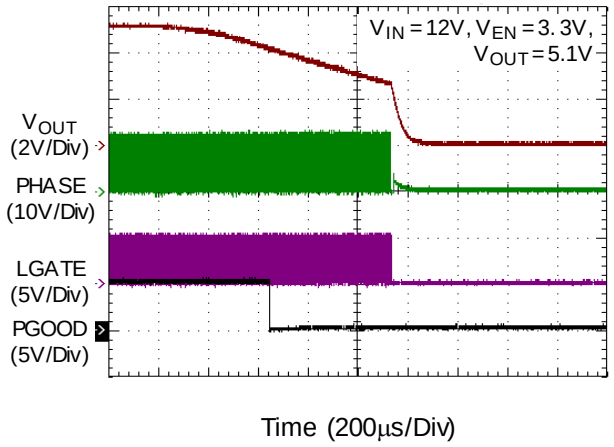
Power On from EN



Overvoltage Protection



Undervoltage Protection



Operation

The RT6575K includes a Constant Current Ripple Constant-On-Time synchronous step-down controller and one linear regulator.

Buck Controller

In normal operation, the high-side N-MOSFET is turned on when the output is lower than VREF, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Soft-Start

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

PGOOD

The power good output is an open-drain architecture. After soft-start is complete, the PGOOD open-drain output will be high impedance.

Current Limit

The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

Overvoltage Protection (OVP) & Undervoltage Protection (UVP)

The output voltage is continuously monitored for overvoltage and undervoltage conditions. When the output voltage exceeds overvoltage threshold (113% of VOUT), UGATE goes low and LGATE is forced high. When it is less than 52% of reference voltage, under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until EN is reset.

LDO5

When the VIN voltage exceeds the POR rising threshold, the LDO5 can be powered on by EN. The linear regulator LDO5 provides 5V regulated output.

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT6575K is a single-channel, low quiescent, Mach Response™ DRV™ mode synchronous Buck controller targeted for Ultrabook system power supply solutions. Richtek's Mach Response™ technology provides fast response to load steps. The topology solves the poor load transient response timing problems of fixed frequency current mode PWMs, and avoids the problems caused by widely varying switching frequencies in CCR (constant current ripple) constant on-time and constant off-time PWM schemes. The RT6575K includes a 5V (LDO5) linear regulator. The LDO5 linear regulator steps down the battery voltage to supply both internal circuitry and gate drivers. The synchronous switch gate drivers are directly powered by LDO5.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so that the output ripple voltage provides the PWM ramp signal. Referring to the RT6575K's Function Block Diagram, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one-shot is determined by the converter's input output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (200ns typ.). The on-time one-shot will be triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

PWM Frequency and On-time Control

For each specific input voltage range, the Mach Response™ control architecture runs with pseudo constant frequency by feed forwarding the input and output voltage into the on-time one-shot timer. The high-side switch on-time is inversely proportional to the input voltage as measured by VIN and proportional to the output voltage. The inductor ripple current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

The RT6575K adaptively changes the operation frequency according to the input voltage. Higher input voltage usually comes from an external adapter, so the RT6575K operates with higher frequency to have better performance. Lower input voltage usually comes from a battery, so the RT6575K operates with lower switching frequency for lower switching losses. For a specific input voltage range, the switching cycle period is given by:

For 5V VOUT,

$$\text{Period}\ (\text{sec.}) = \frac{V_{IN} \times 2.7 \times 10^{-6}}{V_{IN} - 3.79}$$

For 3.3V VOUT,

$$\text{Period}\ (\text{sec.}) = \frac{V_{IN} \times 2.45 \times 10^{-6}}{V_{IN} - 2.59}$$

where the VIN is in volt.

The on-time guaranteed in the Electrical Characteristics table is influenced by switching delays in the external high-side power MOSFET.

Diode Emulation Mode

In diode emulation mode, the RT6575K automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative

current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 4. and can be calculated as follows:

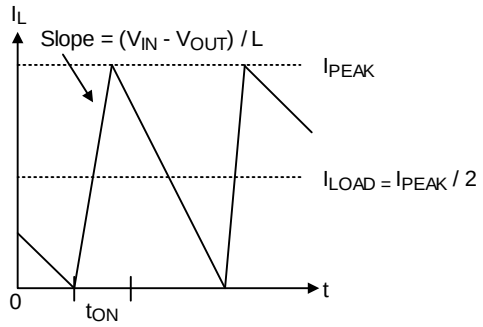


Figure 4. Boundary Condition of CCM/DEM

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation. But this is a normal operating condition that results in high light load efficiency. Trade-offs in DEM noise vs. light load efficiency is made by varying the inductor value. The disadvantages for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

Linear Regulators (LDO)

The RT6575K includes a 5V (LDO5) linear regulator. The regulators can supply up to 100mA for external loads. Bypass LDO with a 1μF to 4.7μF, and recommended value is 1μF ceramic capacitor.

Current Limit Setting

The RT6575K has cycle-by-cycle current limit control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 5). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, battery and output voltage.

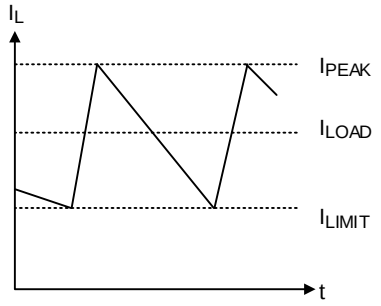


Figure 5. "Valley" Current Limit

The RT6575K uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The R_{LIMIT} resistor between the CS pin and GND sets the current-limit threshold. The resistor R_{LIMIT} is connected to a current source from CS which is 11μA (typ.) at room temperature. The current source has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across the sense resistor or low-side MOSFET equals 1/8 the voltage across the R_{LIMIT} resistor, positive current limit will be activated. The high-side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/8 the voltage across the R_{LIMIT} resistor.

Choose a current limit resistor according to the following equation:

$V_{LIMIT} = (R_{LIMIT} \times 11\mu A)/8 = I_{LIMIT} \times R_{DS(ON)}$

$R_{LIMIT} = ((I_{LIMIT} \times R_{DS(ON)}) \times 8)/11\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal at PHASE and GND. Mount or place the IC close to the low-side MOSFET.

MOSFET Gate Driver (UGATE, LGATE)

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the

LDO5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOT and PHASE pins. A dead-time to prevent shoot through is internally generated from high-side MOSFET off to low-side MOSFET on and low-side MOSFET off to high-side MOSFET on.

The low-side driver is designed to drive high current low $R_{DS(ON)}$ N-MOSFET(s). The internal pull-down transistor that drives LGATE low is robust, with a 1Ω typical on- resistance. A 5V bias voltage is delivered from the LDO5 supply. The instantaneous drive current is supplied by an input capacitor connected between LDO5 and GND.

For high current applications, some combinations of high and low-side MOSFETs may cause excessive gate drain coupling, which leads to efficiency killing, EMI producing, and shoot through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time. See Figure 6.

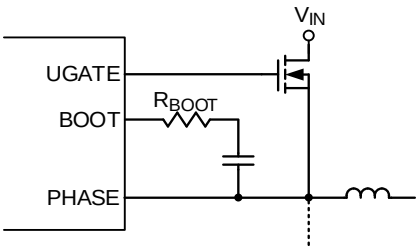


Figure 6. Increasing the UGATE Rise Time

Soft-Start

The RT6575K provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft- start, it clamps the ramping of internal reference voltage which is compared with FB signal. The typical soft-start duration is 1.4ms. A unique PWM duty limit control that prevents output overvoltage during soft-start period is designed specifically for FB floating.

UVLO Protection

The RT6575K has LDO5 undervoltage lock out protection (UVLO). When the LDO5 voltage is lower than 3.9V (typ.), the switch power supplies are shut off. This is a non- latch protection.

Power Good Output (PGOOD)

PGOOD is an open-drain output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. For RT6575K, PGOOD is released when both output voltages are above 88% of nominal regulation point. The PGOOD signal goes low if either output turns off or is 20% below or 13% over its nominal regulation point.

Output Overvoltage Protection (OVP)

The output voltage can be continuously monitored for over- voltage condition. If the output voltage exceeds 13% of its set voltage threshold, the overvoltage protection is triggered and the LGATE low-side gate drivers are forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor and pulls the output voltage downward.

The RT6575K is latched once OVP is triggered and can only be released by either toggling EN or cycling VIN. There is a 1μs delay built into the overvoltage protection circuit to prevent false transition.

Note that latching LGATE high will cause the output voltage to dip slightly negative due to previously stored energy in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the overvoltage condition is caused by a shorted in high-side switch, turning the low-side MOSFET on 100% will create an electrical shorted circuit between the battery and GND to blow the fuse and disconnecting the battery from the output.

Output Undervoltage Protection (UVP)

The output voltage can be continuously monitored for undervoltage condition. If the output is less than 52% (typ.) of its set voltage threshold, the undervoltage protection will be triggered and then both UGATE and LGATE gate drivers will be forced low. The UVP is

ignored for at least 2.2ms (typ.) after a start-up or a rising edge on EN. Toggle EN or cycle VIN to reset the UVP fault latch and restart the controller.

Thermal Protection

The RT6575K features thermal shutdown to prevent damage from excessive heat dissipation. Thermal shutdown occurs when the die temperature exceeds 150°C. All internal circuitries are turned off during thermal shutdown.

Discharge Mode (Soft Discharge)

When EN is low the output undervoltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

Power-Up Sequencing and On/Off Controls (EN)

EN control the power-up sequencing of the Buck converter. The 0.4V falling edge threshold on EN can be used to detect a specific analog voltage level and to shutdown the device. Once in shutdown, the 1.6V rising edge threshold activates, providing sufficient hysteresis for most applications.

Output Voltage Setting (FB)

Connect a resistive voltage divider at the FB pin between VOUT and GND to adjust the output voltage from 2V to 5.5V, as shown in Figure 7. The recommended R2 value is between 10kΩ to 20kΩ, and solve for R1 using the equation below:

$$V_{OUT(Valley)} = V_{FB} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FB} is 2V (typ.).

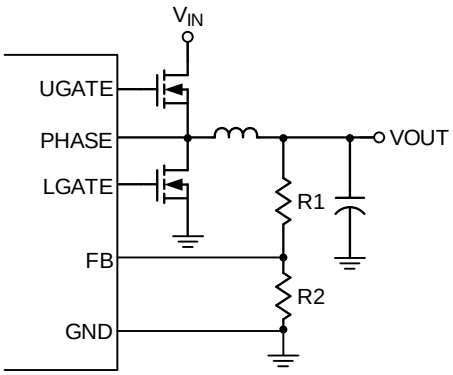


Figure 7. Setting VOUT with a resistive voltage divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below:

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current, I_{PEAK}:

$I_{PEAK} = I_{LOAD(MAX)} + [\ (LIR/2) \times I_{LOAD(MAX)}\ ]$

The calculation above shall serve as a general reference. To further improve transient response, the output inductance can be further reduced. Of course, besides the inductor, the output capacitor should also be considered when improving transient response.

Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from the equations below:

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \times \left[V_{IN} \times t_{ON} - V_{OUT}(t_{ON} + t_{OFF(MIN)})\right]}$$

$$V_{SOAR} = \frac{(\Delta I_{LOAD})^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f} \right)$$

where V_{SAG} and V_{SOAR} are the allowable amount of undershoot and overshoot voltage during load transient, V_{p-p} is the output ripple voltage, and $t_{OFF(MIN)}$ is the minimum off-time.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)}-T_{TA})/ \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For VQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at TA = 25°C can be calculated by the following formula:

PD(MAX) = (125°C - 25°C)/(30°C/W) = 3.33W for VQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 8Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

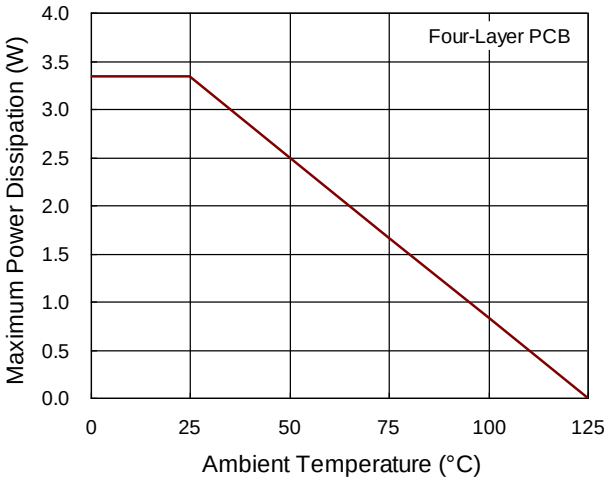


Figure 8. Derating Curve of Maximum Power Dissipation

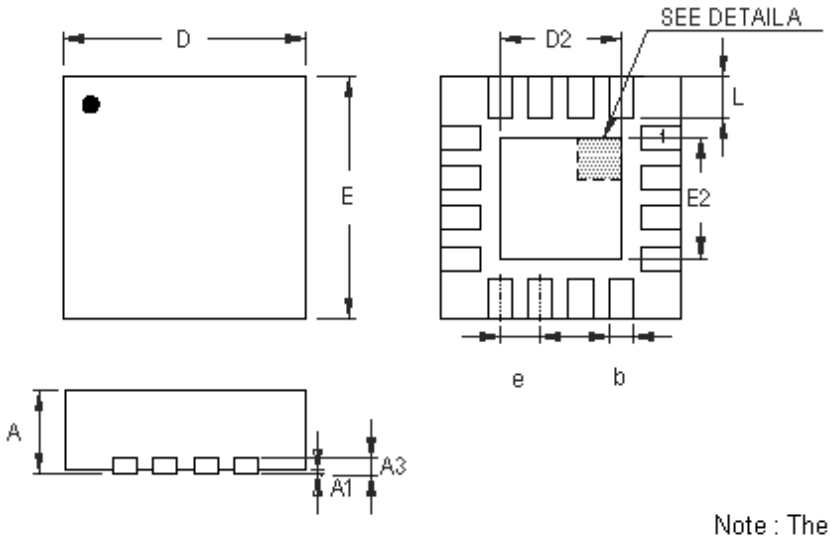
Layout Considerations

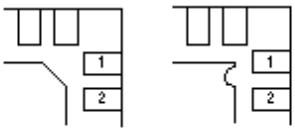
Layout is very important in high frequency switching converter design. Improper PCB layout can radiate excessive noise and contribute to the converter's instability. The following points must be considered before starting a layout with the RT6575K.

- Place the filter capacitor close to the IC, within 12mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25 mils) or wider trace.
- All sensitive analog traces and components such as FB, PGOOD, and should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.

- Place ground terminal of VIN capacitor(s), VOUT capacitor(s), and Source of low-side MOSFETs as close to each other as possible. The PCB trace of PHASE node, which connects to Source of high-side MOSFET, Drain of low-side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Outline Dimension





DETAIL A

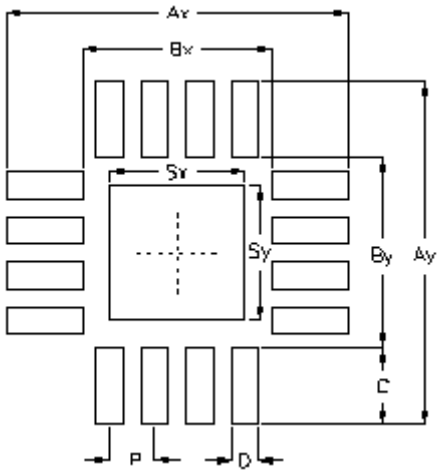
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 16L QFN 3x3 Package

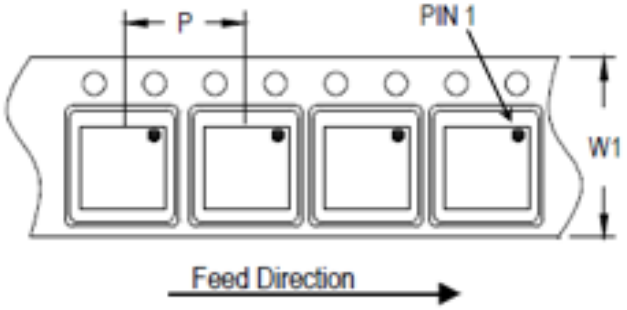
Footprint Information

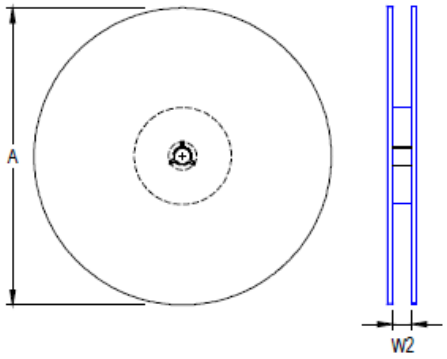


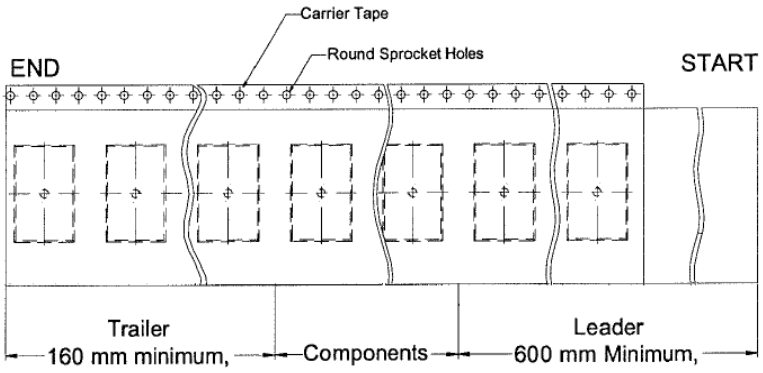
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-16	16	0.50	3.80	3.80	2.10	2.10	0.85	0.30	1.50	1.50	±0.05

Packing Information

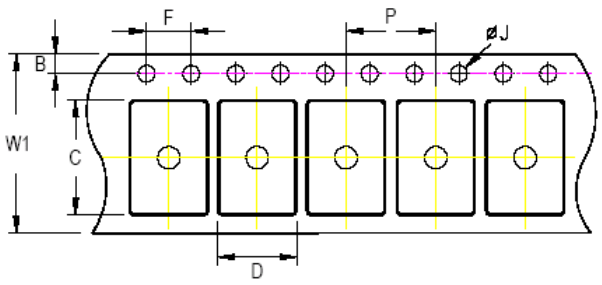
Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
00	2023/8/8	Final	