PMIC for TFT LCD TV Panels

General Description

The RT6908 provides a complete set of programmable multi-functional power solution for TFT LCD panel. The RT6908 contains a step-up converter for main power and step-down controllers to provide the logic voltages for the system. Moreover, a positive charge pump regulator provides the adjustable gate-high voltage, V_{GH}; a negative charge pump regulator provides the gate-low voltage, V_{GL}. AVDD, V_{GH} and V_{GL} outputs and power sequence can be programmable through I^2C interface.

With its high current capabilities, the device is ideal for large screen monitor panels and LCD TV applications with 12V supply voltage. The RT6908 is available in a WQFN-40L 5x5 package.

Ordering Information

RT6908 □□

Package Type
QW : WQFN-40L 5x5 (W-Type)

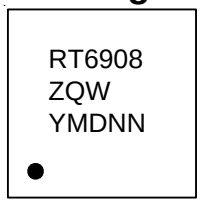
Lead Plating System
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT6908ZQW : Product Number

YMDNN : Date Code

Features

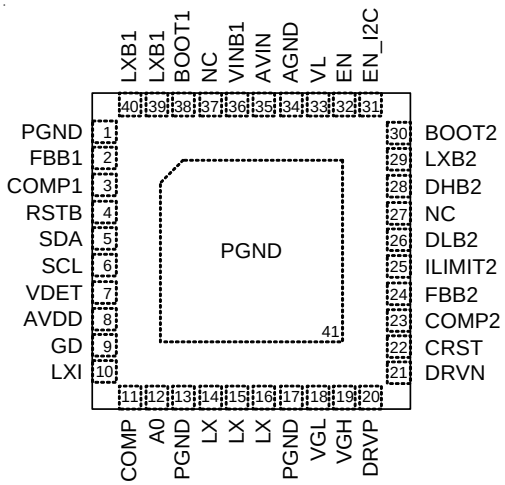
- **9V to 16V Input Supply Voltage**
- **4.4A Boost Regulator for AVDD with 12.7V to 19V Programmable Output**
- **1-CH Sync. Buck Converter for $V_{I/O}$**
- **1-CH Sync. Buck Controller for V_{CORE}**
- **Negative Charge Pump Regulator for VGL with –8.1V to –1.8V Programmable Output**
- **Positive Charge Pump Regulator for VGH with 24.5V to 40V Programmable Output**
- **Programmable Sequencing**
- **Voltage Detection Output**
- **Over Temperature Protection**
- **I^2C Compatible Interface for Register Control**
- **Thin 40-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- TFT LCD TV Panel

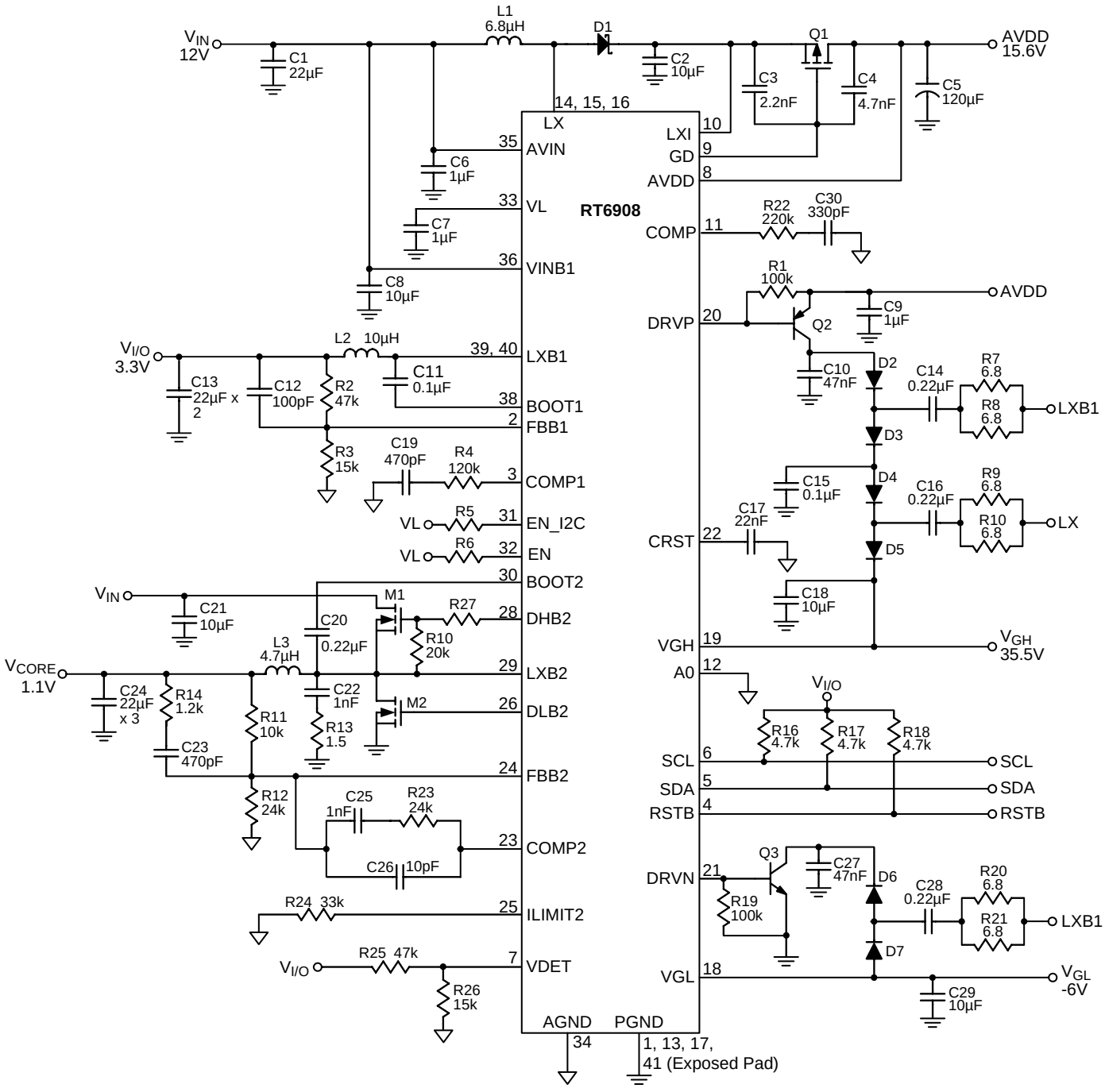
Pin Configurations

(TOP VIEW)



WQFN-40L 5x5

Typical Application Circuit



Timing Diagram

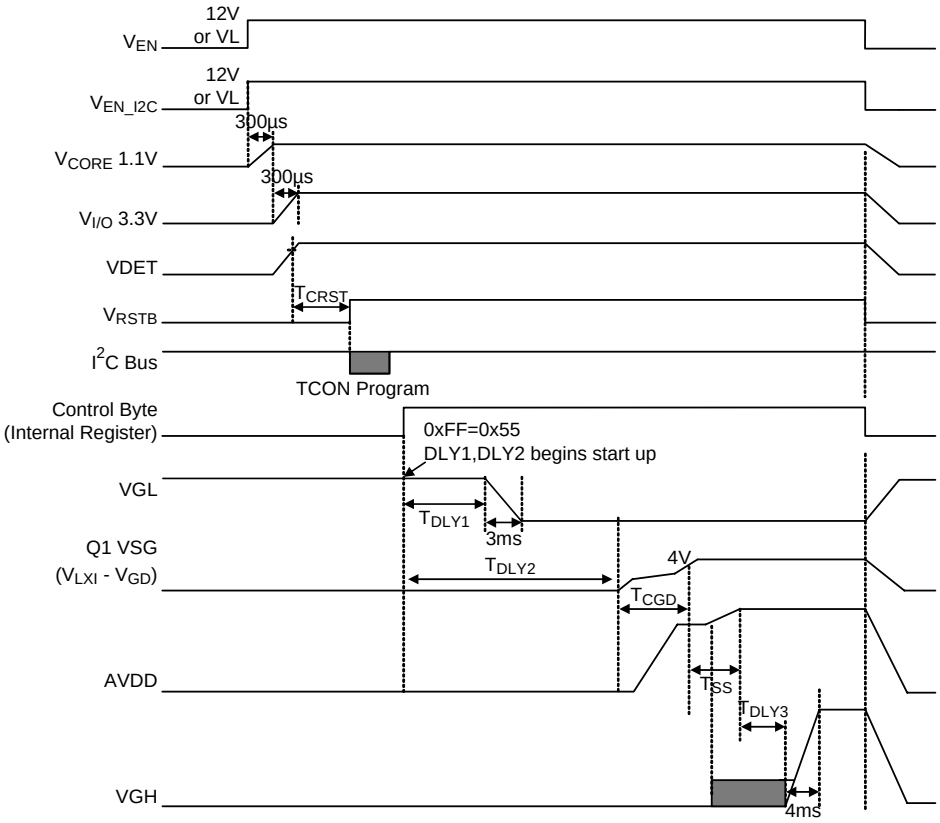


Figure 1. I^2C Mode Power Sequence (V_{EN_I2C} = 1)

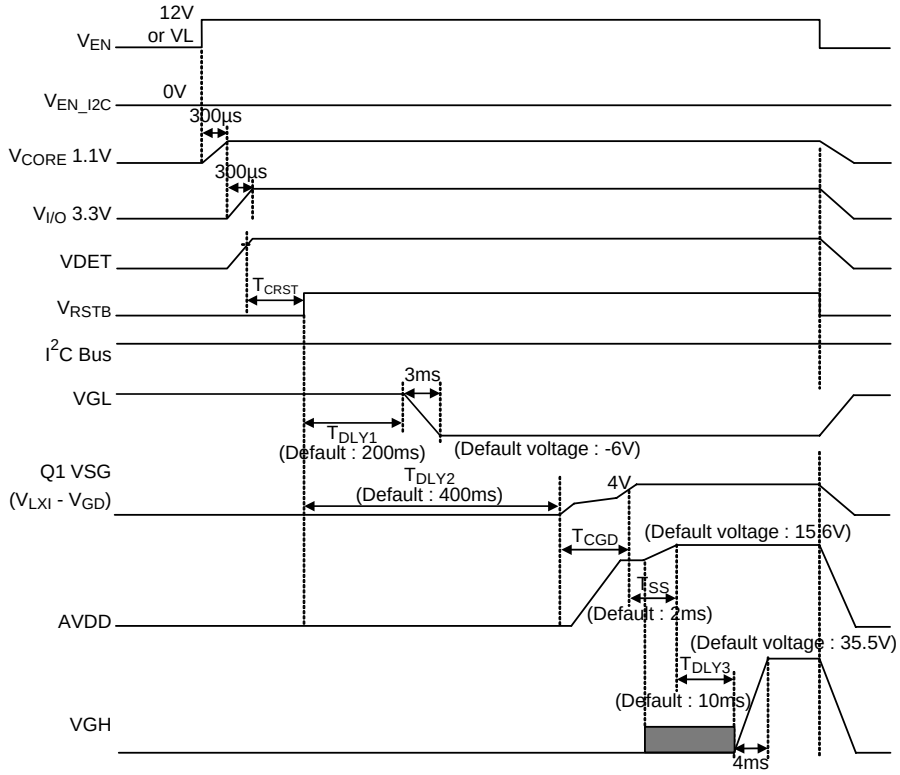


Figure 2. Default Mode Power Sequence (V_{EN_I2C} = 0)

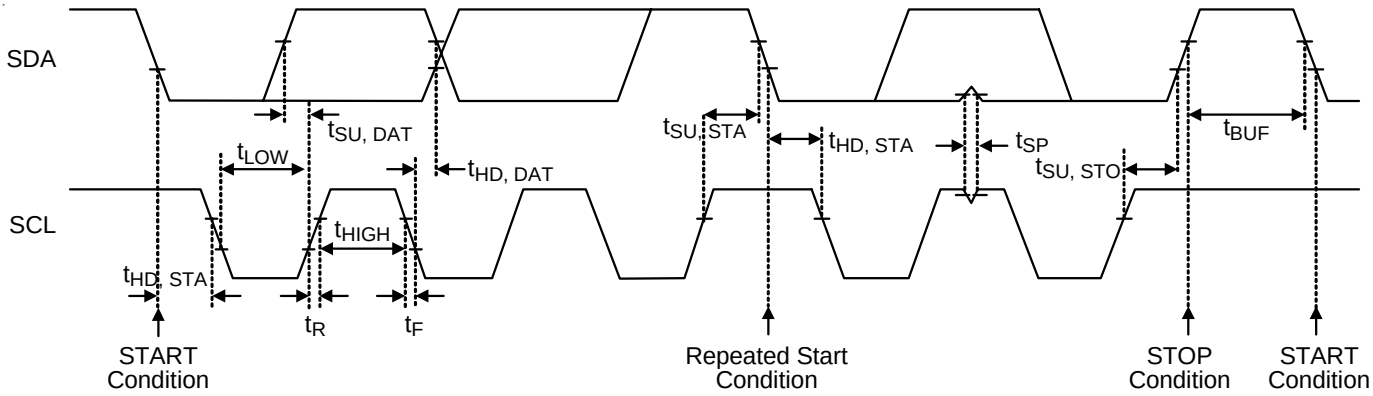


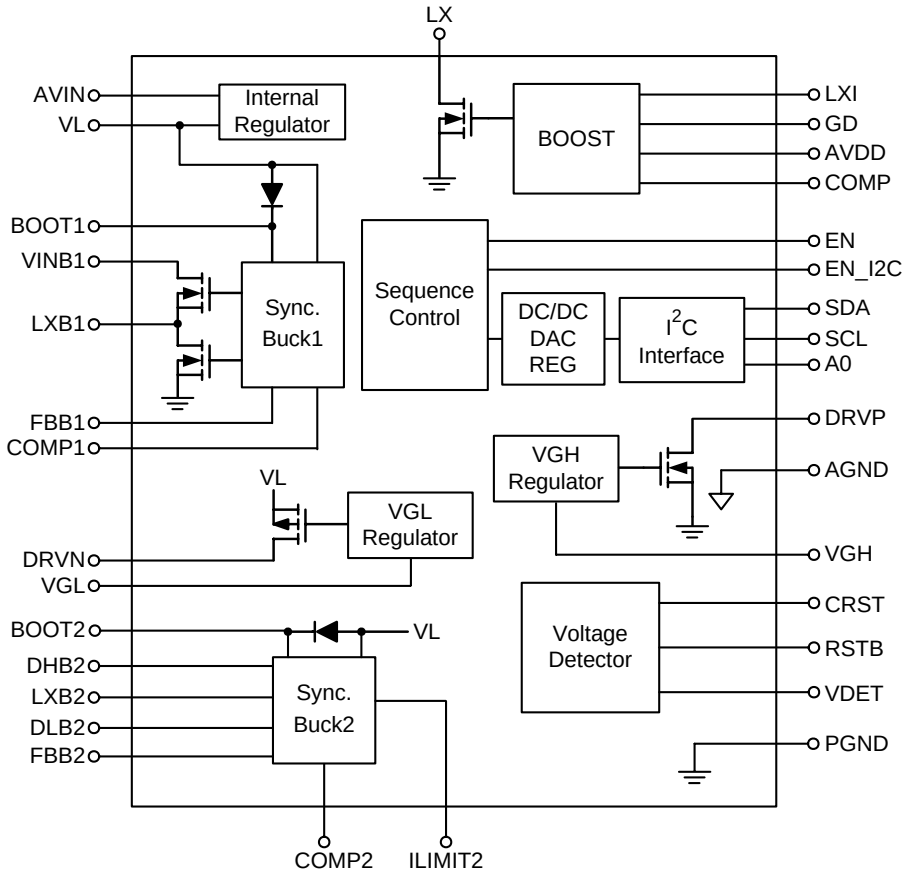
Figure 3. I²C Interface Timing Diagram

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 13, 17, 41(Exposed Pad)	PGND	Power Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum thermal dissipation.
2	FBB1	Feedback Input for Buck1 Converter.
3	COMP1	Compensation Pin for Buck1 Converter. This pin is the output node of the error amplifier.
4	RSTB	Voltage Detector Open-Drain Output.
5	SDA	I²C Compatible Serial Data Input/Output.
6	SCL	I²C Compatible Serial Clock Input.
7	VDET	Voltage Detector Input.
8	AVDD	Output Sense Pin for Boost Converter AVDD.
9	GD	Gate Drive. Used to control an external MOSFET switch to provide input to output isolation of AVDD.
10	LXI	Isolation Switch Input.
11	COMP	Boost Converter (AVDD) Compensation. Connect a compensation network to ground.
12	A0	I²C Compatible Device Address Bit 0.
14, 15, 16	LX	Boost Converter (AVDD) Switch. Connect an inductor between this pin and input voltage source.
18	VGL	Output Sensing Pin of VGL Negative Charge Pump.
19	VGH	Output Sensing Pin of VGH Positive Charge Pump.
20	DRVP	Base Drive of External PNP Transistor for VGH Positive Charge Pump.
21	DRVN	Base Drive of External NPN Transistor for VGL Negative Charge Pump.
22	CRST	Voltage Detector Delay Capacitor Connection. Connect capacitor from this pin to ground.
23	COMP2	Compensation Pin for Buck2 Converter.
24	FBB2	Feedback Input for Buck2 Converter.
25	ILIMIT2	Current Limit Adjustment for Buck2 Converter. Connect a resistor from ILIMIT2 to AGND to adjust the current limit threshold below 300mV.
26	DLB2	Low Side Gate Driver Output for Buck2 Converter.
27, 37	NC	Not Internal Connected. Should be floating or connected to GND

Pin No.	Pin Name	Pin Function
28	DHB2	High Side Gate Driver Output for Buck2 Converter.
29	LXB2	Buck2 Converter Switch node Between High Side MOSFET and Low Side MOSFET.
30	BOOT2	N-MOSFET Gate Drive Voltage for Buck2 Converter. Connect a capacitor from the switch node LXB2 to this pin.
31	EN_I2C	Enable for I^2C Control. AVDD, VGL, VGH enabled by I^2C Control.
32	EN	Chip Enable (Active High). Tie to VL to enable the device.
33	VL	Internal Logic Regulator Output. Connect this pin with a decoupling capacitor.
34	AGND	Analog Ground.
35	AVIN	Analog Input Voltage of the Device. This is the input for the analog circuits. Connect this pin with a decoupling capacitor.
36	VINB1	Power Input Voltage Pins for the $V_{I/O}$ Buck Converter.
38	BOOT1	N-MOSFET Gate Drive Voltage for Buck1. Connect a capacitor from the switch node LXB1 to this pin.
39	LXB1	Buck1 Switch node Between High Side MOSFET and Low Side MOSFET.
40	LXB1	Buck1 Switch node Between High Side MOSFET and Low Side MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- EN, EN_I2C, AVIN, VINB1, LXI, GD, AVDD, LX, LXB1, LXB2, BOOT1, BOOT2, DHB2, VDET to PGND ---------- –0.3 to 26V
- SDA, SCL, A0, RSTB, CRST, VL, COMP, COMP1, COMP2, FBB1, FBB2, ILIMIT2, DLB2, DRVN to PGND ---------- –0.3 to 6V
- BOOT1 to LXB1 ---------- –0.3 to 6V
- BOOT2, DHB2 to LXB2 ---------- –0.3 to 6V
- DRVP, VGH to PGND ---------- –0.3 to 44V
- VGL to PGND ---------- –26V to 26V
- PGND to AGND ---------- ±0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 36°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(Typical values V_{IN} = V_{AVIN} = V_{INB} = 12V, V_{AVDD} = 15.6V, $V_{I/O}$ = 3.3V, V_{CORE} = 1.1V, V_{GH} = 35.5V, V_{GL} = –6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Input Voltage Range	V_{IN}		9	--	16	V
AVIN Quiescent Current	I_{QIN}	LX, LXBx Not Switching	--	3.5	--	mA
Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	--	8.6	9	V
		V_{IN} Falling	7.2	7.6	--	
		V_{IN} Falling Latch Reset	--	5	--	
VL Output Voltage	V_L		--	5	--	V
Fault Detection						
Fault Trigger Duration			--	50	--	ms
Thermal Shutdown Threshold		Temperature Rising	--	150	--	°C
Thermal Shutdown Hysteresis			--	50	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Inputs (SDA, SCL, EN, EN_I2C)						
Input High Voltage	V_{IH}		1.7	--	--	V
Input Low Voltage	V_{IL}		--	--	0.6	V
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0 or 3.3V	–1	0.01	1	µA
Input Capacitance			--	5	--	pF
SDA Output Low Voltage	V_{OL}	I_{SINK} = 6mA	--	0.3	--	V
I^2C Timing Characteristics						
Serial-Clock Frequency	f_{SCL}		0	--	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3	--	--	µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6	--	--	µs
SCL Pulse-Width Low	t_{LOW}		1.3	--	--	µs
SCL Pulse-Width High	t_{HIGH}		0.6	--	--	µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6	--	--	µs
Data Hold Time	$t_{HD, DAT}$		0	--	800	ns
Data Setup Time	$t_{SU, DAT}$		100	--	--	ns
SDA and SCL Receiving Rise Time	t_R		20 + 0.1C_B	--	300	ns
SDA and SCL Receiving Fall Time	t_F		20 + 0.1C_B	--	300	ns
SDA Transmitting Fall Time	t_F		20 + 0.1C_B	--	250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6	--	--	µs
Bus Capacitance	C_B		--	--	400	pF
Pulse Width of Suppressed Spike	t_{SP}		--	--	50	ns
Reset Voltage Detector						
Minimum Operating Voltage		AVIN Minimum Voltage for RSTB	2.2	--	--	V
VDET Detecting Threshold	V_{TH}	VDET Falling	--	0.6	--	V
VDET Threshold Hysteresis	ΔV_{TH}		--	100	--	mV
RSTB Output Low Voltage	V_{OL}	I_{SINK} = 500µA	--	--	0.3	V
RSTB Leakage Current	I_{LEAK}	V_{RSTB} = 5.0V	--	0.01	0.1	µA
CRST Charge Current	I_{CRST}		--	8	--	µA
CRST Threshold	V_{CRST}		--	1.25	--	V
Boost Converter (AVDD)						
Adjustable Output Voltage Range	V_{AVDD}	Register Address = ”00h”, 6 bits, AVDD = (12.7V to 19V) [00h to 3Fh]	12.7	--	19	V
AVDD Regulation Voltage (Default)	V_{AVDD}	No load	15.444	15.6	15.756	V
Oscillator Frequency	f_{OSC}		600	750	900	kHz
Maximum Duty Cycle			--	90	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
N-MOSFET On-Resistance	$R_{DS(ON)}$	I_{LX} = 500mA	--	120	--	mΩ
N-MOSFET Switch Current Limit	I_{LIM}		4.4	5.6	--	A
Switch Leakage Current	I_{leak}	V_{LX} = 19V	--	1	10	μA
LXI Over Voltage Protection	V_{OVP}	V_{LX} Rising, Hysteresis = 1V	19.5	20	--	V
AVDD Line Regulation		9V ≤ V_{IN} ≤ 16V, I_{OUT} = 1mA	--	0.004	--	%/V
AVDD Load Regulation		1mA ≤ I_{OUT} ≤ 2A	--	0.1	--	%/A
Trans-Conductance of Error Amplifier	gm		--	100	--	μA/V
AVDD Fault Trip Level	V_{FT_AVDD}	V_{AVDD} Falling	V_{AVDD} x 76%	V_{AVDD} x 80%	V_{AVDD} x 84%	V
Isolation Switch Control						
GD Pull Down Voltage		V_{LXI} – V_{GD}	5	6	7	V
GD Sink Current	I_{GD}		8	12	16	μA
GD Pull Up Resistance	R_{GD}		8	12	16	kΩ
Short-Circuit Trigger Duration		I_{AVDDD} ≥ ILIMGD / $R_{ON, PMOS}$	--	200	--	μs
Buck1 Controller ($V_{I/O}$)						
FBB1 Regulation Voltage	V_{FBB1}	No Load	0.788	0.8	0.812	V
Oscillator Frequency	f_{OSC}		400	500	600	kHz
Phase Shift Between Buck1 and Buck2			--	180°	--	--
Maximum Duty Cycle			--	86	--	%
Trans-Conductance of Error Amplifier	gm		--	100	--	μA/V
LXB1 to VINB1 N-MOSFET On-Resistance	$R_{DS(ON)}$	I_{LXB1} = 500mA	--	200	--	mΩ
LXB1 to PGND N-MOSFET On-Resistance		I_{LXB1} = 500mA	--	150	--	mΩ
Soft-Start Period	$T_{SS\_I/O}$		--	300	--	μs
FBB1 Fault Trip Level		V_{FBB1} Falling	0.6144	0.64	0.6656	V
LXB1 Positive Current Limit	I_{LIM}		3	3.8	--	A
Buck2 Controller (V_{CORE})						
FBB2 Regulation Voltage	V_{FBB2}	No Load	0.788	0.8	0.812	V
Oscillator Frequency	f_{OSC}		400	500	600	kHz
Phase Shift Between Buck1 and Buck2			--	180°	--	--
Maximum Duty Cycle			--	50	--	%
BOOT2 to DHB2 P-MOSFET On-Resistance	$R_{UG(ON)\_DHB2}$	I_{LXB2} = 100mA	--	1.8	--	Ω
DHB2 to LXB2 N-MOSFET On-Resistance	$R_{LG(ON)\_DHB2}$	I_{LXB2} = 100mA	--	0.6	--	Ω
LXB2 to DLB2 P-MOSFET On-Resistance	$R_{UG(ON)\_DLB2}$	I_{LXB2} = 100mA	--	2	--	Ω
DLB2 to PGND N-MOSFET On-Resistance	$R_{LG(ON)\_DLB2}$	I_{LXB2} = 100mA	--	0.5	--	Ω
Soft-Start Period	T_{SS_CORE}		--	300	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FBB2 Fault Trip Level		V_{FBB2} Falling	0.6144	0.64	0.6656	V
FBB2 Short Trip Level		V_{FBB2} Falling	--	0.16	--	V
ILIMIT2 Source Current			--	40	--	μA
Low Side Switch Current Limit		Cycle by Cycle	--	$V_{ILIMIT2}$ / 8	--	V
Maximum ILIMIT2 Voltage Setting			--	2.4	--	V
Negative Charge Pump Controller (VGL)						
VGL Adjustable Output Voltage Range	V_{GL}	Register Address = "02h", 6 bits, V_{GL} = (–1.8V to –8.1V) [00h to 3Fh]	–8.1	--	–1.8	V
VGL Regulation Voltage (Default)	V_{GL}	V_{DRVN} = 0.6V, I_{DRVN} = –100μA	–6.3	–6	–5.7	V
DRVN Sink Current Limit	$I_{DRVN,MAX}$	V_{DRVN} = 0.6V	--	3.5	5	mA
DRVN Short Circuit Current	$I_{DRVN,SC}$	V_{GL} > –0.5V	--	300	--	μA
VGL Load Regulation Error		V_{DRVN} = 0.6V, –50μA < I_{DRVN} < –1mA	--	60	--	mV/mA
Soft-Start Period	T_{SS}		--	3	--	ms
VGL Fault Trip Level		V_{GL} Rising	V_{GL} + 1.5	--	V_{GL} + 2.5	V
VGL Short Trip Level		V_{GL} Rising		–0.5		V
Positive Charge Pump Controller (VGH)						
VGH Adjustable Output Voltage Range	V_{GH}	Register Address = "01h", 5 bits, V_{GH} = (24.5V to 40V) [00h to 1Fh]	24.5	--	40	V
VGH Regulation Voltage (Default)	V_{GH}	V_{DRVP} = 15.6V, I_{DRVP} = 100μA	34.79	35.5	36.21	V
DRVP Source Current Limit	$I_{DRVP,MAX}$	V_{DRVP} = 15.6V	--	3.5	5	mA
DRVP Short Circuit Current	$I_{DRVP,SC}$	V_{GH} < 20%	--	80	--	μA
VGH Load Regulation Error		V_{DRVP} = 15.6V, 50μA < I_{DRVP} < 1mA	--	300	--	mV/mA
Soft-Start Period	T_{SS}		--	4	--	ms
VGH Fault Trip Level		V_{GH} Falling	V_{GH} x 70	V_{GH} x 75	V_{GH} x 80	%
VGH Short Trip Level		V_{GH} Falling	--	20	--	%

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

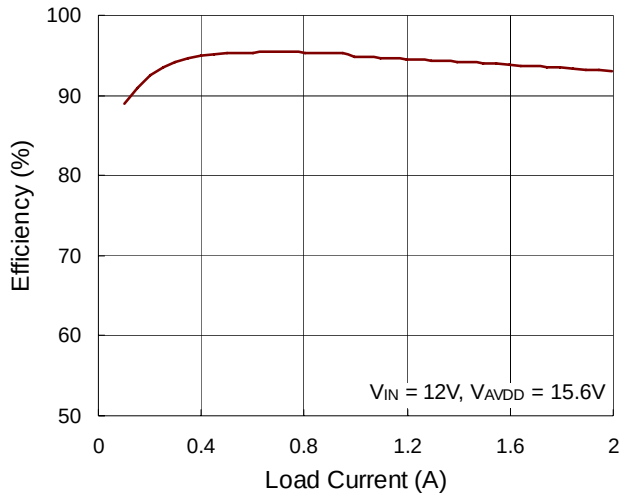
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

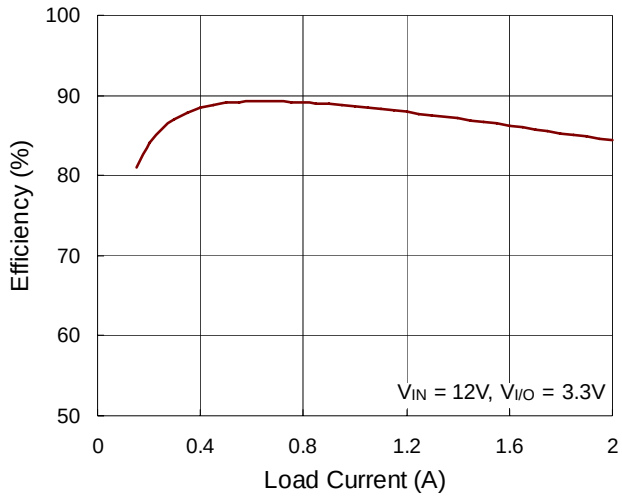
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

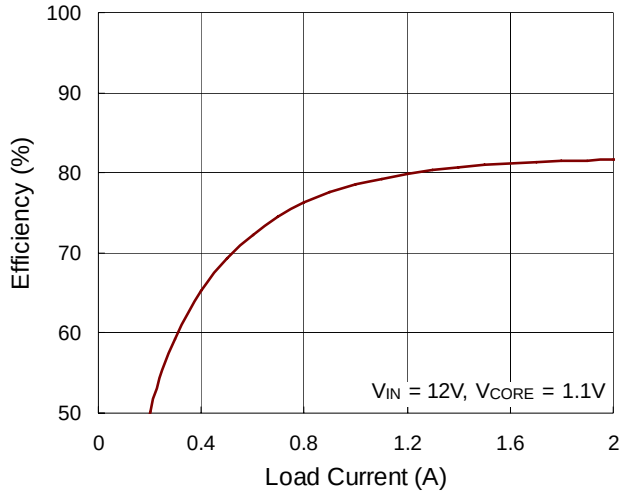
Boost Efficiency vs. Load Current



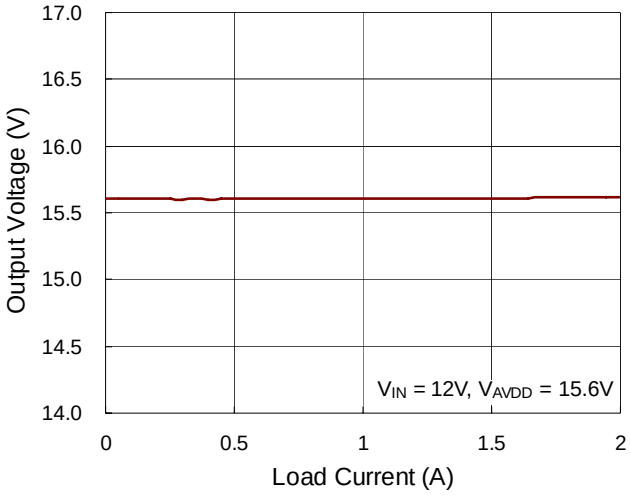
Buck1 Efficiency vs. Load Current



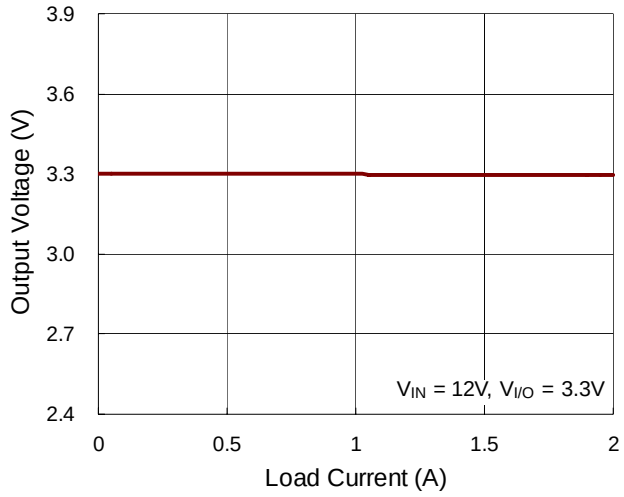
Buck2 Efficiency vs. Load Current



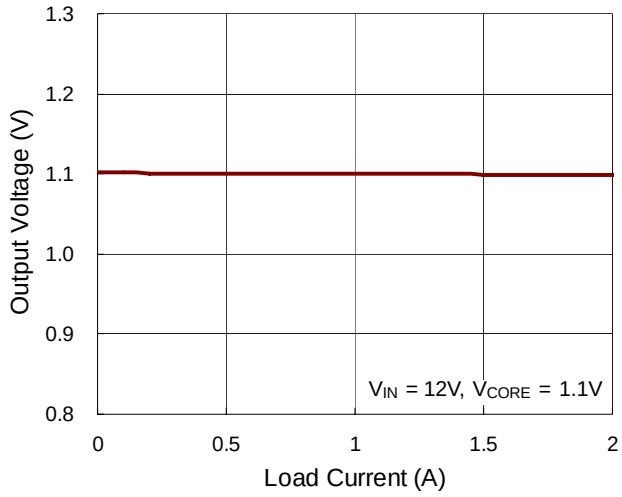
Boost Output Voltage vs. Load Current



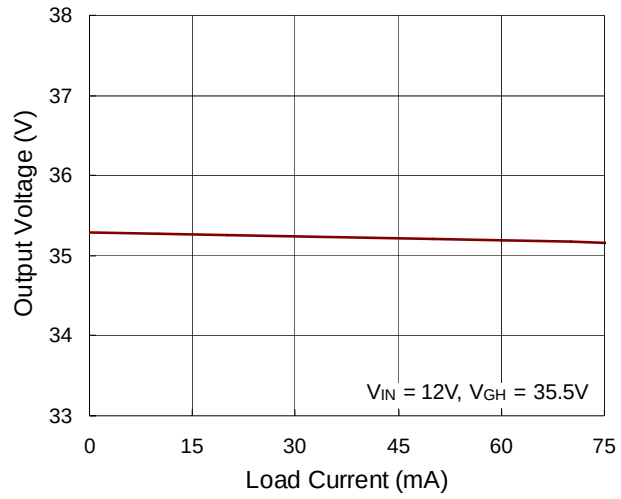
Buck1 Output Voltage vs. Load Current



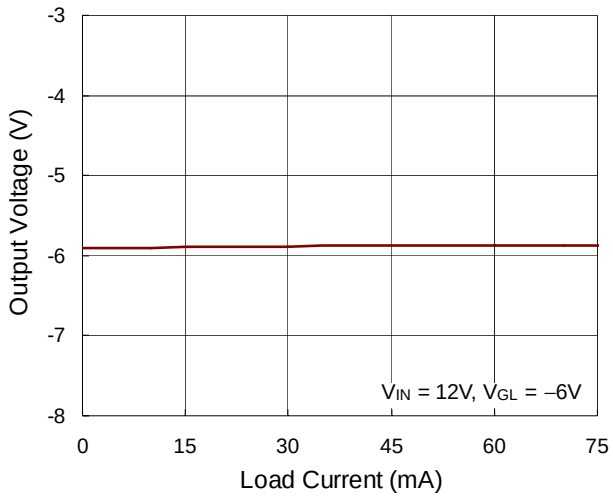
Buck2 Output Voltage vs. Load Current



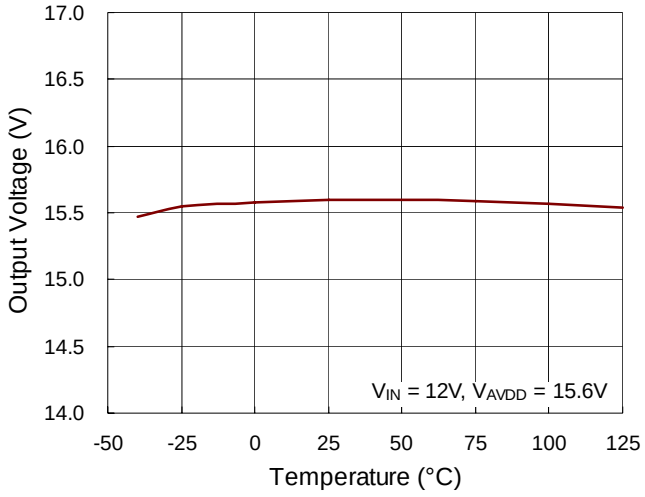
VGH Output Voltage vs. Load Current



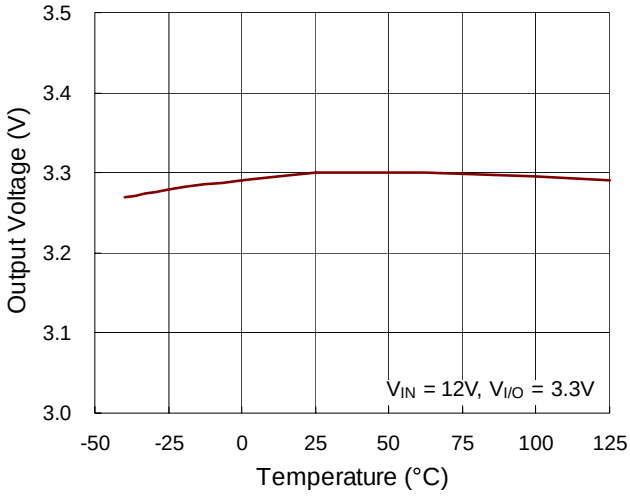
VGL Output Voltage vs. Load Current



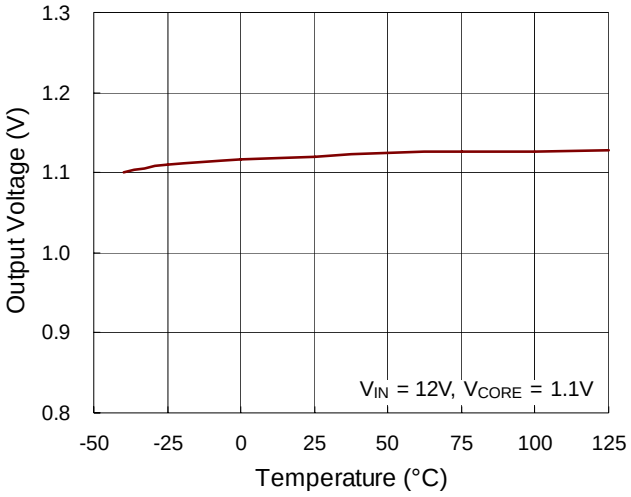
Boost Output Voltage vs. Temperature



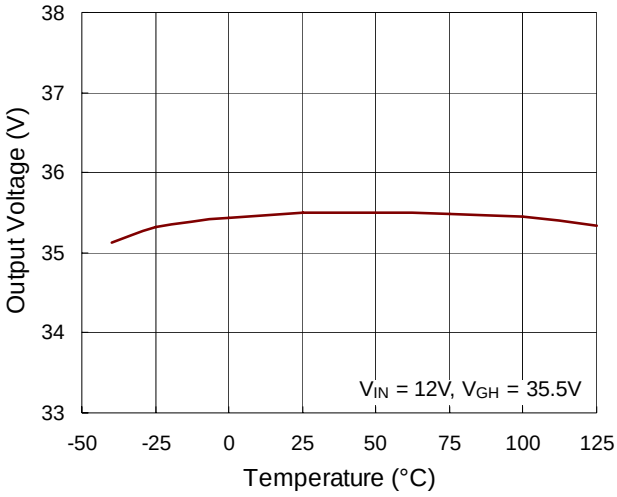
Buck1 Output Voltage vs. Temperature



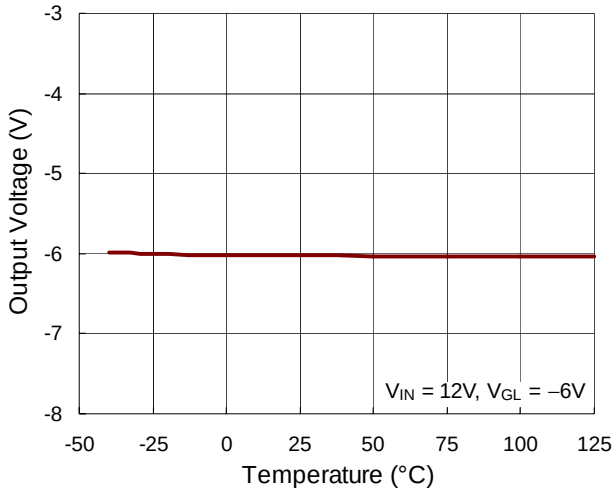
Buck2 Output Voltage vs. Temperature



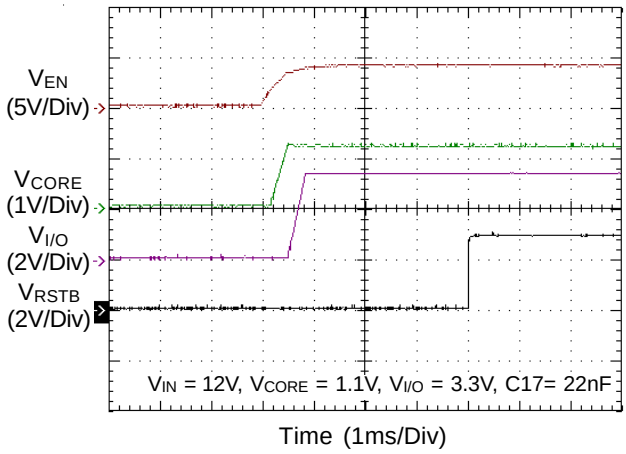
VGH Output Voltage vs. Temperature



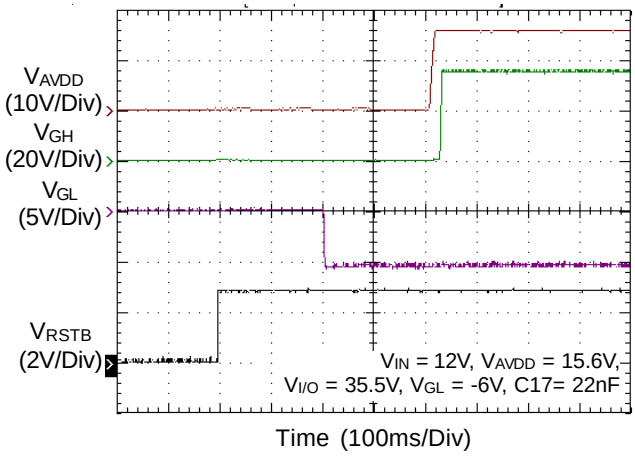
VGL Output Voltage vs. Temperature



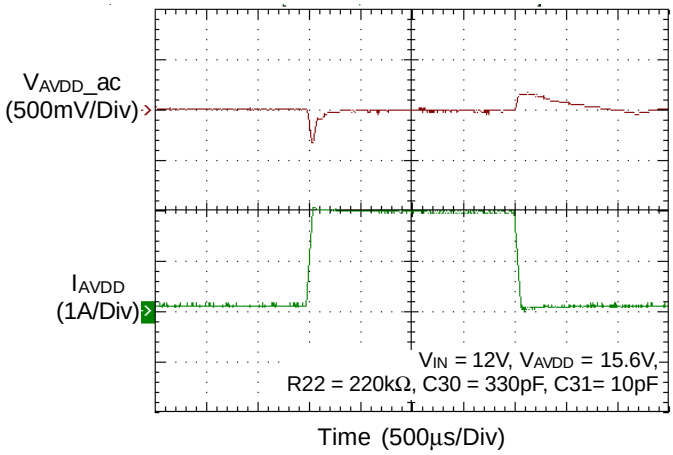
Power On Sequence 1



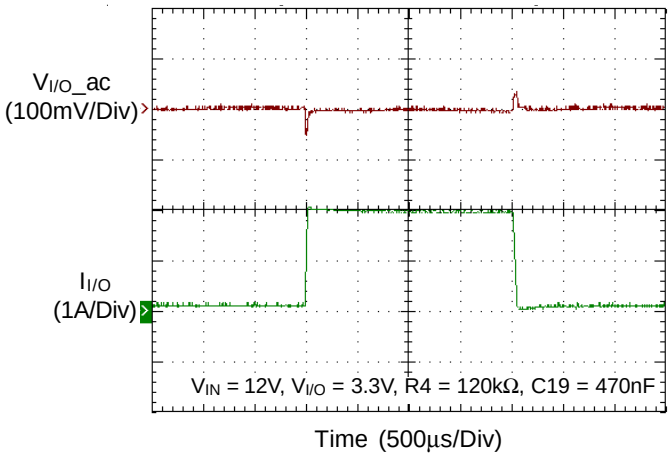
Power On Sequence 2



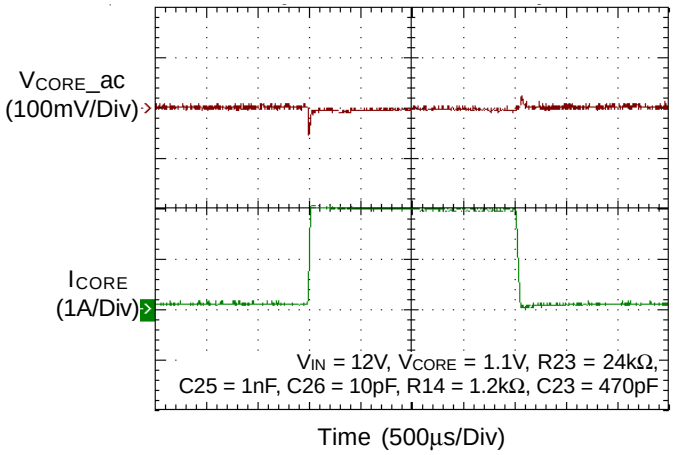
Boost Load Transient Response



Buck1 Load Transient Response



Buck2 Load Transient Response



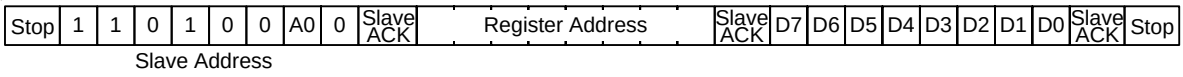
Application Information

I²C Command

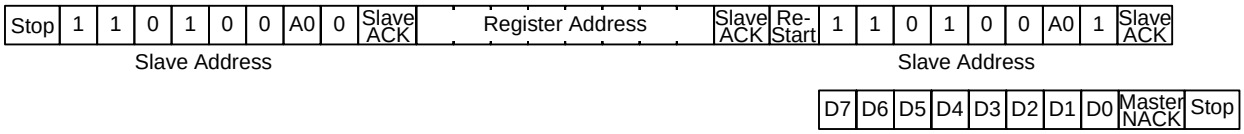
Slave Address

7	6	5	4	3	2	1	0 = LSB
1	1	0	1	0	0	A0	R/$\overline{W}$

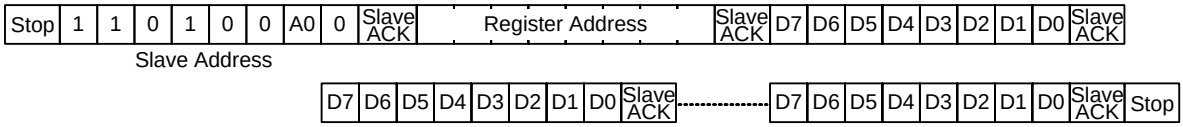
Single I²C Register Write Protocol



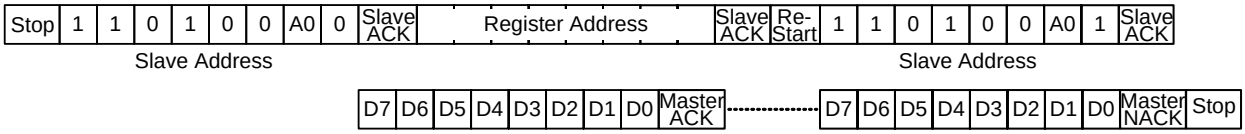
Single I²C Register Read Protocol



Multiple I²C Register Write Protocol



Multiple I²C Register Read Protocol



Register Map

Address	Name	Description	Default Value	Resolution	Range
00h	AVDD	[5 : 0] Boost	15.6V (1Dh)	0.1V	12.7V to 19V (00h to 3Fh)
01h	VGH	[4 : 0] VGH	35.5V (16h)	0.5V	24.5V to 40V (00h to 1Fh)
02h	VGL	[5 : 0] VGL	–6V (2Ah)	–0.1V	–1.8V to –8.1V (00h to 3Fh)
03h	VIO	[3 : 0] VIO adjustment	0% (07h)	1%	–7% to 7% (00h to 0Eh)
04h	V_{CORE}	[3 : 0] V_{CORE} adjustment	0% (07h)	1%	–7% to 7% (00h to 0Eh)
05h	DLY1	[3 : 0] VGL Delay Time	200ms (01h)	DLYR1	0 to 15 x DLYR1 (00h to 0Fh)
06h	DLY2	[3 : 0] AVDD Delay Time	400ms (02h)	DLYR2	0 to 15 x DLYR2 (00h to 0Fh)
07h	DLY3	[3 : 0] VGH Delay Time	10ms (01h)	DLYR3	0 to 15 x DLYR3 (00h to 0Fh)
08h	DLYR1	[1 : 0] DLY1 Resolution	200ms (02h)		1ms, 10ms, 200ms
09h	DLYR2	[1 : 0] DLY2 Resolution	200ms (02h)		1ms, 10ms, 200ms
0Ah	DLYR3	[1 : 0] DLY3 Resolution	10ms (01h)		1ms, 10ms, 200ms
0Bh	SS	[3 : 0] AVDD Soft-Start Time	2ms (02h)	1ms	0ms to 15ms (00h to 0Fh)
0Ch	ILIMGD	[3 : 0] Isolation Switch Current Limit	Disable (00h)	50mV	Disable, 100mV to 800mV (00h to 0Fh)
FFh	CTRL	[7 : 0] ”55h” Start Power On Sequence	00h		

Output Code Table (unit : V)

Register Code	AVDD	VGH	VGL	VIO	V_{CORE}	DLY1	DLY2	DLY3	DLYR1	DLYR2	DLYR3	SS	ILIMGD
00h	12.7	24.5	–1.8	–7%	–7%	0ms	0ms	0ms	1ms	1ms	1ms	0ms	disable
01h	12.8	25.0	–1.9	–6%	–6%	1ms	1ms	1ms	10ms	10ms	10ms	1ms	100mV
02h	12.9	25.5	–2.0	–5%	–5%	2ms	2ms	2ms	200ms	200ms	200ms	2ms	150mV
03h	13.0	26.0	–2.1	–4%	–4%	3ms	3ms	3ms				3ms	200mV
04h	13.1	26.5	–2.2	–3%	–3%	4ms	4ms	4ms				4ms	250mV
05h	13.2	27.0	–2.3	–2%	–2%	5ms	5ms	5ms				5ms	300mV
06h	13.3	27.5	–2.4	–1%	–1%	6ms	6ms	6ms				6ms	350mV
07h	13.4	28.0	–2.5	0	0	7ms	7ms	7ms				7ms	400mV
08h	13.5	28.5	–2.6	1%	1%	8ms	8ms	8ms				8ms	450mV
09h	13.6	29.0	–2.7	2%	2%	9ms	9ms	9ms				9ms	500mV
0Ah	13.7	29.5	–2.8	3%	3%	10ms	10ms	10ms				10ms	550mV
0Bh	13.8	30.0	–2.9	4%	4%	11ms	11ms	11ms				11ms	600mV
0Ch	13.9	30.5	–3.0	5%	5%	12ms	12ms	12ms				12ms	650mV
0Dh	14.0	31.0	–3.1	6%	6%	13ms	13ms	13ms				13ms	700mV
0Eh	14.1	31.5	–3.2	7%	7%	14ms	14ms	14ms				14ms	750mV
0Fh	14.2	32.0	–3.3			15ms	15ms	15ms				15ms	800mV
10h	14.3	32.5	–3.4										
11h	14.4	33.0	–3.5										
12h	14.5	33.5	–3.6										
13h	14.6	34.0	–3.7										
14h	14.7	34.5	–3.8										
15h	14.8	35.0	–3.9										
16h	14.9	35.5	–4.0										
17h	15.0	36.0	–4.1										
18h	15.1	36.5	–4.2										
19h	15.2	37.0	–4.3										
1Ah	15.3	37.5	–4.4										
1Bh	15.4	38.0	–4.5										
1Ch	15.5	38.5	–4.6										
1Dh	15.6	39.0	–4.7										
1Eh	15.7	39.5	–4.8										
1Fh	15.8	40.0	–4.9										
20h	15.9		–5.0										
21h	16.0		–5.1										
22h	16.1		–5.2										
23h	16.2		–5.3										
24h	16.3		–5.4										
25h	16.4		–5.5										

Register Code	AVDD	VGH	VGL	VIO	V_{CORE}	DLY1	DLY2	DLY3	DLYR1	DLYR2	DLYR3	SS	ILIMGD
26h	16.5		–5.6										
27h	16.6		–5.7										
28h	16.7		–5.8										
29h	16.8		–5.9										
2Ah	16.9		–6.0										
2Bh	17.0		–6.1										
2Ch	17.1		–6.2										
2Dh	17.2		–6.3										
2Eh	17.3		–6.4										
2Fh	17.4		–6.5										
30h	17.5		–6.6										
31h	17.6		–6.7										
32h	17.7		–6.8										
33h	17.8		–6.9										
34h	17.9		–7.0										
35h	18.0		–7.1										
36h	18.1		–7.2										
37h	18.2		–7.3										
38h	18.3		–7.4										
39h	18.4		–7.5										
3Ah	18.5		–7.6										
3Bh	18.6		–7.7										
3Ch	18.7		–7.8										
3Dh	18.8		–7.9										
3Eh	18.9		–8.0										
3Fh	19.0		–8.1										
40h													

If register data out of spec, IC will be into default value.

The RT6908 is a programmable multi-functional power solution for TFT LCD panels. The RT6908 contains a step-up converter for main power, a synchronous buck converter and a synchronous buck controller to provide the logic voltages for timing controller, voltage detector for the system. Moreover, a positive charge pump regulator provides the adjustable gate-high voltage and a negative charge pump regulator provides the gate low voltage.

Boost Converter

The boost converter is high efficiency PWM architecture. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows use of smaller components to minimize the thickness of the LCD panel. The output voltage can be achieved by setting the I^2C register 00h [5:0]. The Boost minimum gain ratio depends on minimum on time. It suggested that AVDD higher than 1.14XVIN for better performance.

Boost Soft-Start

The main boost converter has an internal soft-start function to reduce the input inrush current. The soft-start time can be achieved from 0ms to 15ms by setting the I^2C register 0Bh [3:0].

Boost Over Voltage Protection

The main boost converter has an over voltage protection to protect the main switch at the LXI pin. When the LXI pin voltage rises above 20V, the boost converter turns the switch off. As soon as the output voltage falls below the over voltage threshold, the converter will resume operation.

Boost Over Current Protection

The RT6908 senses the inductor current that is flowing into the LX pin. The internal N-MOSFET will be turned off if the peak inductor current reaches 5.6A (typ.). Thus, the output current at the current limit boundary, denoted as $I_{OUT(LIM)}$, can be calculated according to the following equation :

$$I_{OUT(LIM)} = \eta \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{LIM} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

where η is the efficiency of the boost converter, I_{LIM} is the value of the current limit and T_S is the switching period.

Boost Short Circuit Protection

The main boost converter has a short circuit protection. This function disables the boost converter and isolation P-MOSFET if the difference voltage between the LXI and AVDD pin larger than ILIMGD I^2C register 0Ch [3:0] setting. The IC will shut down if this difference voltage remains above setting value after 200µs. Besides, IC will also shut down if input voltage below UVLO threshold at AVDD short circuit period. Only input voltage below 5V (typ.) then re-power on and remove fault condition, IC can return to normal operation.

Boost Under Voltage Fault Protection

The main boost converter has a fault protection. This function disables the boost converter if AVDD is detected to be below 80%. The IC will shut down if AVDD remains below 80% after 50ms.

Boost Inductor Selection

The inductor value depends on the maximum input current. As a general rule the inductor ripple current is 20% to 40% of maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the boost converter, $I_{IN(MAX)}$ is the maximum input current and I_{RIPPLE} is the inductor ripple current. The input peak current can be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$I_{PEAK} = I_{RIPPLE} + I_{IN(MAX)} = 1.2\ I_{IN(MAX)}$$

Note that the saturated current of inductor must be greater than I_{PEAK}. The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Diode Selection

The schottky diode is a good choice for any asynchronous boost converter due to the small forward voltage. However, when selecting a schottky diode, important parameters such as power dissipation, reverse voltage rating, and pulsating peak current must all be taken into consideration. A suitable schottky diode's reverse voltage rating must be greater than the maximum output voltage, and its average current rating must exceed the average output current.

Boost Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input ripple voltage caused by the switching operation. Another consideration is the voltage rating of the input capacitor, which must be greater than the maximum input voltage.

Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. A 120μF low ESR OS-CAP is sufficient for most applications. This portion consists of two parts, one is the product of I_{IN} and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. As shown in Figure 4, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

Where f_{OSC} is the switching frequency and the ΔI_L is the inductor ripple current. Move C_{OUT} to the left side to estimate the value of ΔV_{OUT1} as the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

Finally, the output ripple voltage can be determined as following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

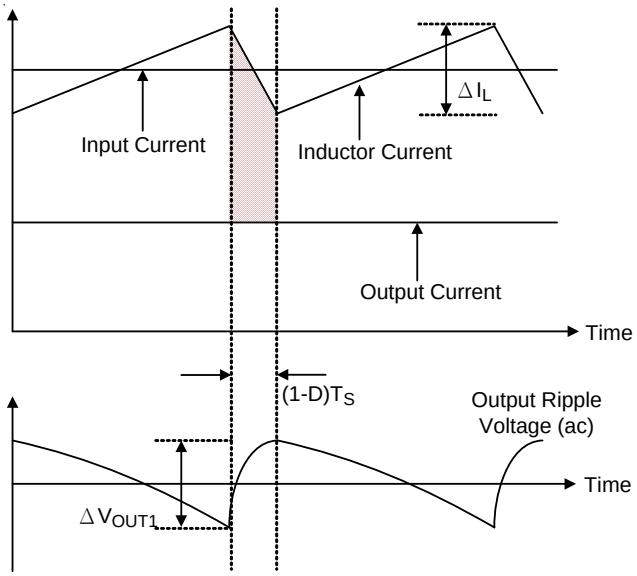


Figure 4. The Output Ripple Voltage without the Contribution of ESR

Boost Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R22 and C30. Choose R22 to set the high frequency integrator gain for fast transient response. And choose C30 to set the integrator zero to maintain stability.

VI/O Synchronous Buck Converter

The buck converter is a high efficiency PWM architecture with 500kHz operation frequency and fast transient response. The converter drives an internal N-MOSFET, connected between the VINB1 and LXB1 pin. Connect a 100nF low ESR ceramic capacitor between the BOOT1 pin and LXB1 pin to provide gate driver voltage for the high side MOSFET.

VI/O Buck Output Voltage Setting

The regulated default output voltage is as shown in the following equation :

$$V_{I/O} = V_{FBB1} \times \left(1 + \frac{R2}{R3} \right), \text{ where } V_{FBB1} = 0.8V \quad (typ.)$$

The recommended value for R2 should be up to 10kΩ without some sacrificing. To place the resistor divider as close as possible to the chip can reduce noise sensitivity. The output voltage also can be adjusted from –7% to 7% by setting the I^2C register 03h [3:0].

VI/O Buck Soft-Start

The step-down converter has an internal soft-start to reduce the input inrush current. When the buck converter is enabled, the output voltage rises slowly from zero to the regulated voltage. The typical soft-start time is around 300μs.

VI/O Buck Over Current Protection

The IC senses the inductor current that is flowing out the LXB1 pin. The internal MOSFET will be turned off if the peak inductor current reaches 3.8A (typ.).

VI/O Buck Short Circuit Protection

To limit the short circuit current, the device has a cycle-by-cycle current limit. To avoid the short circuit current from rising above the internal current limit when the output is shorted to GND, the switching frequency is reduced as well. The switching frequency is reduced to one-half of original frequency when the output voltage is below 80% and to one-fourth of the original frequency when the output voltage is below 20%. If the "short" is removed, the buck converter will resume operation. If the voltage remains below 80% after 50ms, the IC will shut down.

VI/O Buck Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of the R4 and C19. Choose R4 to set high frequency integrator gain for fast transient response. And choose the C19 to set the integrator zero to maintain stability.

VCORE Synchronous Buck Controller

The synchronous buck controller is a high efficiency PWM architecture with 500kHz operation frequency and fast transient response. The controller need external high side and low side N-MOSFET as synchronous rectifier and does not required Schottky diode on the LXB2 pin. The high side MOSFET is connected between VIN and the LXB2 pin, while the low side MOSFET is connected between the LXB2 pin and GND.

VCORE Buck Output Voltage Setting

The regulated default output voltage as shown in the following equation :

$$V_{CORE} = V_{FBB2} \times \left(1 + \frac{R11}{R12}\right), \text{ where } V_{FBB2} = 0.8V \quad \text{(typ.)}$$

The recommended value for R11 should be up to 10kΩ without some sacrificing. Place the resistor divider as close as possible to the chip can reduce noise sensitivity. The output voltage also can be adjusted from –7% to 7% by setting the I^2C register 04h [3:0].

VCORE Buck Soft-Start

The synchronous buck converter has an internal soft-start to reduce the input inrush current. When the converter is enabled, the output voltage rises slowly from zero to the regulated voltage. The typical soft-start time is around 300μs.

VCORE Buck Over Current Protection

The IC has a cycle-by-cycle low side source current sensing algorithm that uses the on-resistance of the low side MOSFET as a current sensing element, so that costly sense resistors are not required. The DHB2 and DLB2 will be turned off if the low side MOSFET source current reaches setting value. Moreover, IC will restart after 50ms if over current remains 7 cycles. Low side source peak current limit threshold is 1/8 voltage at the ILIMT2 pin. Meanwhile, the real current limit value need consider the on-resistance of the low side MOSFET.

$$I_{LIM\_M2} = \frac{V_{ILIMIT2}}{8 \times R_{ON}(switch)} \quad \text{(A)}$$

when I_{LIM_M2} is "Low side switch current limit".

VCORE Buck Short Circuit Protection

To limit the short circuit current, the device has a cycle-by-cycle current limit. To avoid the short circuit current from low side MOSFET source current limit when the output is shorted to GND, the switching operation will be stop. The switching operation will stop when the output voltage is below 20%. If the short is removed, the buck converter will resume operation. If the voltage remains below 80% after 50ms, the IC will shut down.

VCORE Buck Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R23 and C25 and C26. Choose R23 to set high frequency integrator gain for fast transient response, C25 and C26 to set the integrator zero to maintain stability.

VCORE Buck External MOSFET Selection

The V_{CORE} buck controller drives two external N-MOSFETs as the switch. There are some considerations to choose the external MOSFET. It includes MOSFET drain to source voltage stress, on-resistance, total gate charge characteristics and power dissipation for thermal performance.

Buck Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, will increase with higher V_{IN} and decrease with higher inductance, as shown in below equation :

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{OSC} \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, the value of $I_{L(MAX)}$ = 0.4 is a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left(\frac{V_{OUT}}{f_{OSC} \times \Delta I_{L(MAX)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Buck Input Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at VIN = $2V_{OUT}$, where I_{RMS} = I_{OUT} / 2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10µF low ESR ceramic capacitor is recommended.

Buck Output Capacitor Selection

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, V_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

The output ripple will be highest at the maximum input voltage since I_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Suitable candidates such as dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications requiring high ripple current rating and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. Nevertheless, higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input, VIN, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

VGL Negative Regulator

The VGL negative regulator controller provides low level voltage for gate driver. The linear regulator can provide a programmable output voltage. The output voltage can be adjusted by setting the I^2C register 02h [5:0]. The VGL negative regulator controller has a fault protection. This function can disable the VGL negative regulator controller when the VGL voltage is detected to be above VGL + 2V. If the voltage remains above VGL + 2V after 50ms, the IC will shut down. Moreover, If VGL voltage above –0.5V, the IDRVN source current will be limited to 300μA for short circuit protection.

VGH Positive Regulator

The VGH positive regulator controller provides high level voltage for gate driver. The linear regulator can provide a programmable output voltage. The output voltage can be adjusted by setting the I^2C register 01h [4:0]. The VGH positive regulator controller has a fault protection. This function can disable the VGH regulator controller when the VGH voltage is detected to be below 75%. If the VGH voltage remains below 75% after 50ms, the IC will shut down. Moreover, If VGH voltage remains below 20%, the I_{DRVP} sink current will be limited to 80μA for short circuit protection.

Voltage Detector

The voltage detector monitors the V_{DET} voltage to generate the RSTB pin signal. The RSTB pin will be floating and pulled high by $V_{I/O}$ if V_{DET} is higher than the detecting level. Moreover, the detector power on delay can be determined by connect capacitor to the CRST pin and ground. The detecting level and delay time can be determined as the following equations :

$$\text{Detect voltage, falling} = V_{DET} \times \left(1 + \frac{R25}{R26}\right),$$

where V_{DET} = 0.6V (typ.)

$$\text{Detector delay time} = 0.1563 \times C17 \times 10^9 \quad \text{(ms)}$$

Under Voltage Lockout Protection

The UVLO circuit compares the input voltage at the AVIN pin with the UVLO threshold (8.6V rising, typ.) to ensure that the input voltage is high enough for reliable operation. The 1V (typ.) hysteresis prevents supply transients from causing a shutdown. Once the input voltage exceeds the UVLO rising threshold, start-up begins. When the input voltage falls below the UVLO falling threshold, all switch will be turned off and latched. Otherwise, input voltage need below 5V (typ.), the IC can be reset.

Over Temperature Protection

The RT6908 equips an Over Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 50°C, the RT6908 will resume operation. To maintain continuous operation maximum, the junction temperature should be prevented from rising above 125°C.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT6908, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 36°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (36°C/W) = 2.778W for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT6908 package, the derating

curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

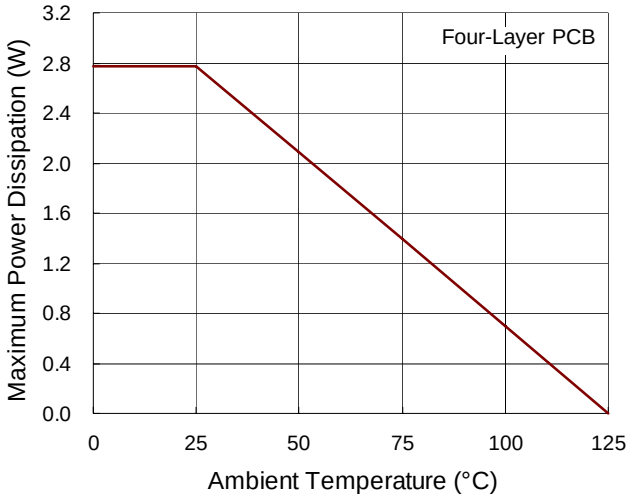


Figure 5. Derating Curve for the RT6908 Package

Layout Consideration

For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short enough especially for the high current loop.
- The compensation circuit should be kept away from the power loops and be shielded with a ground trace to prevent any noise coupling.
- Minimize the size of all LX nodes and keep them wide and shorter.
- The exposed pad of the chip should be connected to a strong ground plane for maximum thermal consideration.

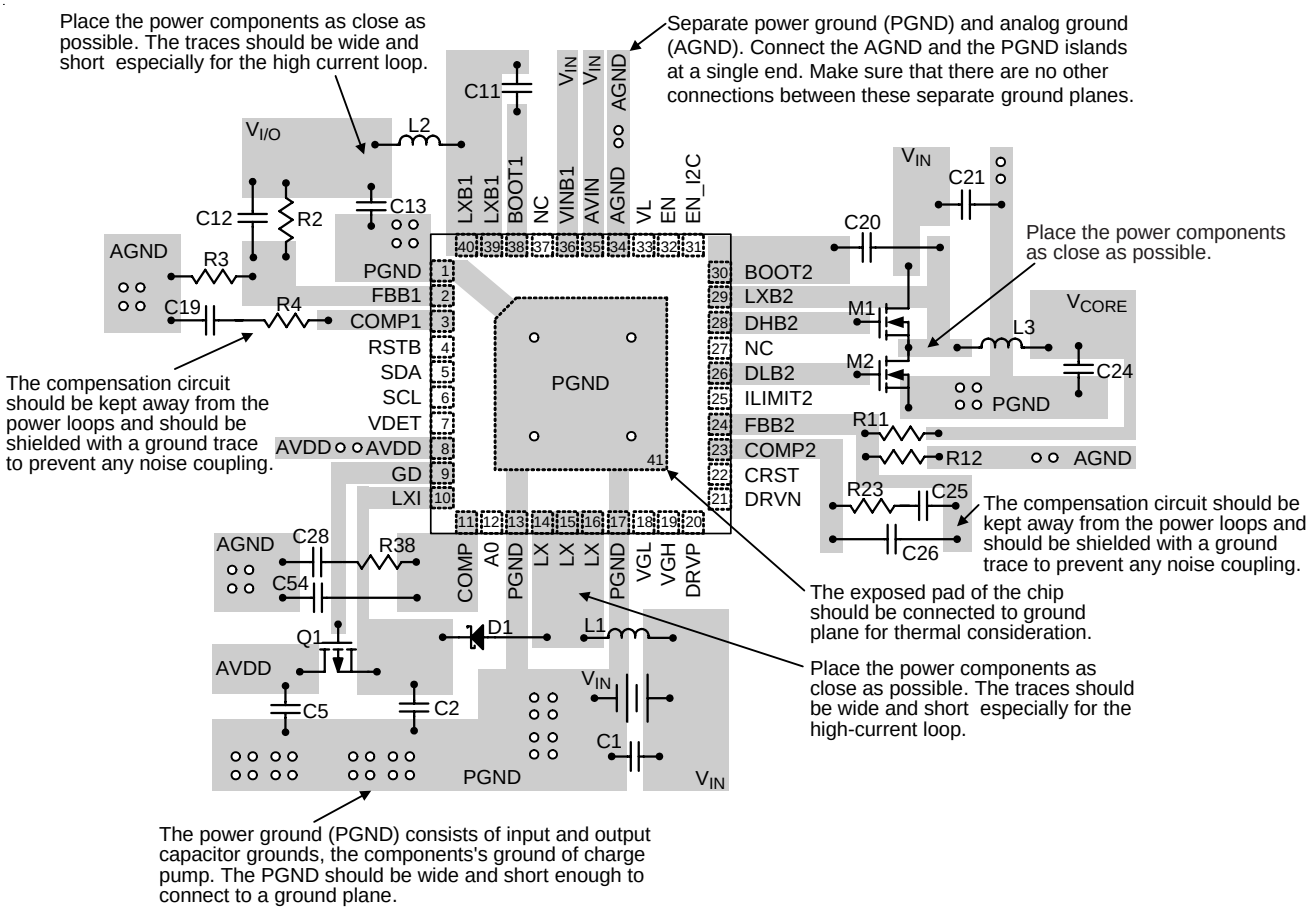
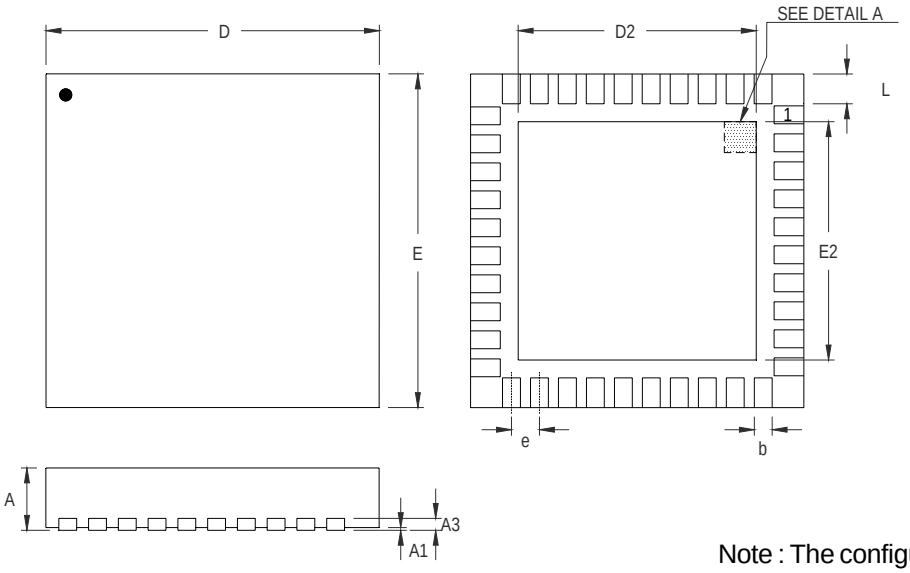
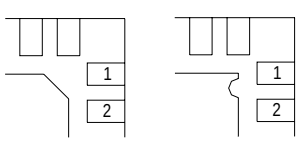


Figure 6. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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