System Integrated Power Module (sIPM™) for PMSM/BLDC Motor Drive

General Description

The RT7056 is one of Richtek's sIPM™ family, which are designed for advanced motor drive applications. This ASIC consists of a PMSM/ BLDC controller, LDOs, the gate driver, bootstrap diodes and MOSFETs. It optimizes these devices specifically designed for PMSM/BLDC motor applications so as to provide great benefits to users with cost-effectiveness, easy design, board space saving and high reliability.

The RT7056 is available in a SOP-23 package.

Ordering Information

RT7056□□□-□□□□□

- Programmed Firmware Code
- Package Type
  S : SOP-23
- Lead Plating System
  G : Green
  (Halogen Free and Pb Free)
- MOSFET Type
  A : 1.7A
  B : 5A

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Integrated 3-Phase PMSM/BLDC Controller, LDOs, Gate Driver, Bootstrap Diodes and MOSFETs**
- **Sensorless and Sinewave Field Oriented Control**
- **Optimized Switching Loss and EMI Trade-Offs**
- **Built-In Short Circuit, Under-Voltage Lockout (UVLO) and Locked-Rotor Protection**
- **Temperature Sensor Embedded**
- **Motor Controller**
  - **ARM 32-bit Cortex-M0 CPU**
  - **Memory Size 16KB MTP, Internal ROM with Embedded Motor Control Library and 4KB SRAM**
  - **Normal or Deep Sleep Mode for Power Saving**
  - **I^2C and UART Communication Interface**
  - **7-Channel 10-bit ADC**
    - **AD0 to AD5 for Differential Mode Current Sense**
    - **AD6 to AD9 for System Application**
  - **1-Channel 8-bit DAC for Debugging**
- **Gate Driver**
  - **Built-In UVLO Function**
  - **Shoot through Prevention**
  - **Matched Propagation Delay**
- **MOSFETs**
  - **Low On-Resistance**
  - **Low Reverse Recovery Charge**

Applications

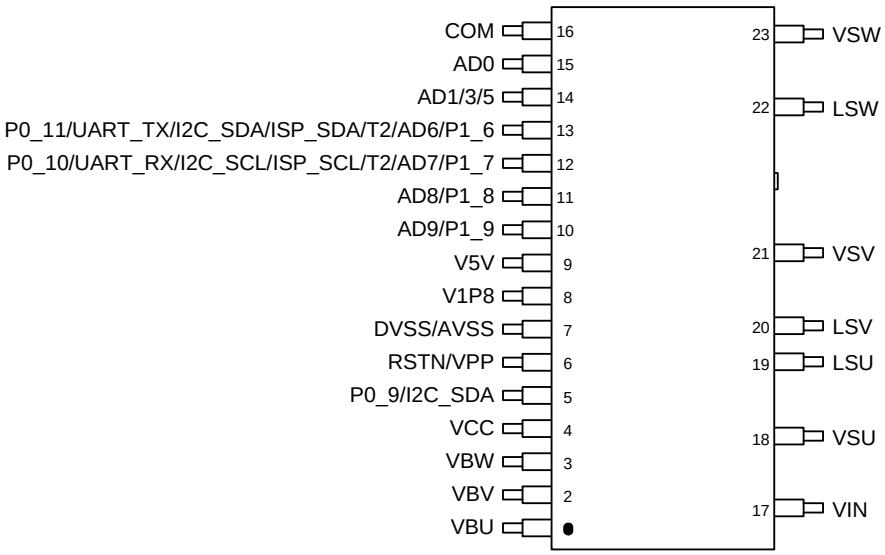
- PMSM/BLDC motor
- Air conditioner indoor/outdoor fan
- Range-hood
- Ceiling fan
- Pedestal fan

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

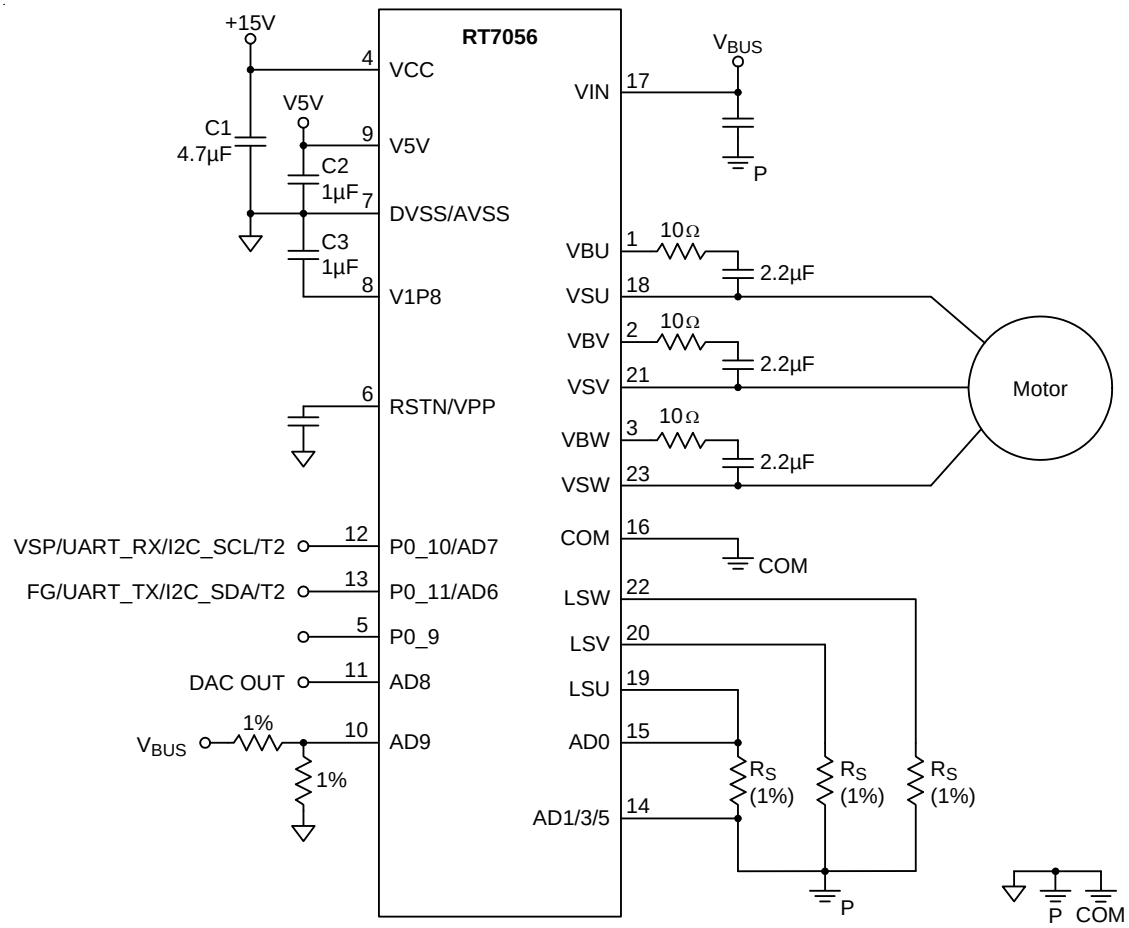
Pin Configuration

(TOP VIEW)



SOP-23

Typical Application Circuit



Note :
C1, C2 and C3 are as close as possible to the IC.
(If C2 and C3 can't close to the IC, it should put another 0.1µF close to the IC.)

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	VBU	HVI	High-side floating supply voltage of U-phase.
2	VBV	HVI	High-side floating supply voltage of V-phase.
3	VBW	HVI	High-side floating supply voltage of W-phase.
4	VCC	P	5V LDO and high/low-side driver supply voltage.
5	P0_9	DIO	Pin 9 of GPIO port 0.
	I2C_SDA	DIO	I^2C data pin.
6	RSTN	DI	Low active reset pin.
	VPP	P	8V input power for MTP fast programming.
7	DVSS/AVSS	GND	Digital and analog ground.
8	V1P8	P	1.8V power pin.
9	V5V	P	5V power pin.
10	AD9	AI	ADC channel 9 input pin.
	P1_9	DIO	Pin 9 of GPIO port 1.
11	AD8	AIO	ADC channel 8 input pin. Voltage type DAC output pin for debugging.
	P1_8	DIO	Pin 8 of GPIO port 1.
12	P0_10	DIO	Pin 10 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	I2C_SCL	DI	I^2C clock pin.
	ISP_SCL	DI	In system programming clock input pin.
	T2	DI	T2 external enable or external clock input pin.
	AD7	AI	ADC channel 7 input pin.
	P1_7	DI	Pin 7 of GPIO port 1.
13	P0_11	DIO	Pin 11 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	I2C_SDA	DIO	I^2C data pin.
	ISP_SDA	DIO	In system programming data input pin.
	T2	DI	T2 external enable or external clock input pin.
	AD6	AI	ADC channel 6 input pin.
	P1_6	DI	Pin 6 of GPIO port 1.
14	AD1/3/5	AI	ADC channel 1/3/5 differential input pin only.
15	AD0	AI	ADC channel 0 differential input pin only.
16	COM	GND	Gate driver ground.
17	VIN	P	Positive DC bus supply voltage.
18	VSU	HVO	U-phase output.
19	LSU	VO	Low-side MOSFET source pin for U-phase.

Pin No.	Pin Name	Type	Pin Function
20	LSV	VO	Low-side MOSFET source pin for V-phase.
21	VSV	HVO	V-phase output.
22	LSW	VO	Low-side MOSFET source pin for W-phase.
23	VSW	HVO	W-phase output.

IO Type Definition :

DIO : Digital input/output pin.

DI : Digital input pin.

DO : Digital output pin.

AI : Analog input pin.

P : Power pin.

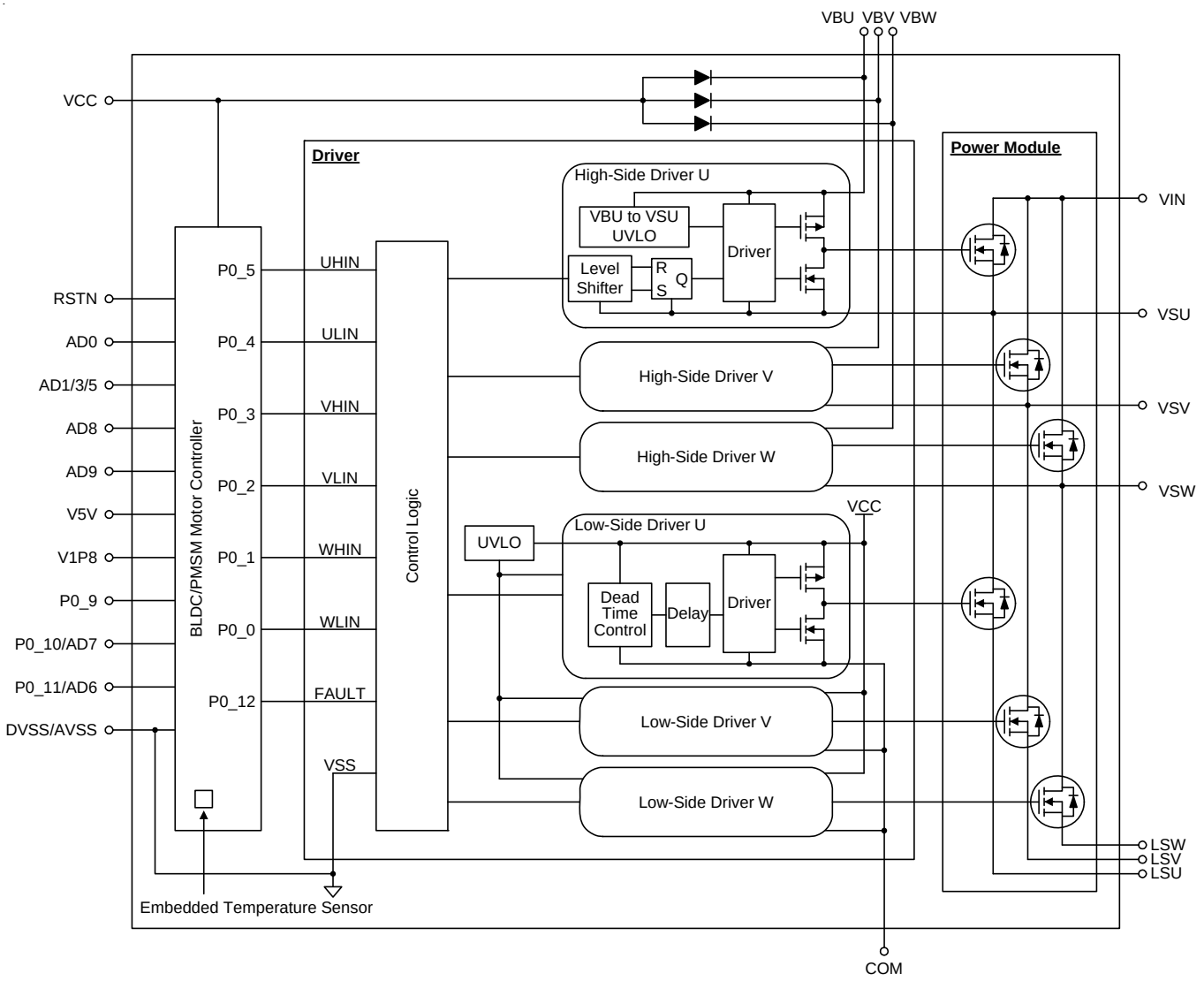
HVI : High voltage input pin.

HVO : High voltage output pin.

VO : Voltage output pin.

GND : Ground pin.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Main Supply Voltage, VIN to LSU/V/W ---------- –0.3V to 600V
- Controller Supply Voltage and Driver Supply Voltage, VCC ---------- –0.3V to 20V
- High-Side Driver Supply Voltage, VBU/V/W to VSU/V/W ---------- –0.3V to 20V
- Digital Input/Output, P0_9 ---------- –0.2V to 6.5V
- Analog Input and Digital Input/Output, P0_10/AD7, P0_11/AD6 ---------- –0.2V to 20V
- Analog Input, AD0, AD1/3/5 ---------- –5V to 11V
- Analog Input and Digital Input/Output, AD8, AD9 ---------- –0.2V to 6.5V
- Reset Pin, RSTN ---------- –0.2V to 9V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-23 ---------- 3.86W
- Package Thermal Resistance (Note 2)
  SOP-23, θ_{JA} ---------- 25.9°C/W
  SOP-23, θ_{JC} ---------- 1.25°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model)
  Except HV Pin ---------- TBD

Recommended Operating Conditions (Note 4)

- Main Supply Voltage, VIN to LSU/V/W ---------- 0V to 450V
- Controller Supply Voltage and Driver Supply Voltage, VCC ---------- 10V to 16.5V
- Digital Input/Output, P0_9 ---------- 0V to 5V
- Analog Input and Digital Input/Output, P0_10/AD7, P0_11/AD6 ---------- 0V to 15V
- Analog Input, AD0, AD1/3/5 ---------- –0.375V to 0.375V
- Analog Input and Digital Input/Output, AD8, AD9 ---------- 0V to 5V
- Input Voltage for MTP Fast Programming, V_{VPP} ---------- 8V to 8.2V
- Capacitance on V1P8 ---------- 1µF
- Capacitance on V5V ---------- 1µF
- Minimum Time Period of RSTN, t_{RSTN} ---------- 100µs
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(V_{CC} = 15V, V_{V5V} = 5V, T_A = 25°C, unless otherwise specified)

Characteristics of Controller Parts

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Section						
System Frequency	f_{SCLK}		--	60	--	MHz
Slow Clock for Sleep Mode	f_{LCLK}		--	80	--	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Management Section						
V_{V5V} UVLO ON Threshold	V_{V5V_UVLON}		--	4.2	--	V
V_{V5V} UVLO OFF Threshold	V_{V5V_UVLOFF}		--	3.8	--	V
V_{V5V} UVLO Hysteresis	V_{V5V_HYS}		--	0.4	--	V
LDO Output Voltage of V5V Pin	V_{V1P8}		--	1.8	--	V
V_{V5V} Current at Operation Mode	I_{V5V_OPER}	20kHz PWM output	--	30	--	mA
V_{V5V} Current at Normal Sleep Mode	I_{V5V_NSLP}		--	7	--	mA
V_{V5V} Current at Deep Sleep Mode	I_{V5V_DSLP}		--	750	--	μA
V_{VILDO} UVLO ON Threshold	V_{VILDO_UVLON}		--	4.2	--	V
V_{VILDO} UVLO OFF Threshold	V_{VILDO_UVLOFF}		--	3.8	--	V
V_{VILDO} UVLO Hysteresis	V_{VILDO_HYS}		--	0.4	--	V
LDO Output Voltage of VILDO Pin	V_{V5V}		--	5	--	V
ADC Section (0V to 3V, 10-bit, Single End Mode, Gain = 1) (Note 5)						
Minimum Conversion Voltage	V_{I_MIN}	Code 000h	--	0	--	V
Maximum Conversion Voltage	V_{I_MAX}	Code 3FFh	--	3	--	V
SCDAC Section (0V to 1.2V, 8-bit for Short Current) (Note 5)						
Minimum Conversion Voltage	V_{SCDAC_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{SCDAC_MAX}	Code FFh	--	1.2	--	V
DAC Offset	V_{SCDAC_Offset}		--	4	--	LSB
CSUMDAC Section (0V to 0.6V, 8-bit for Current Sum) (Note 5)						
Minimum Conversion Voltage	V_{CSUM_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{CSUM_MAX}	Code FFh	--	0.6	--	V
DAC Offset	V_{CSUM_Offset}		--	4	--	LSB
VDAC Section (0V to 3V, 8-bit for General Purposed Comparator) (Note 5)						
Minimum Conversion Voltage	V_{VDAC_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{VDAC_MAX}	Code FFh	--	3	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DAC Offset	V_{VDAC_Offset}		--	4	--	LSB
Output Resistance of DAC	R_O	(Note 6)	--	5	--	kΩ
Current Limit Comparator (Short Circuit) (Note 6)						
Input Voltage Range of Comparator	V_{SC_CMP}		0	--	1.2	V
Comparator Offset	V_{SCCMP_Offset}		–20	0	20	mV
Current Limit Comparator (Current Sum) (Note 6)						
Input Voltage Range of Comparator	V_{CS_CMP}		0	--	0.6	V
Comparator Offset	V_{CSCMP_Offset}		–20	0	20	mV
General Purposed Comparator (Level Comparator) (Note 6)						
Input Voltage Range of Comparator	V_{LV_CMP}		0.5	--	3	V
Comparator Offset	V_{LVCMP_Offset}		–20	0	20	mV
IO of P0_9						
Input High Voltage	V_{IH}		--	2.85	--	V
Input Low Voltage	V_{IL}		--	1.9	--	V
Hysteresis (V_{IH} - V_{IL})	V_{HYS}		--	0.95	--	V
Pull-Up Resistor	R_{UP}		--	76	--	kΩ
Pull-Down Resistor	R_{DOWN}		--	40	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_10 and P0_11						
Input High Voltage	V_{IH}		--	2.85	--	V
Input Low Voltage	V_{IL}		--	1.9	--	V
Hysteresis (VIH - VIL)	V_{HYS}		--	0.95	--	V
Pull-Up Resistor	R_{UP}		--	76	--	kΩ
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of RSTN						
Input High Voltage	V_{IH}		--	2.3	--	V
Input Low Voltage	V_{IL}		--	0.5	--	V
Hysteresis (V_{IH} - V_{IL})	V_{HYS}		--	1.8	--	V
IO of AD0 and AD1/3/5						
Time Constant of Input RC Filter	t_{AD_RC}		--	60	--	ns
IO of AD6 to AD7						
Time Constant of Input RC Filter	t_{AD6-7_STEP1}	Set Register AD6/7_FLT = 0, AD6/7_DIV = 0	--	6	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time Constant of 2-Steps Input RC Filter	t_{AD6-7_STEP2}	Set Register AD6/7_FLT = 1, AD6/7_DIV = 0	--	120	--	μs
Voltage Divider of Input Resistor	Div_Ratio	$(R_{UP} + R_{DOWN}) / R_{DOWN}$	--	3	--	--
Positive Going Threshold Voltage	V_{IH}		--	2.8	--	V
Negative Going Threshold Voltage	V_{IL}		--	1.85	--	V
IO of AD8 to AD9						
Time Constant of Input RC Filter	t_{AD8-9_RC}		--	4.5	--	μs
Positive Going Threshold Voltage	V_{IH}		--	2.8	--	V
Negative Going Threshold Voltage	V_{IL}		--	1.85	--	V
Current Source for External Bias	I_{BIAS}		--	100	--	μA
I^2C Interface						
I^2C Clock	f_{I2C}		100	--	400	kHz

Characteristics of Driver Parts

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-Side Driver Supply Section						
VDRVL Under-Voltage Lockout Threshold (On)	V_{VDRVL_UVLON}		--	8.4	--	V
VDRVL UVLO On Threshold	V_{VDRVL_UVLOFF}		--	7.2	--	V
VDRVL UVLO Hysteresis	V_{VDRVL_HYS}		--	1	--	V
High-Side Driver Supply Section						
VBSU/V/W UVLO On Threshold	V_{VBS_UVLON}		--	8.4	--	V
VBSU/V/WUVLO Off Threshold	V_{VBS_UVLOFF}		--	7.2	--	V
VBSU/V/W UVLO Hysteresis	V_{VBS_HYS}		--	1	--	V
VBSU/V/W Quiescent Current for All Channels	I_{VBSX_Q}	HOU/V/W output low	--	180	--	μA
VSU/V/W Leakage Current for All Channels	I_{VSX_LKG}	VBU/V/W = VSU/V/W = 600V	--	--	40	μA
Bootstrap Diode Section						
Maximum Repetitive Peak Reverse Voltage	V_{RRM}		600	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward Voltage	V_{F_BSD}	I_F = 10mA	--	0.7	--	V

Characteristics of MOSFETs Parts

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
MOSFETs Section							
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	RT7056A	600	--	--	V
			RT7056B	600	--	--	
Drain to Source Leakage Current	I_{DSS}	V_{DS} = 600V, V_{GS} = 0V, T_A = 25°C	RT7056A	--	--	100	μA
			RT7056B	--	--	100	
Drain to Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 1A, T_J = 25°C	RT7056A	--	6.2	--	Ω
		V_{GS} = 10V, I_D = 2.5A, T_J = 25°C	RT7056B	--	2	--	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	RT7056A	--	3.3	--	V
			RT7056B	--	3.1	--	
Free-Wheeling Diode Forward Voltage	V_{FFW}	I_S = 1A, V_{GS} = 0V, T_J = 25°C	RT7056A	--	0.9	--	V
		I_S = 1A, V_{GS} = 0V, T_J = 25°C	RT7056B	--	0.82	--	
Dynamic Electrical Characteristics							
MOSFET Output Dead Time	DT	Frequency = 20kHz, VIN = 10V, R_{LOAD} = 100Ω		--	TBD	--	ns
Turn-On Propagation Delay of Phase Output	t_{ON}	Frequency = 20kHz, VIN = 10V		--	TBD	--	ns
Turn-Off Propagation Delay of Phase Output	t_{OFF}	Frequency = 20kHz, VIN = 10V		--	TBD	--	ns
Dead-Time Matching to All Channels	MDT			--	--	TBD	ns
Delay Matching to All Channels	MT			--	--	TBD	ns

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

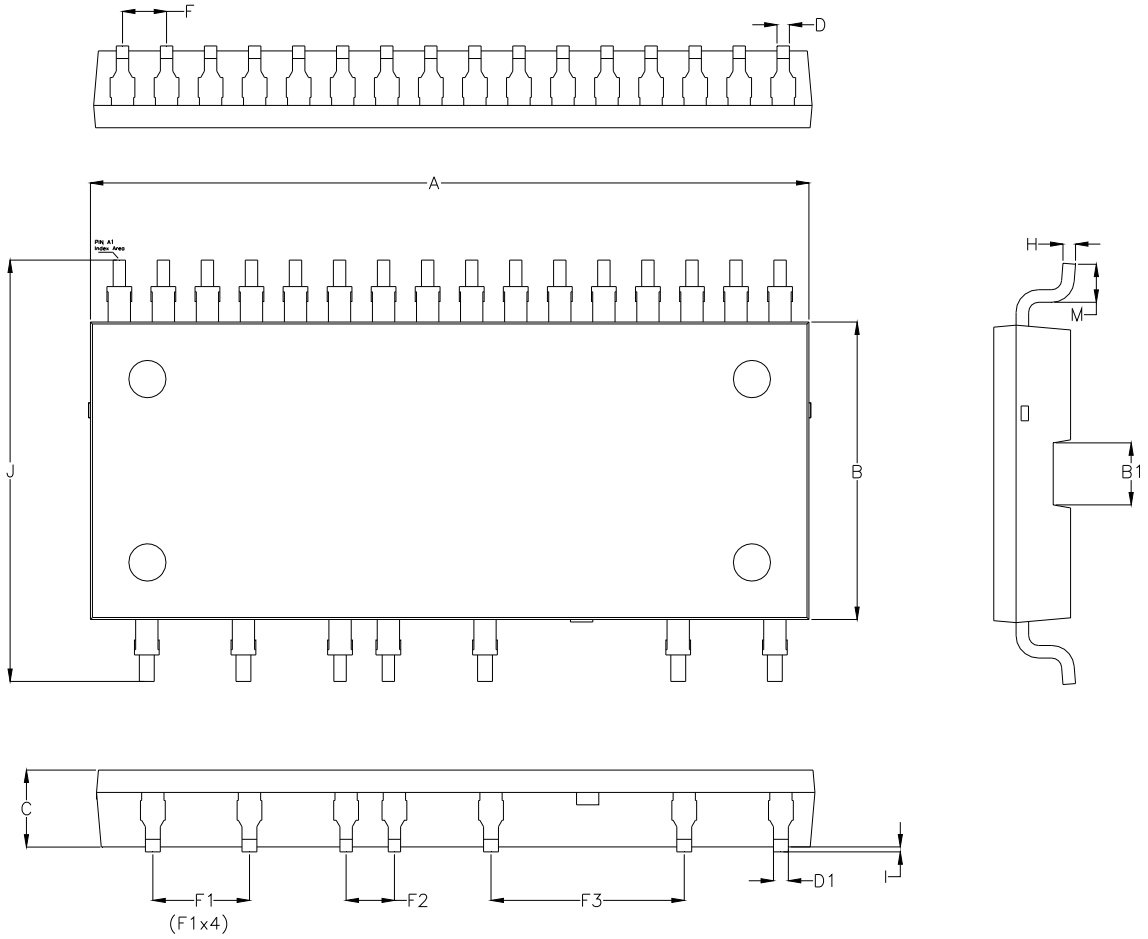
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Characterized, not tested at manufacturing.

Note 6. This parameter is guaranteed by design.

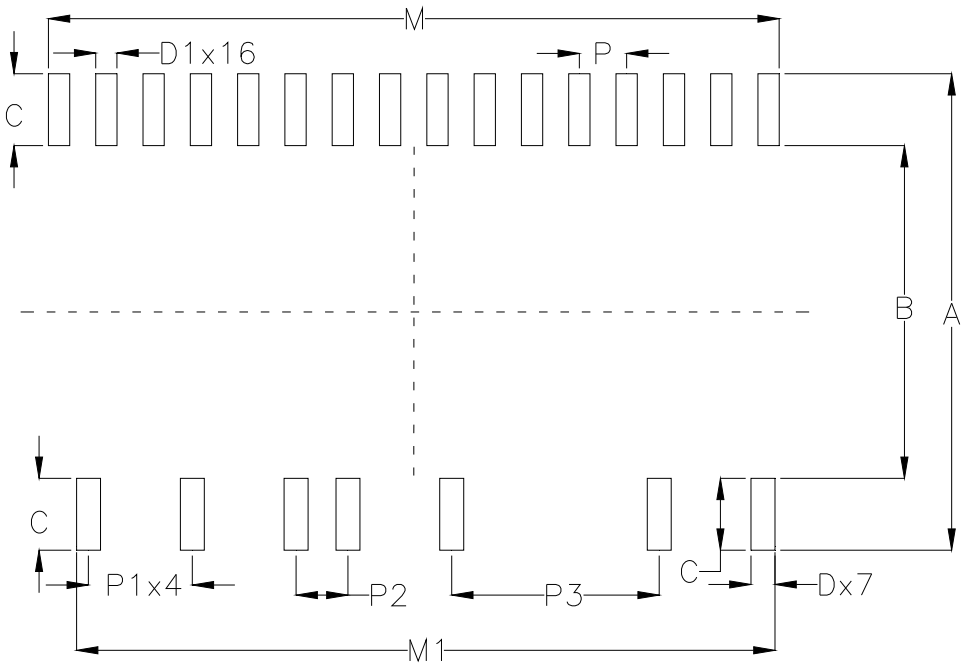
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	28.800	29.800	1.134	1.173
B	11.800	12.200	0.465	0.480
B1	2.300	2.700	0.091	0.106
I	0.050	0.300	0.002	0.012
C	2.900	3.300	0.114	0.130
D	0.400	0.600	0.016	0.024
D1	0.500	0.700	0.020	0.028
F	1.778		0.070	
F1	3.900		0.154	
F2	1.950		0.077	
F3	7.800		0.307	
H	0.400	0.600	0.016	0.024
J	16.900	17.100	0.665	0.673
M	1.300	1.700	0.051	0.067

23-Lead SOP Plastic Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
SOP-23	23	P	P1	P2	P3	A	B	±0.10
		1.778	3.900	1.950	7.800	17.900	12.500	
		C	D	D1	M	M1	NA	
		2.700	0.900	0.800	27.470	26.250	NA	

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Item	Description
P00	2020/3/27		First Edition