# 3 Phase PMSM/BLDC Motor Controller with Gate Driver

## General Description

The RT7075 series is the two-in-one IC which consists of 3 phase motor controller and gate driver delicatedy designed for PMSM/BLDC motor applications.

RT7075 series integrates the ARM 32-bit Cortex-M0 core and peripheral circuits to perform a FOC and sensorless motor control. The IC has integrated various system level peripheral functions, such as ADC, DAC, communication interface, SVPWM, watchdog timer, current sensing, over current protection and over temperature protection, so as to reduce component count, board space and system cost. Furthermore, RT7075 series drives the external devices N-MOSFETs or IGBTs in a half-bridge configuration with an external bootstrap network up to 600V. A dead time control prevents shoot-through of the external devices. The RT7075 series is available in a LQFP-48L 7x7 package.

## Applications

- PMSM/BLDC Motor
- Pedestal Fan
- Ceiling Fan
- Air Conditioner Indoor/Outdoor Fan
- Pump

## Marking Information


RT7075XGPL : Product Number
YMDNN : Date Code
GXYYY : Firmware Code

## RT7075 Version Table

| Version | RT7075A | RT7075B | RT7075C |
|---|---|---|---|
| Sourcing Current | 290mA | 125mA | 70mA |

## Features

- **Integrated 3 Phase PMSM/BLDC Controller with Gate Driver**
- **Sensorless, Sinewave Field Oriented Control**
- **Protections : OCP, UVLO and OTP**
- **PMSM/BLDC Motor Controller :**
  - **ARM 32-Bit Cortex-M0 CPU, Up to 60MHz**
  - **Memories Size : 16KB MTP, Internal ROM with embedded motor control library and 4KB SRAM**
  - **Power Management : Normal or Deep Sleep**
  - **Programming Soft-Start**
  - **Communication Interface : $I^2C$ and UART**
  - **Programmable Clock for PFC control**
  - **10-Channel 10-Bit ADC**
  - **1-Channel Current Type 6-Bit DAC**
  - **1-Channel Voltage Type 8-Bit DAC**
- **Gate Driver :**
  - **Floating Channel Designed for Bootstrap Operation up to 600V**
  - **Sourcing/Sinking Current :**
    **RT7075A : 290mA/600mA**
    **RT7075B : 125mA/600mA**
    **RT7075C : 70mA/600mA**
  - **Built-In UVLO Functions for All Channels**
  - **Matched Propagation Delays for All Channels**
  - **$V_{V15V}$ and $V_{VBU/V/W}$ Supply Range : 13V to 20V**
  - **Shoot-Through Prevention**

## Ordering Information

RT7075□□□-□□□□□

- Programmed Firmware Code
- Package Type
  PL : LQFP-48L 7x7 (L-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- RT7075 Version
  (Refer to Version Table)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

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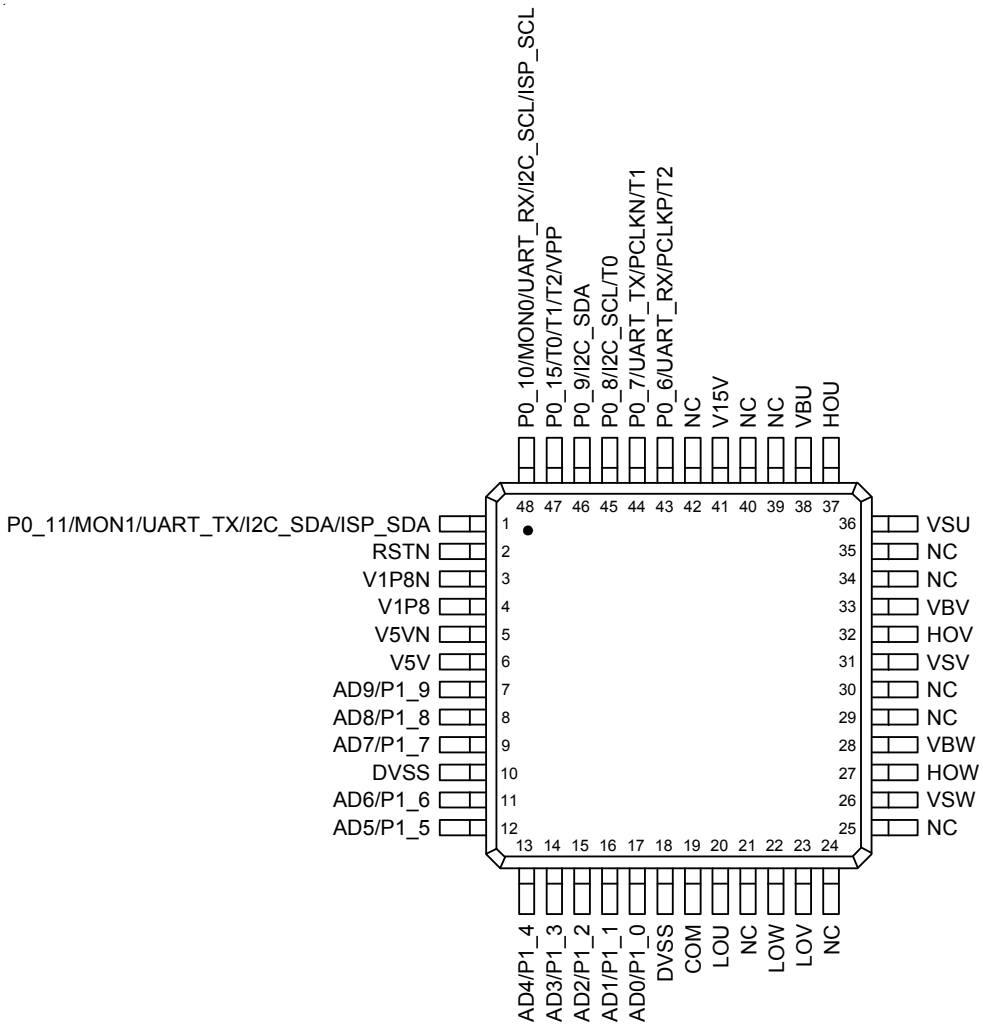
## Pin Configuration

(TOP VIEW)




LQFP-48L 7x7

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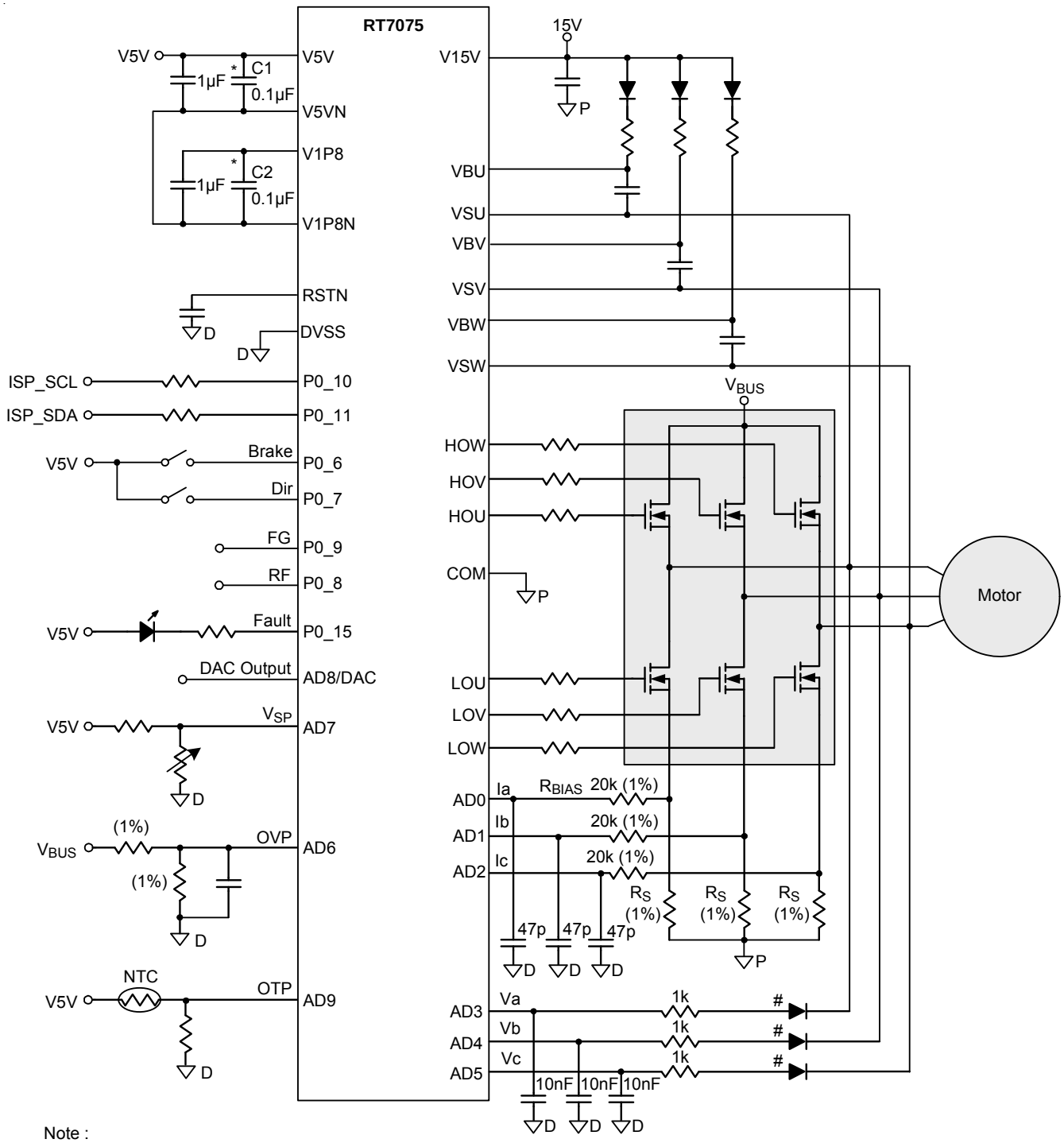
## Typical Application Circuit




Note :
1. C1 & C2 as close as possible to the IC.
2. * : Option
3. # : General-purpose diodes, but pay attention to the voltage stress for different operating voltage of the motor.

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## Functional Pin Description

| Pin No. | Pin Name | Type | Pin Function |
|---|---|---|---|
| 1 | P0_11 | DIO | Pin 11 of GPIO port 0. |
| | MON1 | DO | Internal digital signal monitoring output pin. |
| | UART_TX | DO | UART transmitting pin. |
| | I2C_SDA | DIO | $I^2C$ data pin. |
| | ISP_SDA | DIO | In system programming data input pin. |
| 2 | RSTN | DI | Pad reset pin. |
| 3 | V1P8N | GND | 1.8V power pin negative terminal. |
| 4 | V1P8 | P | 1.8V power pin. |
| 5 | V5VN | GND | 5V power pin negative terminal. |
| 6 | V5V | P | 5V power pin. |
| 7 | AD9 | AIO | ADC Channel 9 input pin. |
| | AD9 | AIO | Current type DAC input pin. (Sink type) |
| | P1_9 | DIO | Pin 9 of GPIO port 1. |
| 8 | AD8 | AIO | ADC Channel 8 input pin. |
| | AD8 | AIO | Voltage type DAC output pin. |
| | P1_8 | DIO | Pin 8 of GPIO port 1. |
| 9 | AD7 | AIO | ADC Channel 7 input pin. |
| | P1_7 | DIO | Pin 7 of GPIO port 1. |
| 10 | DVSS | GND | Digital ground. |
| 11 | AD6 | AIO | ADC Channel 6 input pin. |
| | P1_6 | DIO | Pin 6 of GPIO port 1. |
| 12 | AD5 | AIO | ADC Channel 5 input pin. |
| | P1_5 | DIO | Pin 5 of GPIO port 1. |
| 13 | AD4 | AIO | ADC Channel 4 input pin. |
| | P1_4 | DIO | Pin 4 of GPIO port 1. |
| 14 | AD3 | AIO | ADC Channel 3 input pin. |
| | P1_3 | DIO | Pin 3 of GPIO port 1. |
| 15 | AD2 | AIO | ADC Channel 2 input pin. |
| | P1_2 | DIO | Pin 2 of GPIO port 1. |
| 16 | AD1 | AIO | ADC Channel 1 input pin. |
| | P1_1 | DIO | Pin 1 of GPIO port 1. |
| 17 | AD0 | AIO | ADC Channel 0 input pin. |
| | P1_0 | DIO | Pin 0 of GPIO port 1. |
| 18 | DVSS | GND | Digital ground. |
| 19 | COM | PGND | Gate driver power ground. |

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| Pin No. | Pin Name | Type | Pin Function |
|---|---|---|---|
| 20 | LOU | HVO | Low-side gate control signal of Phase A. |
| 21, 42 | NC | -- | No internal connection. |
| 22 | LOW | HVO | Low-side gate control signal of Phase C. |
| 23 | LOV | HVO | Low-side gate control signal of Phase B. |
| 24, 25, 29, 30, 34, 35, 39, 40 | NC | -- | For H-V rule. |
| 26 | VSW | HVI | High-side floating supply offset voltage of Phase C. |
| 27 | HOW | HVO | High-side gate control signal of Phase C. |
| 28 | VBW | HVI | High-side floating supply voltage of Phase C. |
| 31 | VSV | HVI | High-side floating supply offset voltage of Phase B. |
| 32 | HOV | HVO | High-side gate control signal of Phase B. |
| 33 | VBV | HVI | High-side floating supply voltage of Phase B. |
| 36 | VSU | HVI | High-side floating supply offset voltage of Phase A. |
| 37 | HOU | HVO | High-side gate control signal of Phase A. |
| 38 | VBU | HVI | High-side floating supply voltage of Phase A. |
| 41 | V15V | P | 15V power pin. |
| 43 | P0_6 | DIO | Pin 6 of GPIO port 0. |
| | UART_RX | DI | UART receiving pin. |
| | PCLKP | DO | Programmable clock positive output pin. |
| | T2 | DI | T2 external enable or external clock input pin. |
| 44 | P0_7 | DIO | Pin 7 of GPIO port 0. |
| | UART_TX | DO | UART transmitting pin. |
| | PCLKN | DO | Programmable clock negative output pin. |
| | T1 | DI | T1 external enable or external clock input pin. |
| 45 | P0_8 | DIO | Pin 8 of GPIO port 0. |
| | I2C_SCL | DIO | $I^2C$ clock pin. |
| | T0 | DI | T0 external enable or external clock input pin. |
| 46 | P0_9 | DIO | Pin 9 of GPIO port 0. |
| | I2C_SDA | DIO | $I^2C$ data pin. |
| 47 | P0_15 | DIO | Pin 15 of GPIO port 0. |
| | T0 | DI | T0 external enable or external clock input pin. |
| | T1 | DI | T1 external enable or external clock input pin. |
| | T2 | DI | T2 external enable or external clock input pin. |
| | VPP | P | 8V input power for MTP fast programming. |

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| Pin No. | Pin Name | Type | Pin Function |
|---|---|---|---|
| 48 | P0_10 | DIO | Pin 10 of GPIO port 0. |
| | MON0 | DO | Internal digital signal monitoring output pin. |
| | UART_RX | DI | UART receiving pin. |
| | I2C_SCL | DIO | $I^2C$ clock pin. |
| | ISP_SCL | DI | In system programming clock input pin. |

IO Type Definition :
DIO : Digital input/output pin.
DI : Digital input pin.
DO : Digital output pin.
AIO : Analog input/output pin.
P : Power pin.
HVI : High voltage input pin.
HVO : High voltage output pin.

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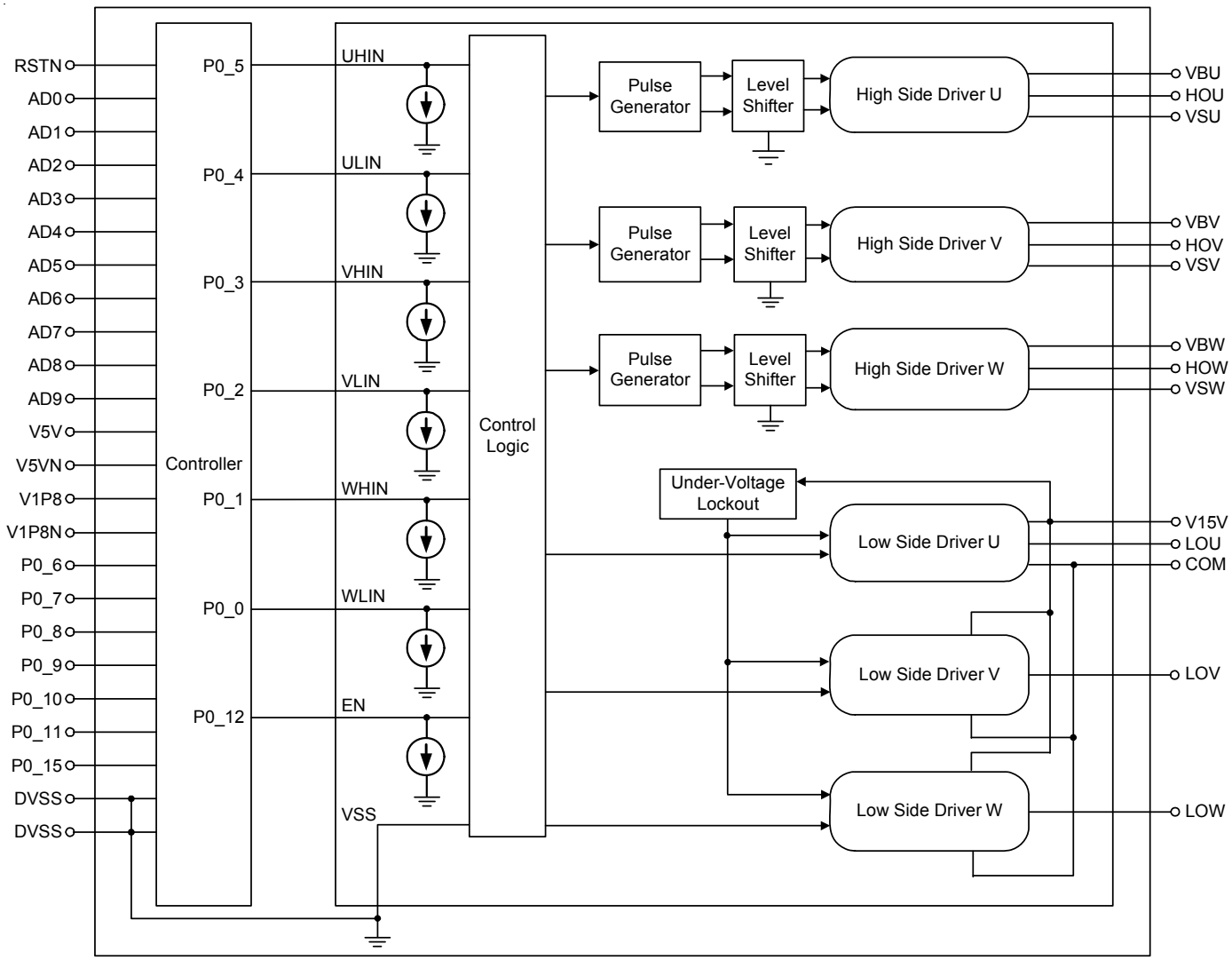
## Functional Block Diagram

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## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V15V ---------- –0.3V to 25V
- Supply Input Voltage, V5V ---------- –0.3V to 6.5V
- VSU/V/W to DVSS ---------- –0.3V to 625V
- VBU/V/W to VSU/V/W, VBU/V/W ---------- –0.3V to 25V
- HOU/V/W to VSU/V/W ---------- –0.3V to ($V_{VBU/V/W}$ + 0.3V)
- LOU/V/W to DVSS ---------- –0.3V to ($V_{V15V}$ + 0.3V)
- Allowable VSU/V/W Voltage Slew Rate, dVSU/V/W /dt ---------- –50V/ns to 50V/ns
- Voltage of I/O Pin and RSTN Pin with Respect to GND ---------- –0.2V to $V_{V5V}$ + 0.2V
- Analog Input Voltage, $V_{AN}$ ---------- –0.2V to $V_{V5V}$ + 0.2V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  LQFP-48L 7x7 ---------- 1.49W
- Package Thermal Resistance (Note 2)
  LQFP-48L 7x7, $\theta_{JA}$ ---------- 67°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model)
  Except HV Pin ---------- 2kV
  HV (VBU/HOU/VSU, VBV/HOV/VSV, VBW/HOW/VSW) to GND ---------- 1kV

## Recommended Operating Conditions (Note 4)

- Supply Voltage, $V_{V15V}$ ---------- 13V to 20V
- VBU/V/W to VSU/V/W, VBSx ---------- 13V to 20V
- VSU/V/W to DVSS ---------- 0 to 600V
- HOU/V/W to VSU/V/W ---------- 0 to VBSX
- LOU/V/W to DVSS ---------- 0 to $V_{V15V}$
- Supply Input Voltage, $V_{V5V}$ ---------- 4.5V to 5.5V
- Input Voltage for MTP Fast Programming, $V_{VPP}$ ---------- 8V to 8.2V
- LDO capacitor on V1P8 ---------- 1µF
- Minimum time period of RSTN, $T_{RSTN}$ ---------- 100µs
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

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## Electrical Characteristics

($V_{V15V}$ = $V_{VBU/V/W}$ = 15V, $V_{V5V}$ = 5V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Clock Section** | | | | | | |
| System Frequency | $f_{SCLK}$ | | 58.8 | 60 | 61.2 | MHz |
| Slow Clock for Sleep Mode | $f_{LCLK}$ | | 77.6 | 80 | 82.4 | kHz |
| **Power Management Section** | | | | | | |
| Turn-On Voltage of V5V | $V_{V5V\_ON}$ | | -- | 4.15 | -- | V |
| V5V On-Off Hysteresis | $V_{V5V\_hys}$ | Turn-Off Voltage = $V_{V5V\_ON}$ - $V_{V5V\_hys}$ | -- | 0.3 | -- | V |
| LDO Output for Internal Operation Voltage | $V_{V1P8}$ | Full speed operation w/i external 20mA sink, $C_{V1P8}$ > 1μF | -- | 1.8 | -- | V |
| V5V Current at Operation Mode | $I_{V5V\_OPER}$ | Typical sensor-less motor control library | -- | 18 | -- | mA |
| V5V Current at Deep Sleep Mode | $I_{V5V\_DSLP}$ | | -- | 400 | -- | μA |
| **ADC Section (0V to 4V, 10-bit, single end mode, gain = 1) (Note 5)** | | | | | | |
| ADC Input Voltage Range | $V_{ADCIN}$ | | 0 | -- | 4 | V |
| **VDAC Section (0V to 4V, 8-bit for short and over current) (Note 5)** | | | | | | |
| Minimum Conversion Voltage | $V_{O\_MIN}$ | | -- | 0 | -- | V |
| Maximum Conversion Voltage | $V_{O\_MAX}$ | | -- | 4 | -- | V |
| DAC Offset | $V_{OFFSET}$ | | -- | 2 | -- | LSB |
| Output Resistance of DAC | $R_O$ | (Note 7) | -- | 5k | -- | Ω |
| Integral Linearity Error | $E_{INL}$ | | −1 | -- | +1 | LSB |
| Differential Linearity Error | $E_{DNL}$ | | −1 | -- | +1 | LSB |
| **VDAC Section (0V to 3V, 8-bit for general purposed comparator) (Note 5)** | | | | | | |
| Minimum Conversion Voltage | $V_{O\_MIN}$ | | -- | 0 | -- | V |
| Maximum Conversion Voltage | $V_{O\_MAX}$ | | -- | 3 | -- | V |
| DAC Offset | $V_{OFFSET}$ | | -- | 2 | -- | LSB |
| Output Resistance of DAC | $R_O$ | (Note 7) | -- | 5k | -- | Ω |
| Integral Linearity Error | $E_{INL}$ | | −1 | -- | +1 | LSB |
| Differential Linearity Error | $E_{DNL}$ | | −1 | -- | +1 | LSB |
| **IDAC Section (0 to 126μA, 6-Bit for current sink) (Note 5)** | | | | | | |
| IDAC Output Bias Voltage Range | $V_{IBIAS}$ | | 0.2 | -- | 5 | V |
| Minimum Sink Current | $I_{O\_MIN}$ | $V_{IBIAS}$ = 2.5V | -- | 0 | -- | μA |
| Maximum Sink Current | $I_{O\_MAX}$ | $V_{IBIAS}$ = 2.5V | -- | 126 | -- | μA |
| Average Current Step | $I_{LSB}$ | Test : ($I_{I\_MIN}$ - $I_{I\_MAX}$)/( 256-1) | -- | 2 | -- | μA |
| DAC Offset | $I_{OFFSET}$ | | -- | 0 | -- | μA |
| Integral Linearity Error | $E_{INL}$ | | −3 | -- | +3 | LSB |
| Differential Linearity Error | $E_{DNL}$ | | −1 | -- | +1 | LSB |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Current Limit Comparator Section (Short and Over-Current)** | | | | | | |
| Comparator Offset | $V_{OFFSET}$ | (Note 6) | –10 | 0 | 10 | mV |
| Input Voltage Range of Comparator | $V_{IN}$ | (Note 7) | 1 | -- | 4 | V |
| Over-Current Level Range | $V_{OC}$ | (Note 7) | 0.5 | -- | 4 | V |
| **General Purposed Comparator (Note 6)** | | | | | | |
| Comparator Offset | $V_{OFFSET}$ | | –5 | 0 | 5 | mV |
| Input Voltage Range of Comparator | $V_{IN}$ | | 0 | -- | 3 | V |
| **IO of P0_6 to P0_7 Section** | | | | | | |
| Input High Voltage | $V_{IH}$ | | -- | -- | 0.7 x V5V | V |
| Input Low Voltage | $V_{IL}$ | | 0.3 x V5V | -- | -- | V |
| Pull-Down Resistor | $R_{DOWN}$ | | -- | 90 | -- | kΩ |
| High Level Output Current | $I_{OH}$ | @ 0.8xV5V | -- | 15 | -- | mA |
| Low Level Output Current | $I_{OL}$ | @ 0.2xV5V | -- | 15 | -- | mA |
| **IO of P0_8 to P0_11 section** | | | | | | |
| Input High Voltage | $V_{IH}$ | | -- | -- | 0.7 x V5V | V |
| Input Low Voltage | $V_{IL}$ | | 0.3 x V5V | -- | -- | V |
| Pull-Up Resistor | $R_{UP}$ | | -- | 70 | -- | kΩ |
| High Level Output Current | $I_{OH}$ | @ 0.8xV5V | -- | 15 | -- | mA |
| Low Level Output Current | $I_{OL}$ | @ 0.2xV5V | -- | 15 | -- | mA |
| **IO of AD0 to AD9 section and P0_15** | | | | | | |
| Input High Voltage | $V_{IH}$ | | -- | -- | 2.7 | V |
| Input Low Voltage | $V_{IL}$ | | 0.6 | -- | -- | V |
| Current Source for External Bias | $I_{BIAS1}$ | AD0 to AD2 | 95 | 100 | 105 | μA |
| Current Source for External Bias | $I_{BIAS2}$ | AD3 to AD9 | -- | 50 | -- | μA |
| Low Level Output Current | $I_{OL}$ | AD0 to AD9 | -- | 2 | -- | mA |

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| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Low Side Power Supply Section** | | | | | | | |
| V15V Under-Voltage Lockout Threshold (On) | $V_{THON\_V15V}$ | | | 9 | 10.5 | 12 | V |
| V15V Under-Voltage Lockout Threshold (Off) | $V_{THOFF\_V15V}$ | | | 8 | 9.5 | 11 | V |
| V15V Under-Voltage Lockout Hysteresis | $V_{HYS\_V15V}$ | | | -- | 1 | -- | V |
| V15V Quiescent Current | $I_{Q\_V15V}$ | Gate driver output low. | | -- | 1000 | -- | μA |
| V15V Operating Current | $I_{P\_V15V}$ | $f_{xLIN}$ = 20kHz, HOU/V/W & LOU/V/W = Open | | -- | 1000 | -- | μA |
| **Bootstrapped Power Supply Section** | | | | | | | |
| VBU/V/W-VSU/V/W Under-Voltage Lockout Threshold (On) | $V_{THON\_VBSX}$ | | | 9 | 10.5 | 12 | V |
| VBU/V/W-VSU/V/W Under-Voltage Lockout Threshold (Off) | $V_{THOFF\_VBSX}$ | | | 8 | 9.5 | 11 | V |
| VBU/V/W-to-VSU/V/W Quiescent Current for Each Channel | $I_{Q\_VBSX}$ | Gate driver output low. | | -- | 100 | 200 | μA |
| VBU/V/W-VSU/V/W Under-Voltage Lockout Hysteresis | $V_{HYS\_VBSX}$ | | | -- | 1 | -- | V |
| VSU/V/W Leakage Current | $I_{VSX}$ | $V_{BU/V/W}$ = $V_{SU/V/W}$ = 600V | | -- | -- | 80 | μA |
| VBU/V/W-to-VSU/V/W Operating Current | $I_{P\_VBSX}$ | $f_{xHIN}$ = 20kHz, HOU/V/W and LOU/V/W = Open | | -- | -- | 600 | μA |
| **Gate Driver Output Section (HOU/V/W, LOU/V/W)** | | | | | | | |
| High Side / Low Side Output Voltage | $V_{OH}$ | $I_O$ = 0mA, $V_{VBU/V/W}$ - $V_{HOU/V/W}$, V15V - $V_{LOU/V/W}$ | | -- | 50 | 200 | mV |
| | $V_{OL}$ | $I_O$ = 0mA, $V_{HOU/V/W}$-$V_{VSU/V/W}$, $V_{LOU/V/W}$-$V_{COM}$ | | -- | 20 | 100 | mV |
| HOU/V/W and LOU/V/W Sourcing Current | IO+ | Gate driver output high, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = 0V, PW < 10μs (Note7) | RT7075A | -- | 290 | -- | mA |
| | | | RT7075B | -- | 125 | -- | |
| | | | RT7075C | -- | 70 | -- | |
| HOU/V/W and LOU/V/W Sinking Current | IO- | Gate driver output low, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = $V_{V15V}$, PW < 10μs (Note7) | | -- | 600 | -- | mA |

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## Dynamic Electrical Characteristics

($V_{V15V}$ = $V_{VBU/V/W}$ = 15V, $V_{V5V}$ = 5V, $V_{VSU/V/W}$ = GND, $C_L$ = 1000pF, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Turn-On Propagation Delay | $t_{ON}$ | $V_{VSX}$ = 0V | | 350 | 500 | 650 | ns |
| Turn-Off Propagation Delay | $t_{OFF}$ | $V_{VSX}$ = 0V | | 350 | 500 | 650 | ns |
| Gate Driver Output Turn-On Rising Time | $t_R$ | | RT7075A | -- | 70 | -- | ns |
| | | | RT7075B | -- | 250 | -- | |
| | | | RT7075C | -- | 450 | -- | |
| Gate Driver Output Turn-Off Falling Time | $t_F$ | | | -- | 35 | -- | ns |
| Gate Driver Output Dead Time | DT | | | 400 | 500 | 600 | ns |
| Delay Matching | MT | | | -- | -- | 120 | ns |
| Dead-Time Matching to All Channels | MDT | | | -- | -- | 120 | ns |

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Characterized, not tested at manufacturing.

**Note 6.** For comparator only.

**Note 7.** This parameter is guaranteed by design.

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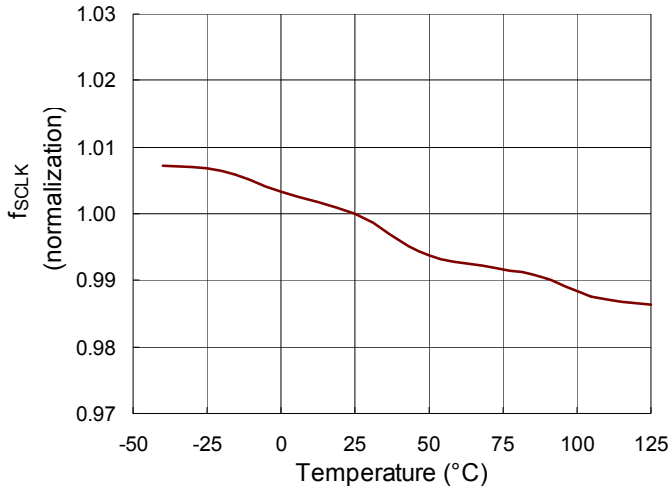
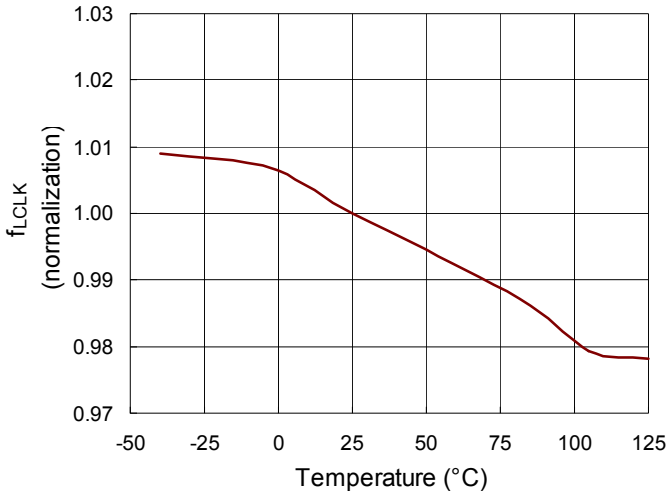
## Typical Operating Characteristics

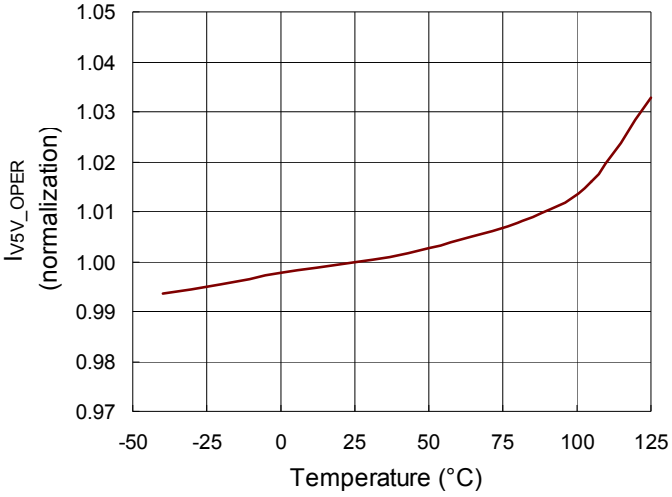
System Frequency vs. Temperature



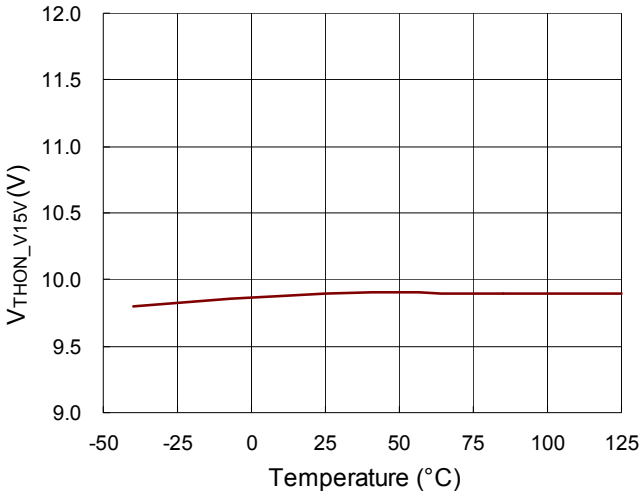

Slow Clock for Sleep Mode vs. Temperature



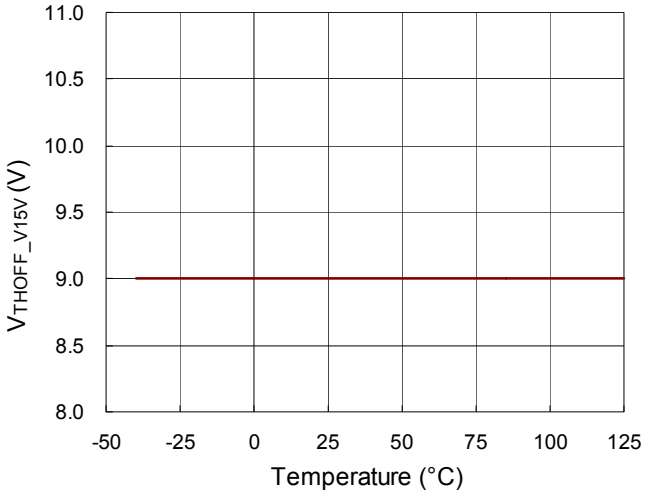

V5V Current at Operation Mode vs. Temperature



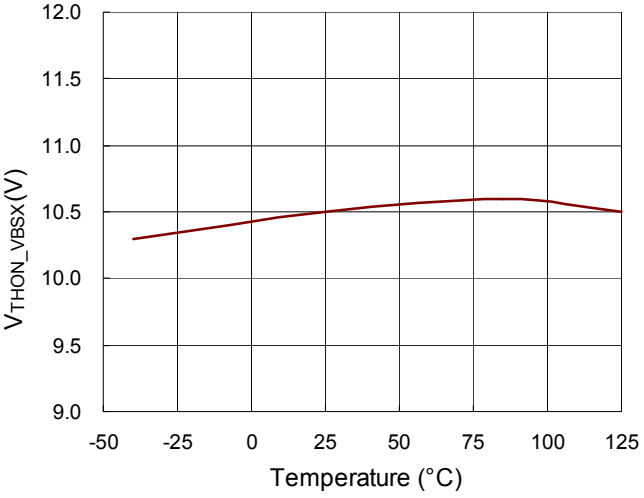

V15V UVLO (On) vs. Temperature




V15V UVLO (Off) vs. Temperature




VBSX UVLO (On) vs. Temperature

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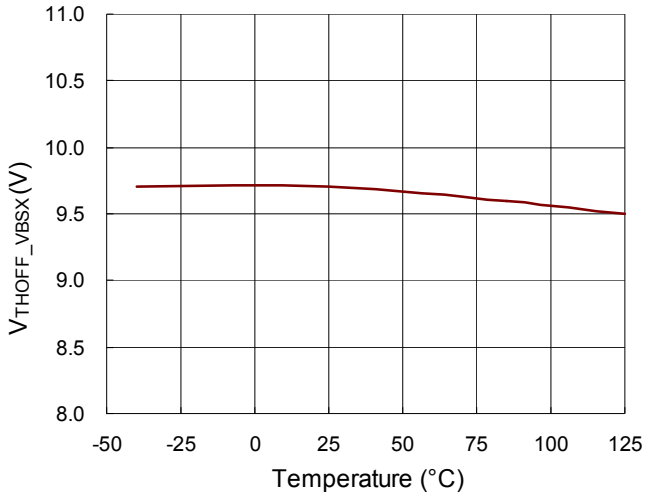
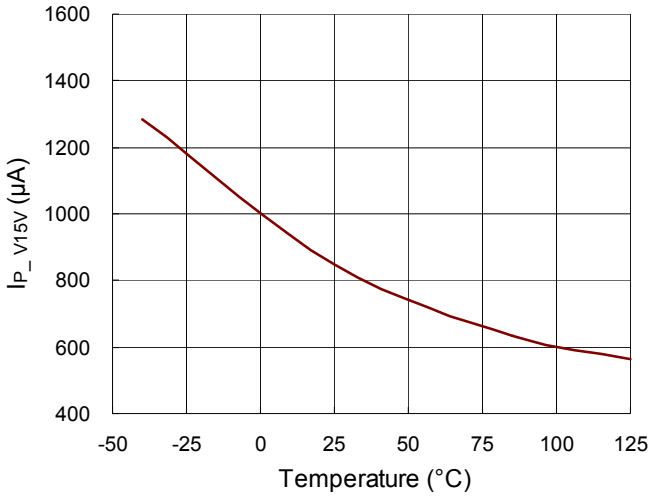
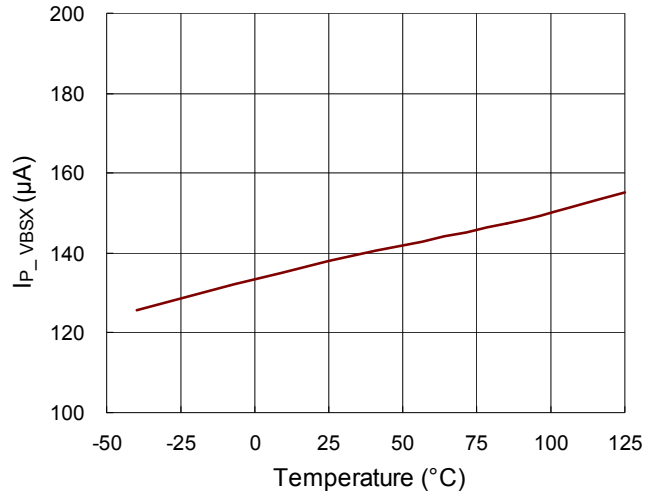
### VBSX UVLO (Off) vs. Temperature



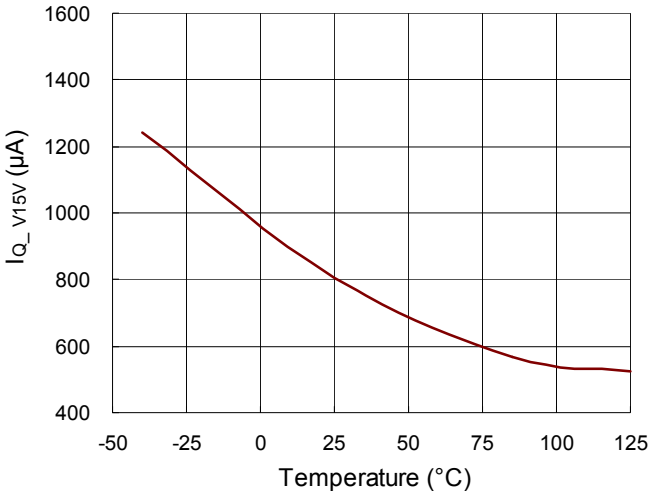

### V15V Operating Current vs. Temperature



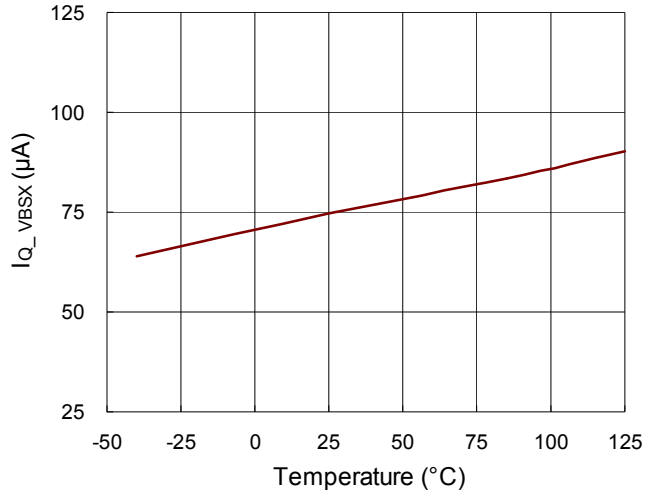

### VBS Operating Current vs. Temperature



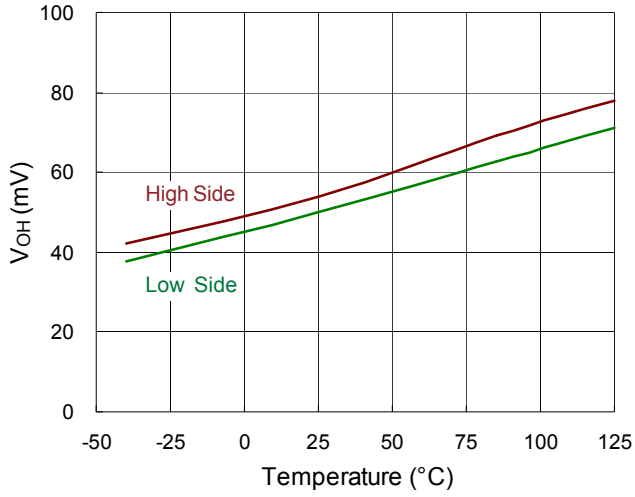

### V15V Quiescent Current vs. Temperature




### VBS Quiescent Current vs. Temperature




### High/Low Side Output Voltage vs. Temperature

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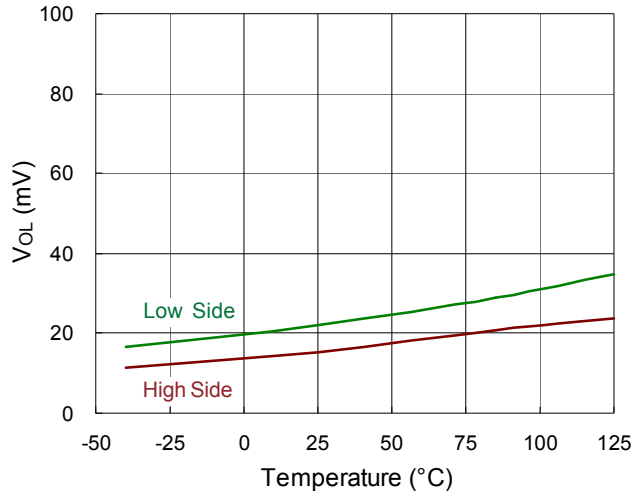
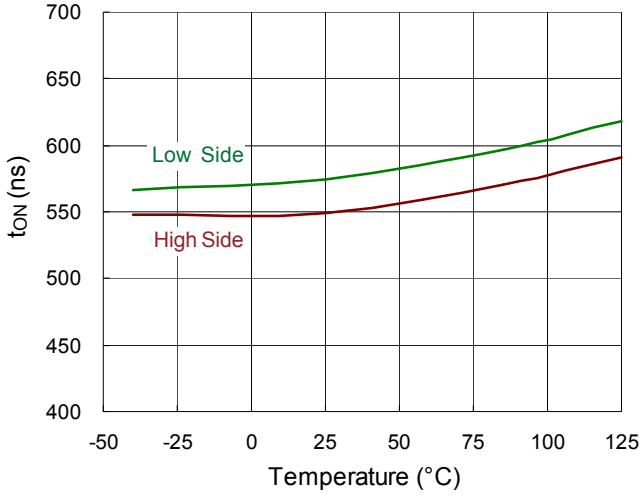
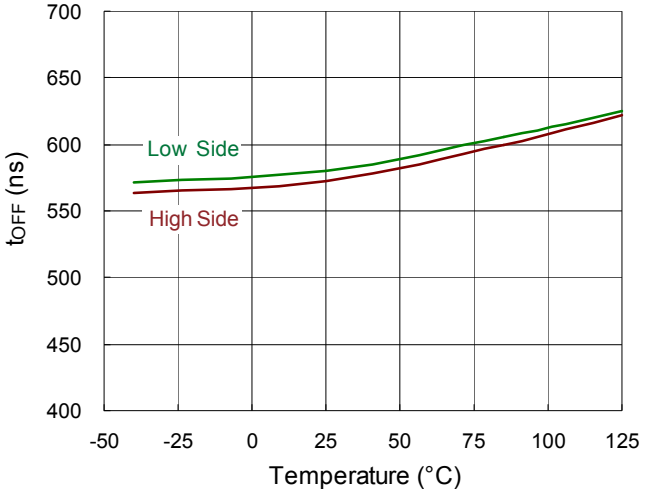
### High/Low Side Output Voltage vs. Temperature



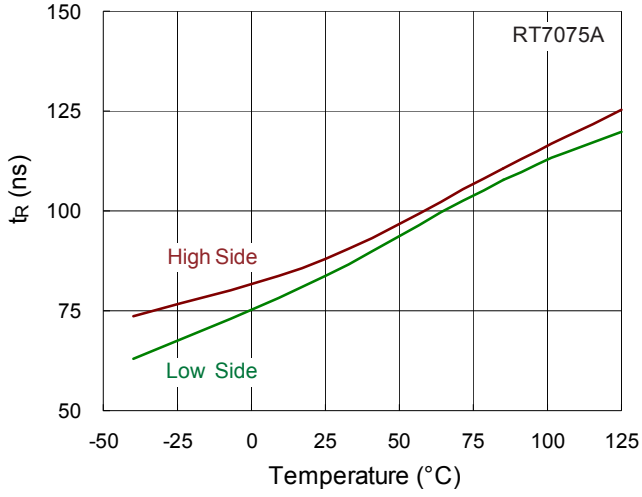

### Turn-on Propagation Delay vs. Temperature



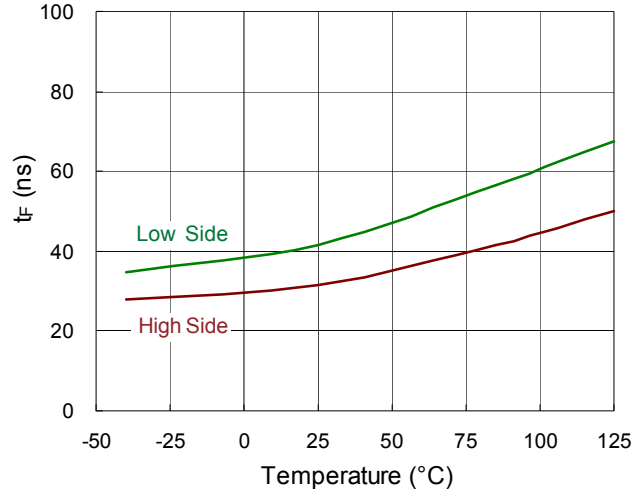

### Turn-off Propagation Delay vs. Temperature



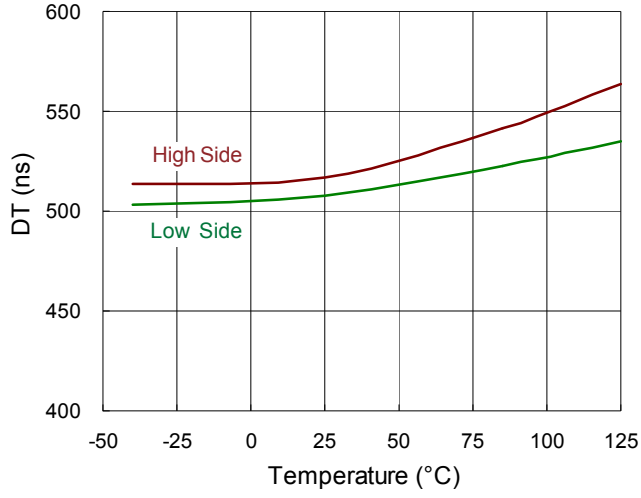

### Turn-on Rising Time vs. Temperature




### Turn-off Falling Time vs. Temperature




### Dead Time vs. Temperature

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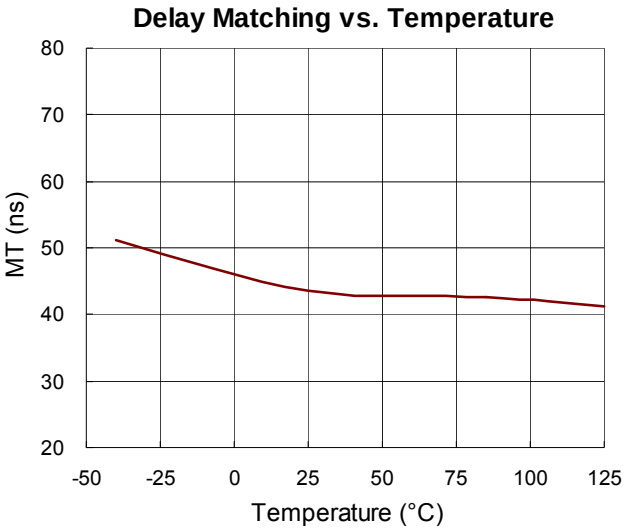


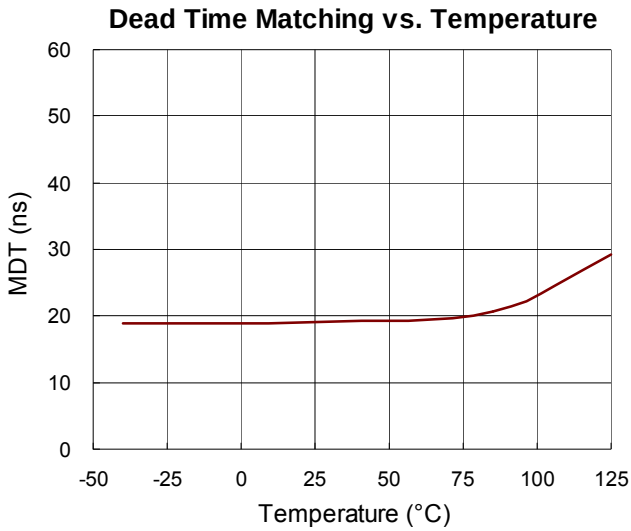


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## Application Information

### Dynamic Waveforms

Figure 1 is a definition of dynamic characteristics. You can know those definitions and the relationship between input and output from these figures. For example : $t_{ON}$ ,$t_{OFF}$, $t_R$, $t_F$, MT....

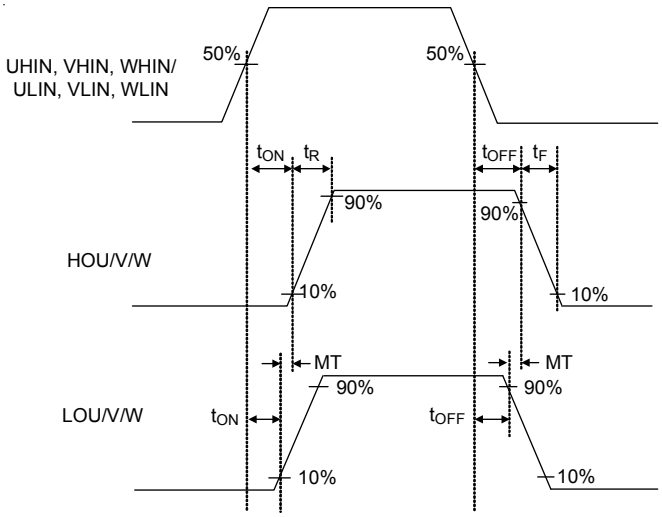


Figure 1. Dynamic Electrical Characteristics Definition

### Deadtime

To avoid the simultaneous conduction of high-side and low-side power switches cause shoot through, the switching operation of the IC control circuit introduces a deadtime function. In the deadtime period, even if the input sends another power switch conduction signal, the control circuit will remain closed drive state. Figure 2 illustrates the definition of deadtime (DT_H & DT_L) and the relationship between the high-side and low-side gate signals.

### Matched Propagation Delays

Because the IC internal level shifter circuit causes the propagation delay of the high-side output signal, the RT7075 add a propagation delay matching circuit in the low-side logic circuit, so that each high-side and low-side output signals ($t_{ON}$, $t_{OFF}$) approximately synchronization.

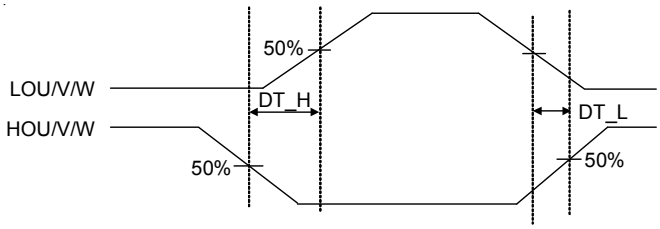


Figure 2. Deadtime Definition

### Shoot-Through Protection

The RT7075 have shoot through protection circuitry to avoid the simultaneous conduction of high-side and low-side power switches cause shoot through, as shown Figure 3.

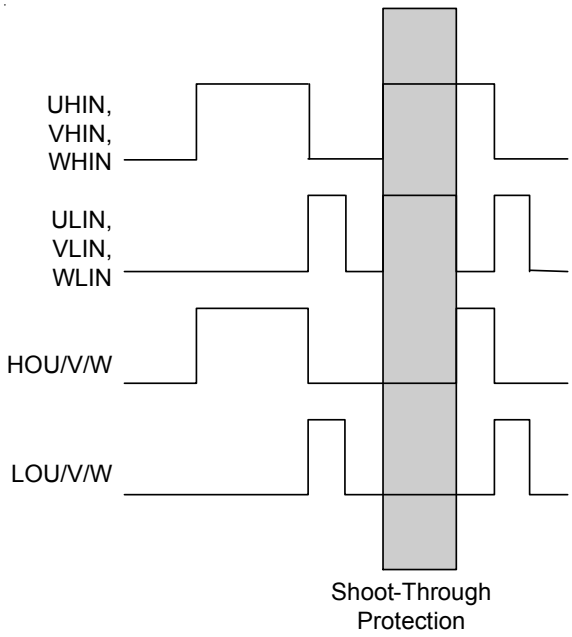


Figure 3. Shoot Through Protection

### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

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$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a LQFP-48L 7x7 package, the thermal resistance, $\theta_{JA}$, is 67°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (67°C/W) = 1.49W for a LQFP-48L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

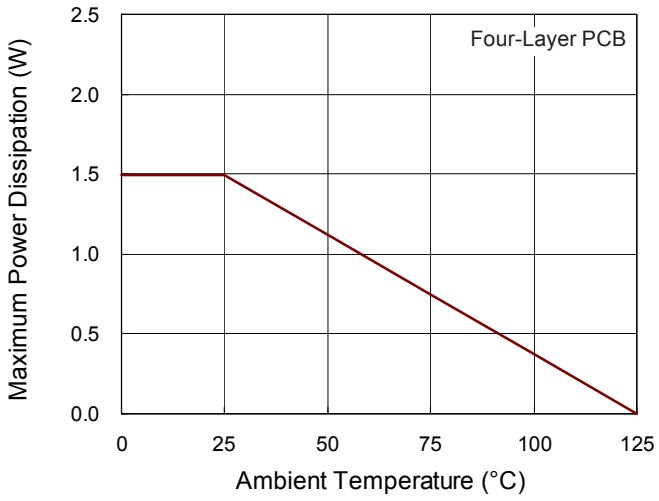


Figure 4. Derating Curve of Maximum Power Dissipation

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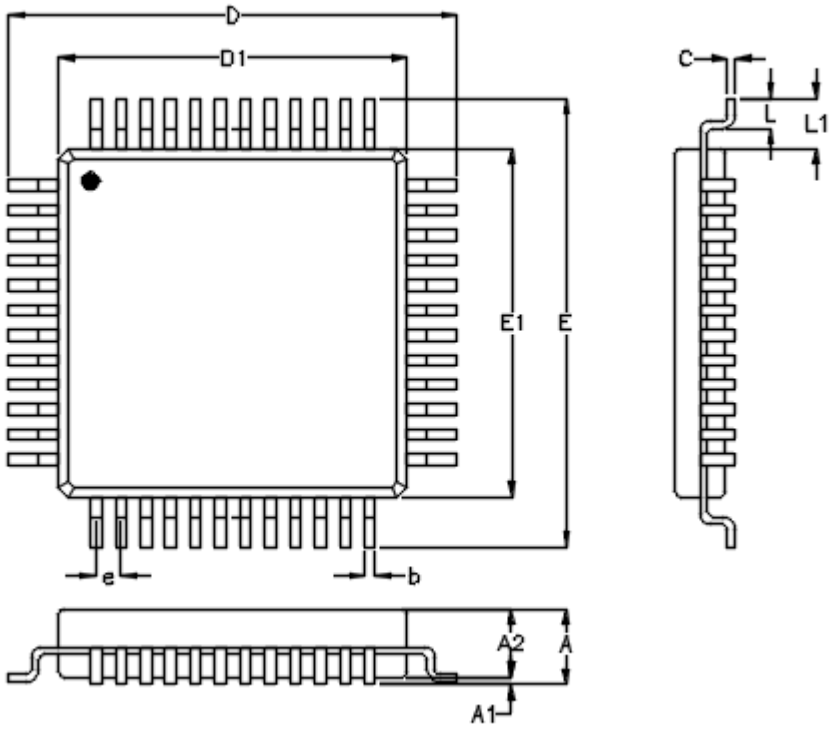
## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max. |
| A | 1.400 | 1.600 | 0.055 | 0.063 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 1.350 | 1.450 | 0.053 | 0.057 |
| b | 0.170 | 0.270 | 0.007 | 0.011 |
| C | 0.090 | 0.200 | 0.004 | 0.008 |
| D | 8.800 | 9.200 | 0.346 | 0.362 |
| E | 8.800 | 9.200 | 0.346 | 0.362 |
| D1 | 6.900 | 7.100 | 0.272 | 0.280 |
| E1 | 6.900 | 7.100 | 0.272 | 0.280 |
| e | 0.500 | | 0.020 | |
| L | 0.450 | 0.750 | 0.018 | 0.030 |
| L1 | 0.800 | 1.200 | 0.031 | 0.047 |

**L-Type 48-Lead QFP 7x7 Plastic Package**

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**Richtek Technology Corporation**

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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