Three-Phase PMSM/BLDC Motor Controller with Pre-Driver

General Description

The RT7079 is an application specific IC designed for PMSM/BLDC motor applications. This two-in-one ASIC integrates several functional circuits, namely a 3-phase motor controller, a 3-phase gate driver, three bootstrap diodes, a 5V LDO regulator and a buck converter.

The RT7079 embeds the ARM 32-bit Cortex-M0 core with peripheral circuits to perform the sensorless with field oriented control (FOC). In addition, several system level peripheral functions, such as ADC, DAC, communication interface, SVPWM, watchdog timer, current sensing, undervoltage-lockout (UVLO), short circuit protection (SCP) and locked-rotor protection are integrated so as to reduce component count, PCB size and system cost.

Furthermore, the RT7079 drives external N-Channel MOSFETs in three half-bridge configuration with a built-in bootstrap network up to 58V. A dead time control is built-in to prevent shoot-through of the external N-Channel MOSFETs.

The RT7079 is available in WQFN-48L 7x7 package.

Ordering Information

RT7079□□-□□□□□

- Programmed Firmware Code
- Package Type
  QW : WQFN-48L 7x7 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Integrated 3-Phase PMSM/BLDC Controller, Gate Driver, Bootstrap Diodes, 5V LDO Regulator and Buck Converter**
- **Input Voltage Range : 8V to 58V**
- **Sensorless, Sine-Wave Field Oriented Control (FOC)**
- **Protections : SCP, UVLO and Locked-Rotor Protection**
- **PMSM/BLDC Motor Controller**
  - **ARM 32-bit Cortex-M0 CPU, Frequency Up to 60MHz**
  - **Memories Size : 16kB MTP, Internal ROM with Embedded Motor Control Library and 4kB SRAM**
  - **Power Management : Normal or Deep Sleep**
  - **Communication Interface : I^2C and UART**
  - **10-Channel 10-Bit ADC**
  - **1-Channel Current Type 6-Bit DAC**
  - **1-Channel Voltage Type 8-Bit DAC**
- **Gate Driver**
  - **Floating Channel Designed for Bootstrap Operation**
  - **Sourcing/Sinking Current : 70mA/500mA**
- **WQFN-48L 7x7 Package**

Applications

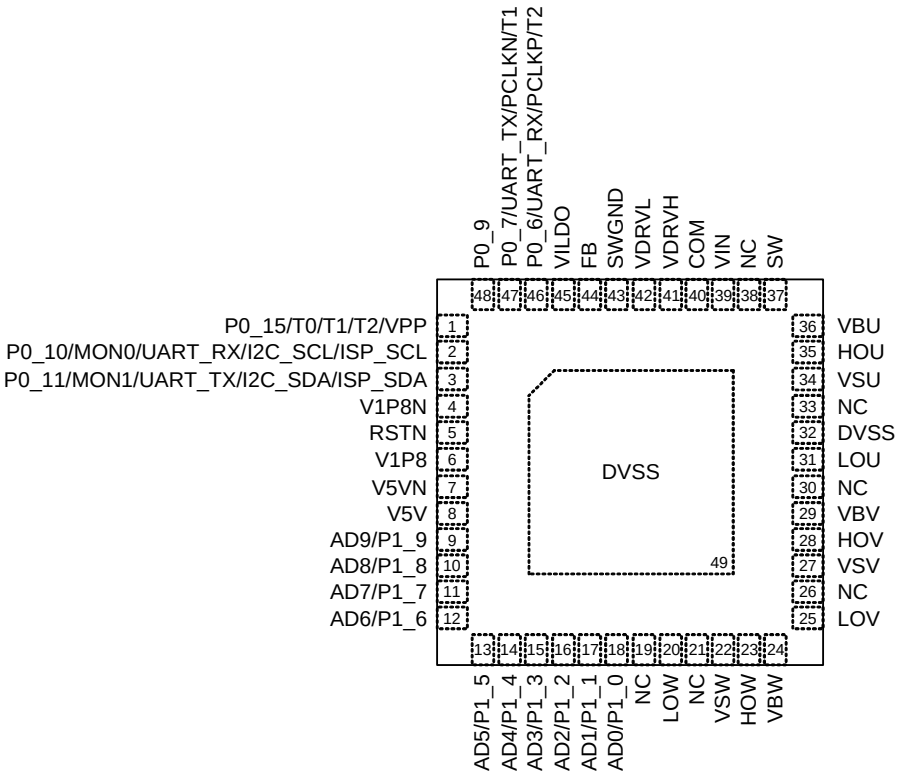
- Fan Applications : Exhaust Fan, Pedestal Fan, Ventilation Fan etc.
- Water Pump
- Vacuum Cleaner

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

(TOP VIEW)



WQFN-48L 7x7

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	P0_15	DIO	Pin 15 of GPIO port 0.
	T0	DI	T0 external enable or external clock input pin.
	T1	DI	T1 external enable or external clock input pin.
	T2	DI	T2 external enable or external clock input pin.
	VPP	P	8V input power for MTP fast programming.
2	P0_10	DIO	Pin 10 of GPIO port 0.
	MON0	DO	Internal digital signal monitoring output pin.
	UART_RX	DI	UART receiving pin.
	I2C_SCL	DIO	I^2C clock pin.
	ISP_SCL	DI	In system programming clock input pin.
3	P0_11	DIO	Pin 11 of GPIO port 0.
	MON1	DO	Internal digital signal monitoring output pin.
	UART_TX	DO	UART transmitting pin.
	I2C_SDA	DIO	I^2C data pin.
	ISP_SDA	DIO	In system programming data input pin.
4	V1P8N	GND	1.8V power pin negative terminal.
5	RSTN	DI	Low active reset pin.
6	V1P8	P	1.8V power pin.
7	V5VN	GND	5V power pin negative terminal.
8	V5V	P	5V power pin.
9	AD9	AI	ADC Channel 9 input pin.
	AD9	AO	Current type DAC output pin. (Sink type)
	P1_9	DIO	Pin 9 of GPIO port 1.
10	AD8	AI	ADC Channel 8 input pin.
	AD8	AO	Voltage type DAC output pin.
	P1_8	DIO	Pin 8 of GPIO port 1.
11	AD7	AIO	ADC Channel 7 input pin.
	P1_7	DIO	Pin 7 of GPIO port 1.
12	AD6	AIO	ADC Channel 6 input pin.
	P1_6	DIO	Pin 6 of GPIO port 1.
13	AD5	AIO	ADC Channel 5 input pin.
	P1_5	DIO	Pin 5 of GPIO port 1.
14	AD4	AIO	ADC Channel 4 input pin.
	P1_4	DIO	Pin 4 of GPIO port 1.

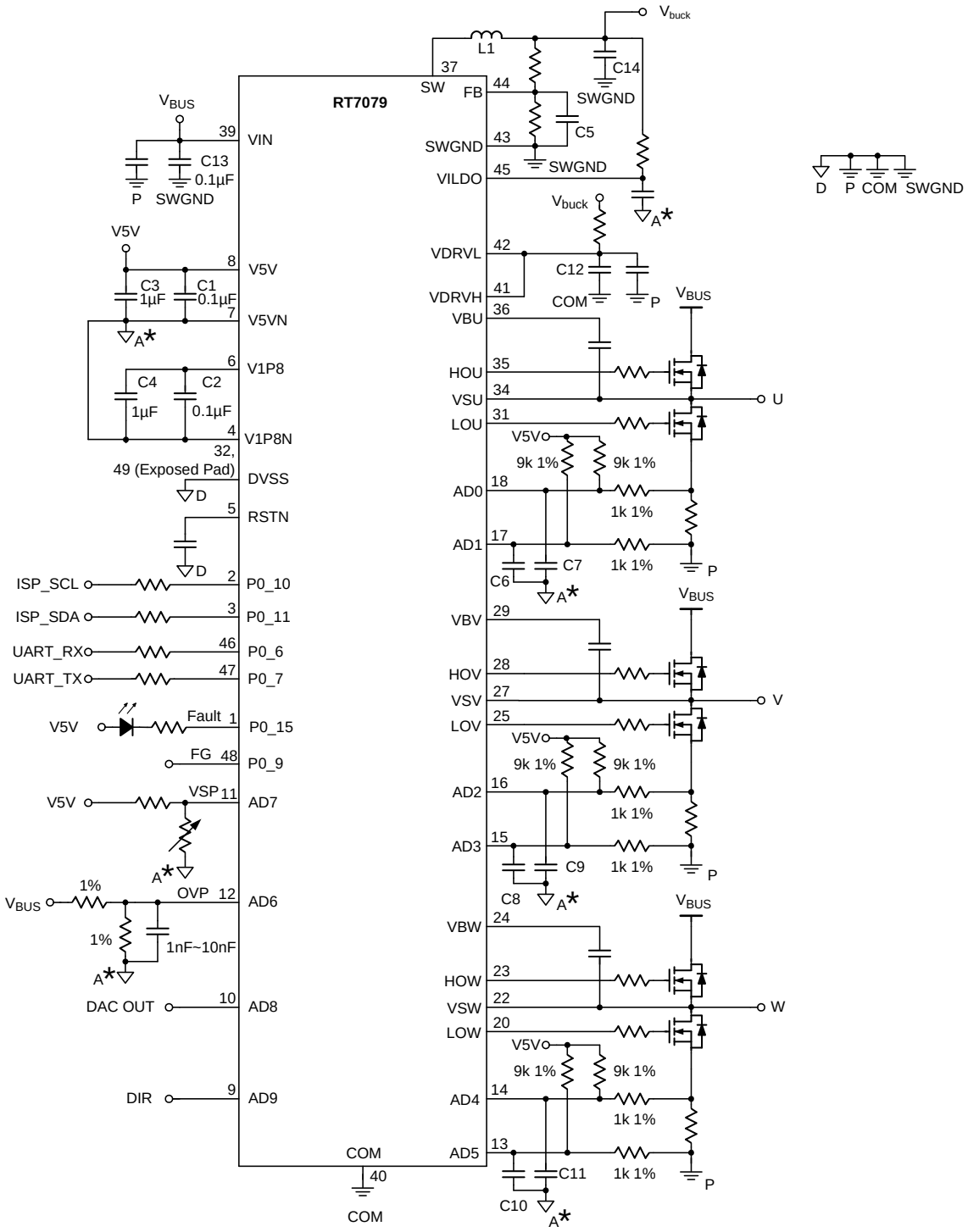
Pin No.	Pin Name	Type	Pin Function
15	AD3	AIO	ADC Channel 3 input pin.
	P1_3	DIO	Pin 3 of GPIO port 1.
16	AD2	AIO	ADC Channel 2 input pin.
	P1_2	DIO	Pin 2 of GPIO port 1.
17	AD1	AIO	ADC Channel 1 input pin.
	P1_1	DIO	Pin 1 of GPIO port 1.
18	AD0	AIO	ADC Channel 0 input pin.
	P1_0	DIO	Pin 0 of GPIO port 1.
19, 21, 26, 30, 33, 38	NC	--	No internal connection.
20	LOW	HVO	Low-side gate signal of Phase W.
22	VSW	HVI	High-side floating supply offset voltage of Phase W.
23	HOW	HVO	High-side gate signal of Phase W.
24	VBW	HVI	High-side floating supply voltage of Phase W.
25	LOV	HVO	Low-side gate signal of Phase V.
27	VSV	HVI	High-side floating supply offset voltage of Phase V.
28	HOV	HVO	High-side gate signal of Phase V.
29	VBV	HVI	High-side floating supply voltage of Phase V.
31	LOU	HVO	Low-side gate signal of Phase U.
32, 49 (Exposed Pad)	DVSS	GND	Digital ground.
34	VSU	HVI	High-side floating supply offset voltage of Phase U.
35	HOU	HVO	High-side gate signal of Phase U.
36	VBU	HVI	High-side floating supply voltage of Phase U.
37	SW	HVO	Switch node of Buck converter.
39	VIN	HVI	Input supply voltage.
40	COM	GND	Gate driver ground.
41	VDRVH	P	High-side driver supply voltage.
42	VDRVL	P	Low-side driver supply voltage.
43	SWGND	GND	Buck converter ground.
44	FB	AI	Feedback voltage input of Buck converter.
45	VILDO	P	5V LDO supply voltage.
46	P0_6	DIO	Pin 6 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	PCLKP	DO	Programmable clock positive output pin.
	T2	DI	T2 external enable or external clock input pin.

Pin No.	Pin Name	Type	Pin Function
47	P0_7	DIO	Pin 7 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	PCLKN	DO	Programmable clock negative output pin.
	T1	DI	T1 external enable or external clock input pin.
48	P0_9	DIO	Pin 9 of GPIO port 0.

IO Type Definition :
DIO : Digital input/output pin.
DI : Digital input pin.
DO : Digital output pin.
AIO : Analog input/output pin.
AI : Analog input pin.
AO : Analog output pin.
P : Power pin.
HVI : High voltage input pin.
HVO : High voltage output pin.

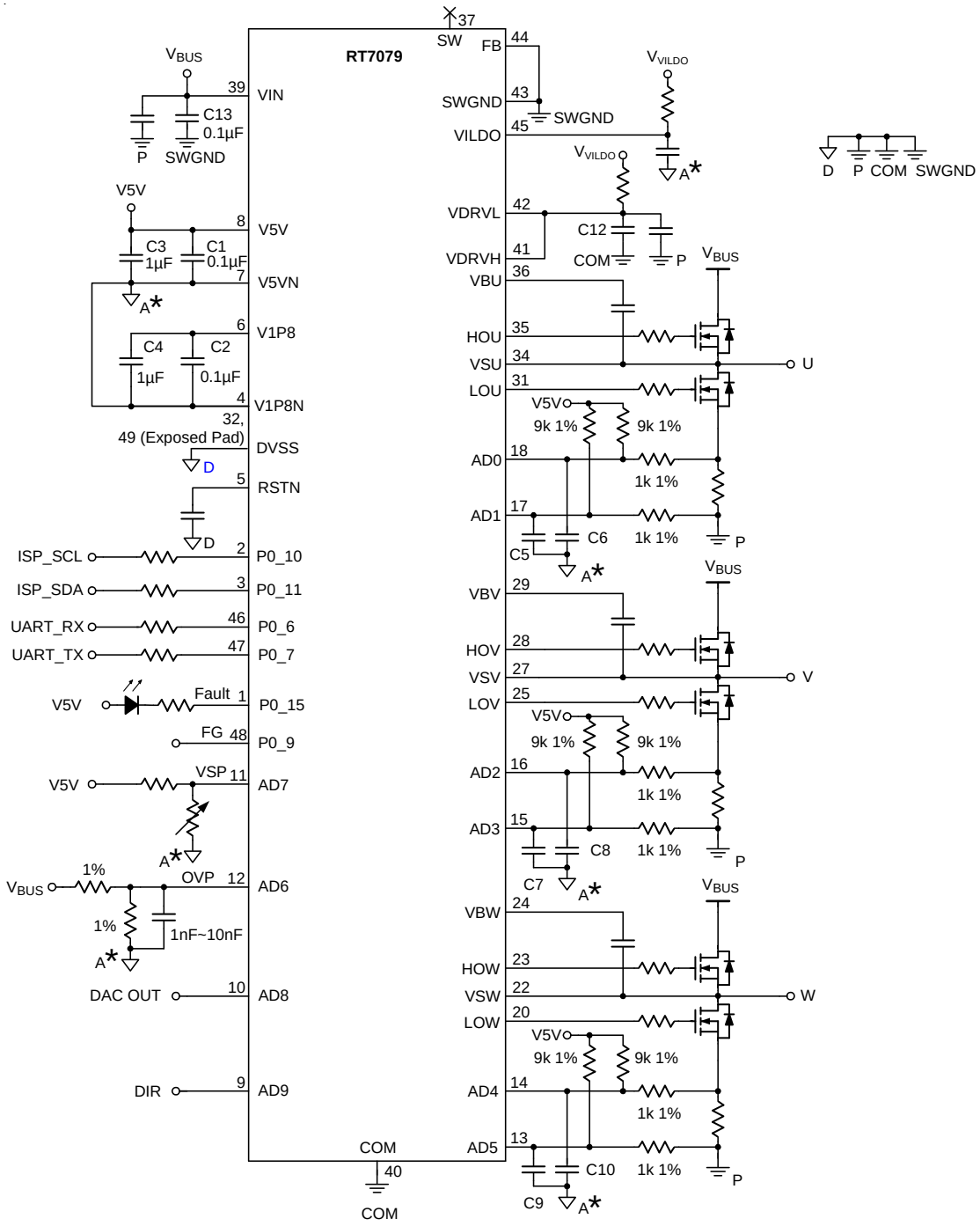
Typical Application Circuit

Application Circuit 1 (With buck converter)



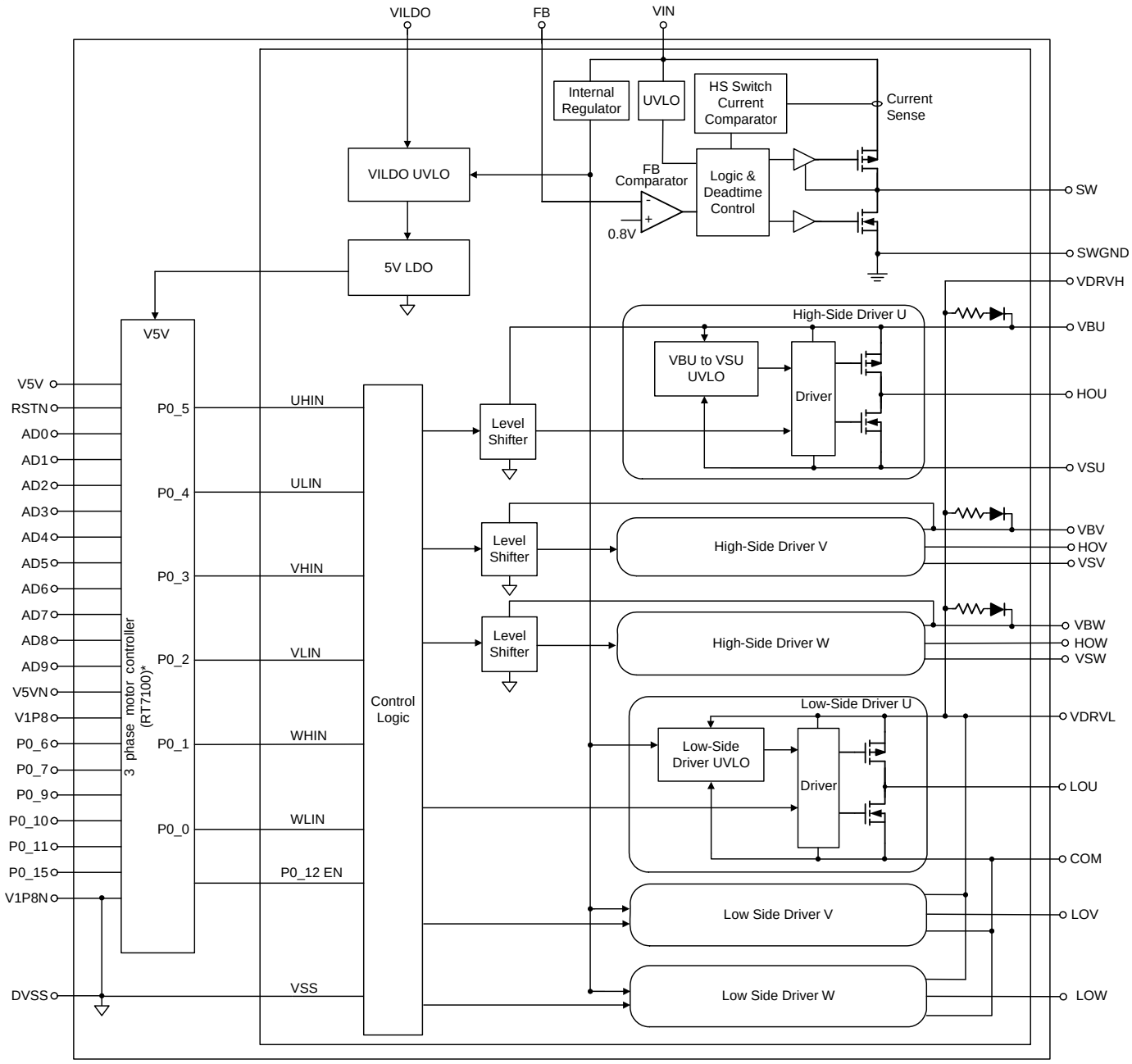
Note :
1. C1, C2, C3, C4, C5 and L1 should be as close as possible to the IC.
2. C12 should be as close as possible to the IC and COM.
3. C13 should be as close as possible to the IC and SWGND.
4. C14 should be as close as possible to the IC and SWGND.
5. C1 and C2 : Option. C1 and C2 are the decoupling capacitors.
6. C6 to C11 : Suggest value : 100pF to 1nF
7. L1 : The value of inductor should be determined by VIN. Please refer to Application Information
8. AGND is a separate loop, do not connect to DGND and PGND.

Application Circuit 2 (Without buck converter)



Note :
1. C1, C2, C3 and C4 should be as close as possible to the IC.
2. C12 should be as close as possible to the IC and COM.
3. C13 should be as close as possible to the IC and SWGND.
4. C1 and C2 : Option. C1 and C2 are the decoupling capacitors.
5. C5 to C10 : Suggest value : 100pF to 1nF
6. V_{VILDO} should be applied by external power.
7. AGND is a separate loop, do not connect to DGND and PGND.

Functional Block Diagram



* : Please refer to AN_RT7100_Introduction_TW for how to use RT7100.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V5V ---------- –0.3V to 6.5V
- Supply Input Voltage, VIN ---------- –0.3V to 60V
- VSU, VSV, VSW to COM ---------- –5V to 70V
- VBU, VBV, VBW to COM ---------- –0.3V to 70V
- LOU, LOV, LOW to COM ---------- –0.3V to 15V
- HOU/V/W to VSU/V/W ---------- –0.3V to 15V
- VDRVH/VDRVL ---------- 15V
- VILDO ---------- 15V
- VSU, VSV, VSW dv/dt ---------- 5V/ns
- Switch Voltage, SW ---------- –0.3V to 60V
- FB ---------- –0.3V to 6V
- Analog/Digital Input Voltage ---------- –0.2V to 5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-48L 7x7 ---------- 3.77W
- Package Thermal Resistance (Note 2)
  WQFN-48L 7x7, θ_{JA} ---------- 26.5°C/W
  WQFN-48L 7x7, θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V5V ---------- 4.5V to 5.5V
- Supply Input Voltage, VIN ---------- 8V to 58V
- VSU, VSV, VSW to COM ---------- –3V to 58V
- VDRVH/VDRVL ---------- 7V to 10V
- VILDO ---------- 7V to 12V
- Input Voltage for MTP Fast Programming, V_{VPP} ---------- 8V to 8.2V
- Minimum Time Period of RSTN, t_{RSTN} ---------- 100µs
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(V_{V5V} = 5V, V_{VIN} = 24V, VDRVH/L = 7V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Section						
System Frequency	f_{SCLK}		58.8	60	61.2	MHz
Slow Clock for Sleep Mode	f_{LCLK}		77.6	80	82.4	kHz
ADC Section (0 to 4V, 10-bit, Single End Mode, Gain = 1) (Note 5)						
ADC Input Voltage Range	V_{ADCIN}		0	--	4	V
VDAC Section (0V to 4V, 8-bit for Short and Over-Current) (Note 5)						
Minimum Conversion Voltage	V_{O_MIN}		--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}		--	4	--	V
DAC Offset	V_{OFFSET}		--	2	--	LSB
Output Resistance of DAC	R_O	(Note 7)	--	5k	--	Ω
VDAC Section (0V to 3V, 8-bit for General Purposed Comparator) (Note 5)						
Minimum Conversion Voltage	V_{O_MIN}		--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}		--	3	--	V
DAC Offset	V_{OFFSET}		--	2	--	LSB
Output Resistance of DAC	R_O	(Note 7)	--	5k	--	Ω
IDAC Section (0 to 126μA, 6-Bit for Current Sink) (Note 5)						
IDAC Output Bias Voltage Range	Vibias		0.2	--	5	V
Minimum Sink Current	I_{O_MIN}	Vibias = 2.5V	--	0	--	μA
Maximum Sink Current	I_{O_MAX}	Vibias = 2.5V	--	126	--	μA
Average Current Step	I_{LSB}	Test : (Ii_min-Ii_max) / (256-1)	--	2	--	μA
DAC Offset	I_{OFFSET}		--	0	--	μA
Current Limit Comparator Section (Short and Over-Current)						
Comparator Offset	V_{OFFSET}	(Note 6)	–10	0	10	mV
Input Voltage Range of Comparator	V_{IN}	(Note 7)	1	--	4	V
Over-Current Level Range	V_{OC}	(Note 7)	0.5	--	4	V
General Purposed Comparator (Note 6)						
Comparator Offset	V_{OFFSET}		–5	0	5	mV
Input Voltage Range of Comparator	V_{IN}		0	--	3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IO of P0_6 to P0_7 Section						
Input High Voltage	V_{IH}		--	--	0.7 x V5V	V
Input low Voltage	V_{IL}		0.3 x V5V	--	--	V
Pull-Down Resistor	R_{DOWN}		--	90	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_9 to P0_11 Section						
Input High Voltage	V_{IH}		--	--	0.7 x V5V	V
Input Low Voltage	V_{IL}		0.3 x V5V	--	--	V
Pull-Up Resistor	R_{UP}		--	70	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of AD0 to AD9 Section and P0_15						
Input High Voltage	V_{IH}		--	--	2.7	V
Input Low Voltage	V_{IL}		0.6	--	--	V
Current Source for External Bias	I_{BIAS1}	AD0 to AD2	97	100	103	μA
Current Source for External Bias	I_{BIAS2}	AD3 to AD9	--	50	--	μA
Low Level Output Current	I_{OL}	AD0 to AD9	--	2	--	mA
RSTN Pin Pull-Up Resistor	R_{UP}		--	10	--	kΩ
Power Supply Section						
VIN Quiescent Current	I_{VIN_Q}	In the sleep mode and disable gate driver	--	1.5	--	mA
VIN Operating Current	I_{VIN_OP}		--	23	28	mA
V5V Under-Voltage Lockout Threshold (On)	V_{V5V_UVLON}		--	4.15	--	V
V5V Under-Voltage Lockout Threshold (Off)	V_{V5V_UVLOFF}		--	3.85	--	V
LDO Output for Internal Operation Voltage	V_{V1P8}	Full speed operation w/i external 20mA sink, $C_{V1P8} \geq 1\mu F$	--	1.8	--	V
V5V Current at Operation Mode	I_{V5V_OPER}	Typical sensor-less motor control library	--	23	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Buck Converter						
VIN Under-Voltage Lockout Threshold (On)	V_{IN_UVLON}		5.9	6.4	6.9	V
VIN Under-Voltage Lockout Threshold (Off)	V_{IN_UVLOFF}		5.6	6.1	6.6	V
Rdson (High-Side)	$R_{DS(ON)\_H}$		--	3.25	--	Ω
Rdson (Low-Side)	$R_{DS(ON)\_L}$		--	3	--	Ω
FB UVP for Over Load or SC	V_{FB_UVP}	Latch function, no switching	--	0.45	--	V
UVP Blanking Time	t_{BLK}		--	27	--	ms
High-Side Peak Current Limit	I_{PK_H}	V_{IN} < 21V, V_{FB} = 0.6V	--	225	--	mA
		$V_{IN} \geq$ 23V, V_{FB} = 0.6V	--	120	--	
Feedback Comparator Trip Voltage	V_{FB}		0.76	0.8	0.84	V
Feedback Comparator Hysteresis	V_{FB_HYS}		--	5	--	mV
High-Side and Low-Side Driver Section						
High-Side Under-Voltage Lockout Threshold (On)	V_{HS_UVLON}		2.9	--	3.5	V
High-Side Under-Voltage Lockout Threshold (OFF)	V_{HS_UVLOFF}		2.7	--	3.3	V
Low-Side Under-Voltage Lockout Threshold (On)	V_{LS_UVLON}		4	--	4.5	V
Low-Side Under-Voltage Lockout Threshold (OFF)	V_{LS_UVLOFF}		3.8	--	4.3	V
VDRVH/VDRVL Operating Current	I_{VDRV_OP}	fs = 20kHz (no load)	--	--	1	mA
VBSx Quiescent Current	I_{BSX_Q}	HOU/V/W = 0, 3-channels	--	400	--	μA
Bootstrap Diode Forward Voltage	V_{F_BOOT}	Id = 5mA	--	0.8	--	V
		Id = 0.1A	--	2.9	--	
High-Side / Low-Side Output Voltage	V_{OH}	I_O = 0mA, $V_{VBU/V/W}$ - $V_{HOU/V/W}$, V_{VDRVL} - $V_{LOU/V/W}$	--	50	200	mV
	V_{OL}	I_O = 0mA, $V_{HOU/V/W}$ - $V_{VSU/V/W}$, $V_{LOU/V/W}$ - V_{COM}	--	20	100	
HOU/V/W and LOU/V/W Sourcing Current	I_{O+}	Gate driver output high, VBS = 7V, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = 0V	--	70	--	mA
HOU/V/W and LOU/V/W Sinking Current	I_{O-}	Gate driver output low, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = 7V	--	500	--	mA
Turn-On Propagation Delay	t_{ON}		50	--	250	ns
Turn-Off Propagation Delay	t_{OFF}		50	--	250	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay Matching	MT		--	--	150	ns
5V LDO Section						
VILDO Under-Voltage Lockout Threshold (On)	V_{ILDO_UVLON}		5.1	5.6	6.1	V
VILDO Under-Voltage Lockout Threshold (OFF)	V_{ILDO_UVLOFF}		4.6	5.1	5.6	V
Output Short Current	I_{SC}		60	--	--	mA
Output Voltage (V5V)	V_{V5V}	V_{VILDO} = 7V, I_{LOAD} = 0 to 30mA	4.85	5	5.15	V

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Characterized, not tested at manufacturing.

Note 6. For comparator only.

Note 7. This parameter is guaranteed by design.

Application Information

Buck Description

The RT7079 includes a step-down voltage regulator performing as a high-efficiency, synchronous step-down DC-DC converter and driving up to 60mA output current within the input range of 8V to 58V. This Buck converter achieves the Hysteresis Mode control by adopting the Boundary Conduction Mode (BCM) with the features of low quiescent current and high-side peak current limit.

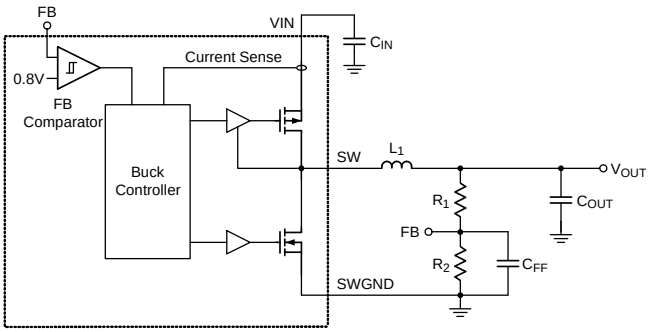


Figure 1. Buck Regulator

Table 1. Recommended Value for Buck Regulator

V_{OUT} (V)	7.3
C_{OUT} (μF)	4.7
R_1 (kΩ)	220
R_2 (kΩ)	27
C_{FF} (pF)	47

Output Voltage Setting and Feedback Network

The resistive divider allows the FB pin to sense the output voltage. Thus the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where V_{REF} is the reference voltage (0.8V typ.).

The saturation current of inductor must be chosen to be greater than 400mA, in which the propogation delay will increase the peak current limit.

Respective to the input voltage, the inductor value should be chosen as follows :

Table 2. Inductor Selection

$V_{IN(MAX)}$ (V)	Under 30V	Over 30V
L (μH)	10	22
I_{sat} (mA)	> 400mA	

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-48L 7x7 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)} = (125°C - 25°C) / (26.5°C/W) = 3.77W$

for a WQFN-48L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves shown in Figure 2 allows the designer to evaluate the effect of rising ambient temperature on the maximum power dissipation.

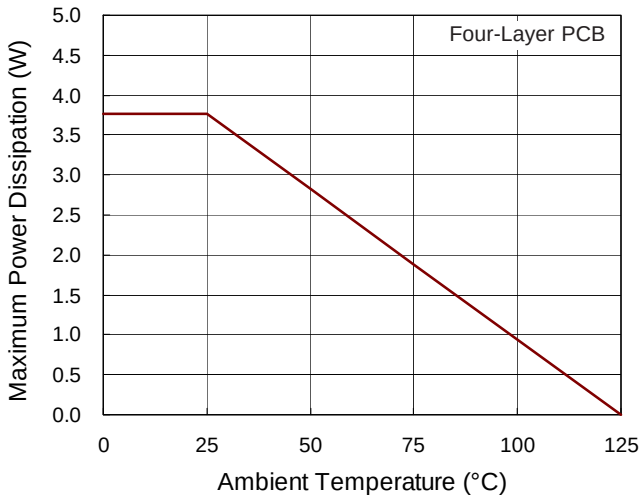
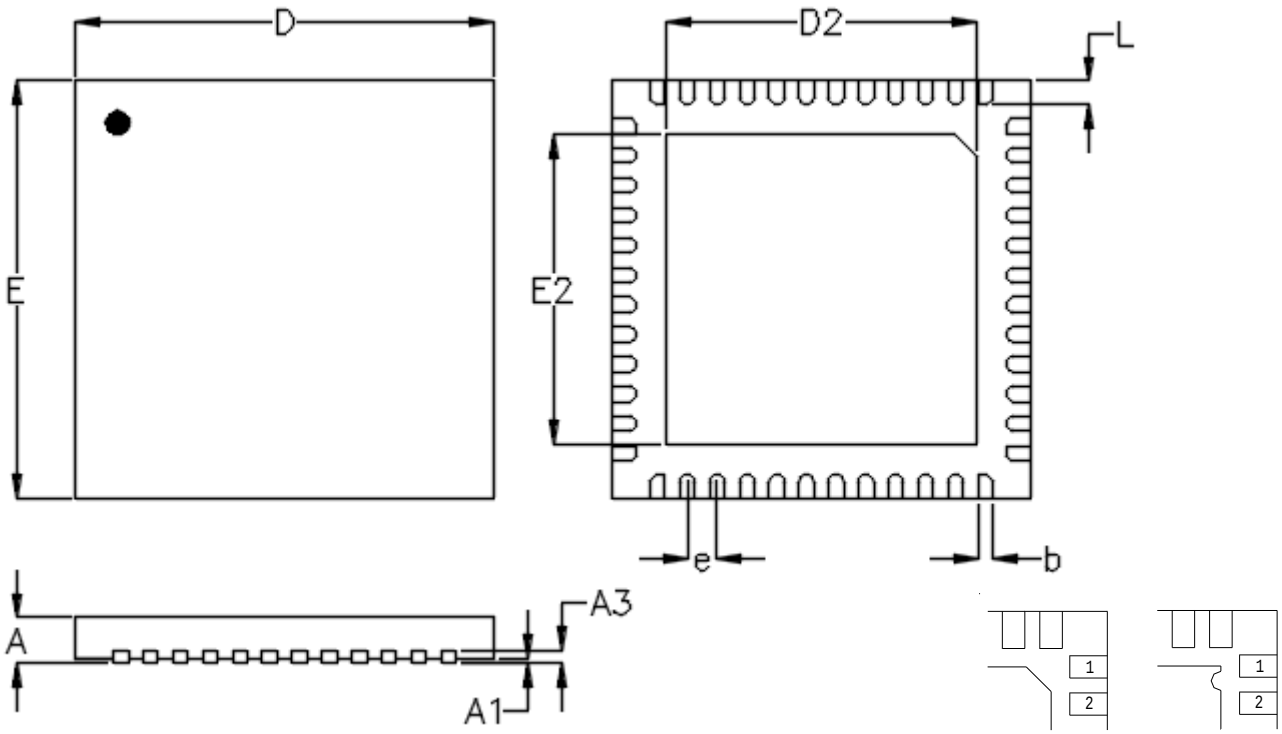


Figure 2. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

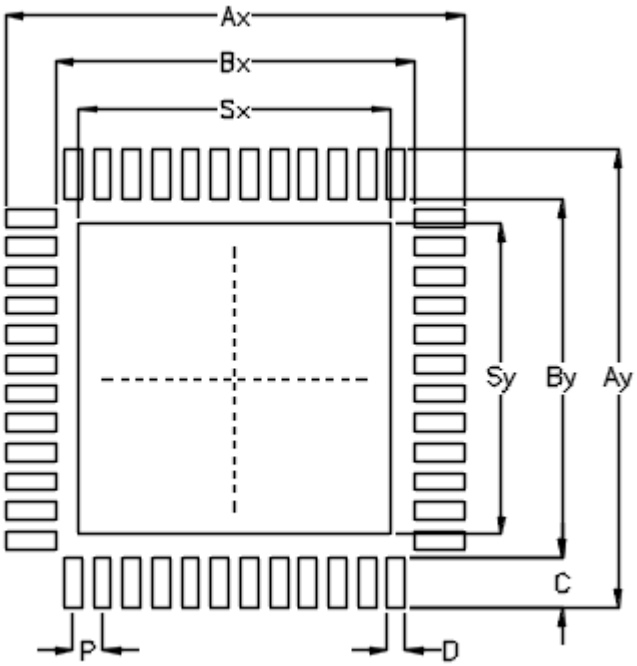
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		6.950	7.050	0.274	0.278
D2	Option1	5.050	5.250	0.199	0.207
	Option2	5.600	5.700	0.220	0.224
E		6.950	7.050	0.274	0.278
E2	Option1	5.050	5.250	0.199	0.207
	Option2	5.600	5.700	0.220	0.224
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 48L QFN 7x7 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7*7-48	Option1	48	0.50	7.80	7.80	6.10	6.10	0.85	0.30	5.30	5.30	±0.05
	Option2									5.65	5.65	

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789