A High Integrated 3 Phase PMSM/BLDC Motor Controller with Gate Driver, Bootstrap Diodes and LDO

General Description

The RT7081 is a two–in-one application specific IC which consists of a 3 phase motor controller, a gate driver, three bootstrap diodes, a 5V LDO regulator and RC filters for current sense.

The RT7081 integrates the ARM 32-bit Cortex-M0 core with peripheral circuits to perform field oriented control (FOC) and sensor-less motor control. In additions, system level peripheral functions, such as ADC, DAC, communication interface, SVPWM, watchdog timer, current sensing, under voltage-lockout (UVLO), short circuit protection (SCP), thermal detection and locked-rotor protection are integrated so as to reduce component count, PCB size and total BOM cost.

Furthermore, the RT7081 drives external N-Channel MOSFETs or IGBTs in a half-bridge configuration with a building bootstrap network up to 600V. A dead time control is built-in to prevent shoot-through of the external N-Channel MOSFETs.

The RT7081 is available in a WQFN-37L 7x7 package.

Ordering Information

RT7081□□-□□□□□

- Programmed Firmware Code
- Package Type
  QW : WQFN-37L 7x7 (W-Type)
- Lead Plating System
  G : Green
  (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Integrated 3 Phase PMSM/BLDC Controller, Gate Driver, Bootstrap Diodes and 5V LDO Regulator**
- **Integrated Filters at ADC Input**
- **Sensor-Less, Sine-Wave Field Oriented Control (FOC)**
- **Protections : Over-Current, UVLO, Locked-Rotor and Thermal Detection**
- **PMSM/BLDC Motor Controller :**
  - **ARM 32-bit Cortex-M0 CPU, Up to 60MHz**
  - **Memories Size : 16kB MTP, Internal ROM with Embedded Motor Control Library and 4kB SRAM**
  - **Power Management : Normal or Deep Sleep**
  - **Communication Interface : I^2C and UART**
  - **Support Two-Wire programming**
  - **10-Channel 10-bit ADC**
  - **1-Channel Voltage Type 8-bit DAC**
- **Gate Driver :**
  - **Floating Channel Designed for Bootstrap Operation up to 600V**
  - **Sourcing/Sinking Current: 300mA/600mA**
  - **Built in UVLO Functions for All Channels**
  - **Matched Propagation Delays for All Channels**
  - **Shoot Through Prevention**
  - **WQFN-37L 7x7 Package**

Applications

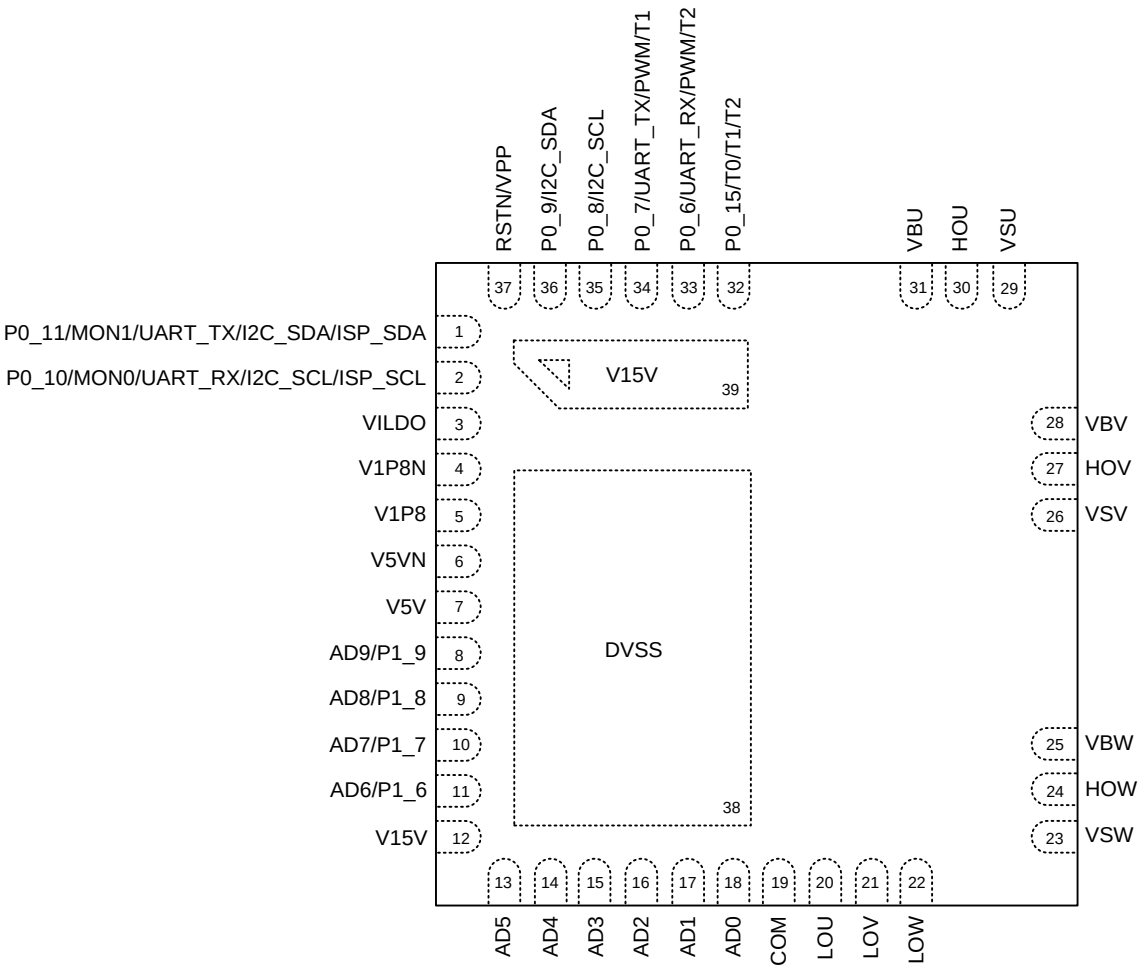
- PMSM/BLDC Motor
- Pedestal Fan
- Ceiling Fan
- Air Conditioner Indoor/Outdoor Fan
- Pump

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

(TOP VIEW)



WQFN-37L 7x7

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	P0_11	DIO	Pin 11 of GPIO port 0.
	MON1	DO	Internal digital signal monitoring output pin.
	UART_TX	DO	UART transmitting pin.
	I2C_SDA	DIO	I^2C data pin.
	ISP_SDA	DIO	In system programming data input pin.
2	P0_10	DIO	Pin 10 of GPIO port 0.
	MON0	DO	Internal digital signal monitoring output pin.
	UART_RX	DI	UART receiving pin.
	I2C_SCL	DI	I^2C clock pin.
	ISP_SCL	DI	In system programming clock input pin.
3	VILDO	P	5V LDO supply voltage.
4	V1P8N	GND	Digital ground.
5	V1P8	P	1.8V power pin.
6	V5VN	GND	Analog ground.
7	V5V	P	5V power pin.
8	AD9	AIO	ADC channel 9 input pin.
	P1_9	DIO	Pin 9 of GPIO port 1.
9	AD8	AIO	ADC channel 8 input pin. Voltage type DAC output pin.
	P1_8	DIO	Pin 8 of GPIO port 1.
10	AD7	AIO	ADC channel 7 input pin.
	P1_7	DI	Pin 7 of GPIO port 1.
11	AD6	AIO	ADC channel 6 input pin.
	P1_6	DI	Pin 6 of GPIO port 1.
12, 39 (Exposed Pad)	V15V	P	15V power pin.
13	AD5	AIO	ADC channel 5 input pin.
14	AD4	AIO	ADC channel 4 input pin.
15	AD3	AIO	ADC channel 3 input pin.
16	AD2	AIO	ADC channel 2 input pin.
17	AD1	AIO	ADC channel 1 input pin.
18	AD0	AIO	ADC channel 0 input pin.
19	COM	GND	Gate driver power ground.
20	LOU	HVO	Low-side gate control signal of phase A.
21	LOV	HVO	Low-side gate control signal of phase B.
22	LOW	HVO	Low-side gate control signal of phase C.
23	VSW	HVI	High-side floating supply offset voltage of phase C.
24	HOW	HVO	High-side gate control signal of phase C.

Pin No.	Pin Name	I/O	Pin Function
25	VBW	HVI	High-side floating supply voltage of phase C.
26	VSV	HVI	High-side floating supply offset voltage of phase B.
27	HOV	HVO	High-side gate control signal of phase B.
28	VBV	HVI	High-side floating supply voltage of phase B.
29	VSU	HVI	High-side floating supply offset voltage of phase A.
30	HOU	HVO	High-side gate control signal of phase A.
31	VBU	HVI	High-side floating supply voltage of phase A.
32	P0_15	DIO	Pin 15 of GPIO port 0.
	T0	DI	T0 external enable or external clock input pin.
	T1	DI	T1 external enable or external clock input pin.
	T2	DI	T2 external enable or external clock input pin.
33	P0_6	DIO	Pin 6 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	PWM	DO	Programmable PWMA output pin.
	T2	DI	T2 external enable or external clock input pin.
34	P0_7	DIO	Pin 7 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	PWM	DO	Programmable PWMB output pin.
	T1	DI	T1 external enable or external clock input pin.
35	P0_8	DIO	Pin 8 of GPIO port 0.
	I2C_SCL	DIO	I^2C clock pin.
	T0	DI	T0 external enable or external clock input pin.
36	P0_9	DIO	Pin 9 of GPIO port 0.
	I2C_SDA	DIO	I^2C data pin.
37	RSTN	DI	Pad reset pin.
	VPP	P	8V input power for MTP fast programming.
38 (Exposed Pad)	DVSS	GND	Digital ground.

IO Type Definition :

DIO : Digital input/output pin.

DI : Digital input pin.

DO : Digital output pin.

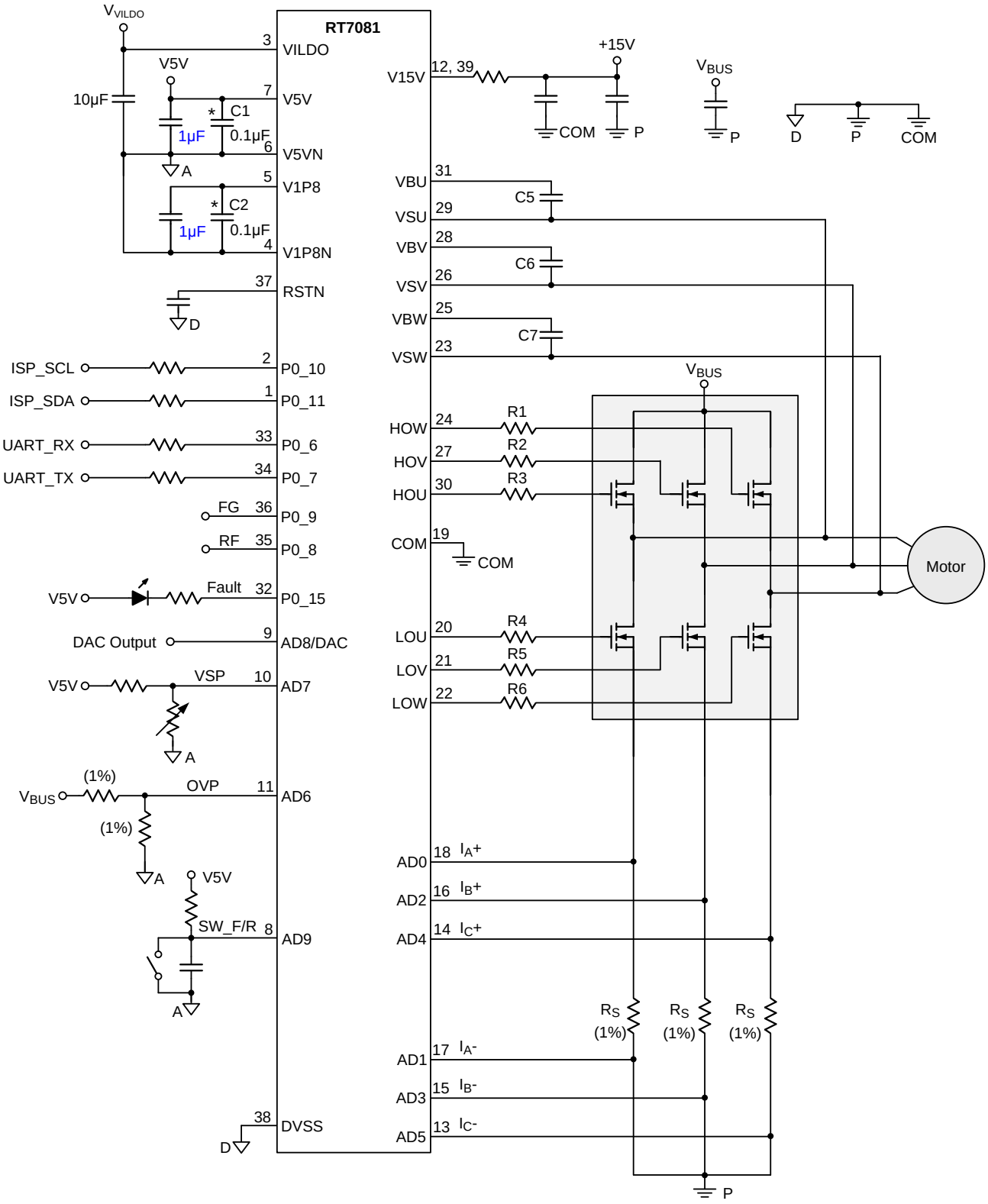
AIO : Analog input/output pin.

P : Power pin.

HVI : High voltage input pin.

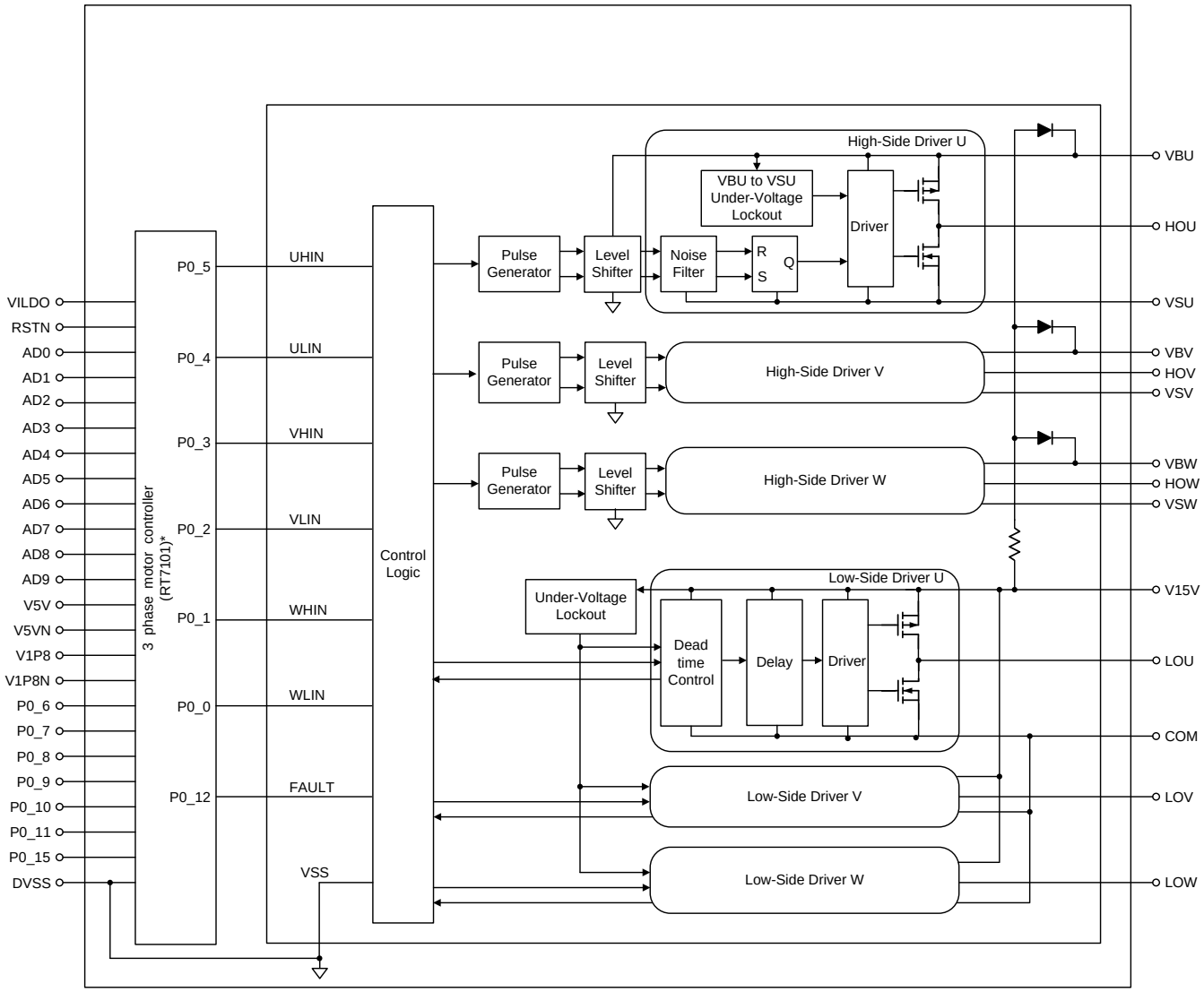
HVO : High voltage output pin.

Typical Application Circuit



Note :
1. C1 and C2 as close as possible to the IC.
2. * : Option

Functional Block Diagram



* : Please refer to the RT7101 data sheet.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V15V ---------- –0.3V to 25V
- Supply Input Voltage, VILDO ---------- –0.3V to 25V
- Supply Input Voltage, V5V ---------- –0.3V to 6.5V
- VSU/V/W to DVSS ---------- –5V to 600V
- VBU/V/W to VSU/V/W, VBU/V/W ---------- –0.3V to 25V
- HOU/V/W to VSU/V/W ---------- –0.3V to 25V
- LOU/V/W to DVSS ---------- –0.3V to 25V
- Voltage of I/O Pin (P0_0 to P0_9) ---------- –0.2V to 6.5V
- Voltage of I/O Pin (P0_10/P0_11/P0_15) ---------- –0.2V to 20V
- Voltage of I/O Pin (RSTN) ---------- –0.2V to 9V
- Analog Input Voltage (AD0 to AD5) ---------- –0.2V to 11V
- Analog Input Voltage (AD6/AD7) ---------- –0.2V to 20V
- Analog Input Voltage (AD8/AD9) ---------- –0.2V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-37L 7x7 ---------- 3.81W
- Package Thermal Resistance (Note 2)

  WQFN-37L 7x7, θ_{JA} ---------- 26.2°C/W

  WQFN-37L 7x7, θ_{JC} ---------- 4.7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model)

  Except HV Pin ---------- 200V

  HV (VBU/HOU/VSU, VBV/HOV/VSV, VBW/HOW/VSW) to GND ---------- 1kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V15V ---------- 13V to 20V
- Supply Input Voltage, VILDO ---------- 13V to 20V
- VBU/V/W to VSU/V/W, VBSx ---------- 0V to 20V
- VSU/V/W to DVSS ---------- 0V to 600V
- HOU/V/W to VSU/V/W ---------- 0V to VBSx
- LOU/V/W to DVSS ---------- 0V to V15V
- Supply Input Voltage, V5V ---------- 4.5V to 5.5V
- LDO Capacitor on V1P8 ---------- 1µF
- Minimum Time Period of RSTN, t_{RSTN} ---------- 100µs
- Ambient Temperature Range ---------- –40°C to 105°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V15V = VBU/V/W - VSU/V/W = 15V, V5V = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Section						
System Frequency	f_{SCLK}		--	60	--	MHz
Slow Clock for Sleep Mode	f_{LCLK}		--	80	--	kHz
Power Management Section						
Turn-On Voltage of V5V	V_{V5V_ON}		--	4.2	--	V
V5V On-Off Hysteresis	V_{V5V_HYS}	Turn-off voltage = V_{V5V_ON} - V_{V5V_hys}	--	0.4	--	V
LDO Output for Internal Operation Voltage	V_{V1P8}	Full speed operation w/i external 20mA sink, $C_{V1P8} \geq 1\mu F$	--	1.8	--	V
V5V Current at Operation Mode	I_{V5V_OPER}	20kHz PWM output, room temp, 25°C	--	30	--	mA
V5V Current at Normal Sleep Mode	I_{V5V_NSLP}	Room temp, 25°C	--	7	--	mA
V5V Current at Deep Sleep Mode	I_{V5V_DSLP}	Room temp, 25°C	--	750	--	μA
Turn-On Voltage of LDO	V_{VILDO_ON}		--	4.2	-	V
LDO On-Off Hysteresis	V_{VILDO_HYS}		--	0.4	--	V
LDO Current Limit	I_{VILDO_OC}		60	--	100	mA
ADC Section (0V to 3V, 10-Bit, Single End Mode, Gain = 1) (Note 5)						
Minimum Conversion Voltage	V_{I_MIN}	Code 000h	--	0	--	V
Maximum Conversion Voltage	V_{I_MAX}	Code 3FFh	--	3	--	V
CSUMDAC Section (0V to 0.6V, 8-Bit for Current Sum) (Note 5)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	0.6	--	V
DAC Offset	V_{OFFSET}	4LSB	--	4	--	LSB
SCDAC Section (0V to 1.2V, 8-Bit for Short Current) (Note 5)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	1.2	--	V
DAC Offset	V_{OFFSET}		--	4	--	LSB
VDAC Section (0V to 3V, 8-Bit for General Purposed Comparator) (Note 5)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	3	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DAC Offset	V_{OFFSET}		--	4	--	LSB
Output Resistance of DAC	R_O	(Note 7)	--	5	--	kΩ
Current Limit Comparator Section (Current Sum)						
Input Voltage Range of Comparator	V_{IN}		0	--	0.6	V
Comparator Offset	V_{OFFSET}	V_{OFFSET} = Comparator offset + Level shift matching + DAC (Note 6)	–20	0	20	mV
Current Limit Comparator Section (Short Circuit)						
Input Voltage Range of Comparator	V_{IN}		1	--	1.2	V
Comparator Offset	V_{OFFSET}	V_{OFFSET} = Comparator offset + Level shift matching + DAC (Note 6)	–20	0	20	mV
General Purposed Comparator						
Input Voltage Range of Comparator	V_{IN}		0.5	--	3	V
Comparator Offset	V_{OFFSET}	Include buffer (Note 6)	–20	0	20	mV
IO of P0_6 to P0_7 Section						
Positive Going Threshold Voltage	V_{IH}		--	2.85	--	V
Negative Going Threshold Voltage	V_{IL}		--	1.9	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	0.95	--	V
Pull-Down Resistor	R_{DOWN}		--	100	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_8 to P0_9 section						
Input High Voltage	V_{IH}		--	2.85	--	V
Input Low Voltage	V_{IL}		--	1.9	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	0.95	--	V
Pull-Up Resistor	R_{UP}		--	76	--	kΩ
Pull-Down Resistor	R_{DOWN}		--	40	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_10 to P0_11 section						
Input High Voltage	V_{IH}		--	2.85	--	V
Input Low Voltage	V_{IL}		--	1.9	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	0.95	--	V
Pull-Up Resistor	R_{UP}		--	76	--	kΩ
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IO of P0_15 (Open Drain)						
Input High Voltage	V_{IH}		--	2.3	--	V
Input Low Voltage	V_{IL}		--	0.8	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	1.5	--	V
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of RSTN/VPP						
Input High Voltage	V_{IH}		--	2.3	--	V
Input Low Voltage	V_{IL}		--	0.5	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	1.8	--	V
Input Voltage for MTP Fast Programming	VPP		--	8	--	V
IO of AD6 to AD7						
Positive Going Threshold Voltage	V_{IH}		--	2.5	--	V
Negative Going Threshold Voltage	V_{IL}		--	1.7	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	0.8	--	V
IO of AD8 to AD9						
Positive Going Threshold Voltage	V_{IH}		--	2.5	--	V
Negative Going Threshold Voltage	V_{IL}		--	1.7	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	0.8	--	V
Current Source for External Bias	I_{BIAS}		--	100	--	μA
AD0 to AD5 Section						
Time Constant of Input RC Filter	t_{AD0-5_RC}		--	--	100	ns
AD0to AD55 Offset at Pre-Amp x8	V_{OFFSET_x8}		--	--	--	mV
AD6 to AD7 Section						
Time Constant of Input RC Filter	t_{AD6-7_STEP1}	AD6/7_FLT = 0, AD6/7_DIV = 0	--	6	--	μs
Time constant of 2-Steps Input RC Filter	t_{AD6-7_STEP2}	AD6/7_FLT = 1	--	120	--	μs
Voltage Divider of Input Resistor		(R_{UP} + R_{DOWN}) / R_{DOWN}	--	3	--	--
AD8 to AD9 Section						
Time Constant of Input RC Filter	t_{AD8-9_RC}		--	4.5	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C Interface Section						
I²C Clock Cycle Time	t_{SCL}		t_{SYS} x 80	--	--	ns
I²C Start Bit Setup Time	t_{START}		--	t_{SCL} / 2	--	ns
I²C Stop Bit Setup Time	t_{STOP}		--	t_{SCL} / 2	--	ns
I²C Data Setup Time	t_{SETUP}		--	t_{SYS}	--	ns
I²C Data Hold Time	t_{HOLD}		--	t_{SYS}	--	ns
Low-Side Power Supply Section						
V15V Under-Voltage Lockout Threshold (On)	V_{THON_V15V}		--	10	--	V
V15V Under-Voltage Lockout Threshold (Off)	V_{THOFF_V15V}		--	9	--	V
V15V Under-Voltage Lockout Hysteresis	V_{HYS_V15V}		--	1	--	V
Bootstrapped Power Supply Section						
VBU/V/W-VSU/V/W Under-Voltage Lockout Threshold (On)	V_{THON_VBSx}		9	10	12	V
VBU/V/W-VSU/V/W Under-Voltage Lockout Threshold (Off)	V_{THOFF_VBSx}		8	9	11	V
VBU/V/W-VSU/V/W Under-Voltage Lockout Hysteresis	V_{HYS_VBSx}		--	1	--	V
VBU/V/W-to-VSU/V/W Quiescent Current for Each Channel	I_{Q_VBSx}	Gate driver output low.	--	100	--	μA
VSU/V/W Leakage Current	I_{VSx}	$V_{VBU/V/W} = V_{VSU/V/W} = 600V$	--	--	50	μA
Gate Driver Output Section (HOU/V/W, LOU/V/W)						
High-Side / Low-Side Output Voltage	V_{OH}	I_O = 0mA, $V_{VBU/V/W} - V_{HOU/V/W}$, $V15V - V_{LOU/V/W}$	--	50	200	mV
	V_{OL}	I_O = 0mA, $V_{HOU/V/W}$ - $V_{VSU/V/W}$, $V_{LOU/V/W}$ - V_{COM}	--	20	100	mV
HOU/V/W and LOU/V/W Sourcing Current	IO+	Gate driver output high, $V_{HOU/V/W} = V_{LOU/V/W} = 0V$, PW < 10μs (Note7)	--	290	--	mA
HOU/V/W and LOU/V/W Sinking Current	IO−	Gate driver output low, $V_{HOU/V/W} = V_{LOU/V/W} = V_{V15V}$, PW < 10μs (Note7)	--	600	--	mA
Bootstrap Diode Section						
Maximum Repetitive Peak Reverse Voltage	VRRM		--	--	600	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Average Forward Rectified Current	IAV		--	--	0.6	A

Dynamic Electrical Characteristics

(V_{V5V} = $V_{VBU/V/W}$ = 15V, V_{V5V} = 5V, $V_{VSU/V/W}$ = GND, C_L = 1000pF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-On Propagation Delay	t_{ON}		--	350	--	ns
Turn-Off Propagation Delay	t_{OFF}		--	350	--	ns
Gate Driver Output Turn-On Rising Time	t_R		--	70	--	ns
Gate Driver Output Turn-Off Falling Time	t_F		--	35	--	ns
Gate Driver Output Dead Time	DT	Motor controller set zero deadtime.	--	500	--	ns
Delay Matching	MT		--	120	--	ns
Dead-Time Matching to All Channels	MDT		--	135	--	ns

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Characterized, not tested at manufacturing.

Note 6. For comparator only.

Note 7. This parameter is guaranteed by design.

Application Information

Dynamic Waveforms

Figure 1 is a definition of dynamic characteristics. You can know those definitions and the relationship between input and output from these figures. For example : t_{ON} ,t_{OFF}, t_R, t_F, MT....

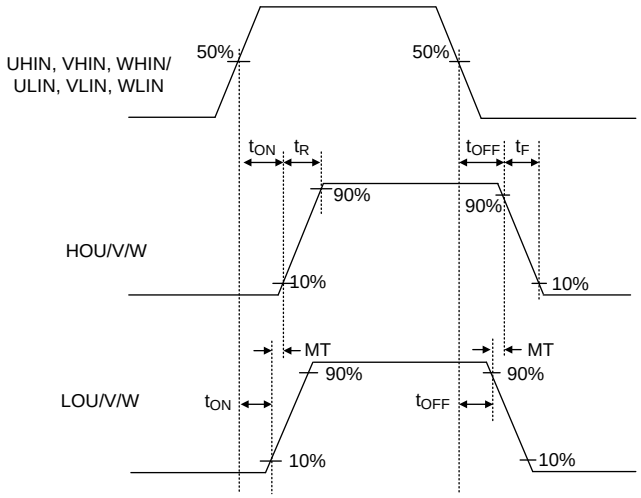


Figure 1. Dynamic Electrical Characteristics Definition

Deadtime

To avoid the simultaneous conduction of high-side and low-side power switches cause shoot through, the switching operation of the IC control circuit introduces a deadtime function. In the deadtime period, even if the input sends another power switch conduction signal, the control circuit will remain closed drive state. Figure 2 illustrates the definition of deadtime (DT_H and DT_L) and the relationship between the high-side and low-side gate signals.

The motor controller also has a deadtime function. If the controller's deadtime is greater than the gate driver deadtime, the output deadtime is equal to the controller's setting. Otherwise, the output deadtime is the gate driver's deadtime. Please refer to Figure 3 for details.

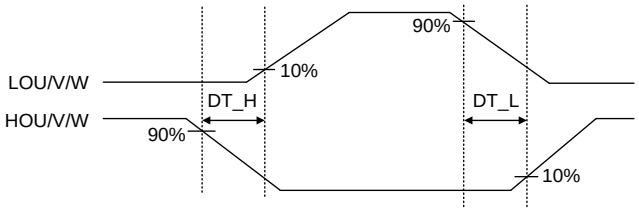
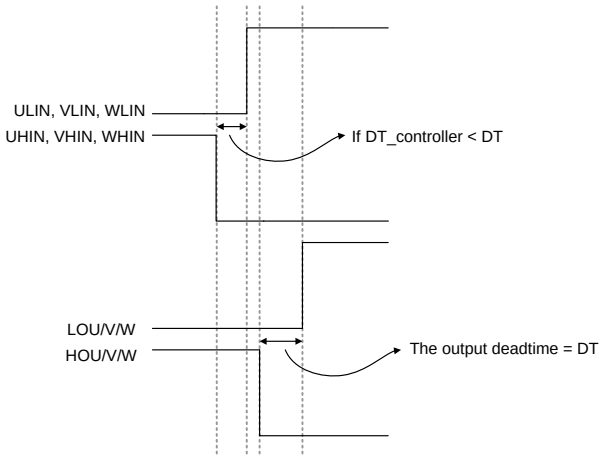


Figure 2. Deadtime Definition



Note :
DT_controller : deadtime setting from motor controller.
DT : the gate driver output deadtime.

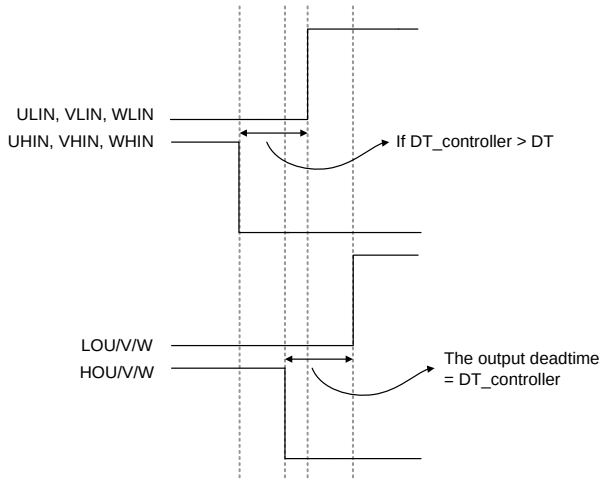


Figure 3. The Relationship of Deadtime

Matched Propagation Delays

Because the IC internal level shifter circuit causes the propagation delay of the high-side output signal, the RT7081 add a propagation delay matching circuit in the low-side logic circuit, so that each high-side and low-side output signals (t_{ON}, t_{OFF}) approximately synchronization.

Undervoltage-Lockout (UVLO)

The UVLO function prevents incorrect operation when the voltage falls below the threshold voltage. The RT7081 has UVLO protection for V15V and VBU/V/W-VSU/V/W.

Figure 4 is an explanation of UVLO. When powered up, V_{V15V} and $V_{VBU/V/W}$ rise to the threshold voltage (V_{THON_V15V} and V_{THON_VBSX}), the RT7081 will operate normally, and if the V_{V15V} drops below the threshold voltage (V_{THOFF_V15V}), it will turn off the high and low-side output.

If the $V_{VBU/V/W}$ is below the threshold voltage (V_{THOFF_VBSx}), only the high-side gate driver output will be turned off.

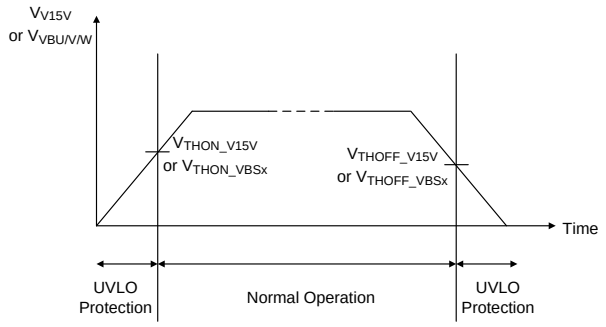


Figure 4. UVLO Description

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-37L 7x7 package, the thermal resistance, θ_{JA}, is 26.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (26.2°C/W) = 3.81W for a WQFN-37L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

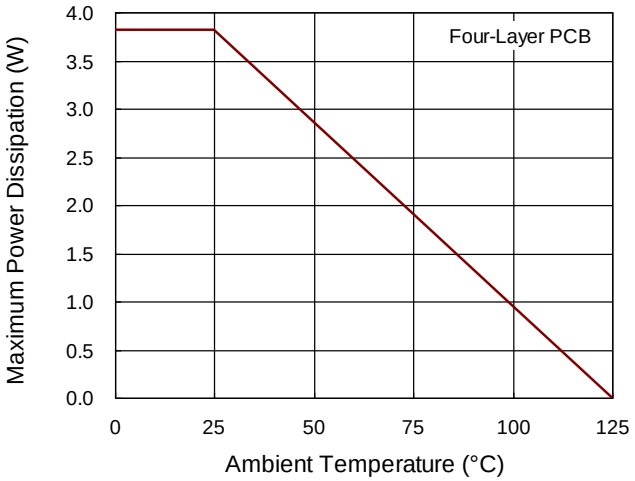
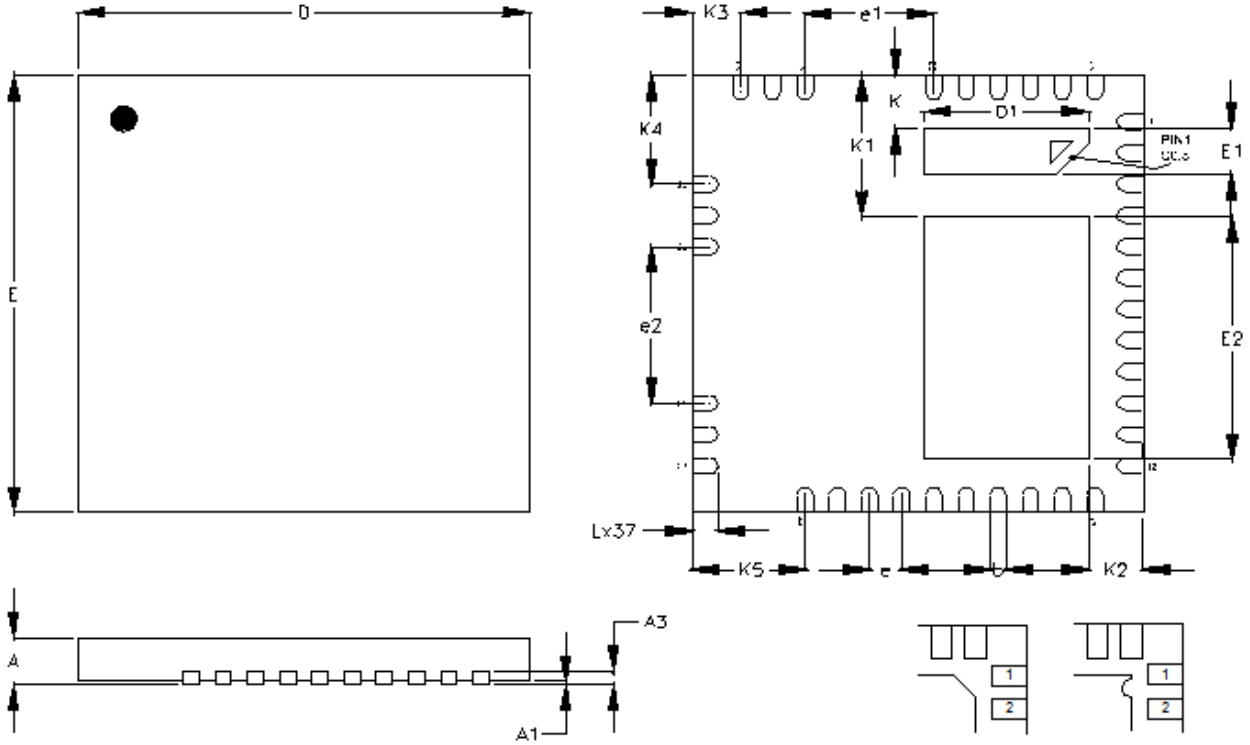


Figure 5. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

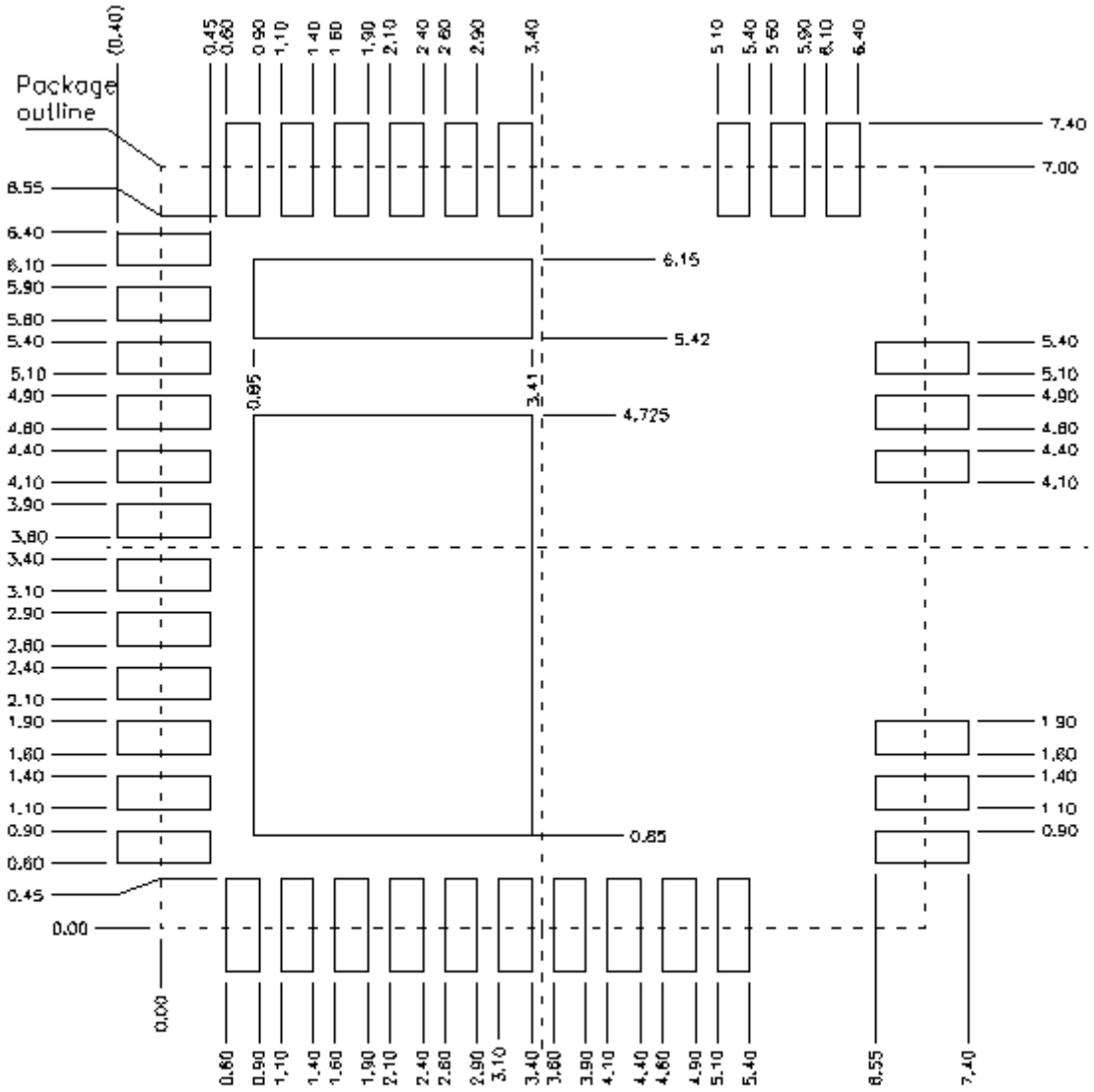
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	6.950	7.050	0.274	0.278
D1	2.410	2.610	0.095	0.103
E	6.950	7.050	0.274	0.278
E1	0.580	0.780	0.023	0.031
E2	3.725	3.925	0.147	0.155
e	0.500		0.020	
e1	2.000		0.079	
e2	2.500		0.098	
K	0.850		0.033	
K1	2.275		0.090	
K2	0.850		0.033	
K3	0.750		0.030	
K4	1.750		0.069	
K5	1.750		0.069	
L	0.350	0.450	0.014	0.018

W-Type 37L QFN 7x7 Package

Footprint Information



Tolerance (mm)
±0.05

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Datasheet Revision History

Version	Date	Item	Description
P00	2019/5/8		First Edition