Programmable Multi-Protocol Controller for 20V Output with Power Sharing

General Description

The RT7202KLA is a programmable controller with high integration, including the internal feedback compensation and V2 (regulated voltage for internal MCU) inside. An internal MCU is designed to meet proprietary protocols via the CC1/CC2/D+/D- interface. This controller is a specific design for off-line AC-DC converters to achieve the high power density of a fast charge system. The RT7202KLA can share the output power through Master/Slave I^2C communication. The built-in feedback compensation not only reduces the external components, but also enhances the transient response. For the safety consideration, the RT7202KLA provides comprehensive protections, including LPS protection and accurate internal Over-Temperature Protection (OTP).

In applications requiring high-precision control, a dual operational amplifier is adopted in the Digital-to-Analog Converter (DAC) to serve reference voltages used for regulation of voltage loop and current loop in programming the constant voltage (CV) and the constant current (CC).

Applications

- USB Type-C Controller in Source Application for Single-Port or Multi-Port Charger/Adapter of Smartphone, Tablet, Notebook, and Other Electronics
- USB Type-C Controller in Sink Application for IoT Devices of Power Over Ethernet, Smart Speaker, Projector, and Other Electronics

Features

- **Protocol Support**
  - **USB PD2.0/PD3.0 and PPS**
  - **UFCS**
  - **Proprietary Protocols**
- **Highly Integrated**
  - **Suited for 3V to 22V VDD Range**
  - **Embedded MCU with a Mask ROM of 32kB, an OTP-ROM of 16kB, and an SRAM of 2kB**
  - **Built-in Shunt Regulators for Constant Voltage and Constant Current Control**
  - **Built-in Feedback Compensation with Soft Start for LPS**
  - **Built-in V_{CONN} Power (5V/20mA)**
  - **VDD Pin for Quick Discharge of Output Capacitor**
  - **Supported High-Side Current Sensing**
  - **Supported Linear Cable Compensation**
  - **Supported Master/Slave I^2C Communication**
  - **Supported VIN and LPS Detection**
  - **< 6.6mA Operating Current in Normal Mode**
  - **< 2.2mA Operating Current in Sleep Mode**
  - **< 1150μA Operating Current in Green Mode**
- **Protection**
  - **Adaptive Output Over-Voltage Protection**
  - **Adaptive Under-Voltage Protection**
  - **CC1/CC2/D+/D-/RT Over-Voltage Protection**
  - **Firmware-Programmable Over-Current Protection**
  - **Firmware-Programmable Constant Current Protection**
  - **Firmware-Programmable Over-Temperature Protection**
  - **Firmware-Programmable LPS Protection**
  - **Internal Over-Temperature Protection**

Ordering Information

RT7202KLA□□-□

- Programmed Firmware Code AABBX***
  - AA : Application Code
  - BB : Model Code
  - X : Customer Approved Version Code
- Package Type
  - QW : WQFN-24L 4x4 (W-Type)
    (Exposed Pad-Option 2)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

***AABBX is optional, for firmware inside IC only.

Richtek products are :

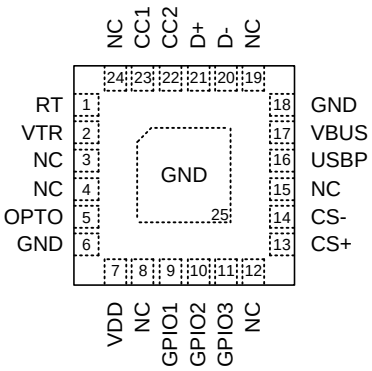
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

(TOP VIEW)

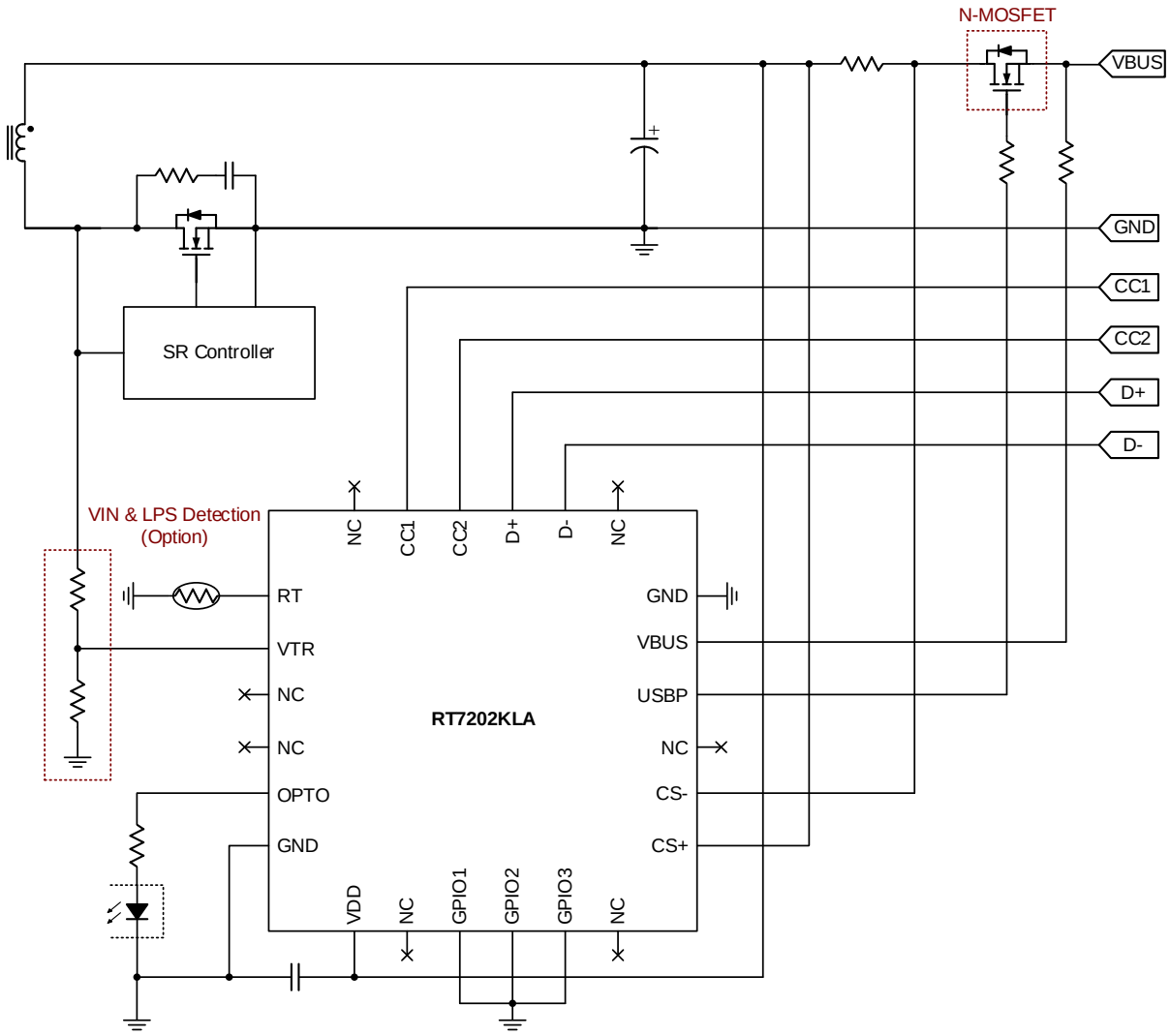


WQFN-24L 4x4

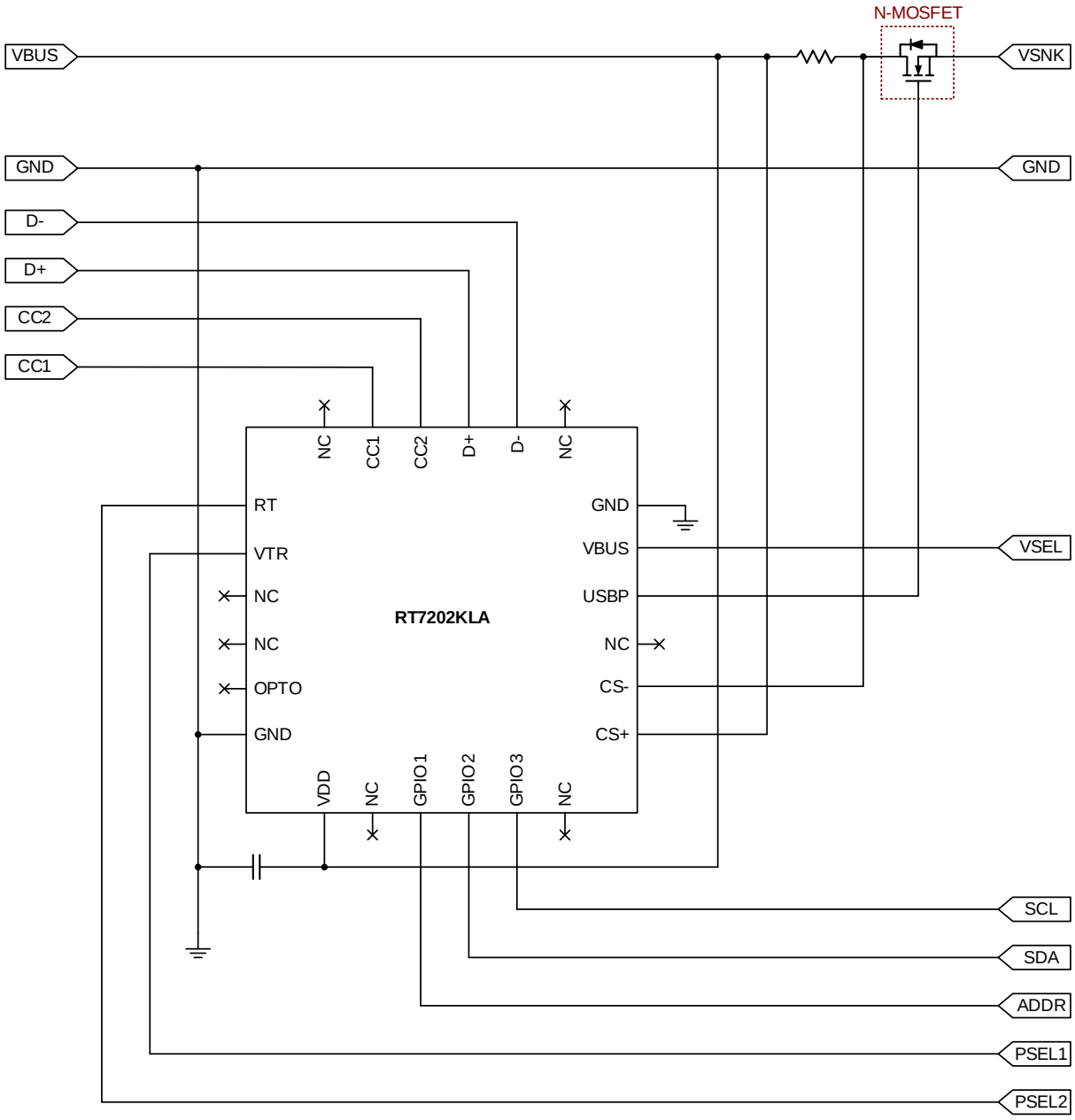
RT7202KLA Functional Table

Version	RT7202KLA
Output Voltage Supported	3V to 22V
V_{OUT} Scaling Factor R_{FB2} / (R_{FB1} + R_{FB2})	1/10
Built-in FB Resistors	O
Blocking MOSFET Driver	N-MOSFET
Package	WQFN-24L 4x4

Simplified Application Circuit



Simplified Circuit in Source Application

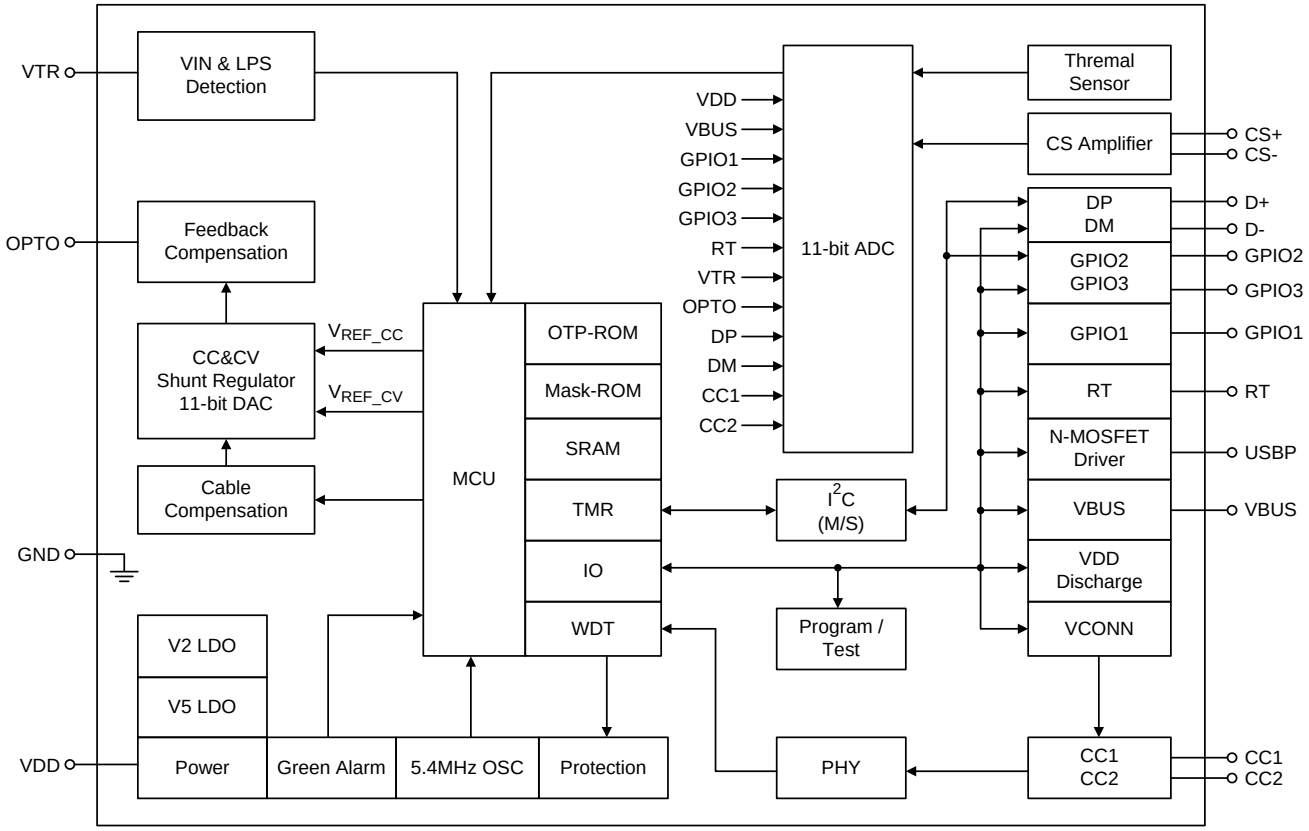


Simplified Circuit in Sink Application

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	RT	A/D IO	Remote thermal sensor connection node for over-temperature protection.
2	VTR	AI	Transformer voltage sense node.
3, 4, 8, 12, 15, 19, 24	NC	NC	No internal connection.
5	OPTO	AO	Current source output for optocoupler connection.
6, 18	GND	GND	Ground.
7	VDD	PWR	Supply input voltage.
9	GPIO1	A/D IO	General purpose input/output.
10	GPIO2	A/D IO	General purpose input/output. (I^2C-SDA)
11	GPIO3	A/D IO	General purpose input/output. (I^2C-SCL)
13	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
14	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
16	USBP	D IO	Control signal of a blocking N-MOSFET.
17	VBUS	A IO	VBUS sensing and bleeder connection node to provide another path to discharge the VBUS capacitor.
20	D-	A/D IO	USB D- channel.
21	D+	A/D IO	USB D+ channel.
22	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.
23	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
25 (Exposed Pad)	GND	GND	Power ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

Functional Block Diagram



Operation

The RT7202KLA is a highly integrated secondary-side programmable controller, providing various functions and comprehensive protections for off-line AC-DC converters.

Power Structure

The internal V5 and V2 regulated voltages, biased by VDD, of the RT7202KLA are used to supply the internal circuit and the internal microprocessor (MCU), respectively.

Constant Voltage and Constant Current (CV/CC) Regulators

The RT7202KLA has two transconductance amplifiers connected in paralleled to the feedback compensator. The feedback compensator sources the current at the OPTO pin to regulate the output voltage and the output current. Noted that the operation of each feedback loop is opposite to that of the traditional TL431 shunt regulator. The OPTO pin is in high impedance state if the VDD voltage is still below the VDD turn-on threshold V_{VDD_ON}, which ensures a smooth power-on sequence. The reference voltages, V_{REF_CV} and V_{REF_CC}, of the voltage feedback loop and the current feedback loop are the analog output voltages of 11-bit DAC. The resolution of DAC output voltage for CV is 10mV, which can achieve high precision CV regulation.

Current Sense Amplifier

To minimize the power loss of the current sense resistor, a low input offset amplifier with voltage gain of 20 or 40 is used. When the 5mΩ (typ.) R_{CS} goes with the voltage gain 40, the resolution of the output current is around 5mA. The operation of the CV and CC loops are shown in Figure 1.

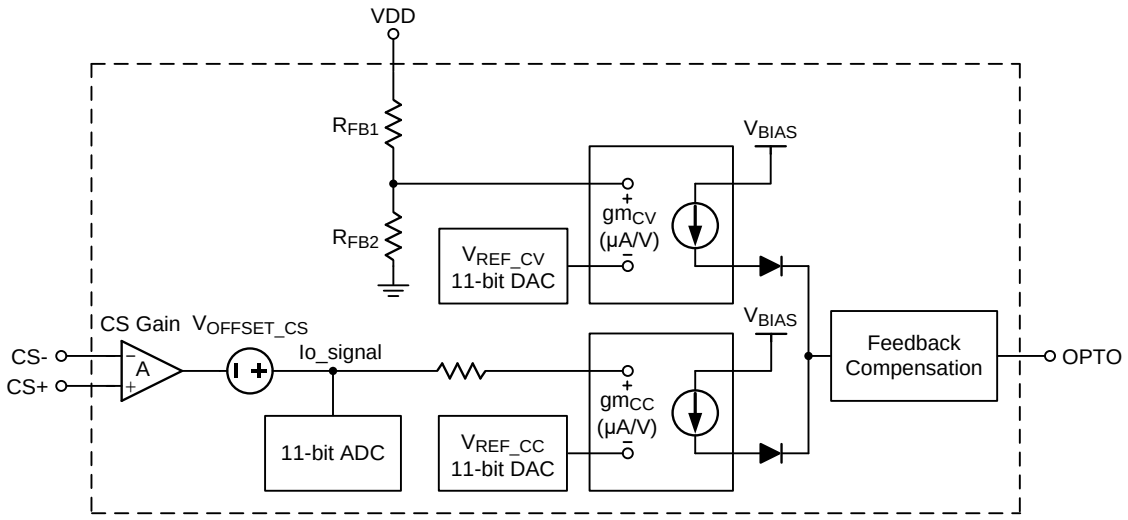


Figure 1. CV and CC Loops

External Temperature Sensing

As shown in Figure 2, the RT7202KLA provides the RT pin as a register-programmable current source to bias a remote thermal sensor, such as a thermistor (NTC). If the RT voltage is below the over-temperature protection (OTP) threshold and the condition sustains for a programmed delay time, the OTP will be triggered.

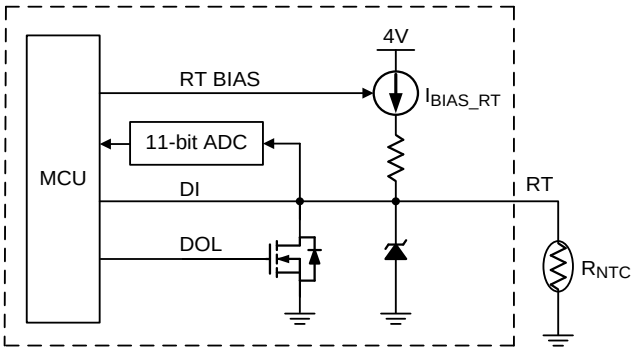


Figure 2. External Temperature Sensing

Interface of D+ and D-

The D+ and D- pins are used for BC1.2 compliance or for communication with other proprietary protocols. The D+ and D- pins, connected to the MCU via an ADC, can be re-programmed for other purposes since they can be used as an analog/digital input or output, as shown in Figure 3.

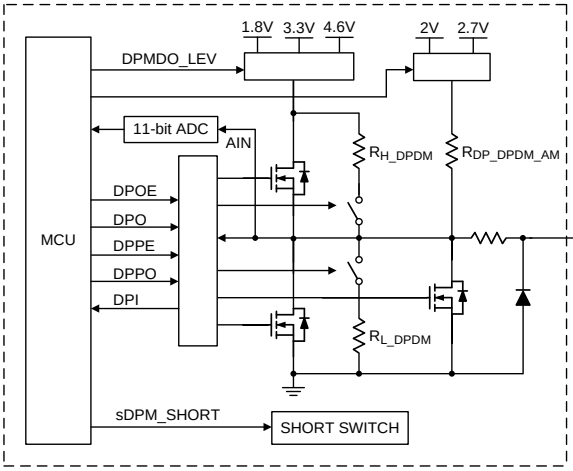


Figure 3. Interface of D+ and D-

Interface of CC1 and CC2

The CC1 and CC2 pins are used for compliance with the USB Type-C specification. When configured as a Downstream Facing Port (DFP), three current capabilities of 80μA, 180μA, and 330μA, provided by each of the CC pin, will be advertised to an Upstream Facing Port (UFP) as the default USB current, 1.5A, and 3.0A, respectively. The interface of CC1 and CC2 is shown in Figure 4.

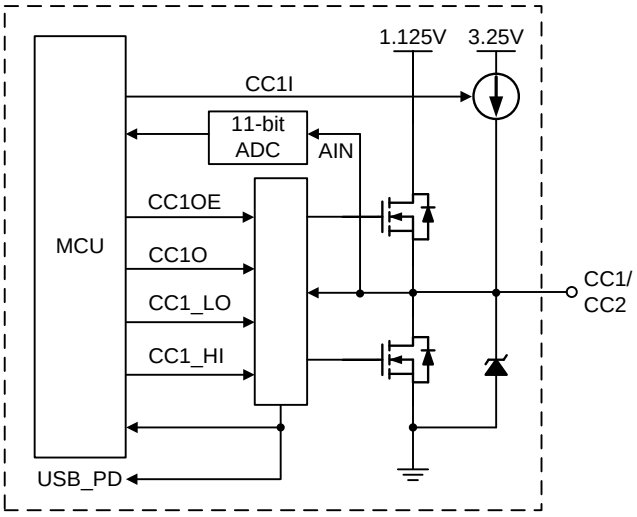


Figure 4. Interface of CC1 and CC2

Open-Drain Driver of VBUS Pin

Figure 5 shows the VBUS pin with the open-drain drivers. The internal bleeder circuit at VBUS pin is used to discharge the VBUS capacitor to Vsafe0V while cable is detached from a device. The VBUS pin voltage can be detected by ADC to achieve VBUS drop protection.

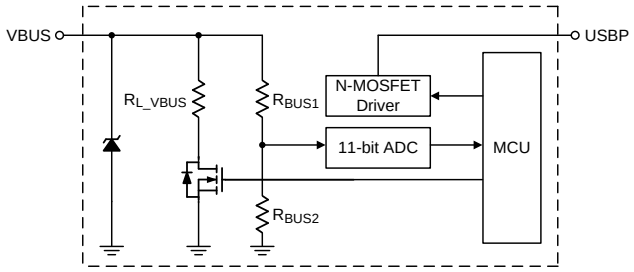


Figure 5. Open Drain Driver of VBUS Pin

I²C Communication

The RT7202KLA can share the output power through Master/Slave I²C communication by connecting GPIO2 (SDA) and GPIO3 (SCL) to the other GPIO pins of RT7202KLA, respectively. The interface of I²C communication is shown in Figure 6.

Capability Selector in Sink Application

When RT7202KLA is utilized in a sink port, two ways are implemented to set the correspond capabilities. The embedded ADCs in VBUS, RT, and VTR resolve the related voltages, V_{BUS}, V_{RT}, and V_{TR} as the analog inputs for setting the voltage and power capabilities. In addition, If the I²C communication is connected to a host controller by GPIO2 and GPIO3, the capabilities can be set directly by the host controller.

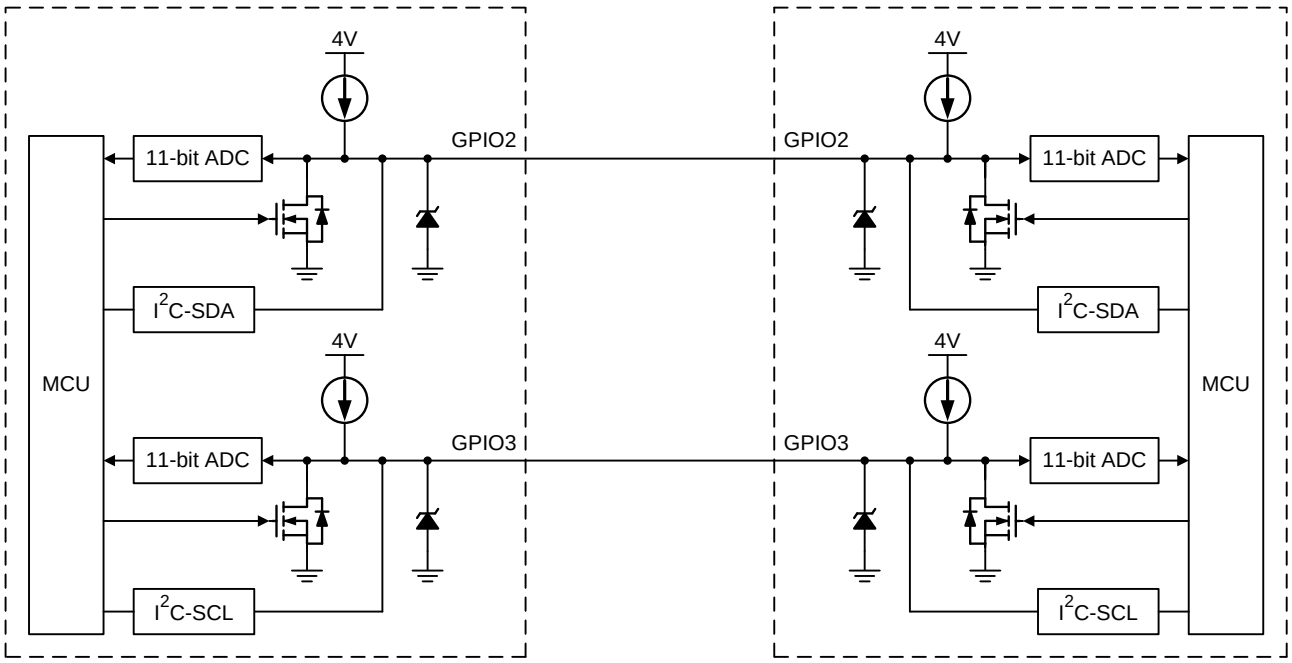


Figure 6. Interface of I²C Communication

Absolute Maximum Ratings (Note 1)

- USBP to GND ---------- –0.3V to 32V
- VDD, VBUS, CS+, CS- to GND ---------- –0.3V to 28V
- OPTO, VTR, GPIO1, GPIO2, GPIO3, CC1, CC2, D+, D-, RT to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-24L 4x4---------- 2.52W
- Package Thermal Resistance (Note 2)

  WQFN-24L 4x4, θ_{JA} ---------- 39.6°C/W

  WQFN-24L 4x4, θ_{JC} ---------- 7.1°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD---------- 3V to 22V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 105°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold	V_{VDD_ON}		2.9	3.05	3.2	V
VDD Turn-Off Threshold	V_{VDD_OFF}		2.8	2.85	2.9	V
VDD Turn-On/Off Hysteresis	V_{VDD_HYS}		0.1	0.2	0.3	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 2.8V	--	200	300	μA
VDD Operating Current	I_{DD_OP}	1. V_{DD} = 5V 2. Disable VTR function	--	5.5	6.6	mA
VDD Sleep-Mode Current	I_{DD_SLEEP}	1. V_{DD} = 5V 2. Disable VTR function	--	1.8	2.2	mA
VDD Green-Mode Current	I_{DD_GREEN}	1. V_{DD} = 5V 2. Disable VTR function	--	950	1150	μA
Maximum VDD Over-Voltage Protection Threshold	$V_{MAX\_VDD\_OVP}$		23	24	25	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Over-Voltage Protection Threshold	V_{VOUT_OVP}	With respect to V_{REF_CV}. (Note 5)	00	106.7	110	113.3	%
			01	109.3	115	120.8	
			10	114	120	126	
			11	Disable			
VDD Over-Voltage Protection Deglitch Time	$t_{D\_VDD\_OVP}$	(Note 5)		25	30	35	µs
Register-Programmable VDD Under-Voltage Wake-Up Threshold	$V_{DD\_UV\_WK}$	With respect to V_{REF_CV}. It can be disabled by register. (Note 5)	0	85.5	90	94.5	%
			1	80.75	85	89.25	
VDD Under-Voltage Deglitch Time	$t_{D\_VDD\_UV}$	(Note 5)		35	55	75	µs
Register-Programmable VDD Discharge Current	I_{DD_DIS}	V_{DD} > 3V	00	15	30	45	mA
			01	42	60	78	
			10	63	90	117	
			11	84	120	156	
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} > 2.8V		5.13	5.4	5.67	MHz
Regulator Section							
V_{DD} Divider Resistor	R_{FB}	$R_{FB} = R_{FB1} + R_{FB2}$ R_{FB1} : VDD to VFB R_{FB2} : VFB to GND (Note 5)		294	420	546	kΩ
V_{DD} Scaling Factor	K_{FB}	$K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2}$		9.9	10	10.1	--
Reference Voltage for Standby CV Regulators	$V_{ST\_REF\_CV}$	(Note 5)		0.485	0.5	0.515	V
Minimum DAC Output Voltage for CV Regulators	$V_{DAC\_MIN\_CV}$	With 11-bit digital to analog converter.		0.12	0.152	0.17	V
Maximum DAC Output Voltage for CV Regulators	$V_{DAC\_MAX\_CV}$			2.178	2.2	2.222	V
Minimum DAC Output Voltage for CC Regulators	$V_{DAC\_MIN\_CC}$	With 11-bit digital to analog converter.		--	0	--	V
Maximum DAC Output Voltage for CC Regulators	$V_{DAC\_MAX\_CC}$			1.98	2	2.02	
Maximum ADC Sense Voltage	V_{ADC_MAX}	With 11-bit analog to digital converter.		2.178	2.2	2.222	V
Maximum OPTO Output Voltage	V_{OPTO_MAX}	V_{DD} = 2.8V to 25V, I_{SRC_OPTO} = 1mA		1.8	--	--	V
Maximum OPTO Output Clamping Voltage	$V_{OPTO\_MAX\_CLAMP}$	V_{DD} = 5V, I_{SRC_OPTO} = 1mA		2.1	2.4	2.7	V
Maximum OPTO Sourcing Current	I_{OPTO_MAX}	100Ω resistor connected in series		2	--	40	mA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Internal Resistor between OPTO and GND	R_{OPTO_GND}			42	60	78	kΩ
OPTO Pull Low Impedance for CV Open Loop	R_{L_OPTO}	OPTO shorted to GND by register setting		--	--	200	Ω
Current Sense Section							
Register-Programmable Current-Sense Voltage Gain	K_{CS}			39.6	40	40.4	V/V
Current-Sense Amplifier Output Offset Voltage	V_{OFFSET_CS}			0.36	0.4	0.44	V
Register-Programmable Exit Green Mode Threshold	V_{GREEN_ED}	$(V_{CS+} - V_{CS-}) \times K_{CS} + V_{OFFSET\_CS}$	0	0.41	0.45	0.49	V
			1	0.51	0.55	0.59	
Register-Programmable Transconductance Amplifier of Cable Compensation	gm_{COMP}	$R_{CS} \times K_{CS}$ = 100m (Note 5)	00	--	1.323	--	μA/V
		$R_{CS} \times K_{CS}$ = 120m (Note 5)	01	--	1.102	--	
		$R_{CS} \times K_{CS}$ = 200m (Note 5)	10	--	0.661	--	
		$R_{CS} \times K_{CS}$ = 400m (Note 5)	11	--	0.331	--	
Register-Programmable Cable Compensation Gain	K_{CC}	Disable cable compensation	000	Disable			V/V
		R_{CABLE} = 50mΩ (Note 5)	001	--	1	--	
		R_{CABLE} = 75mΩ (Note 5)	010	--	1.5	--	
		R_{CABLE} = 100mΩ (Note 5)	011	--	2	--	
		R_{CABLE} = 125mΩ (Note 5)	100	--	2.5	--	
		R_{CABLE} = 150mΩ (Note 5)	101	--	3	--	
		R_{CABLE} = 175mΩ (Note 5)	110	--	3.5	--	
		R_{CABLE} = 200mΩ (Note 5)	111	--	4	--	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Internal Compensation Section							
Register-Programmable R_Z for Zero Point	R_Z	(Note 5)	000	3.5	5	6.5	kΩ
			001	7	10	13	
			010	21	30	39	
			011	35	50	65	
			100	70	100	130	
			101	112	160	208	
			110	161	230	299	
			111	217	310	403	
Register-Programmable C_Z for Zero Point	C_Z	It can be programmed by register. (Note 5)		4.16	--	1064	nF
Register-Programmable Zero Point	f_{ZERO}	It can be programmed by register. (Note 5)		0.48	--	7659	Hz
Register-Programmable Middle Gain		It can be programmed by register. (Note 5)		−26.02	--	15.85	dB
Overshoot Clamping Threshold	V_{VOUT_OVC}	1. Ratio of V_{REF_CV} 2. Default is disable		104.5	110	115.5	%
Register-Programmable Undershoot Clamping Triggered Threshold	$V_{VOUT\_UVC\_Triggered}$	1. Ratio of V_{REF_CV} 2. Default is disable 3. Disable at CC mode (Note 5)	0	85.5	90	94.5	%
			1	87.8	92.5	97.2	
Register-Programmable Undershoot Clamping Released Threshold	$V_{VOUT\_UVC\_Released}$	1. Ratio of V_{REF_CV} 2. Default is disable 3. Disable at CC mode (Note 5)	0	90.3	95	99.8	%
			1	92.6	97.5	102.4	
Register-Programmable Debounce Time of Overshoot and Undershoot Clamping	$t_{D\_OVUV\_CLAMP}$	(Note 5)	0	5	10	15	µs
			1	15	20	25	
Register-Programmable Debounce Time of Disable Undershoot Clamping at CC Mode	$t_{DIS\_UVCC\_CLAMP}$	(Note 5)	0	5	10	15	µs
			1	15	20	25	
RT Section							
Open Loop Voltage	V_{RT_OP}	V_{DD} = 5V, I_{BIAS_RT} = 95µA		3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_RT}	V_{DD} > 3V (Note 5)	00	95	100	105	µA
			01	18	20	22	
			10	4.5	5	5.5	
			11	Open			
RT Over-Voltage Protection Threshold	V_{RT_OVP}	1. Turn-off blocking MOSFET or not by register setting. 2. Send a flag to MCU. 3. V_{DD} > 5.5V (Note 5)		4.6	4.85	5	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable RT Over-Voltage Protection Debounce Time	t_{RT_OVP}	(Note 5)	00	0.04	0.055	0.07	ms
			01	0.11	0.13	0.15	
			10	0.9	1	1.1	
			11	4.7	5	5.3	
GPIO1 Section							
Open-Loop Voltage	V_{GP1_OP}	V_{DD} = 5V, I_{BIAS_GP} = 950μA		3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_GP1}	V_{DD} > 3V	00	900	1150	1400	μA
			01	95	100	105	
			10	18	20	22	
			11	Open			
GPIO1 Over-Voltage Protection Threshold	V_{GP1_OVP}	1. Send a flag to MCU. 2. V_{DD} > 5.5V (Note 5)		4.6	4.85	5	V
GPIO1 Over-Voltage Protection Debounce Time	t_{GP1_OVP}	(Note 5)		50	80	110	μs
GPIO2 and GPIO3 Section							
Open-Loop Voltage	V_{GP_OP}	V_{DD} = 5V, I_{BIAS_GP} = 95μA		3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_GP}	V_{DD} > 3V	00	95	100	105	μA
			01	18	20	22	
			10	4.5	5	5.5	
			11	Open			
GPIO2/GPIO3 Over-Voltage Protection Threshold	V_{GP_OVP}	1. Send a flag to MCU. 2. V_{DD} > 5.5V (Note 5)		4.6	4.85	5	V
GPIO2/GPIO3 Over-Voltage Protection Debounce Time	t_{GP_OVP}	(Note 5)		50	80	110	μs
Input High Trip Voltage	V_{IH_I2C}			1.3	--	--	V
Input Low Trip Voltage	V_{IL_I2C}			--	--	0.4	V
VBUS Section							
Maximum VBUS Discharge Current	I_{VBUS_DIS}			2	--	30	mA
Pull-Low Impedance	R_{L_VBUS}	I_{VBUS_MAX} = 20mA		0.7	1	1.3	kΩ
VBUS Divider Resistor for ADC Sensing	R_{VBUS}	R_{VBUS} = R_{VBUS1} + R_{VBUS2}		294	420	546	kΩ
Trim-Programmable VBUS Scaling Factor for ADC Sensing	K_{VBUS}	K_{VBUS} = (R_{VBUS1} + R_{VBUS2}) / R_{VBUS2}		9.9	10	10.1	--

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable VBUS Drop Threshold for Output Short Protection	V_{DROP_VBUS}	V_{DD} > 3.3V If V_{DD} - V_{BUS} > V_{DROP_VBUS}, 1. Turn-off blocking MOSFET or not by register setting. 2. Send a flag to MCU. (Disable/Enable by register.) (Note 5)	0	0.14	0.24	0.34	V
			1	0.2	0.3	0.4	
Register-Programmable VBUS Drop Debounce Time for Output Short Protection	t_{DROP_VBUS}	V_{DD} > 5V (Note 5)	0	10	12	14	µs
			1	18	22	26	
D+ and D- Section							
Register-Programmable Pull-High Resistance	R_{H_DPDM}	(Note 5)	0	Open			kΩ
			1	10	12.5	15	
Pull-Low Resistance	R_{L_DPDM}	(Note 5)	0	Open			kΩ
			1	16	20	24	
Register-Programmable Output High Voltage	V_{OH_OP}		00	Open Drain			V
	$V_{OH\_3.3V}$	V_{DD} = 5V, R_L = 15kΩ (Note 5)	01	2.97	3.3	3.63	
	$V_{OH\_1.8V}$		10	1.62	1.8	1.98	
	$V_{OH\_4.6V}$		11	4.1	4.6	5.1	
Output Low Voltage	V_{OL_OP}	R_L = 15kΩ		--	--	0.2	V
	$V_{OL\_3.3V}$						
	$V_{OL\_1.8V}$						
	$V_{OL\_4.6V}$						
Register-Programmable DP and DM Input Level	V_{IN_LEV}		0	--	0	--	V
			1	--	0.4	--	
Register-Programmable Input High Trip Voltage	V_{IH_DPDM}		00	0.7 + V_{IN_LEV}	0.8 + V_{IN_LEV}	0.9 + V_{IN_LEV}	V
			01	1.2 + V_{IN_LEV}	1.3 + V_{IN_LEV}	1.4 + V_{IN_LEV}	
			10	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2 + V_{IN_LEV}	
			11	2 + V_{IN_LEV}	2.1 + V_{IN_LEV}	2.2 + V_{IN_LEV}	
Register-Programmable Input Low Trip Voltage	V_{IL_DPDM}		00	0.5 + V_{IN_LEV}	0.6 + V_{IN_LEV}	0.7 + V_{IN_LEV}	V
			01	1.0 + V_{IN_LEV}	1.1 + V_{IN_LEV}	1.2 + V_{IN_LEV}	
			10	1.7 + V_{IN_LEV}	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	
			11	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2.0 + V_{IN_LEV}	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DPDM Switch On-Resistance	R_{ON_DPDM}			--	--	40	Ω
DP Comparison Threshold for Cable Detection	$V_{TH\_DP\_CD}$	Send an interrupt to MCU when cable detached. Disable/enable cable detection by register.		0.2	0.3	0.4	V
Register-Programmable Cable Detection Debounce Time	t_{DP_CD}	Disable/Enable by register. (Note 5)	00	0.4	0.65	0.9	ms
			01	0.9	1.15	1.4	
			10	1.85	2.1	2.35	
			11	3.85	4.1	4.35	
Register-Programmable Input Debounce Time	t_{D_DPDMIN}	Debounce time = t_{D_DPDMIN} x K_{tD_DPDMIN} (Note 5)	00	0.95	1	1.05	µs
			01	1.9	2	2.1	
			10	3.8	4	4.2	
			11	7.6	8	8.4	
Register-Programmable Input Debounce Time Scale	K_{tD_DPDMIN}	(Note 5)	00	--	1	--	--
			01	--	8	--	
			10	--	64	--	
			11	--	512	--	
Register-Programmable DP/DM Over-Voltage Protection Threshold	V_{DPDM_OVP}	1. Turn-off blocking MOSFET or not by register setting. 2. Send a flag to MCU. 3. V_{DD} > 5.5V	0	4.2	4.35	4.5	V
			1	3.85	4	4.15	
Register-Programmable DP/DM Over-Voltage Protection Debounce Time	t_{DPDM_OVP}	(Note 5)	00	0.04	0.055	0.7	ms
			01	0.11	0.13	0.15	
			10	0.9	1	1.1	
			11	4.7	5	5.3	
Sourcing Current for Rust Protection	I_{DM_RUST}	1. V_{DD} > 3.65V 2. Only for DM pin. 3. Disable/Enable by register. (Note 5)		2.4	3	3.6	mA
Pull-High Resistance for Apple Mode	$R_{H\_DPDM\_AM}$			24	30	36	kΩ
Register-Programmable Output High Voltage for Apple Mode	$V_{OH\_2.7V\_AM}$	V_{DD} > 4V	0	2.565	2.7	2.835	V
	$V_{OH\_2V\_AM}$		1	1.88	2	2.12	
CC1 and CC2 Section							
Output High Voltage	V_{OH_CC}			1.05	1.125	1.2	V
Output Low Voltage	V_{OL_CC}			0	0.0375	0.075	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Input High Trip Voltage	V_{IH_CC}		00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	
Register-Programmable Input Low Trip Voltage	V_{IL_CC}		00	0.4	0.5	0.6	V
			01	0.3	0.4	0.5	
			10	0.2	0.3	0.4	
			11	0.1	0.2	0.3	
Open Loop Voltage for CC1/CC2 Sourcing Current	V_{CC_OP}	V_{DD} > 5V		2.9	3.25	3.6	V
Register-Programmable Sourcing Current	I_{CC_SRC}	V_{DD} > 3V	00	High Impedance			µA
			01	76	80	84	
			10	171	180	189	
			11	304	330	356	
Sourcing Current for Rust Protection	I_{CC_RUST}	Disable/Enable by register (Note 5)		0.5	1	1.5	µA
CC1/CC2 Comparison Threshold for Cable Detection	V_{CC_CD}	1. V_{DD} > 3V 2. Disable/Enable by register. 3. Send a flag to MCU		2.5	2.6	2.7	V
Register-ProgrammableCC1/CC2 Comparison Threshold for VBUS Short Detection	V_{CC_OVP}	1. Turn-off blocking MOSFET or not by register setting. 2. Send a flag to MCU. 3. V_{DD} > 5.5V (Note 5)	0	4.2	4.35	4.5	V
			1	3.85	4	4.15	
Register-Programmable CC1/CC2 Cable Detection and Over-Voltage Protection Debounce Time	t_{CC_OVP}	(Note 5)	00	0.04	0.055	0.7	ms
			01	0.11	0.13	0.15	
			10	0.9	1	1.1	
			11	4.7	5	5.3	
V_{CONN} Voltage	V_{VCONN}	V_{DD} = 5V, I_{VCONN} = 0mA		4.8	--	5	V
		V_{DD} = 5V, I_{VCONN} = 30mA		3.3	--	--	
V_{CONN} Short-Circuit Current	I_{VCONN_SC}	(Note 5)		45	70	95	mA
USBP Section							
USBP Output High Voltage	V_{OH_USBP}	R_L = 10MΩ		V_{DD} + 7	V_{DD} + 8.5	V_{DD} + 10	V
Maximum USBP Output High Voltage	$V_{OH\_MAX\_USBP}$			30	31	32	V
USBP Under-Voltage Protection Threshold Voltage	V_{USBP_UVP}	1. Disable/Enable by register. 2. Send a flag to MCU.		V_{DD} + 4	V_{DD} + 4.5	V_{DD} + 5	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
USBP Under-Voltage Deglitch Time	$t_{D\_USBP\_UV}$	(Note 5)		30	50	70	μs
Register-Programmable Pull Low Resistance when VBUS Drop Protection	$R_{OL\_VBUSDR\_USBP}$	If VBUS drop protection is triggered & V_{DD} > V_{USBP}, then R_{USBP} = $R_{OL\_VBUSDR\_USBP}$	0	7	10	13	kΩ
			1	14	20	26	
Pull Low Resistance when USBP Turn-Off	$R_{OL\_USBPOFF}$	If VBUS drop protection is triggered & V_{USBP} >V_{DD}, then R_{USBP} = $R_{OL\_USBPOFF}$		1.62	2.7	3.78	kΩ
Pull Low Resistance when VDD UVLO	$R_{OL\_UVLO\_USBP}$	If V_{DD} < V_{DD_OFF}, then R_{USBP} = $R_{OL\_UVLO\_USBP}$		3.08	4.4	5.72	kΩ
USBP Divider Resistor for Capacitive Loads	R_{USBP}	Capacitive load function can be disabled/enabled by register		294	420	546	kΩ
USBP Scaling Factor for Capacitive Loads	K_{USBP}			4.85	5	5.15	--
Maximum DAC Output Voltage for Capacitive Loads	$V_{DAC\_MAX\_CL}$	With 8-bit digital to analog converter		2.134	2.2	2.266	V
Minimum DAC Output Voltage for Capacitive Loads	$V_{DAC\_MIN\_CL}$			--	0	--	V
VTR Section (For Low-Side SR Application)							
VDS Scaling Factor	K_{VDS}	(R_{VDS1} + R_{VDS2}) / R_{VDS2}		49	50	51	--
VTR Sample and Hold Threshold	K_{VTR_SH}	V_{TH_SH} = K_{VTR_SH} x $V_{VTR\_HIGH[n-1]}$		0.831	0.875	0.919	--
Register-Programmable Mask Time	t_{MASK}	V_{VTR} > V_{TH_SH}	0	170	320	470	ns
			1	60	160	260	
Register-Programmable VTR Blanking Time	t_{BLANK_VTR}	V_{VTR} > V_{TH_SH} VTR Blanking Time Change limit is ±185ns per cycle. (Note 5)	00	0.2	0.285	0.37	μs
			01	0.32	0.47	0.62	
			10	0.85	1.03	1.21	
			11	1.38	1.58	1.78	
Low Level Threshold for Input Voltage	K_{VIN_LOW}	When V_{VTR} x K_{VDS} < K_{VIN_LOW} x V_{OUT}, it will send a VIN Low flag to MCU. (Note 5)		2.05	2.25	2.45	--
VTR Over-Voltage Threshold	$V_{TH\_VTR\_OV}$	1. Send a Flag to MCU. 2. V_{DD} > 5.5V (Note 5)		3	3.3	3.6	V
VTR Over-Voltage Protection Debounce Time	t_{VTR_OVP}	(Note 5)		30	50	70	μs
VTR Rising Edge Threshold for AC OFF Detection	V_{EDGE_VTR}			30	70	110	mV

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VTR Edge Debounce Time for AC OFF Detection	t_{EDGE_VTR}	If V_{VTR} in t_{EDGE_VTR} is lower than V_{EDGE_VTR}, it will send an AC OFF flag to MCU. (Note 5)		90	100	110	ms
Reset Voltage for VTR Sample and Hold	V_{VTR_RST}	V_{DD} = 5V		(1.2±25%) x V_{DD} / K_{VDS} + (20m±10m)			V
VTR Section (For High-Side SR Application)							
Register-Programmable VTR Zero Voltage Clamp Level	V_{CLAMP_VTR}	V_{TR} < 0V	0	–0.1	0	0.1	V
			1	0	0.1	0.2	
VTR Maximum Sourcing Current	$I_{SRC\_VTR\_MAX}$			1.2	1.6	2	mA
VIN Sense Gain	K_{VIN}	$V_{IN}/n = K_{VDS} \times K_{IN} \times I_{SRC\_VTR}$ ($K_{IN} \times I_{SRC\_VTR}$ > 2V at V_{DD} = 3.3V)		2.16	2.4	2.64	mV/µA
VDS Scaling Factor	K_{VDS}	(R_{VDS1} + R_{VDS2}) / R_{VDS2} (External R_{VDS1} = 120kΩ, R_{VDS2} = 2.4kΩ)		49	50	51	--
VTR Sample and Hold Threshold	K_{VTR_SH}	$V_{TH\_SH} = K_{VTR\_SH} \times V_{VTR\_HIGH[n-1]}$		0.831	0.875	0.919	--
Register-Programmable Mask Time	t_{MASK}	V_{VTR} > V_{TH_SH}	0	170	320	470	ns
			1	60	160	260	
Register-Programmable VTR Blanking Time	t_{BLANK_VTR}	V_{VTR} > V_{TH_SH} VTR Blanking Time Change limit is ±185ns per cycle. (Note 5)	00	0.2	0.285	0.37	µs
			01	0.32	0.47	0.62	
			10	0.85	1.03	1.21	
			11	1.38	1.58	1.78	
Low Level Threshold for Input Voltage	K_{VIN_LOW}	When $I_{SRC\_VTR} \times K_{VIN} \times K_{VDS} < K_{VIN\_LOW} \times V_{OUT}$, it will send a VIN Low flag to MCU. (Note 5)		2.05	2.25	2.45	--
VTR Over-Voltage Threshold	$V_{TH\_VTR\_OV}$	1. Send a Flag to MCU. 2. V_{DD} > 5.5V (Note 5)		3	3.3	3.6	V
VTR Over-Voltage Protection Debounce Time	t_{VTR_OVP}	(Note 5)		30	50	70	µs
VTR Rising Edge Threshold for AC OFF Detection	V_{EDGE_VTR}			30	70	110	mV
VTR Edge Debounce Time for AC OFF Detection	t_{EDGE_VTR}	If $K_{VIN} \times I_{SRC\_VTR}$ in t_{EDGE_VTR} is lower than V_{EDGE_VTR}, it will send an AC OFF flag to MCU. (Note 5)		90	100	110	ms

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Reset Voltage for VTR Sample and Hold	V_{VTR_RST}	V_{DD} = 5V		30	70	110	mV
VTR Section (For RT Application)							
Open-Loop Voltage	V_{VTR_OP}	V_{DD} = 5V, I_{VTR} = 95μA		3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_VTR}	V_{DD} > 3V (Note 5)	00	95	100	105	μA
			01	18	20	22	
			10	4.5	5	5.5	
			11	Open			
VTR Over-Voltage Threshold	$V_{TH\_VTR\_OV}$	V_{DD} > 5.5V (Note 5)		4.6	4.85	5	V
VTR Over-Voltage Protection Debounce Time	t_{VTR_OVP}	(Note 5)		50	80	110	μs
Thermal Sensor Section							
Thermal Sensor Error		25°C to 105°C (single point)		−7	--	7	°C

Note1. Stresses beyond those listed under ”Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

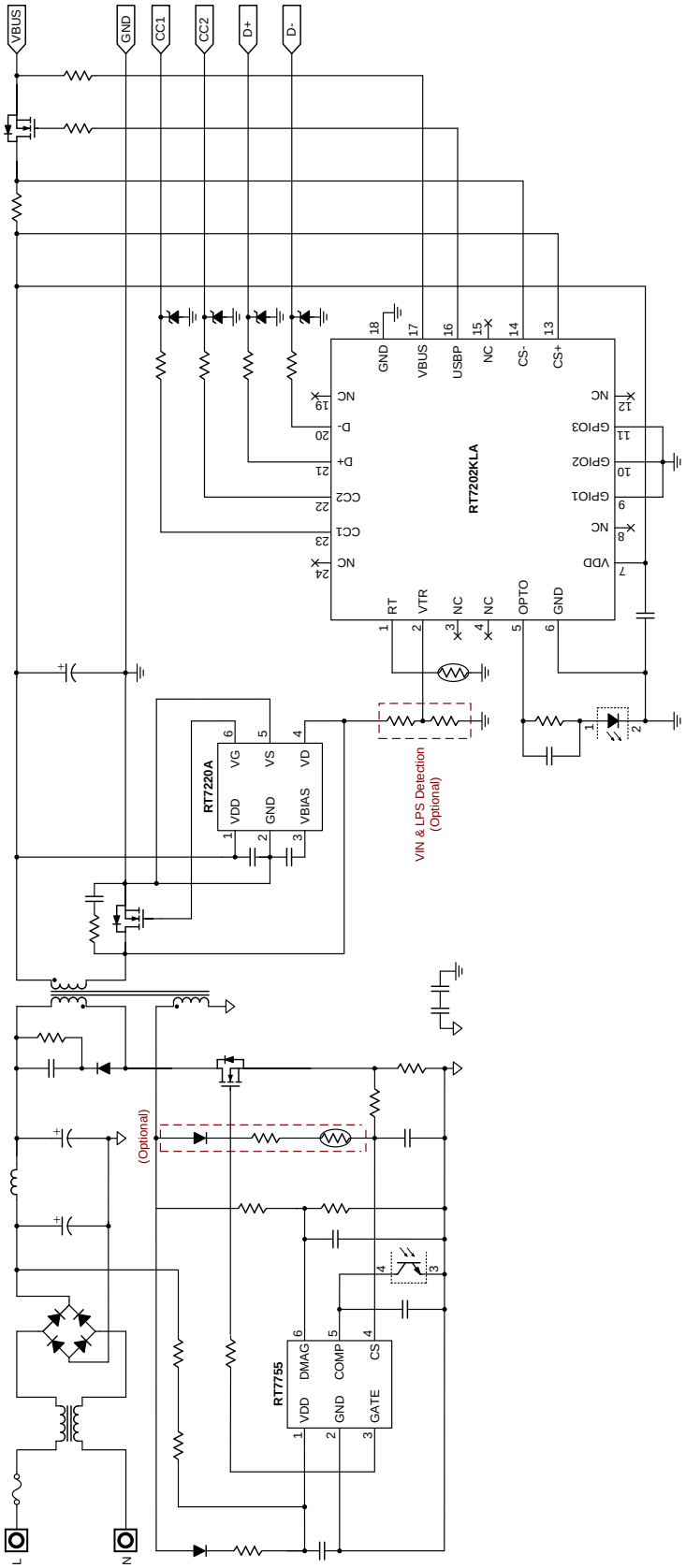
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

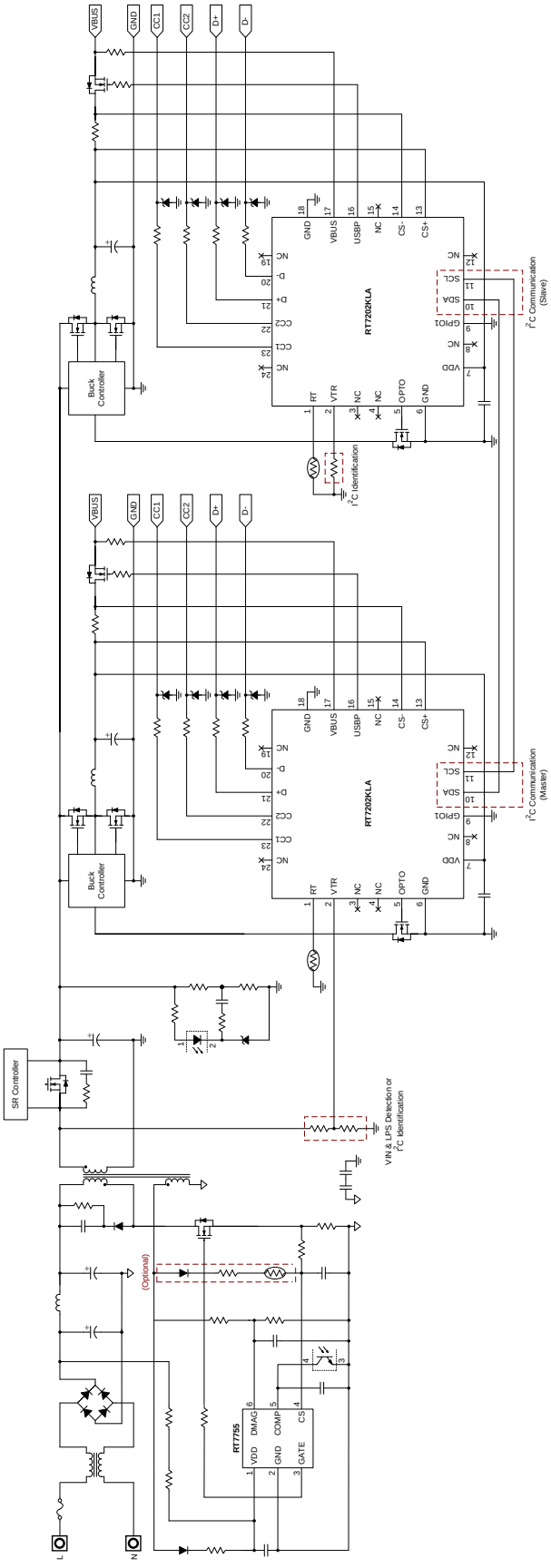
Note 5. Guaranteed by design.

Typical Application Circuit

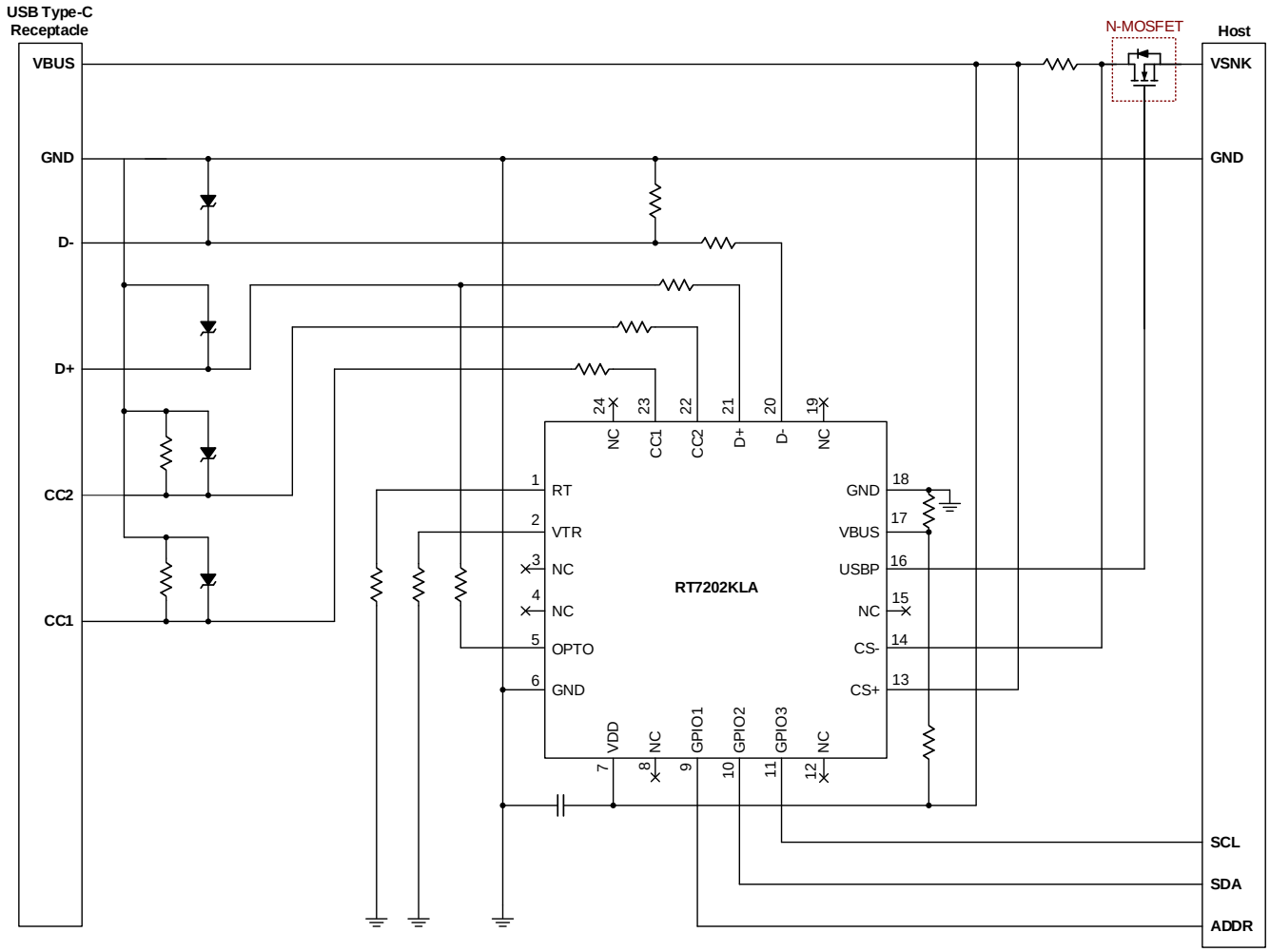
RT7202KLA for Low-Side in Source Application



RT7202KLA for High-Side with Multi-Port in Source Application

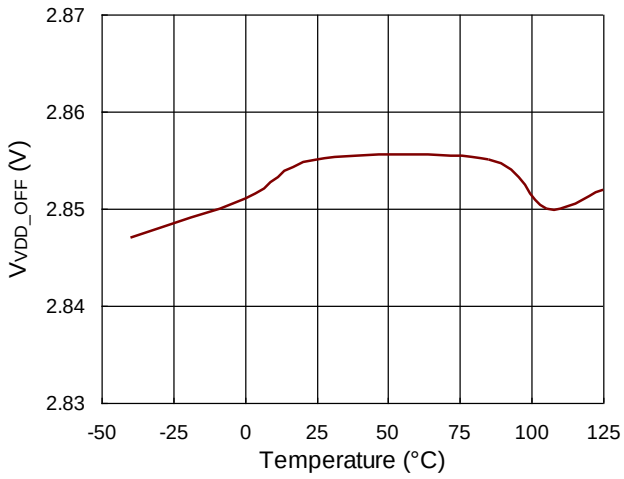


RT7202KLA in Sink Application

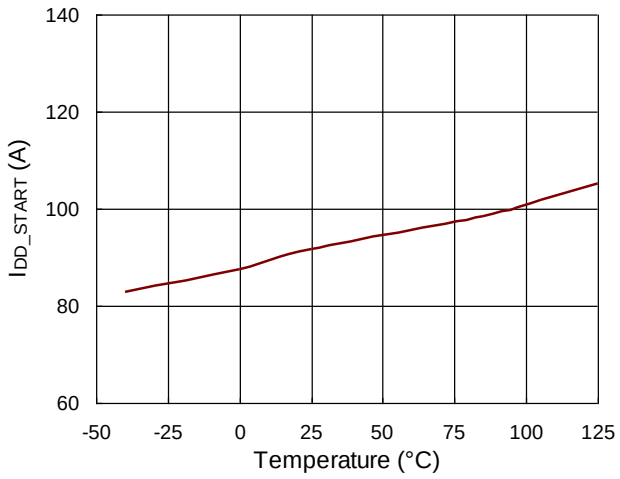


Typical Operating Characteristics

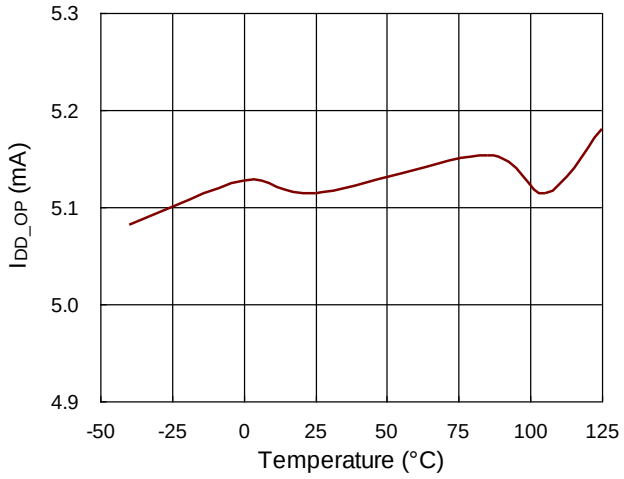
V_{VDD_OFF} vs. Temperature



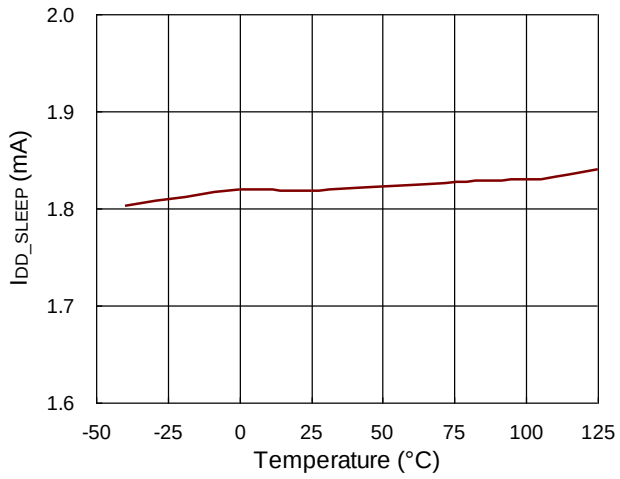
I_{DD_START} vs. Temperature



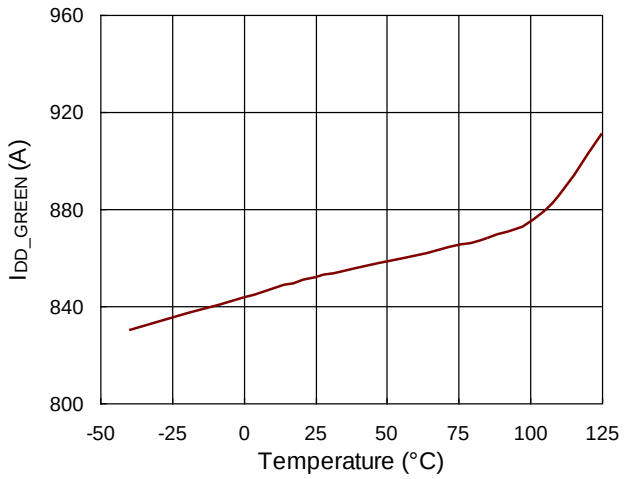
I_{DD_OP} vs. Temperature



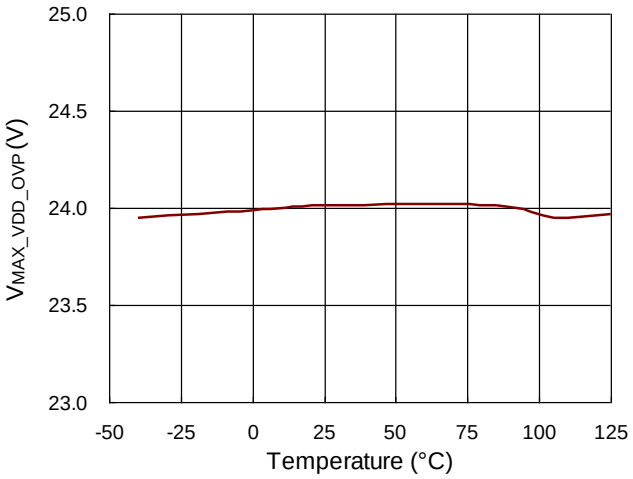
I_{DD_SLEEP} vs. Temperature

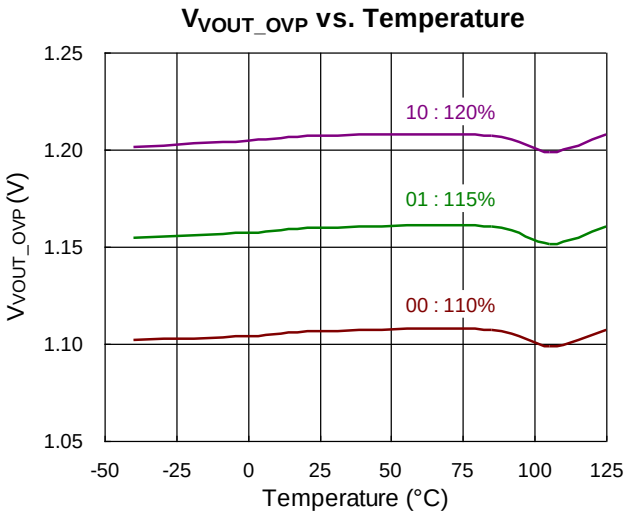


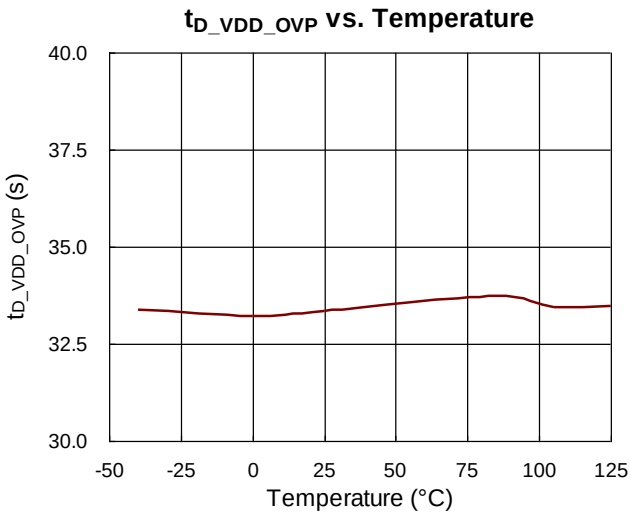
I_{DD_GREEN} vs. Temperature

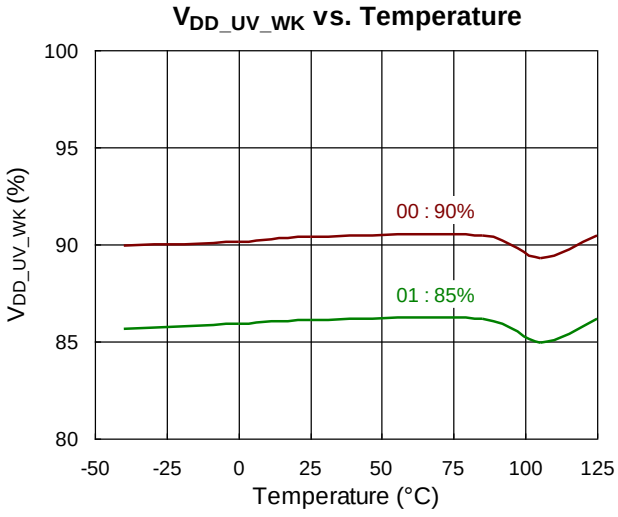


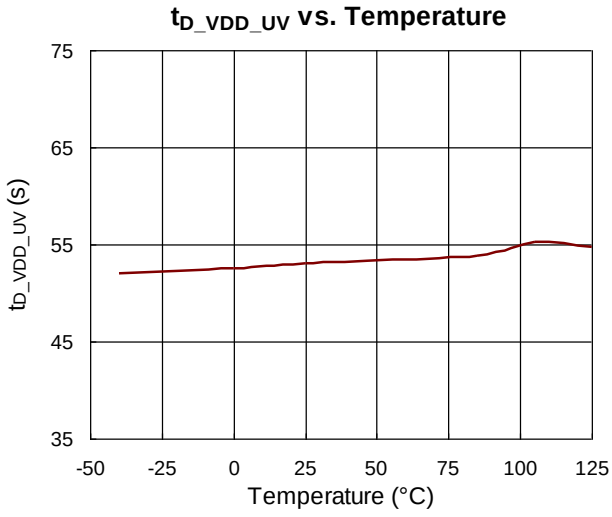
$V_{MAX\_VDD\_OVP}$ vs. Temperature

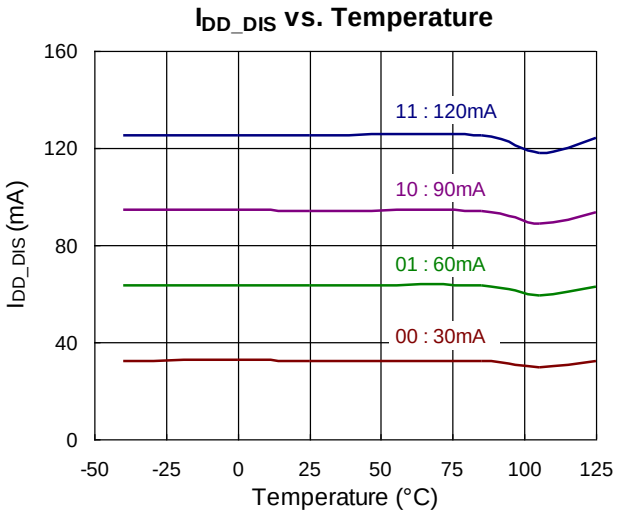


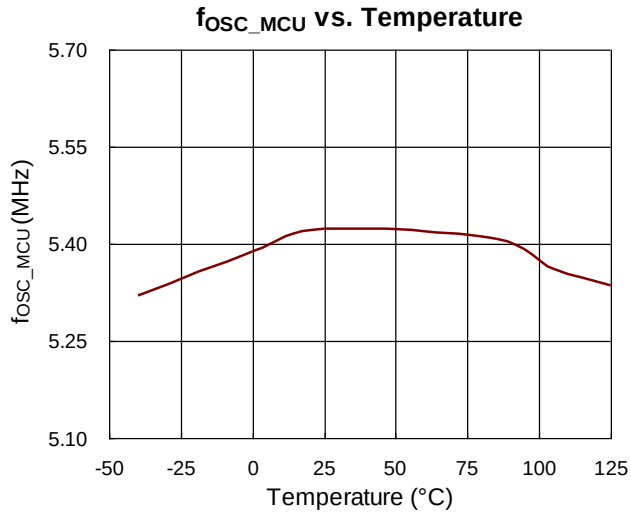




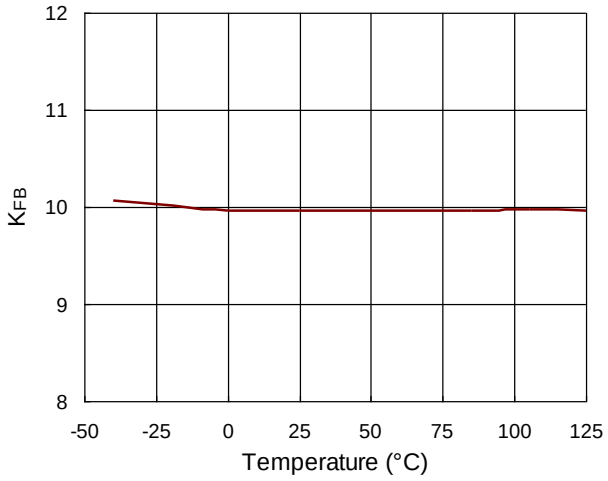




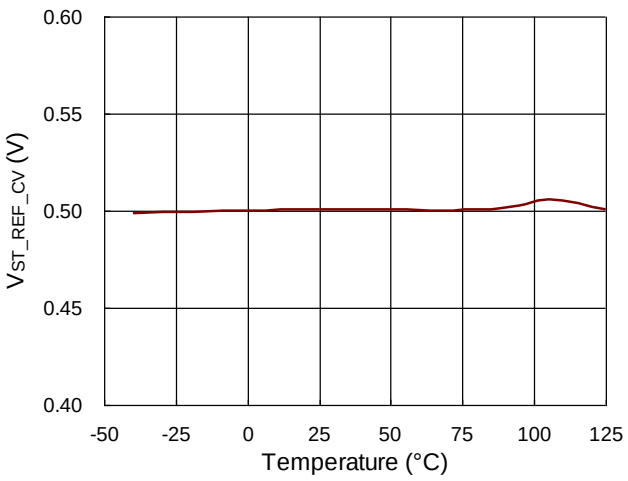




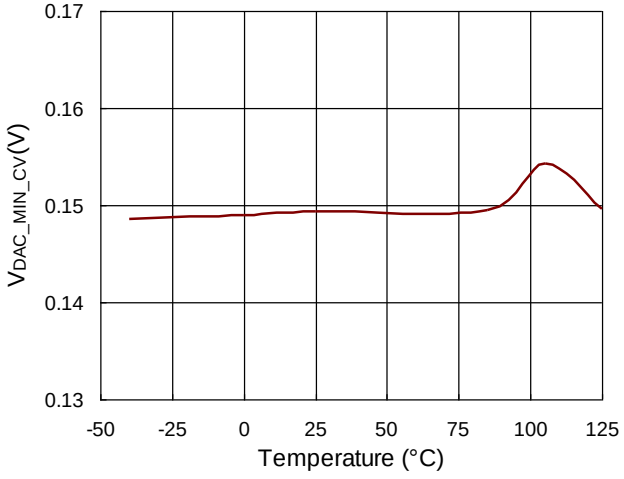
K_{FB} vs. Temperature



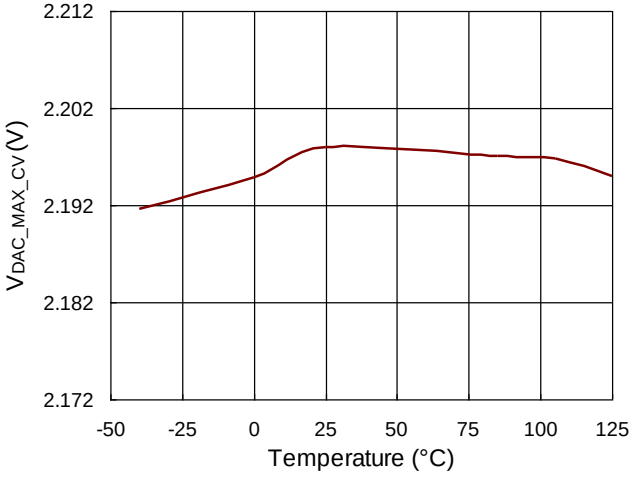
$V_{ST\_REF\_CV}$ vs. Temperature



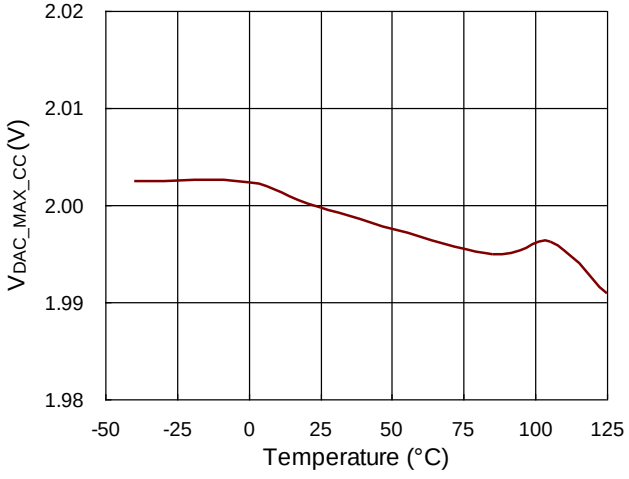
$V_{DAC\_MIN\_CV}$ vs. Temperature



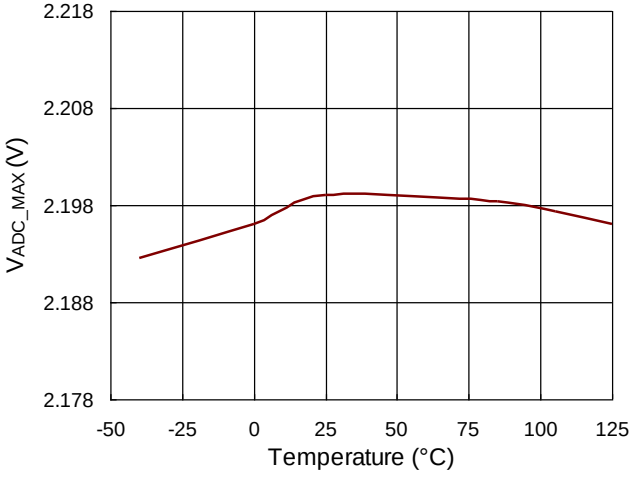
$V_{DAC\_MAX\_CV}$ vs. Temperature



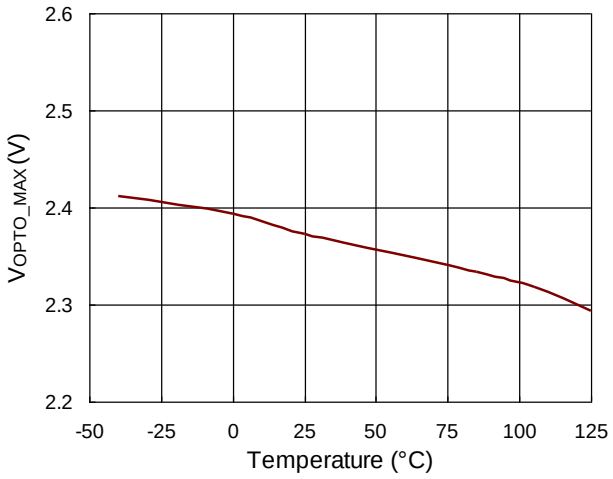
$V_{DAC\_MAX\_CC}$ vs. Temperature



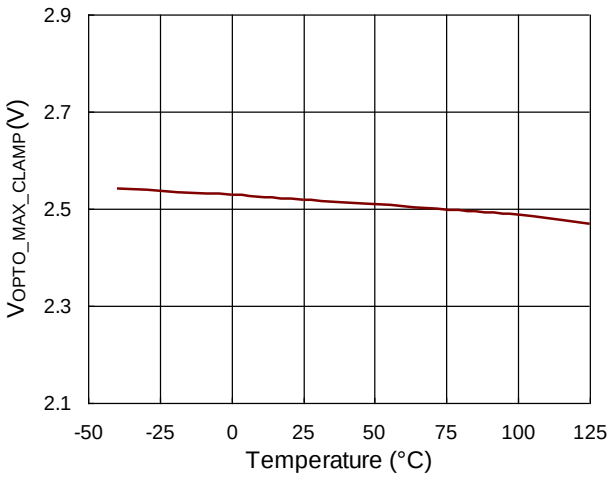
V_{ADC_MAX} vs. Temperature



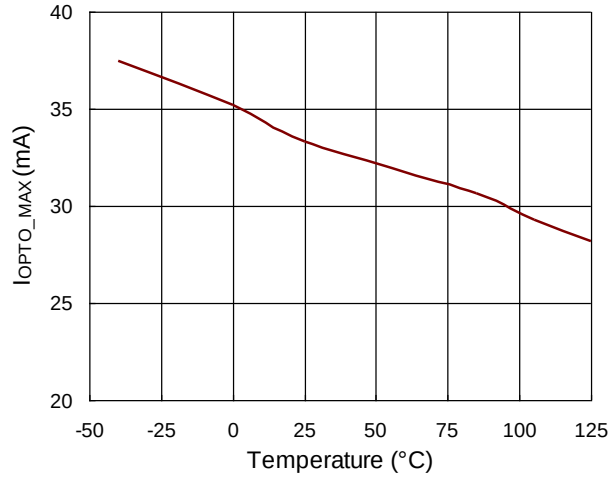
V_{OPTO_MAX} vs. Temperature



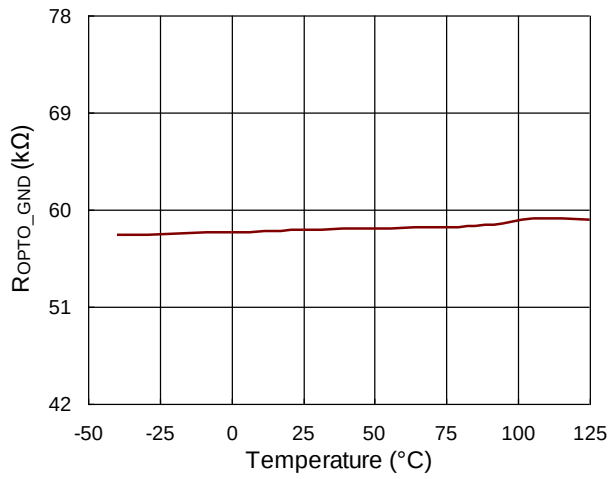
$V_{OPTO\_MAX\_CLAMP}$ vs. Temperature



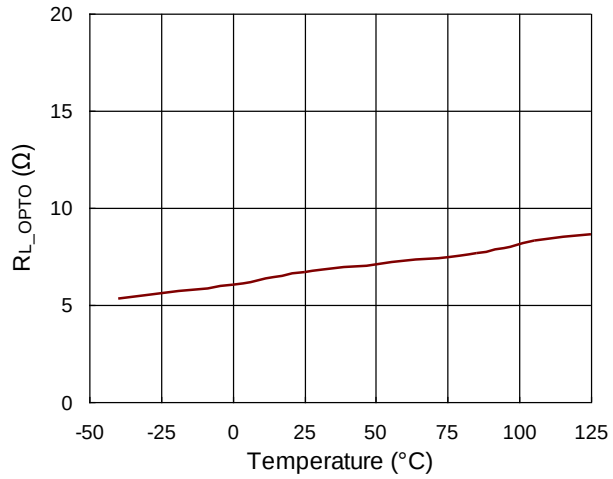
I_{OPTO_MAX} vs. Temperature



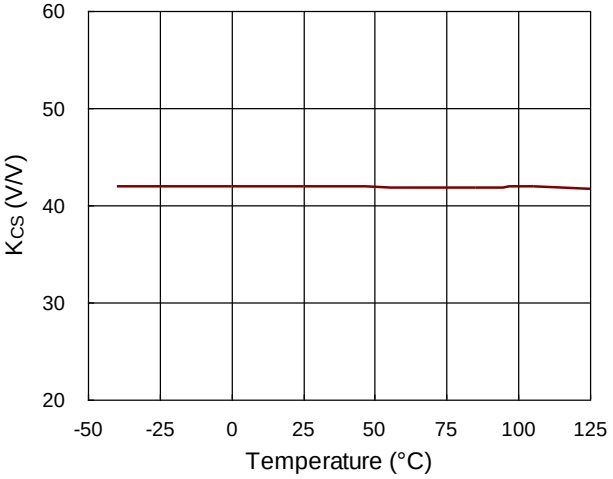
R_{OPTO_GND} vs. Temperature

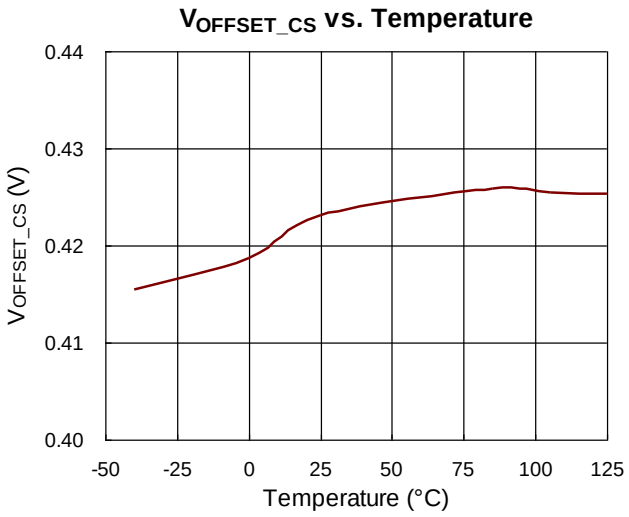


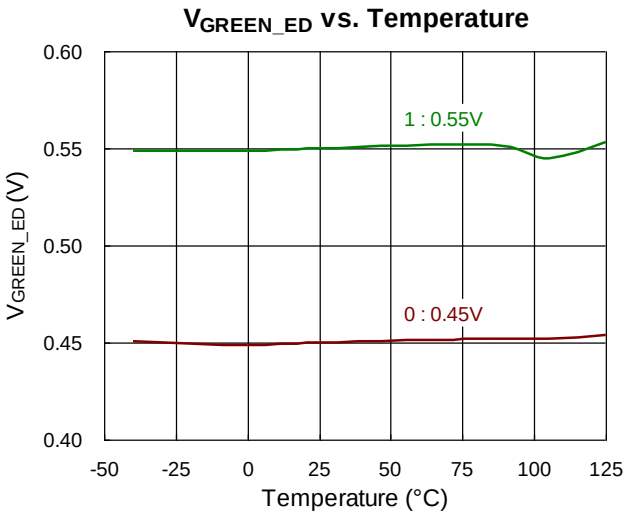
R_{L_OPTO} vs. Temperature

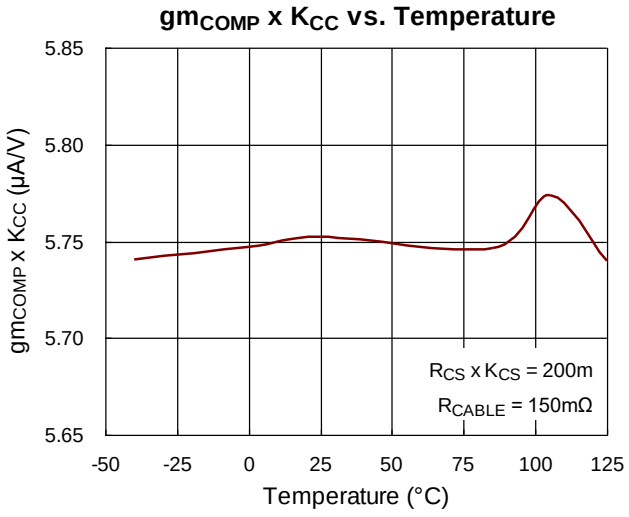


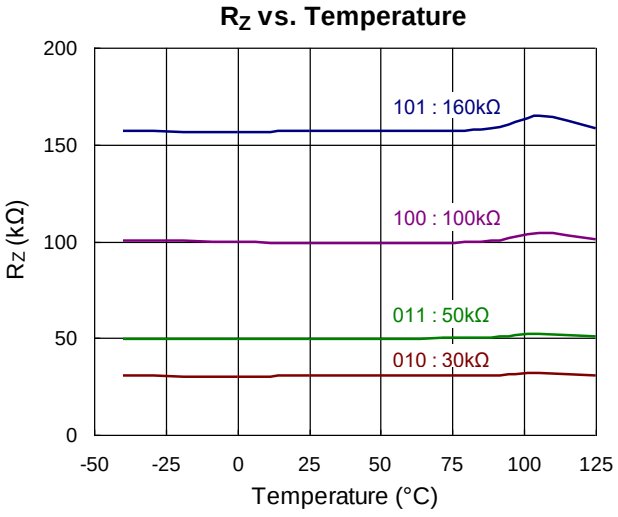
K_{CS} vs. Temperature

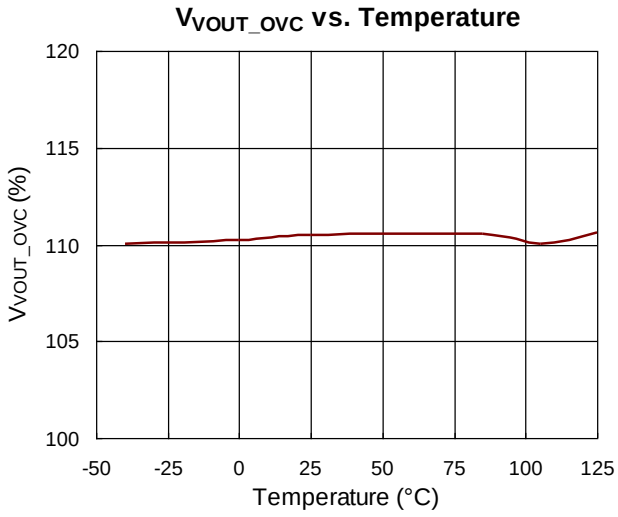


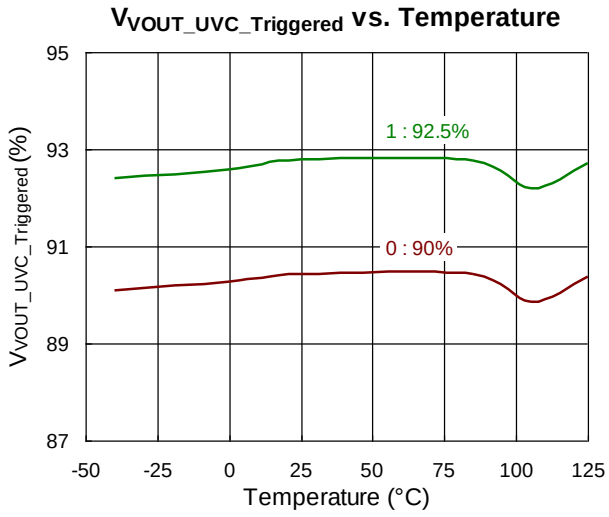




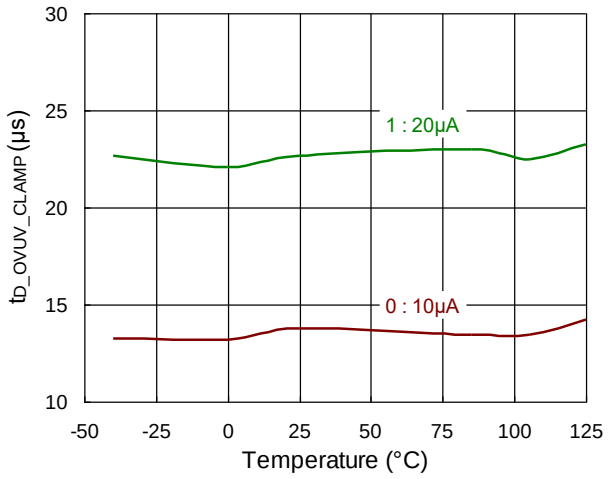




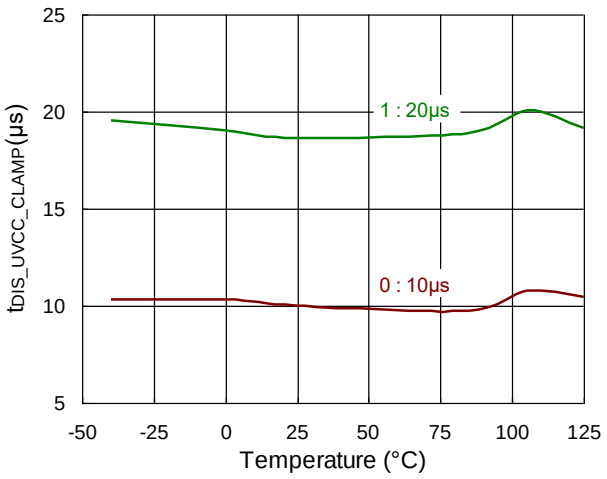




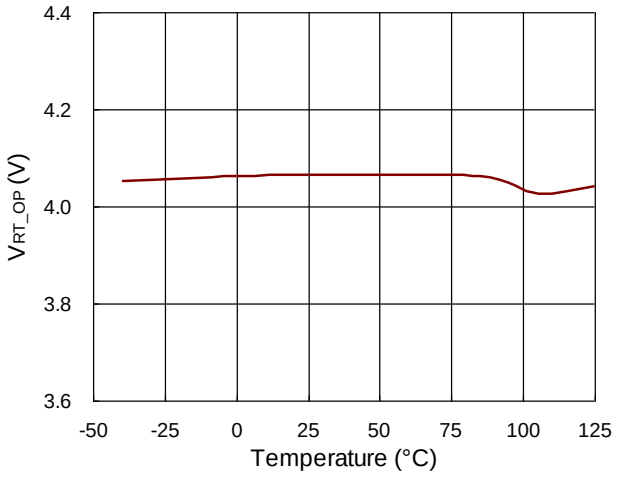
$t_{D\_OVUV\_CLAMP}$ vs. Temperature



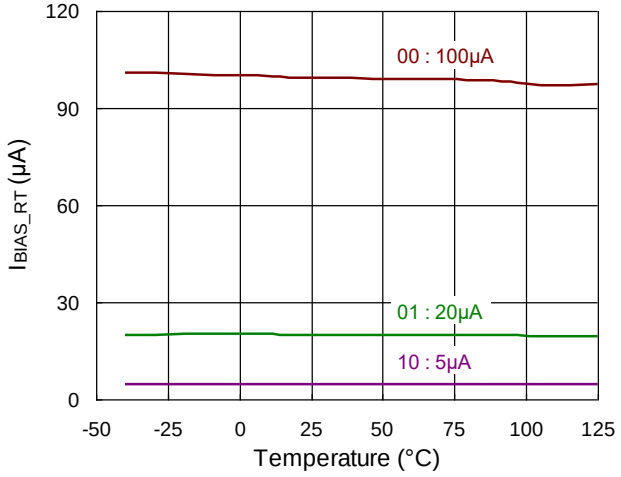
$t_{DIS\_UVCC\_CLAMP}$ vs. Temperature



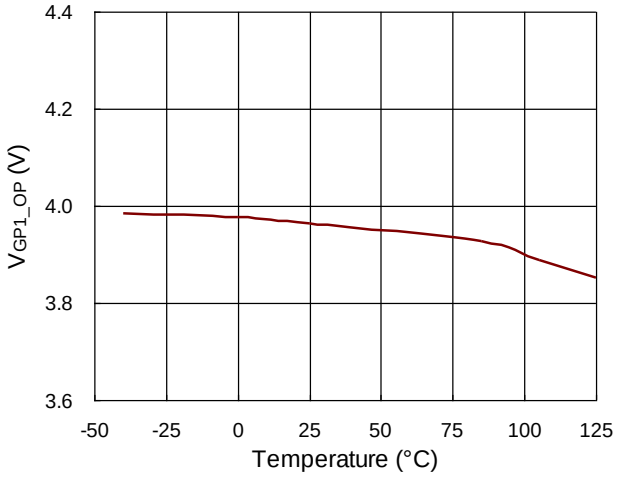
V_{RT_OP} vs. Temperature



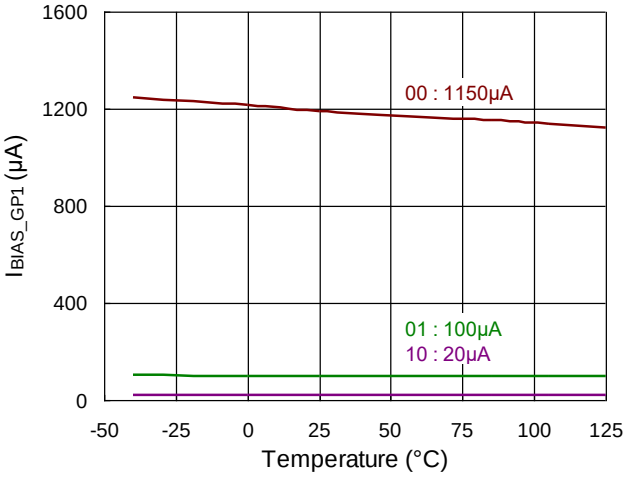
I_{BIAS_RT} vs. Temperature



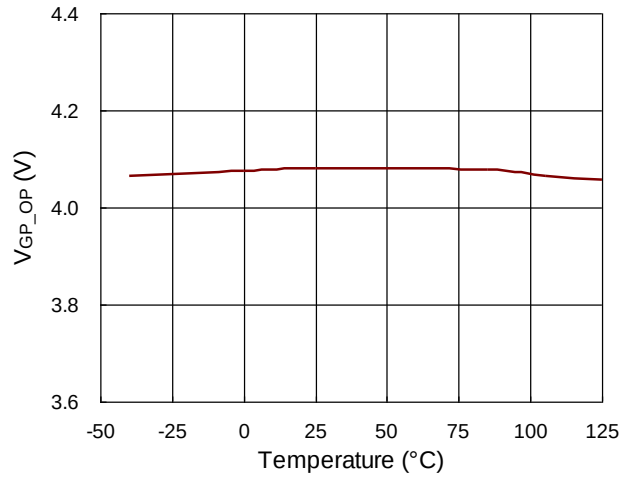
V_{GP1_OP} vs. Temperature



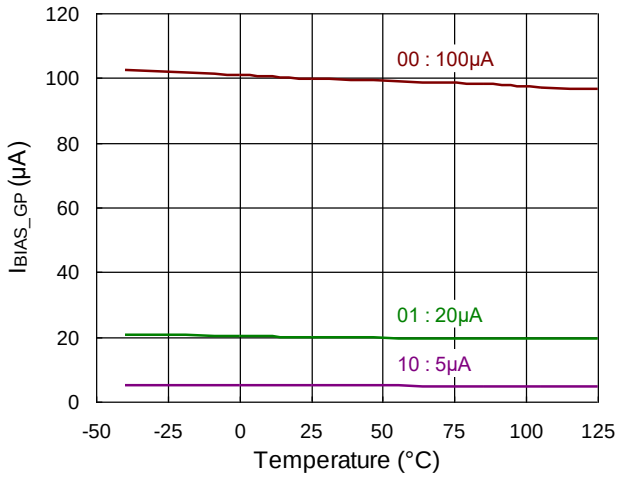
I_{BIAS_GP1} vs. Temperature



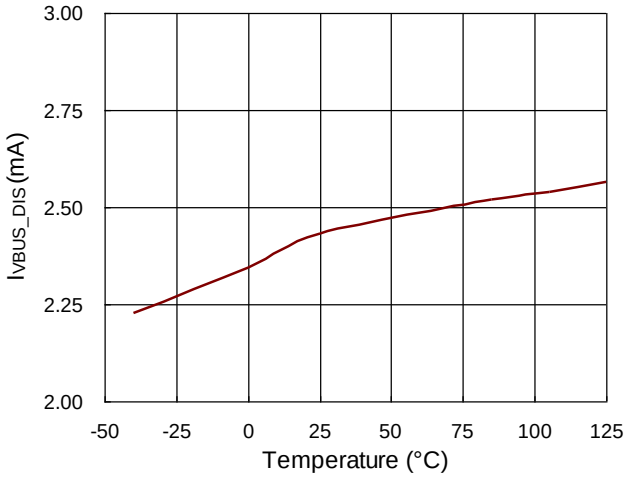
V_{GP_OP} vs. Temperature



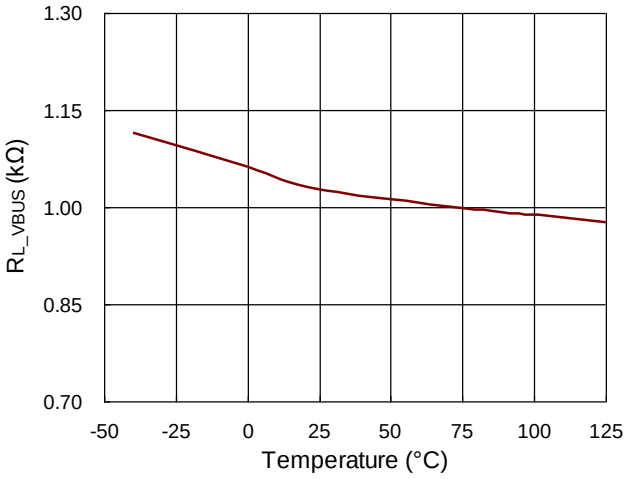
I_{BIAS_GP} vs. Temperature



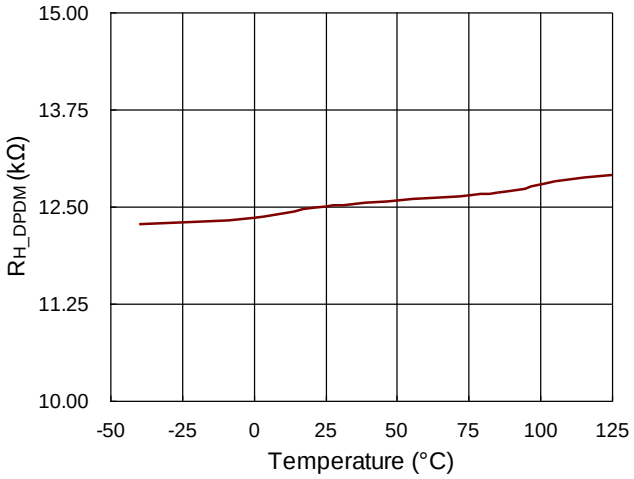
I_{VBUS_DIS} vs. Temperature



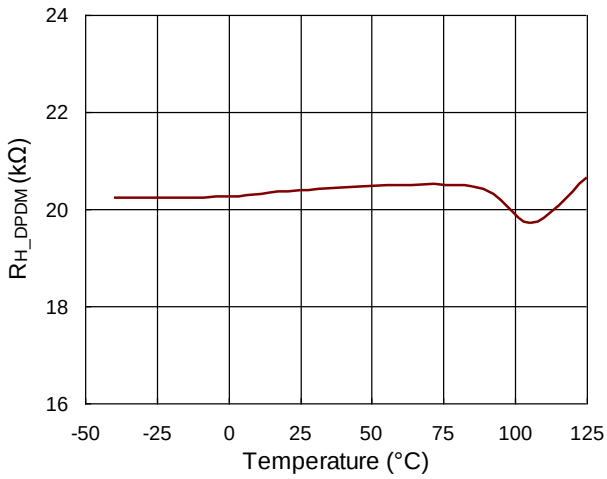
R_{L_VBUS} vs. Temperature

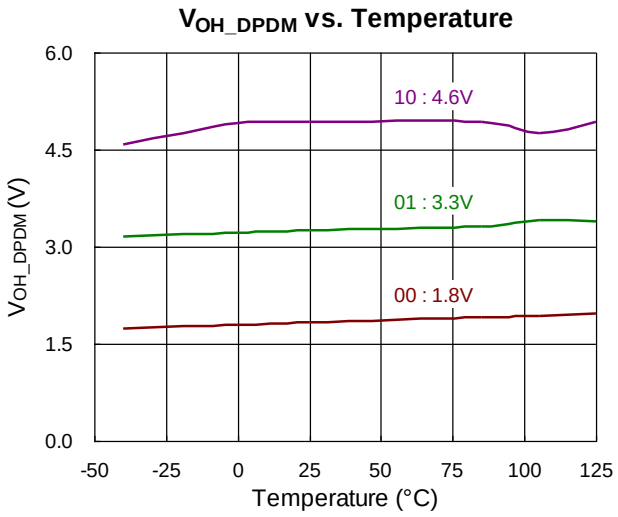


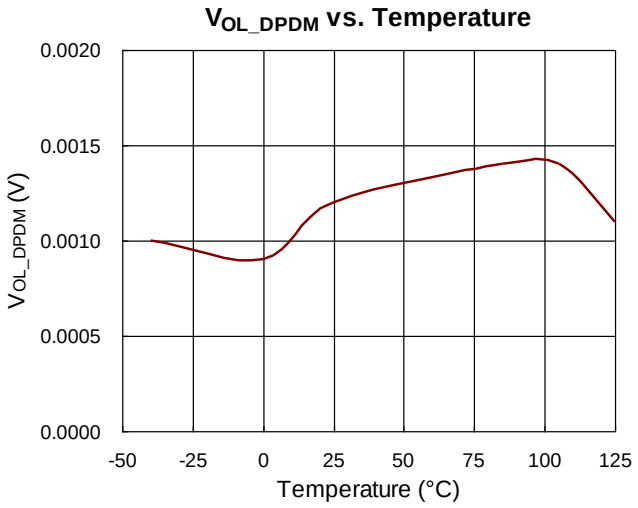
R_{H_DPDM} vs. Temperature

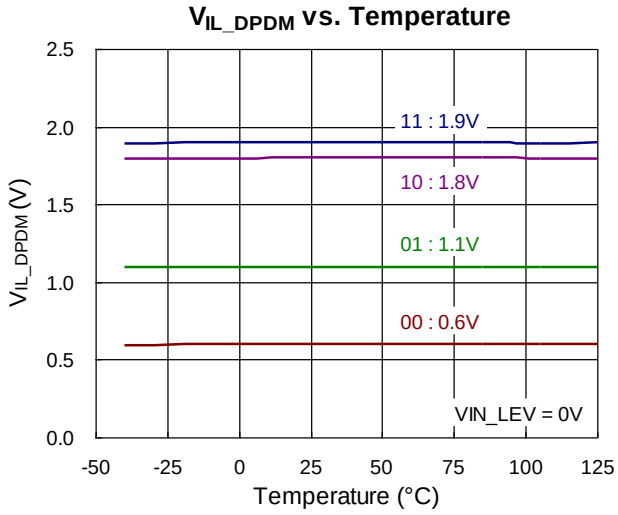


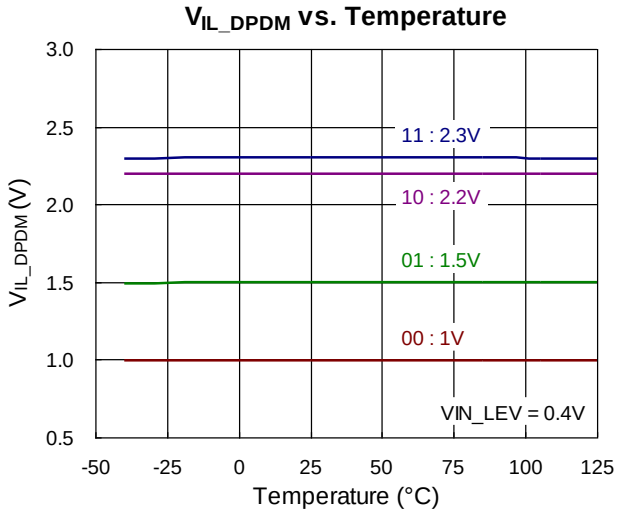
R_{H_DPDM} vs. Temperature

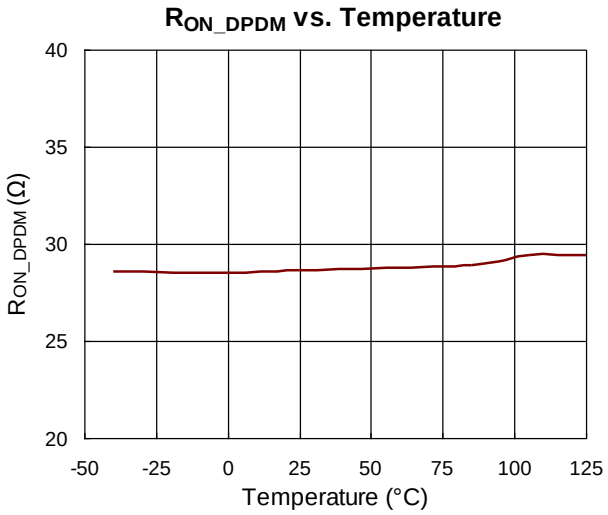


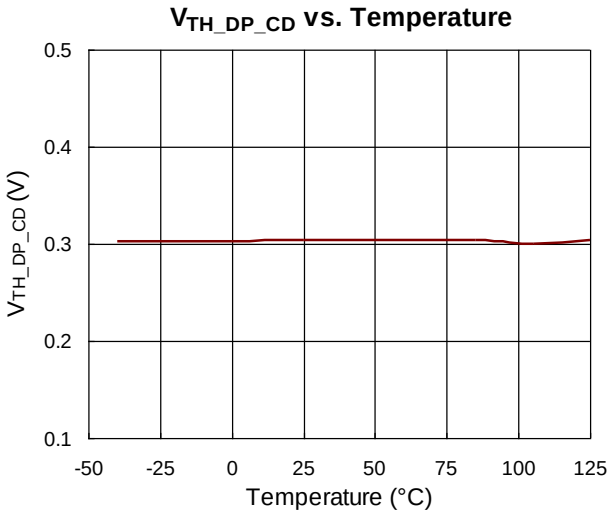


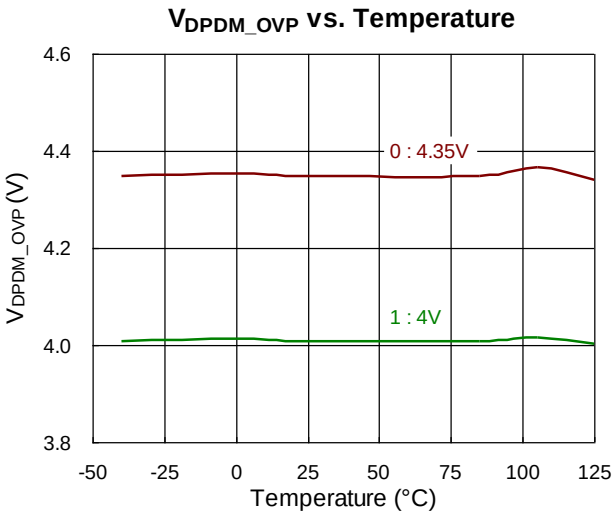


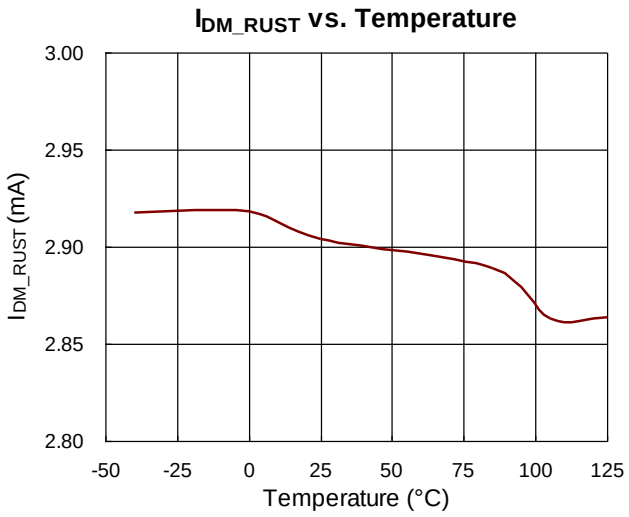


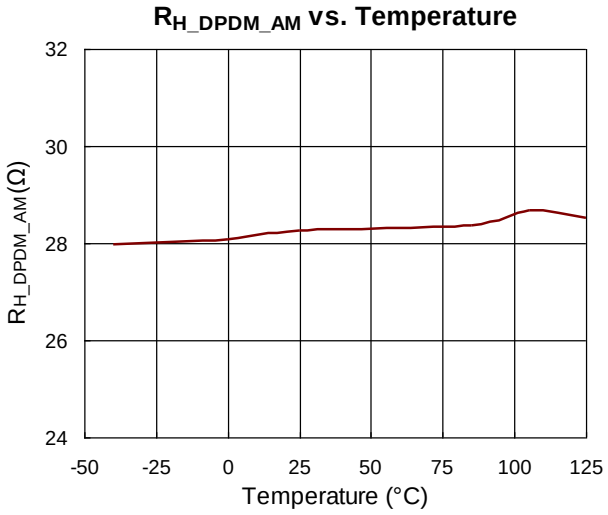


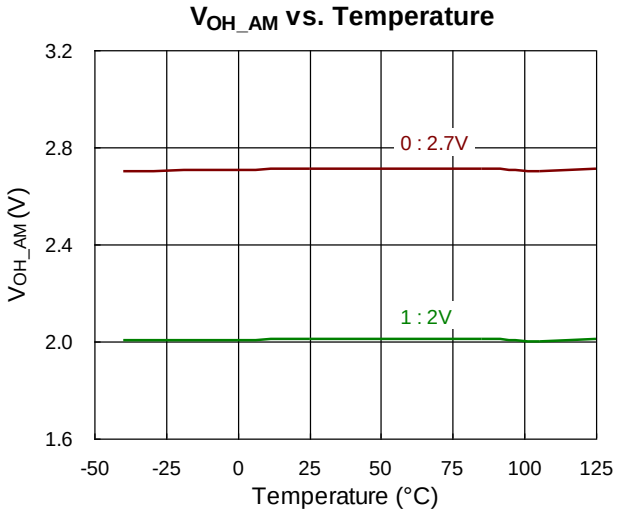


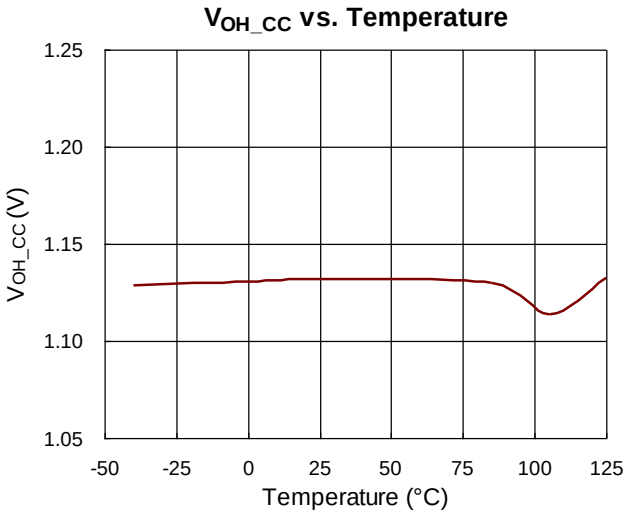


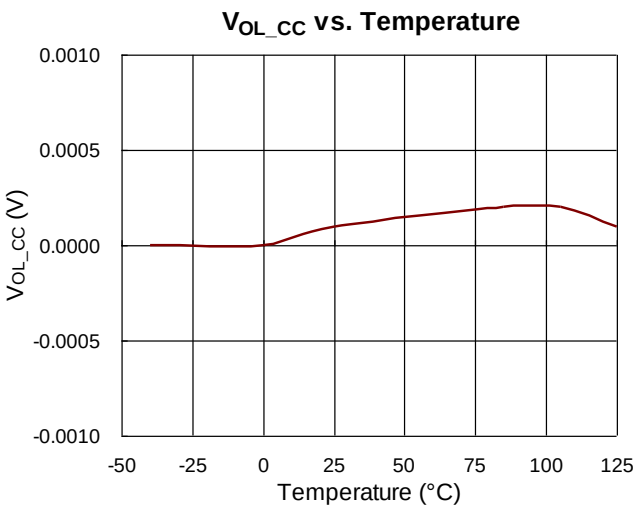


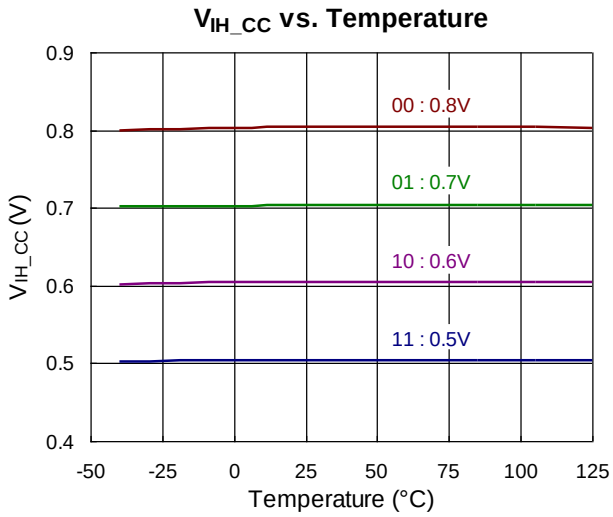


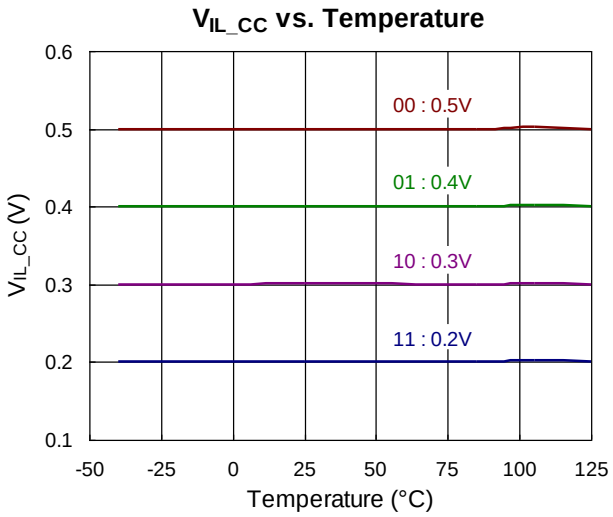


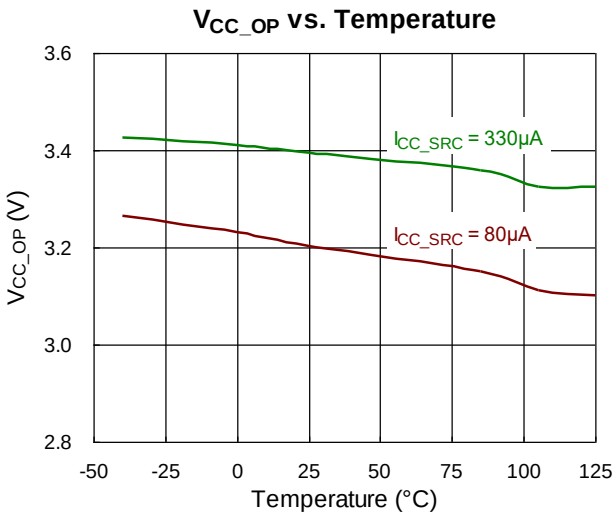


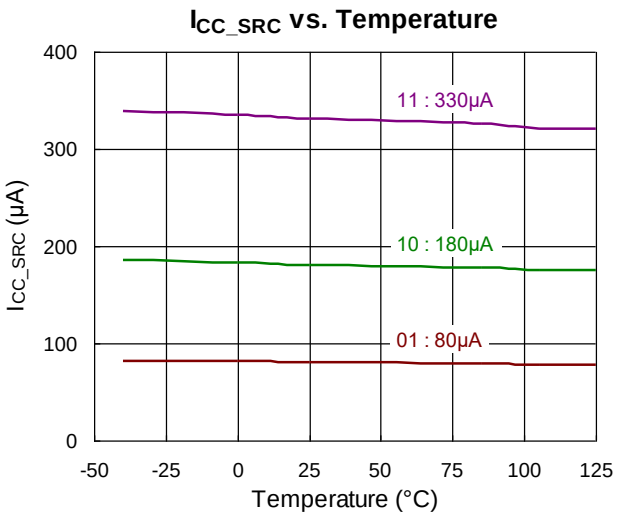


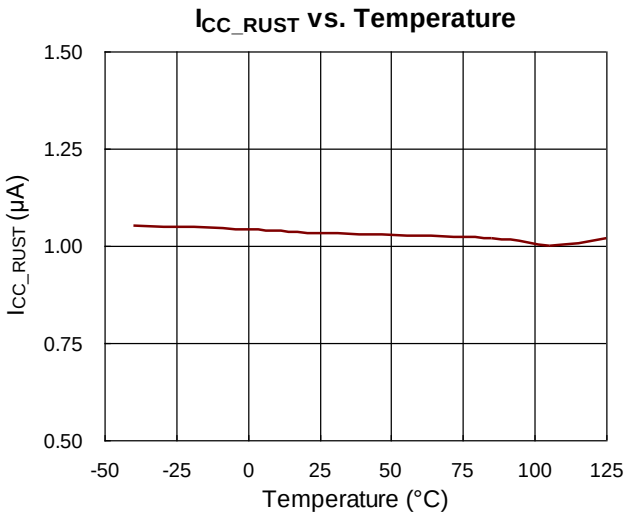


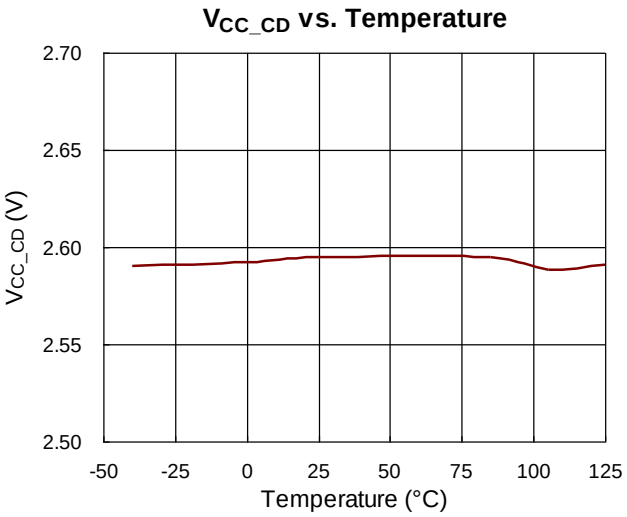




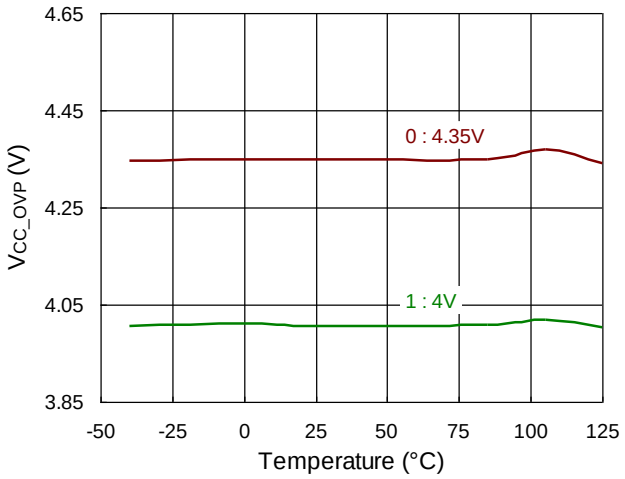




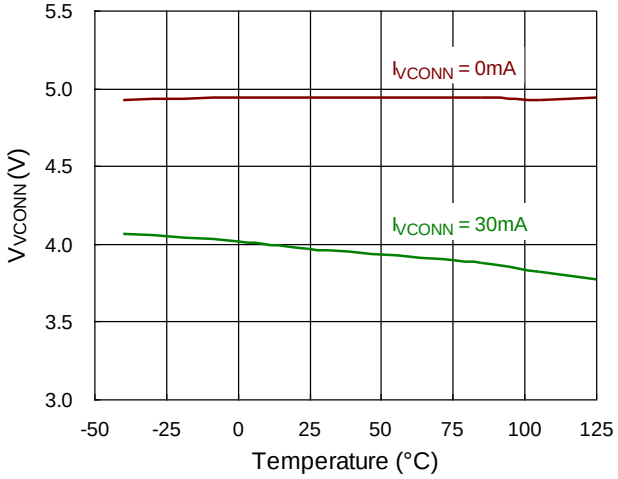




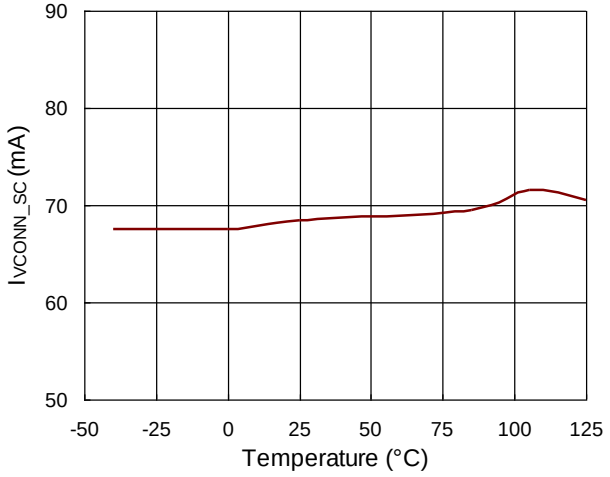
V_{CC_OVP} vs. Temperature



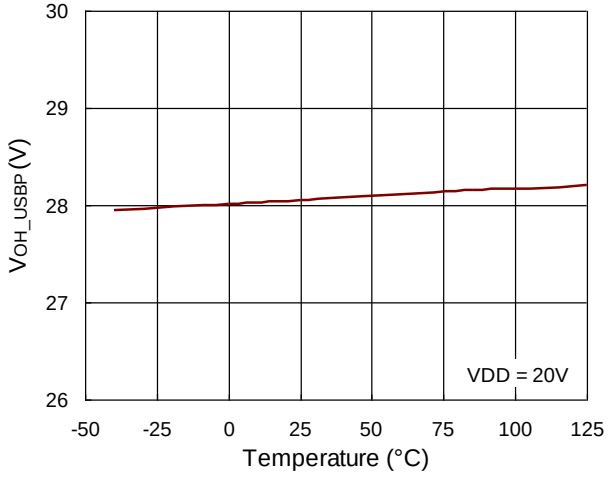
V_{VCONN} vs. Temperature



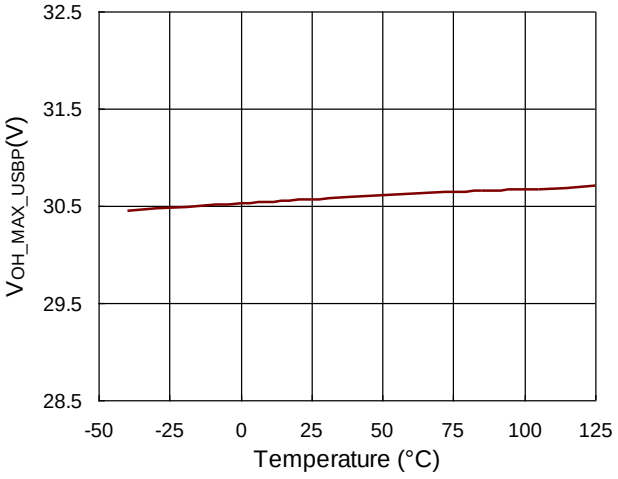
I_{VCONN_SC} vs. Temperature



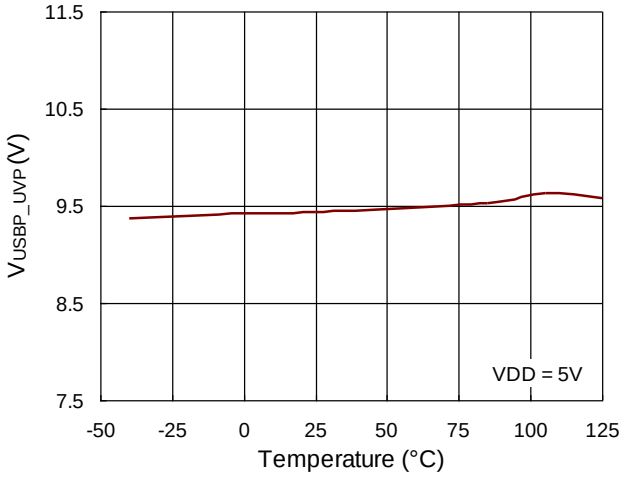
V_{OH_USBP} vs. Temperature

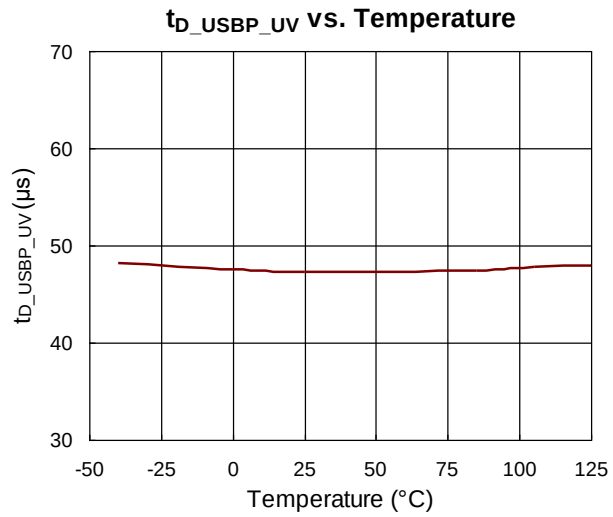


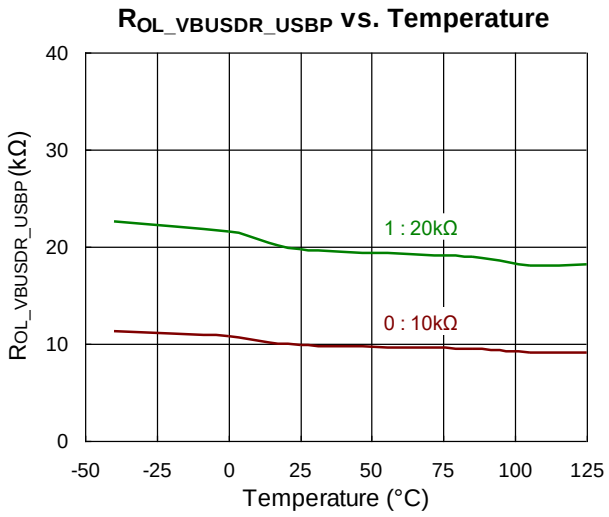
$V_{OH\_MAX\_USBP}$ vs. Temperature

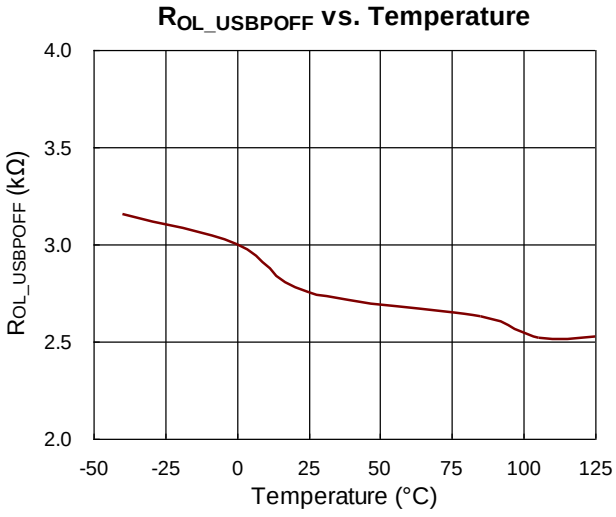


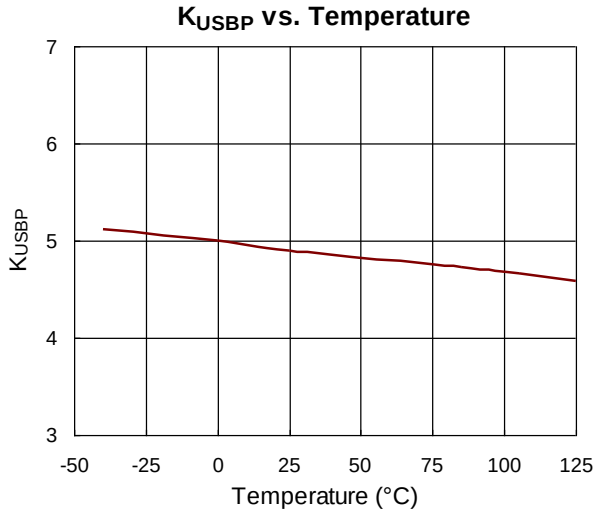
V_{USBP_UVP} vs. Temperature

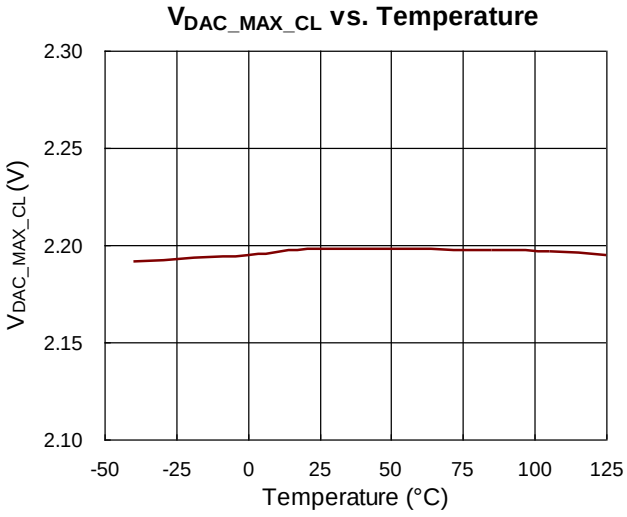


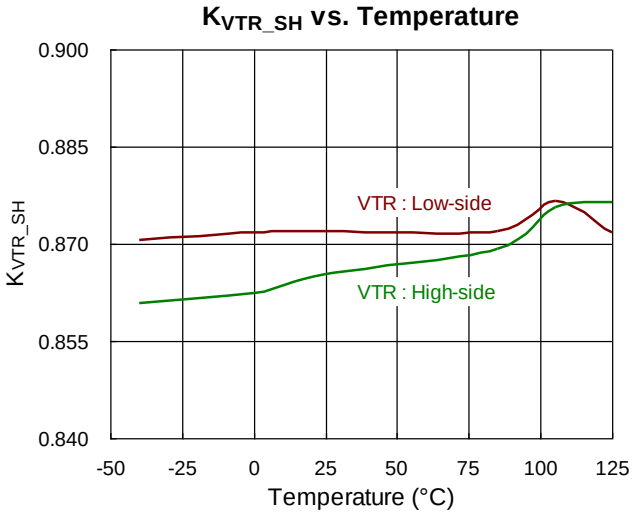


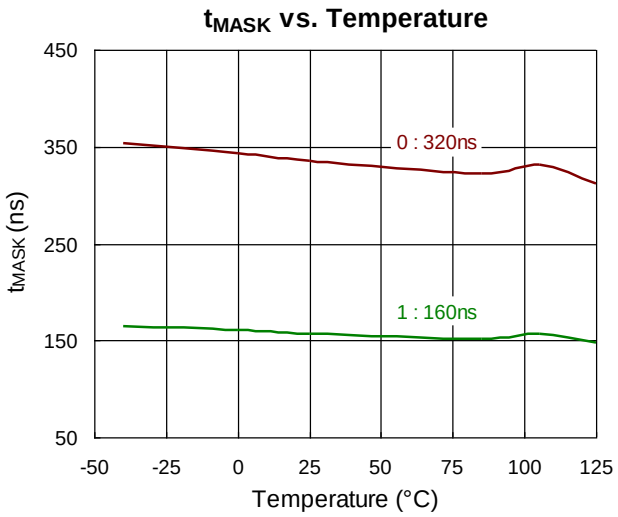


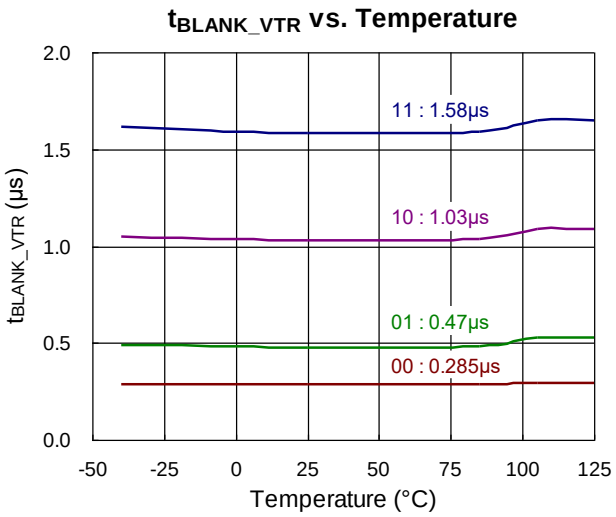


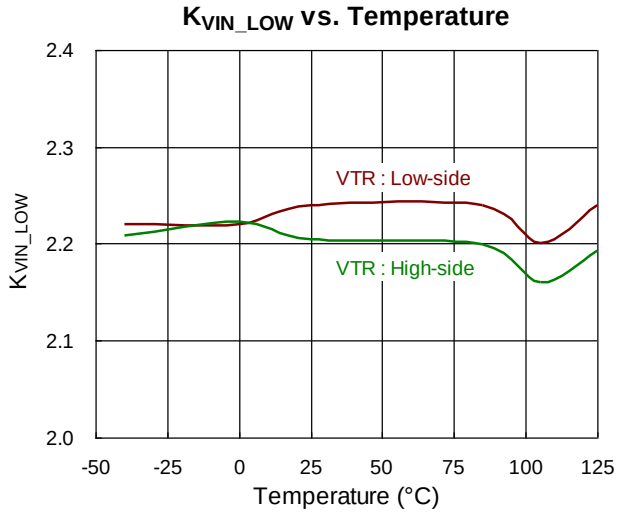


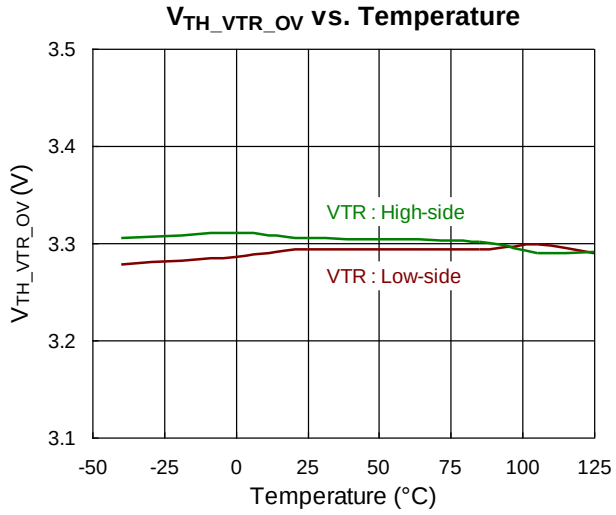


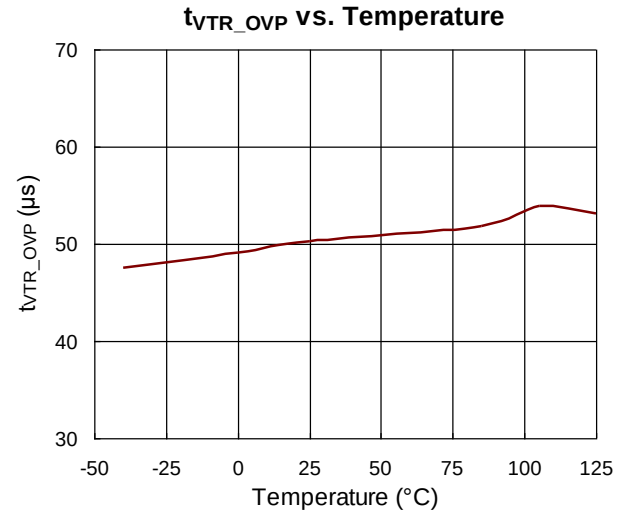


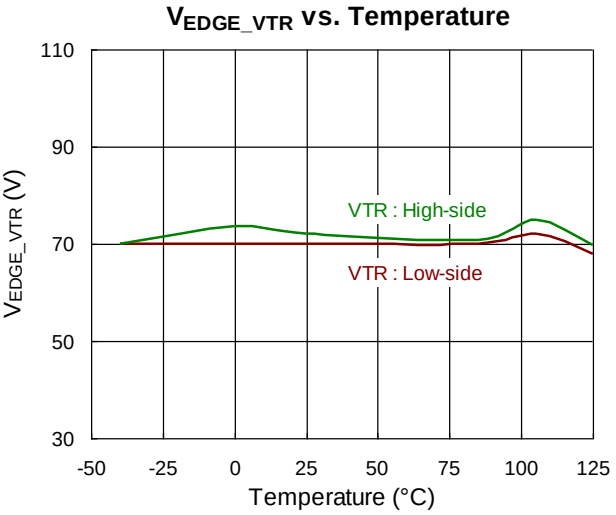




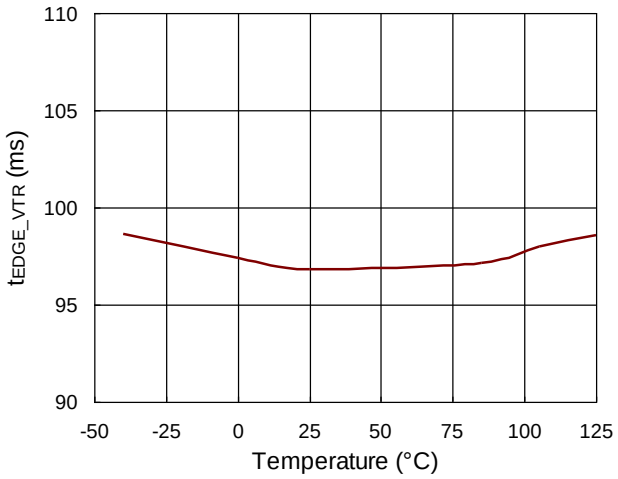




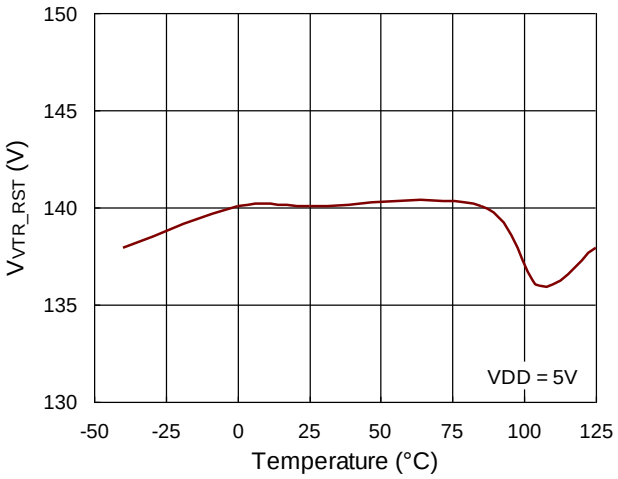




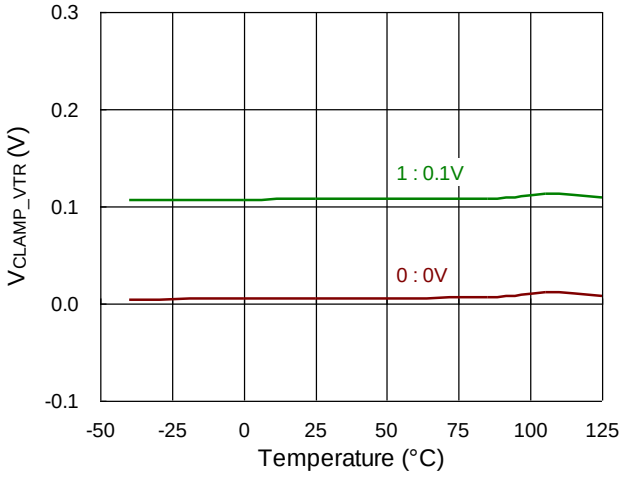
t_{EDGE_VTR} vs. Temperature



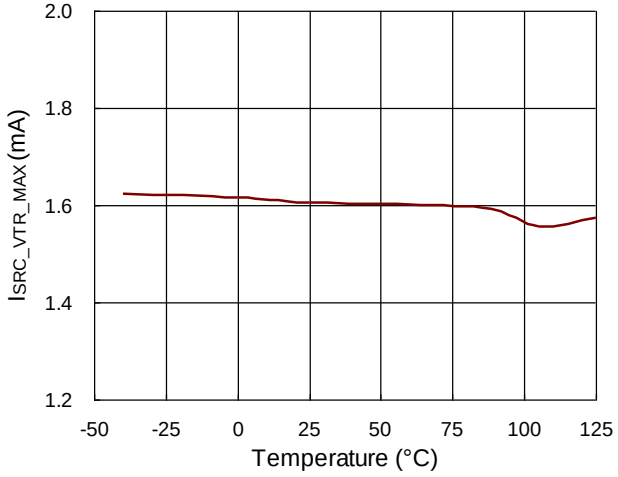
V_{VTR_RST} vs. Temperature



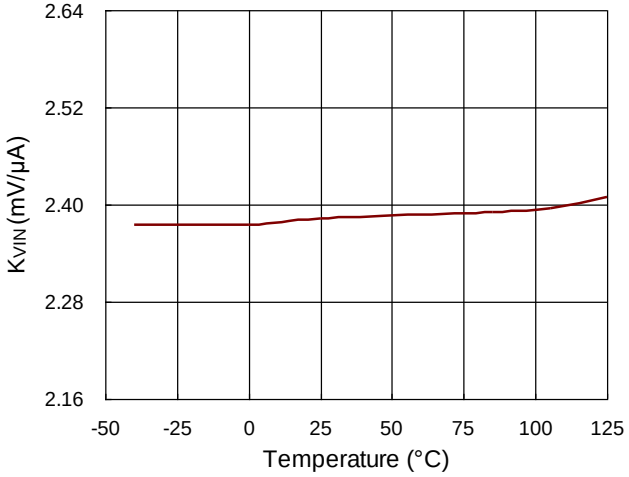
V_{CLAMP_VTR} vs. Temperature



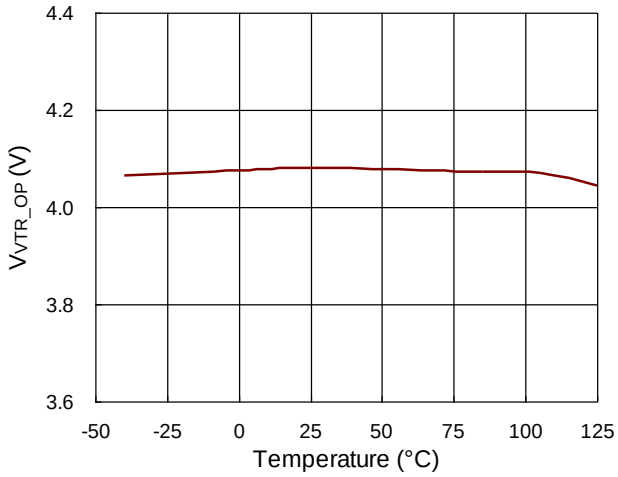
$I_{SRC\_VTR\_MAX}$ vs. Temperature

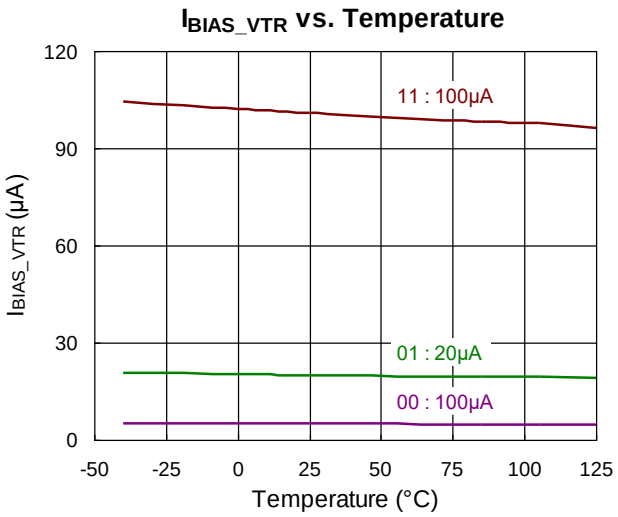


K_{VIN} vs. Temperature



V_{VTR_OP} vs. Temperature





Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

Constant Voltage (CV) Loop

As shown in Figure 7, the RT7202KLA integrates two transconductance amplifiers, which are connected to the feedback compensation to regulate the output voltage and current, respectively. The output voltage is determined as :

$V_{OUT} = K_{FB} \times V_{REF\_CV}$

Where

$K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2} = 10$

Therefore, the V_{OUT} is determined by V_{REF_CV}, the analog output from the DAC, which is controlled by MCU.

Constant Current (CC) Loop

As shown in Figure 7, the RT7202KLA integrates a virtually zero input offset current-sense amplifier with differential mode inputs to minimize noise interference. The sensed signal, I_{o_signal}, is fed into an 11-bit ADC to be monitored and processed by the MCU. The reference voltage of the CC loop is determined by V_{REF_CC} (from the DAC), which is programmed by the requirements of charger.

The constant voltage and the constant current compensation loops are both connected to the feedback compensation. The OPTO driver sources current through an external resistor R_{OPTO} and an optocoupler that isolates the secondary side from the primary side and then feedbacks the compensation signal to the primary side. Note that for better linearity of the loop compensation range, R_{OPTO} should be designed to cover the operation at the minimum output voltage.

$$\frac{(V_{OPTO\_MAX} - V_F)}{R_{OPTO}} \times CTR \geq I_{COMP\_MAX}$$

where

CTR : Current transfer ratio of the optocoupler;

V_F : Forward voltage of the optocoupler;

V_{OPTO_MAX} : The maximum OPTO voltage for the OPTO driver to sourcing 1mA;

I_{COMP_MAX} : The maximum COMP sourcing current of a traditional PWM controller in the primary side. It is a current sourced from an internal bias through a built-in pull-high resistor connected the COMP pin in the PWM controller.

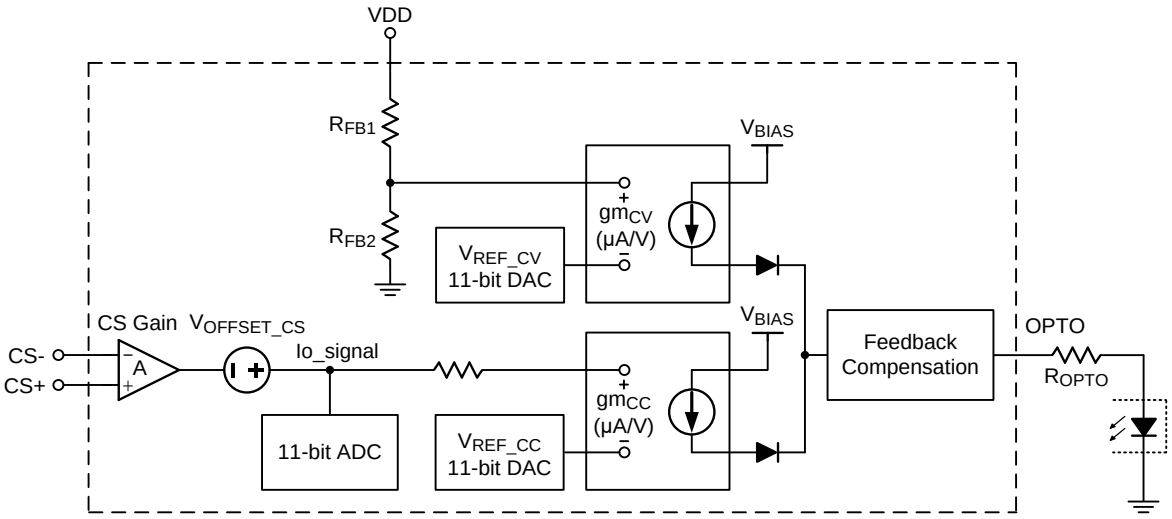


Figure 7. CV and CC Loops

Internal Feedback Compensation

The RT7202KLA has a built-in feedback compensator that optimizes system stability and response for different applications and furthermore reduces the external component counts.

The feedback compensation design is based on the system operation mode and component parameters. An off-line flyback converter mostly uses a Type-II compensator to compensate for the feedback loop. It has a zero frequency pole, a low frequency zero and a high frequency pole. The feedback compensation design is to make the low frequency zero point of compensator to compensate the low frequency pole point of system and make the high frequency pole point to compensate the ESR zero point of output capacitor. By the proper compensation, the system can achieve a better phase margin. In addition, a proper middle gain of compensator is chosen to get the better transient response, and improve the system stability.

The RT7202KLA provides a simple and flexible design for feedback compensation. The RZ, CZ and middle gain of the compensator can be programmed according to different output conditions. With this feature, one can easily achieve a stable system by using this flexible design for compensation.

Power-Up Sequence

Figure 8 shows the timing diagram for the power-up sequence. When start-up, the default output voltage is set at 5V. Once a Type-C cable is attached, the UFP will deliver voltage and current settings to the RT7202KLA for the MCU to decode and to program reference voltages, V_{REF_CV} and V_{REF_CC}, for the CV and CC loops, which are the analog outputs converted by the DAC. If the Type-C cable is detached, or the output current is lower than the power-saving mode threshold, which is typically programmed as 200mA, and consequently the RT7202KLA will enter the power-saving mode, under which the RT7202KLA operates at ultra-low operating current and thus the total input power can be tremendously saved. Meanwhile if the output current increases and exceeds the power-saving mode threshold, or any input/output signal is toggled, the RT7202KLA will exit from the power-saving mode.

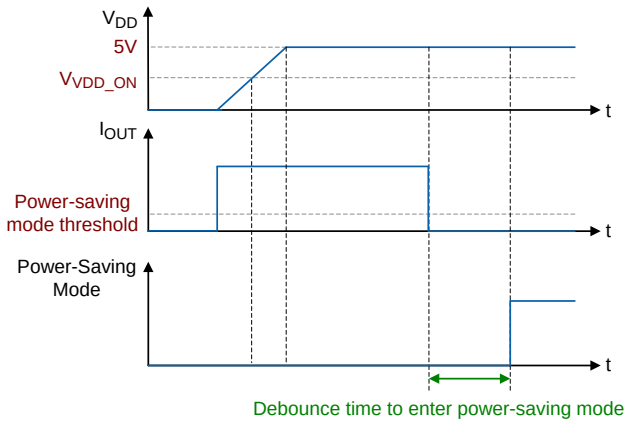
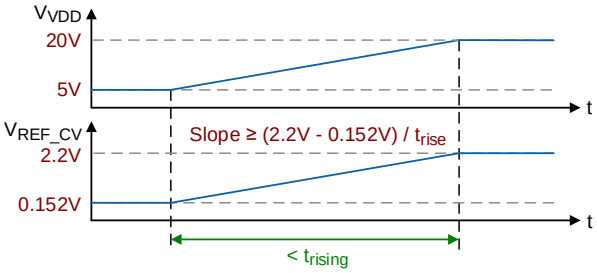


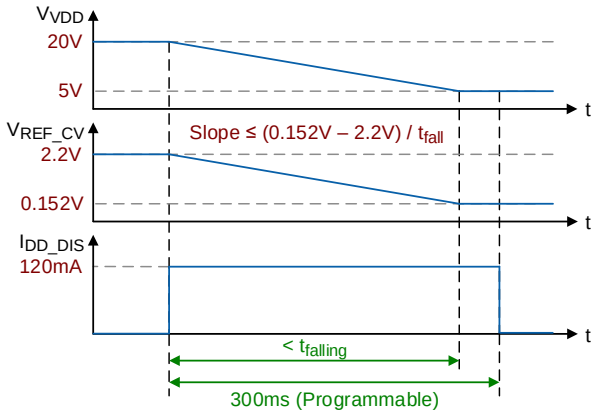
Figure 8. The Bias Voltages Sequence during Start-Up

Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of UFP. Both the rise time and fall time of output voltages should be less than the defined specification, as shown in Figure 9.



(a) Output Voltage Rising



(b) Output Voltage Falling

Figure 9. Output Voltage Transient Waveforms

The RT7202KLA provides a control for the discharge current from the VDD pin. This function utilizes a bleeder to help discharge the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as VOUT from 20V to 5V. The discharge current can be programmed by the internal register according to VDD voltage level, as shown in Figure 10.

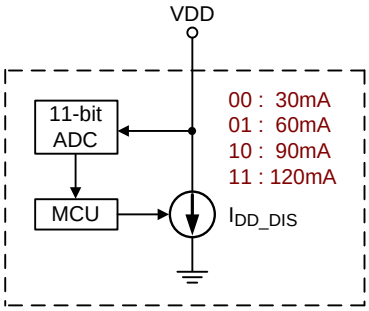


Figure 10. Discharge Current Control from VDD Pin

Linear Cable Compensation with Temperature Compensation

The RT7202KLA is based on the output current to adjust the feedback control voltage (V_{FB}) to implement a linear cable compensation, as shown in Figure 11. The transconductance amplifier gain (gm_{COMP}) and the cable compensation gain (K_{CC}) can be set by the internal register.

$$V_{CABLE\_COMP} = I_{OUT} \times K_{CS} \times K_{CC} \times gm_{COMP} \times R_{FB1}$$

where

K_{CS} : Current sense gain

K_{CC} : Cable Compensation Gain

gm_{COMP} : Transconductance amplifier gain

R_{FB1} : V_{DD} upper divider resistor

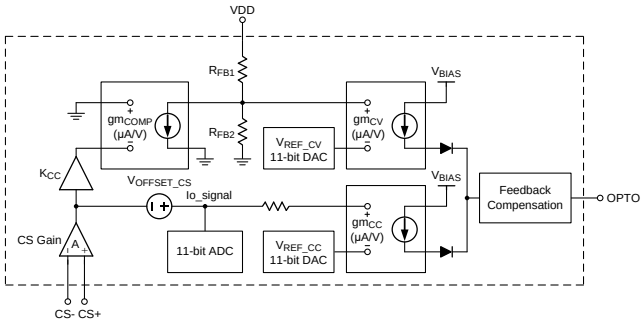


Figure 11. Linear Cable Compensation

Output Over-Voltage Protection

As shown in the Figure 12 and Figure 13, the RT7202KLA provides a fast turn-off blocking N-MOSFET as a backup VOUT over-voltage protection, in case the optocoupler of the feedback loop is malfunction due to aging. If the internal voltage related to VDD is higher than the programmable threshold V_{VOUT_OVP}, the blocking N-MOSFET will be turned-off. The OPTO pin voltage will be latched high until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}.

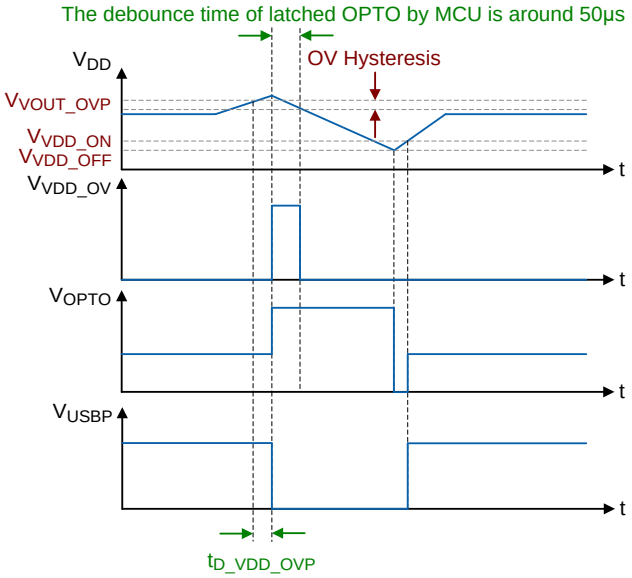


Figure 12. Timing Sequence of the OVP Function

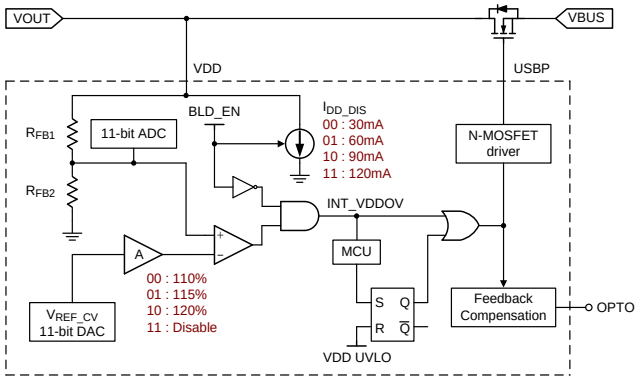


Figure 13. OVP Functional Diagram

Blocking N-MOSFET Control

The RT7202KLA provides a charge-pump driver for controlling an external blocking N-MOSFET, which is shown in figure 14. The blocking N-MOSFET can be quickly turned off in any fault condition. Once the communication is set up with an UFP, or a 5.1kΩ resistor at the CC1/CC2 pin of a Type-C connector is detected, the N-MOSFET will be turned on. If VOUT over-voltage condition occurs, the blocking N-MOSFET will be turned off to prevent the UFP from being damaged. When VOUT is shorted to GND, the N-MOSFET will be turned off automatically and the output power is limited.

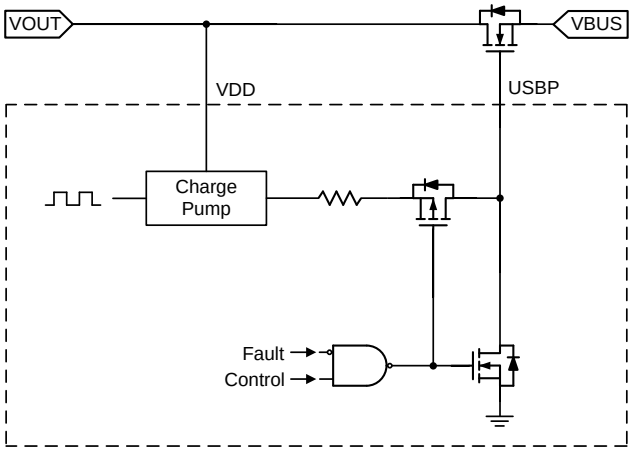


Figure 14. Blocking N-MOSFET Control

VBUS Drop Protection

VBUS drop protection provides another mechanism to protect the output short circuit, as shown in Figure 15. It is used to detect voltage difference of blocking N-MOSFET drain-to-source terminal. When the V_{DS} is higher than the VBUS drop threshold, the blocking N-MOSFET will be clamped-off immediately.

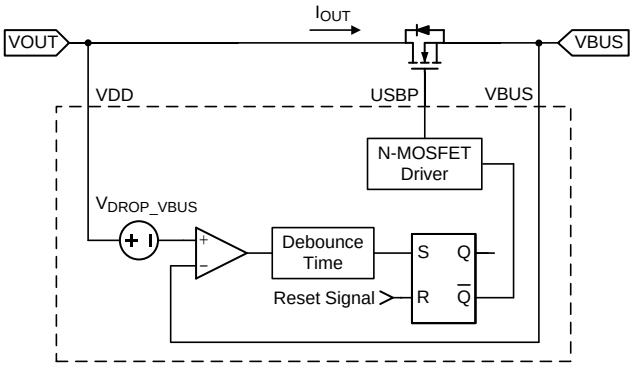


Figure 15. VBUS Drop Protection

Temperature Sensing and Thermal Protection

The RT7202KLA provides the RT pin for over-temperature protection or thermal monitoring. As shown in Figure 2, the RT pin sources a constant bias current for a remote thermal sensor of an NTC thermistor, connected from the RT pin to GND, for temperature sensing. If the RT voltage is below a programmable threshold voltage and the condition sustains for a programmable deglitch time, the over-temperature protection will be triggered.

The bias current through the RT pin can be programmed as 100μA, 20μA, or 5μA register setting. With the appropriate bias current setting, linearity of temperature sensing over the temperature range from 25°C to 100°C can be improved. The RT7202KLA can deliver the sensed RT voltage signal to the UFP via the protocol (Vendor Defined Message), if necessary. Figure 16 shows the RT voltages vary with temperature at three different bias currents with an NTC thermistor TTC104 as an example.

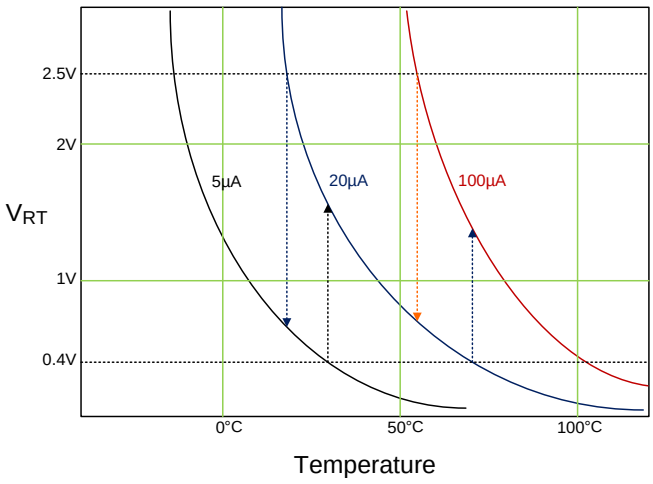
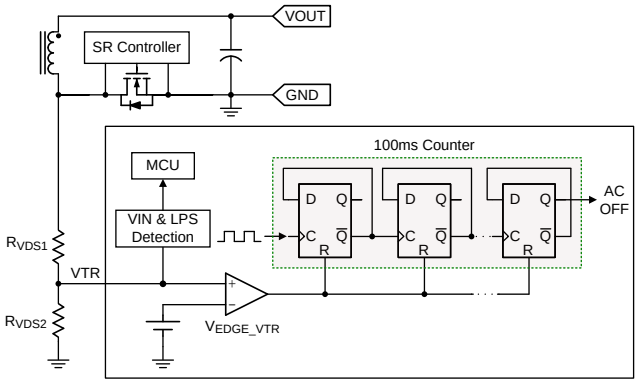


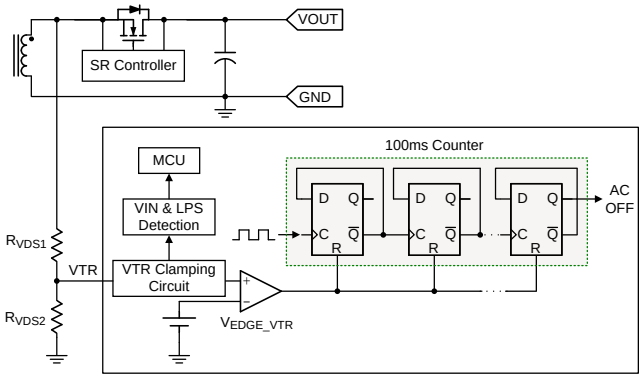
Figure 16. The RT Voltages vs. Temperature at Three Bias Currents

Multifunctional VTR

By connecting VTR pin to the drain of SR MOSFET (for low-side application) or to the source of SR MOSFET (for high-side application) through the divider resistor, R_{VDS1}, the RT7202KLA can detect VIN and implement LPS protection. The VTR pin can be used as RT function for I^2C Master/Slave detection or temperature sensing application. The multifunctional VTR pin also provides AC OFF detection for preventing the RT7202KLA from reverse biased through the body diode of a blocking N-MOSFET. If no switching signal on the VTR and through the 100ms debounce time, it will send a flag to MCU. The multifunctional VTR for low-side SR and high-side SR applications are shown in Figure 17.



(a) Low-Side SR Application



(b) High-Side SR Application

Figure 17. Multifunctional VTR

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24L 4x4 package, the thermal resistance, θ_{JA}, is 39.6°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (39.6°C/W) = 2.52W for a WQFN-24L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 18 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

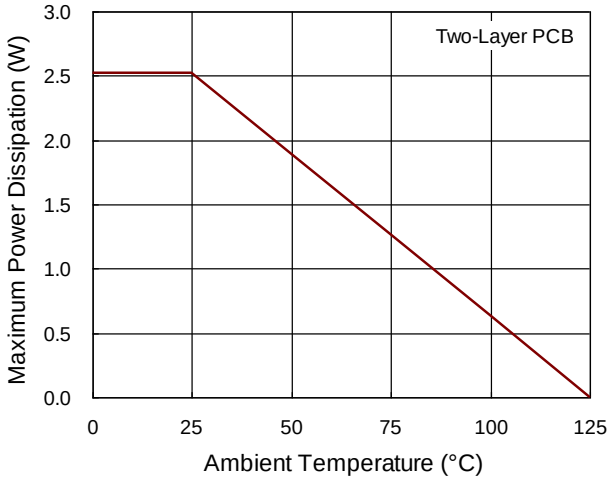
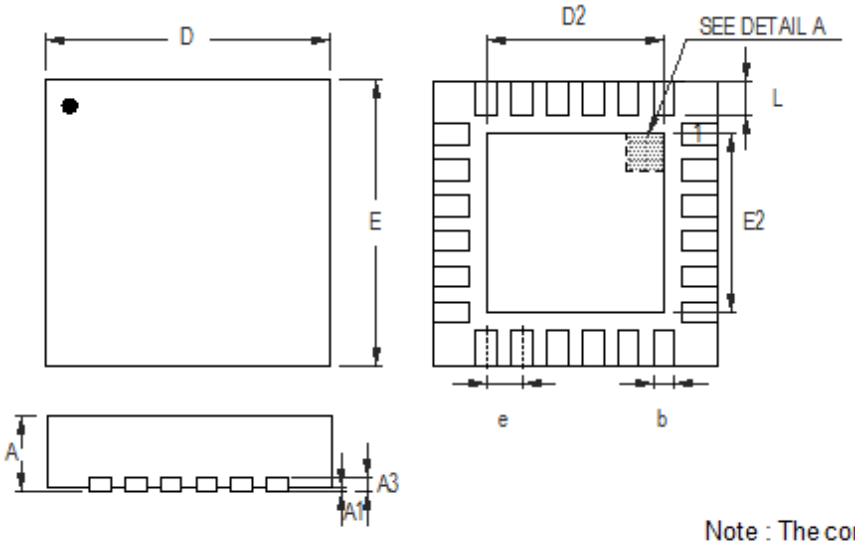
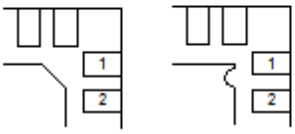


Figure 18. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

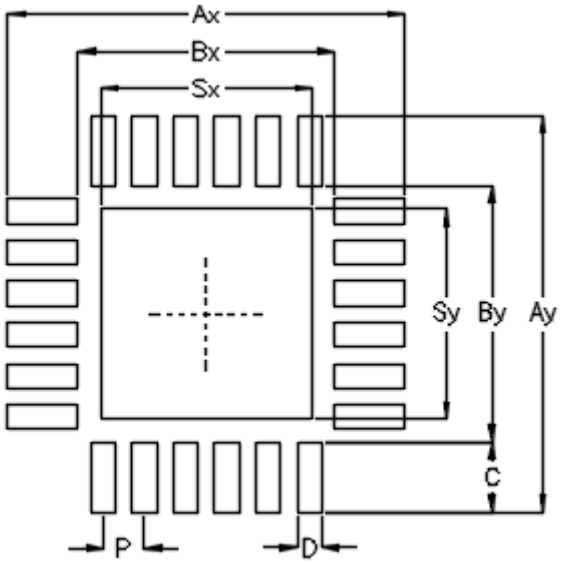
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-24	Option1	24	0.50	4.80	4.80	3.10	3.10	0.85	0.30	2.55	2.55	±0.05
	Option2									2.60	2.60	

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Datasheet Revision History

Version	Date	Description	Item
01	2022/12/6	Modify	Features on P1 Applications on P1 Ordering Information on P2 Simplified Application Circuit on P3, 4 Functional Pin Description on P5 Operation on P8 Electrical Characteristics on P10 to P19 Typical Application Circuit on P20, 21, 22 Application Information on P38