# SmartJitter™ Multi-Mode Flyback Controller

## General Description

The RT7738F is enhanced high efficient multi-mode PWM flyback controller with proprietary SmartJitter™ technology. The innovative SmartJitter™ technology can not only reduces the EMI emissions of SMPS when the system enters green mode, but also eliminates the output jittering ripple. Also, the RT7738F feature Continuous Conduction Mode (CCM) and valley switching multi-mode control to optimize the product performance. To meet the stringent trend toward performance in recent years, the RT7738F is the best choice for product designers.

The RT7738F is available in SOT-23-6 package, and it is a current mode PWM controller. Comprehensive protection and programmable functions are built-in, including a programmable propagation delay time compensation, a programmable output Over-Voltage Protection (OVP), a programmable external Over-Temperature Protection (OTP), and a programmable bulk capacitor Brown-in/Brown-out protection. With the above features, the RT7738F is a cost-effective and compact solution for AC/DC products.

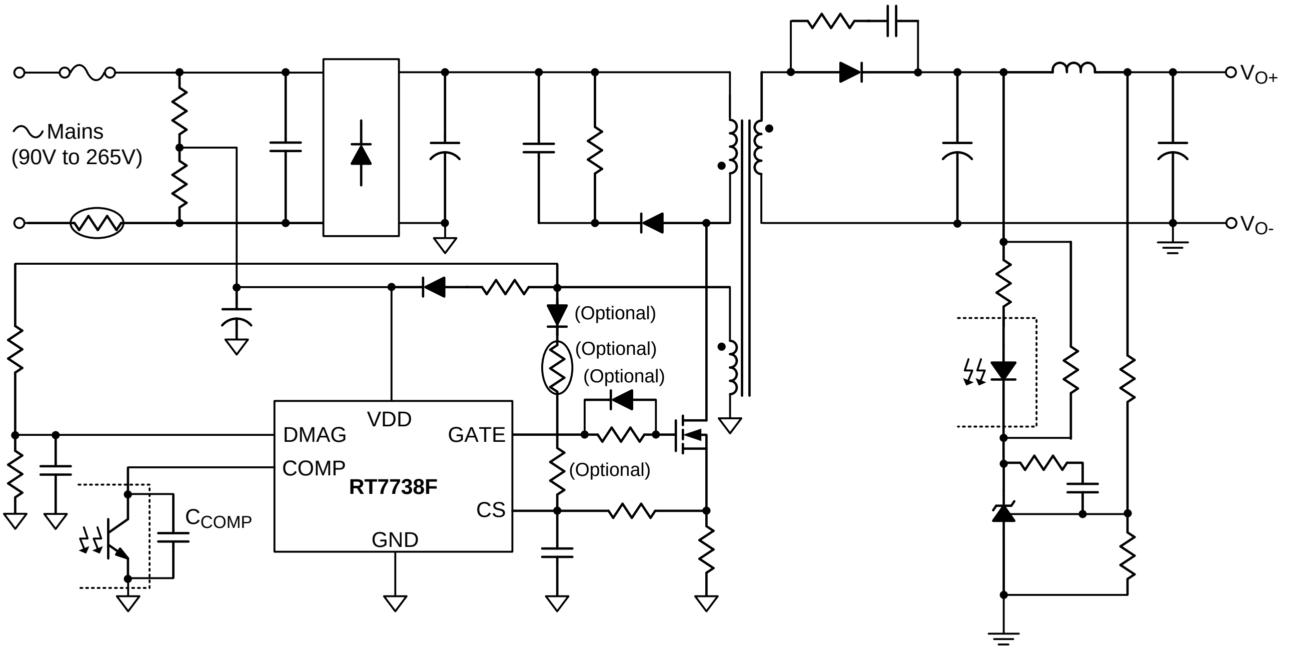
## Features

- **Proprietary SmartJitter™ Technology**
  - **Reducing EMI Emissions of SMPS**
  - **Output Jittering Ripple Elimination**
- **Continuous Conduction Mode (CCM) and Valley Switching Mode Control**
- **Ultra-low Start-up current (<3μA)**
- **Accurate Over-Load Protection (OLP)**
- **Programmable Propagation Delay Time Compensation**
- **Programmable Output Over-Voltage Protection**
- **Programmable External Over-Temperature Protection**
- **Programmable Bulk Capacitor Brown-in/Brown-out Protection**
- **Driver Capability : 200mA/–300mA**
- **High Noise Immunity**

## Applications

- Switching AC/DC Adaptor
- NB Adaptor
- TV/Monitor Standby Power
- PC Peripherals

## Simplified Application Circuit



## Ordering Information

RT7738F□□

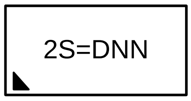
- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

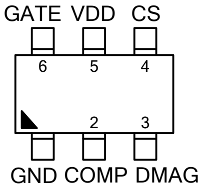
## Marking Information




2S= : Product Code
DNN : Date Code

## Pin Configurations

(TOP VIEW)

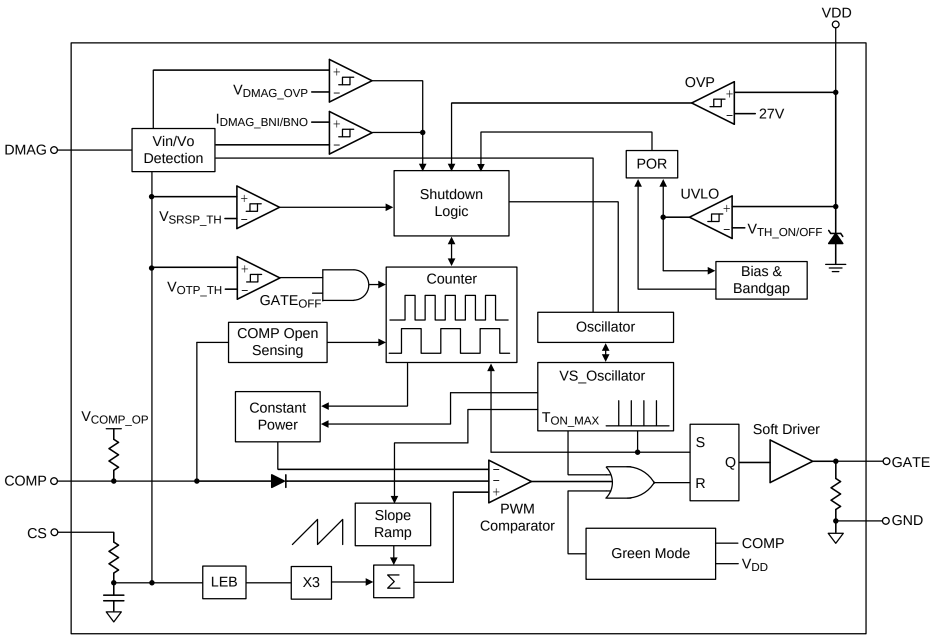



SOT-23-6

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | GND | Ground of the Controller. |
| 2 | COMP | Feedback Voltage Input. Connect an opto-coupler to close the control loop and achieve output voltage regulation. |
| 3 | DMAG | Demagnetization Pin. Input and Output Voltage Detection from Auxiliary Winding. |
| 4 | CS | Current Sense Input. The current sense resistor between this pin and GND is used for current limit setting. |
| 5 | VDD | Supply Voltage Input. The controller will be enabled when VDD exceeds $V_{TH\_ON}$ and disabled when VDD decreases lower than $V_{TH\_OFF}$. |
| 6 | GATE | Gate Driver Output Pin. |

## Function Block Diagram



## Operation

### Multi-mode PWM

The RT7738F is a multi-mode PWM controller, and a constant oscillator is built-in to allow the system operating in CCM. As the load decreases, the system enters DCM, and the oscillator converts to valley switching mode control. In lighter load or no load conditions, the controller enters green mode. The RT7738F provides multi-mode control to optimize the product performance under different load conditions.

### Oscillator

The oscillator runs at 65kHz and features frequency jittering function. The saw-tooth slope compensation, maximum duty cycle pulse and over-load protection slope are built-in. Its jitter depth is proportion of oscillator frequency where $\Delta f$ is frequency jittering range, and $T_{JIT}$ is frequency jittering period.

### Leading Edge Blanking (LEB)

To prevent unexpectedly gate switching interruption from the initial spike on CS pin, the LEB delay is designed to block this spike at the beginning of gate switching.

### Gate Driver

A totem pole gate driver is designed to meet both EMI and efficiency requirements in low power applications. An internal pull-low circuit is activated after pretty low $V_{DD}$ to prevent external MOSFET from accidentally turning on during UVLO.

### DMAG Pin

The DMAG pin detects the input voltages of bulk capacitor and output voltage by auxiliary winding and resistor divider. According to the DMAG signal, the RT7738F provides protections, including output over-voltage protection, and programmable bulk capacitor Brown-in/Brown-out protection.

### Over-Load Protection

In over-load conditions, current limit for a long time will lead to system thermal stress problem. To further protect the system, the RT7738F is designed with a proprietary prolonged turn-off period during hiccup. The power loss and temperature during OLP are averaged to an acceptable level over the ON/OFF cycle.

### CS Pin Open Protection

When the CS pin is opened, the controller will shut down after a few cycles.

### Internal VDD Over-Voltage Protection

Output voltage can be roughly sensed by the VDD pin. If the sensed voltage reaches $V_{OVP}$ threshold, the controller shuts down after deglitch delay.

### Feedback Open and Opto-Coupler Short

If the output voltage feedback loop is open or the opto-coupler is shorted, the OVP/OLP function will be triggered depending on which one occurs first.

### Output Short Protection

The RT7738F implements output short protection by detecting output signal of DMAG pin. It can minimize the power loss and temperature during output short, especially at high line input voltage.

### Secondary Rectifier Short Protection

The current spike during secondary rectifier short test is extremely high because of the saturated main transformer. Meanwhile, the transformer acts like a leakage inductance. During high line, the current in power MOSFET is sometimes too high in OLP delay time. To offer better and easier protection design, the RT7738F shuts down after a few of cycles before fuse is impacted.

## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD to GND ---------- –0.3V to 30V
- GATE to GND ---------- –0.3V to 16.5V
- DMAG, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C

  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)

  SOT-23-6, $\theta_{JA}$ ---------- 260.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM(Human Body Model) ---------- 2.5kV

  MM(Machine Model) ---------- 250V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 12V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{DD}$ = 15V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VDD Section** | | | | | | |
| $V_{DD}$ Over-Voltage Protection Level | $V_{OVP}$ | | 26 | 27 | 28 | V |
| On Threshold Voltage | $V_{TH\_ON}$ | | 13.5 | 14.5 | 15.5 | V |
| Off Threshold Voltage | $V_{TH\_OFF}$ | | 8.5 | 9 | 9.5 | V |
| $V_{DD}$ Holdup Mode Entry Point | $V_{DD\_ET}$ | $V_{COMP}$ < 0.85V | 9.5 | 10 | 10.5 | V |
| $V_{DD}$ Holdup Mode Ending Point | $V_{DD\_ED}$ | $V_{COMP}$ < 0.85V | 10 | 10.5 | 11 | V |
| Start-up Current | $I_{DD\_ST}$ | $V_{DD}$ < $V_{TH\_ON}$ – 0.1V, $T_A$ = –40°C to 85°C | -- | 0.5 | 3 | μA |
| Operating Supply Current | $I_{DD\_OP1}$ | GATE pin open, $V_{COMP}$ = 1.8V | -- | 1.8 | -- | mA |
| | $I_{DD\_OP2}$ | GATE pin open, $V_{COMP}$ = 1.4V | -- | 1.4 | -- | |
| $I_{DD}$ Sinking Current | $I_{DD\_ARP}$ | During entering auto recovery protection, $T_A$ = –40°C to 85°C | 400 | 550 | 700 | μA |
| **Oscillator Section** | | | | | | |
| Normal PWM Frequency | $f_{OSC}$ | $V_{COMP}$ > $V_{GM\_ET}$ | 60 | 65 | 70 | kHz |
| Maximum ON Time | $T_{ON\_MAX}$ | $V_{COMP}$ = $V_{COMP\_OP}$, $f_{OSC}$ = 65kHz | 10 | 11.8 | 13.8 | μs |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Minimum Green Mode Frequency | $f_{GM\_MIN}$ | $V_{COMP} < V_{GM\_ED}$ | -- | 22.5 | -- | kHz |
| PWM Frequency Jittering Range | $\Delta f$ | | -- | ±6 | -- | % |
| PWM Frequency Jittering Period | $T_{JIT}$ | $f_{OSC}$ = 65kHz | -- | 16 | -- | ms |
| Frequency Variation Versus VDD Deviation | $f_{DV}$ | $V_{DD}$ = 9V to 23V | -- | -- | 2 | % |
| Frequency Variation Versus Temperature Deviation | $f_{DT}$ | $T_A$ = –30°C to 105°C | -- | -- | 5 | % |
| **COMP Input Section** | | | | | | |
| Open Loop Voltage | $V_{COMP\_OP}$ | COMP pin open | -- | 2.5 | -- | V |
| Short Circuit Current of COMP | $I_{ZERO}$ | $V_{COMP}$ = 0V | -- | 0.135 | -- | mA |
| Delay Time of COMP Open-loop Protection | $T_{OLP}$ | $f_{OSC}$ = 65kHz | -- | 64 | -- | ms |
| Green Mode Entry Voltage | $V_{GM\_ET}$ | | -- | 1.75 | -- | V |
| Green Mode Ending Voltage | $V_{GM\_ED}$ | | -- | 1.6 | -- | V |
| **Current Sense Section** | | | | | | |
| Maximum Current Limit | $V_{CS\_MAX}$ | | 0.38 | 0.40 | 0.42 | V |
| Leading Edge Blanking Time | $T_{LEB}$ | | 350 | 475 | 600 | ns |
| Threshold Voltage of Secondary Rectifier Short Protection | $V_{SRSP\_TH}$ | (Note 5) | -- | 1.1 | -- | V |
| Threshold Voltage for External Over-temperature Protection Application | $V_{OTP\_TH}$ | | -- | 0.7 | -- | V |
| Delay Time for External Over-temperature Protection | $T_{D\_OTP}$ | $f_{OSC}$ = 65kHz | -- | 64 | -- | ms |
| **GATE Section** | | | | | | |
| Rising Time | $T_R$ | $C_L$ = 1nF | -- | 250 | -- | ns |
| Falling Time | $T_F$ | $C_L$ = 1nF | -- | 30 | -- | ns |
| Gate Output Clamping Voltage | $V_{CLAMP}$ | $V_{DD}$ = 23V | -- | 13 | -- | V |
| **DMAG Section** | | | | | | |
| Threshold Voltage of Over-voltage Protection | $V_{DMAG\_OVP}$ | | 2.45 | 2.5 | 2.55 | V |
| Blanking Time Before Over-voltage Protection of DMAG Pin | $T_{BK\_OVP}$ | $V_{CS}$ = 0.36V | 2.1 | 2.9 | 3.7 | μs |
| Threshold Voltage of Under-voltage Protection | $V_{DMAG\_UVP}$ | After $T_{D\_OSP}$, COMP pin open | 0.3 | 0.4 | 0.5 | V |
| Delay Time of Under-voltage Protection | $T_{D\_OSP}$ | $f_{OSC}$ = 65kHz | -- | 16 | -- | ms |
| On Threshold Current | $I_{DMAG\_BNI}$ | | 141 | 160 | 179 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Threshold Current of Under-current Protection | $I_{DMAG\_BNO}$ | | 128 | 145 | 162 | μA |
| Maximum Sourcing Current of DMAG Pin | $I_{DMAG\_MAX}$ | (Note 5) | -- | -- | 1 | mA |
| Delay Time of Under-current Protection | $T_{D\_BNO}$ | $f_{OSC}$ = 65kHz | -- | 24 | -- | ms |
| **Over-Temperature Protection (OTP) Section** | | | | | | |
| OTP Before Turn On | $T_{OTP\_INTH}$ | Built-in OTP (Note 5) | -- | 130 | -- | °C |
| OTP After Turn On | $T_{OTP\_STTH}$ | Built-in OTP (Note 5) | -- | 140 | -- | °C |

**Note1**. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

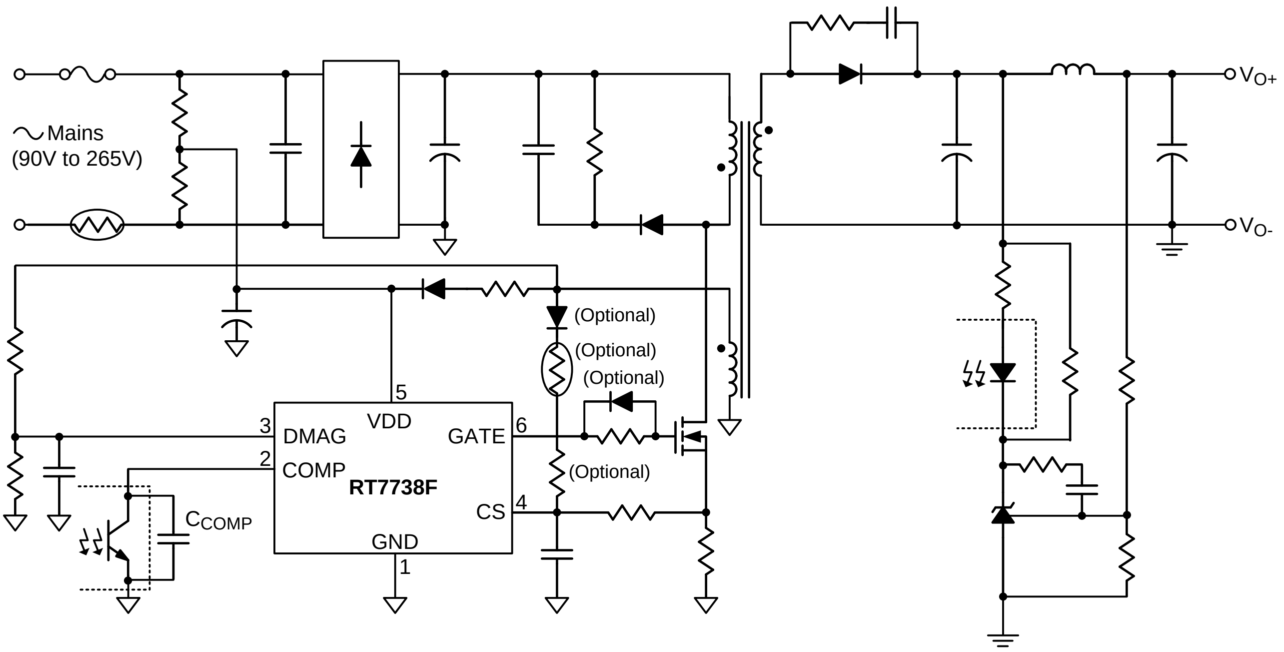
**Note 2**. $\theta_{JA}$ is measured in natural convection (still air) at $T_A$ = 25°C with the component mounted on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3**. Devices are ESD sensitive. Handling precaution is recommended.

**Note 4**. The device is not guaranteed to function outside its operating conditions.

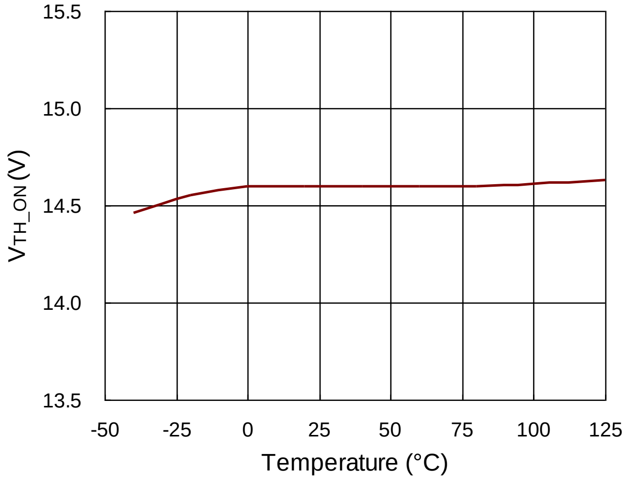
**Note 5**. Guaranteed by design.

## Typical Application Circuit

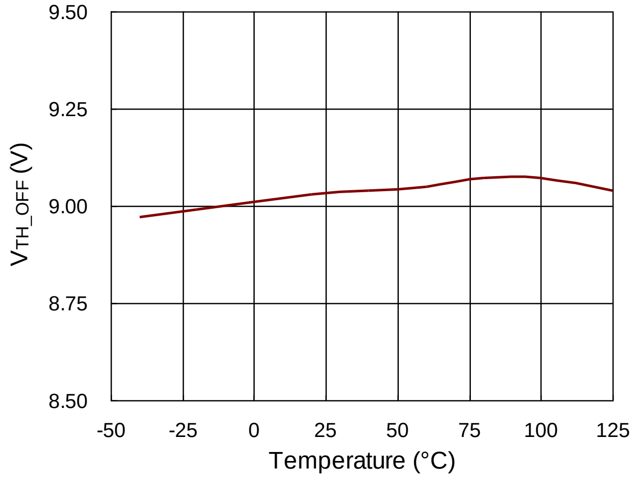


## Typical Operating Characteristics

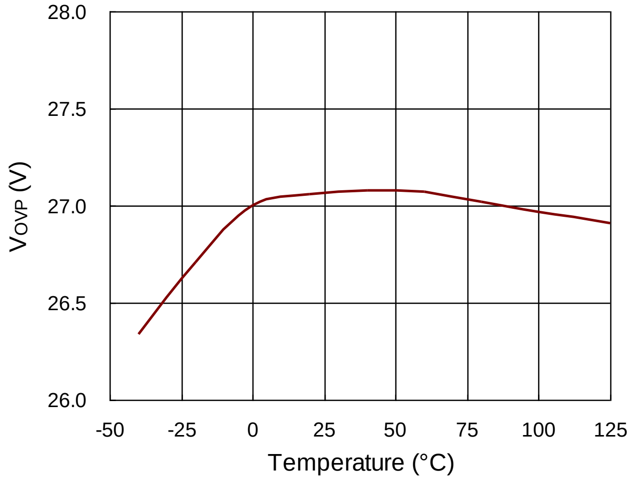
$V_{TH\_ON}$ vs. Temperature



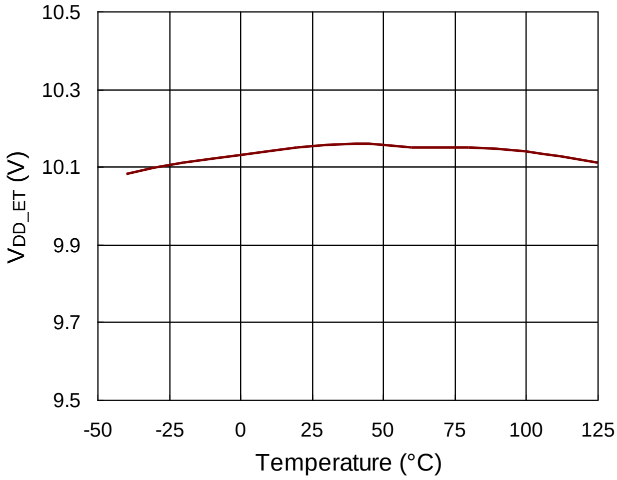

$V_{TH\_OFF}$ vs. Temperature



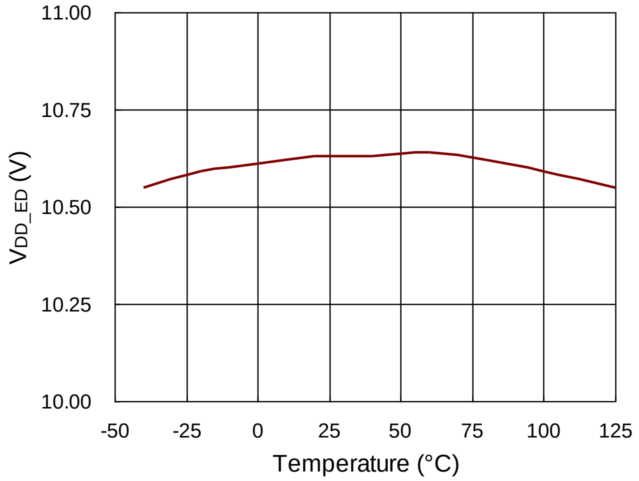

$V_{OVP}$ vs. Temperature



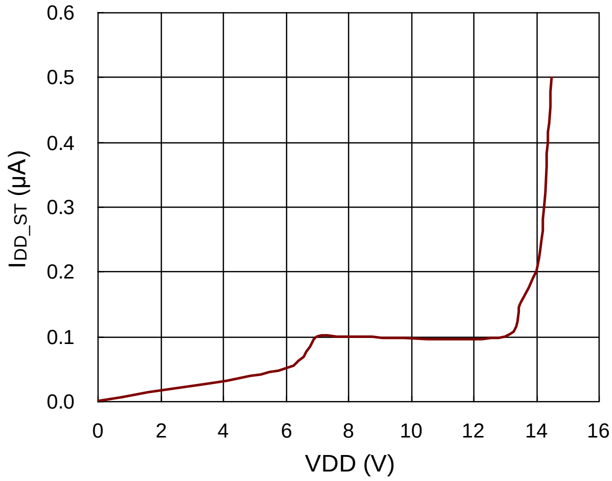

$V_{DD\_ET}$ vs. Temperature



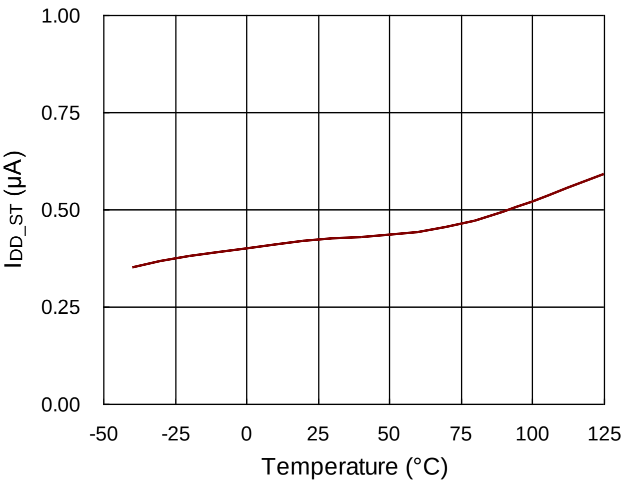

$V_{DD\_ED}$ vs. Temperature



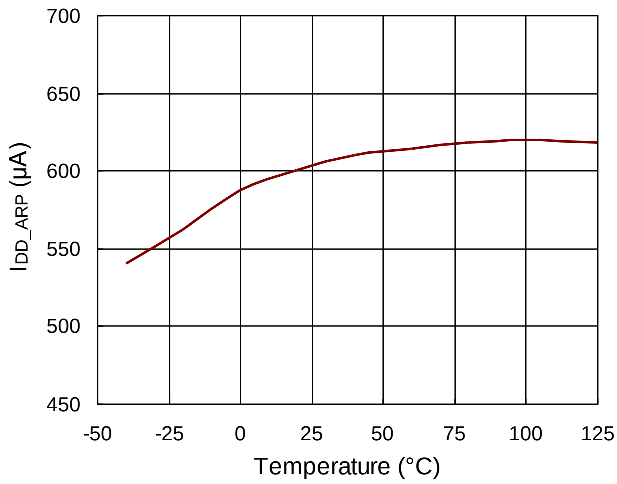

$I_{DD\_ST}$ vs. VDD



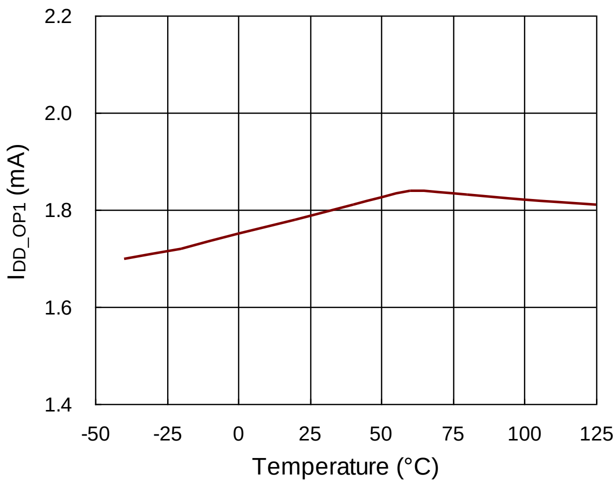
**$I_{DD\_ST}$ vs. Temperature**



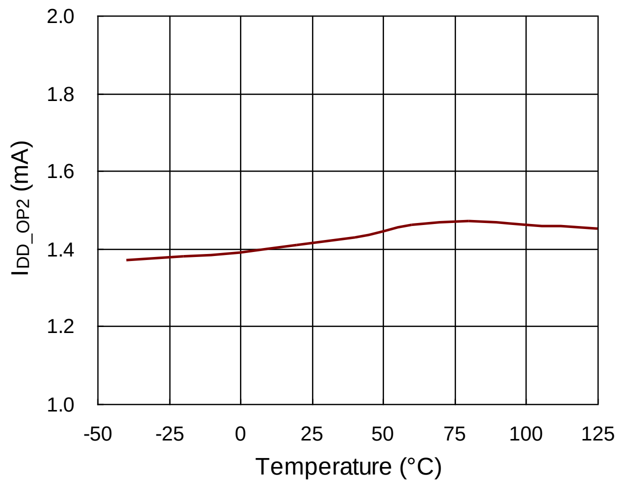

**$I_{DD\_ARP}$ vs. Temperature**



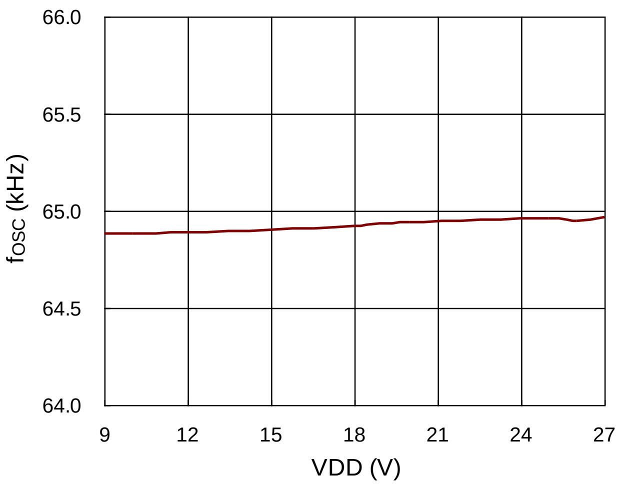

**$I_{DD\_OP1}$ vs. Temperature**



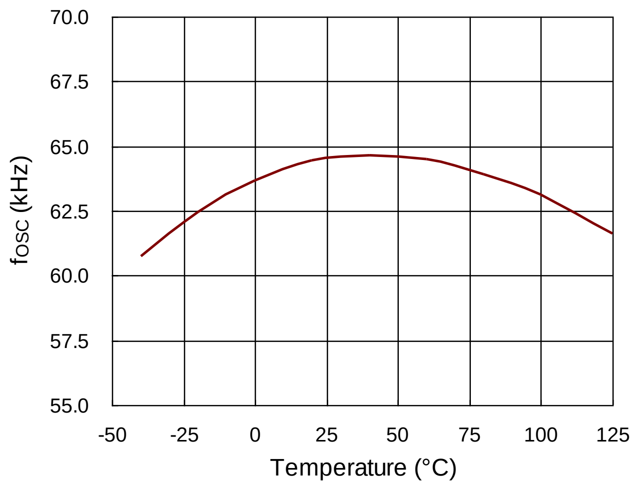

**$I_{DD\_OP2}$ vs. Temperature**



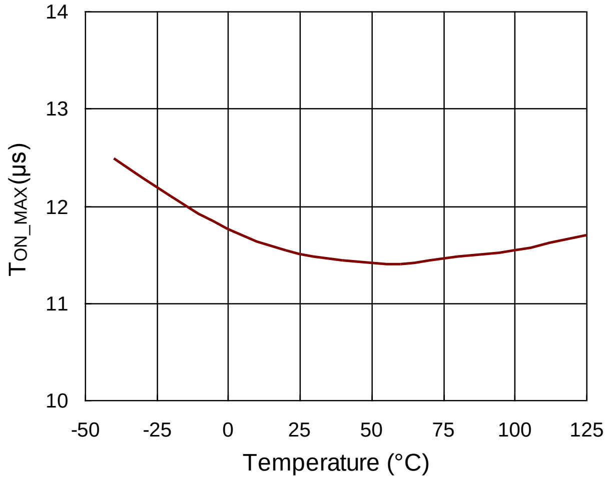

**$f_{OSC}$ vs. VDD**



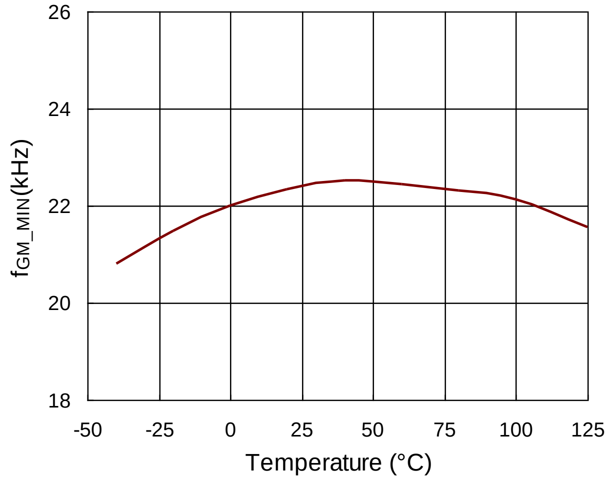

**$f_{OSC}$ vs. Temperature**



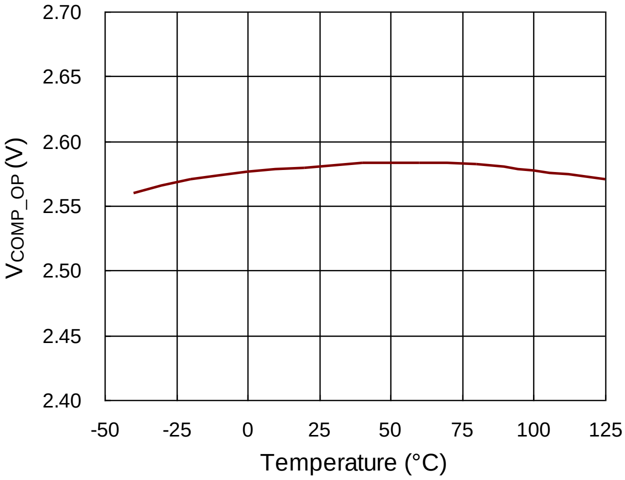
### $T_{ON\_MAX}$ vs. Temperature



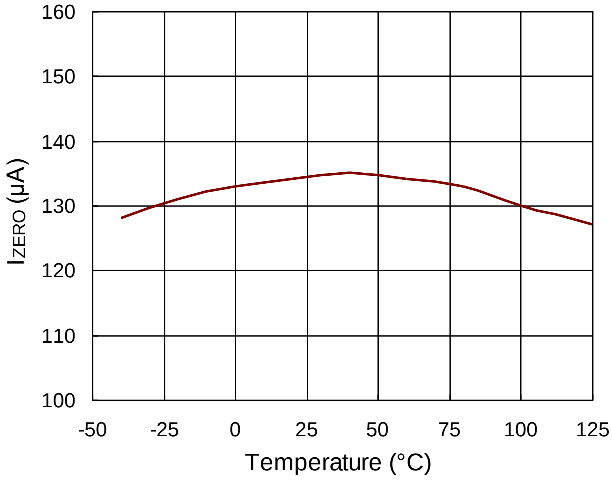

### $f_{GM\_MIN}$ vs. Temperature



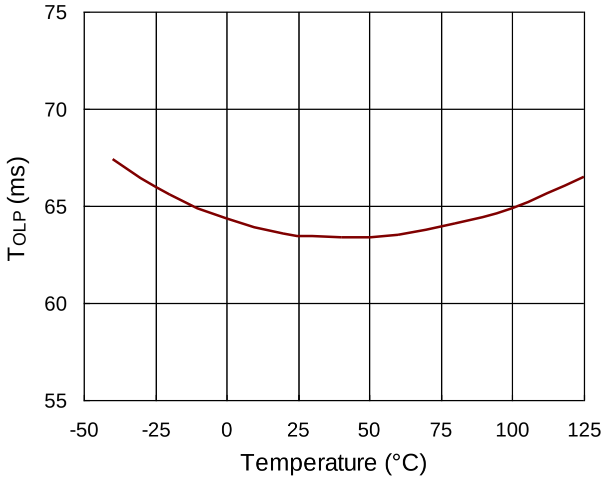

### $V_{COMP\_OP}$ vs. Temperature



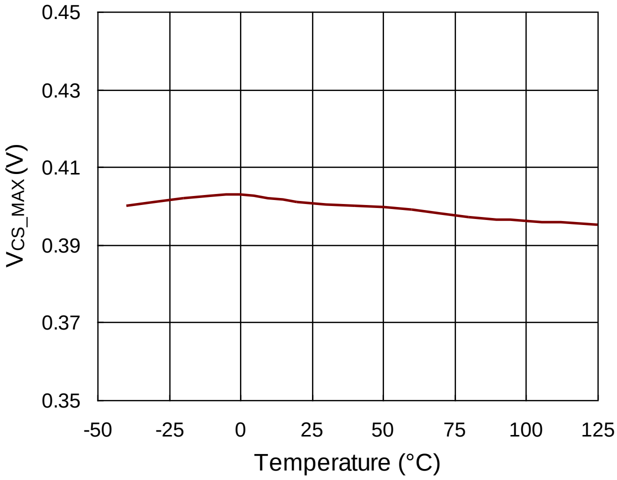

### $I_{ZERO}$ vs. Temperature



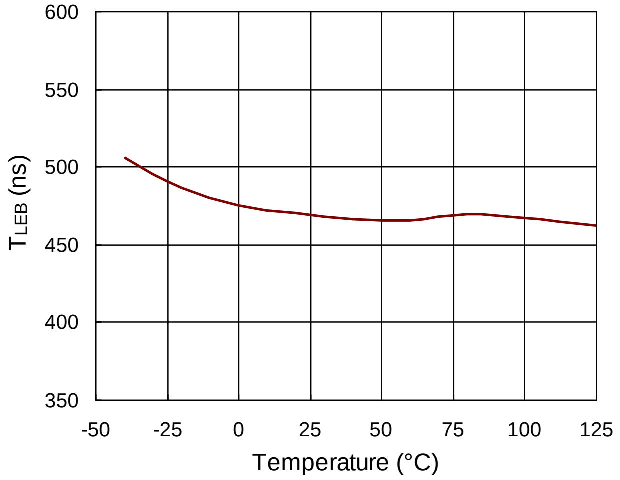

### $T_{OLP}$ vs. Temperature



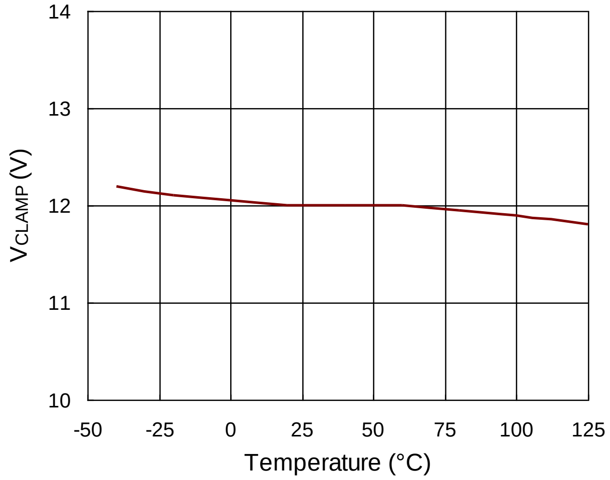

### $V_{CS\_MAX}$ vs. Temperature



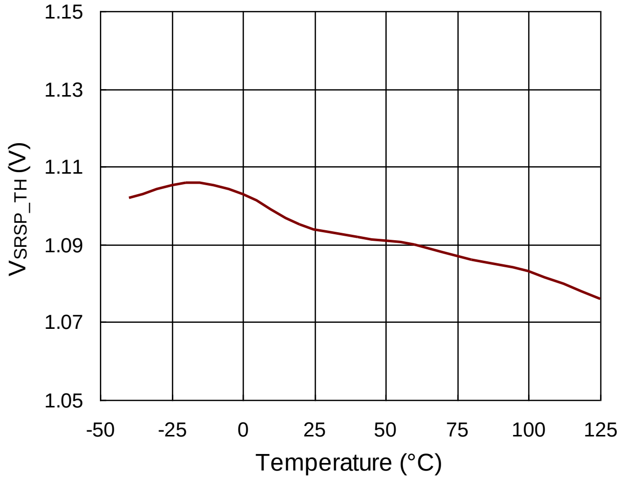
### $T_{LEB}$ vs. Temperature



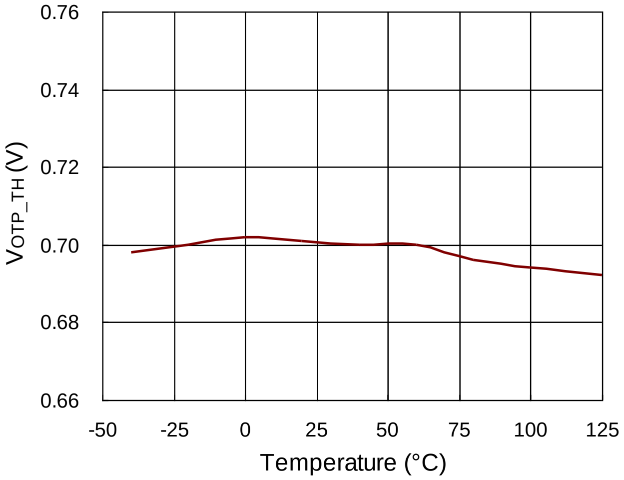

### $V_{CLAMP}$ vs. Temperature



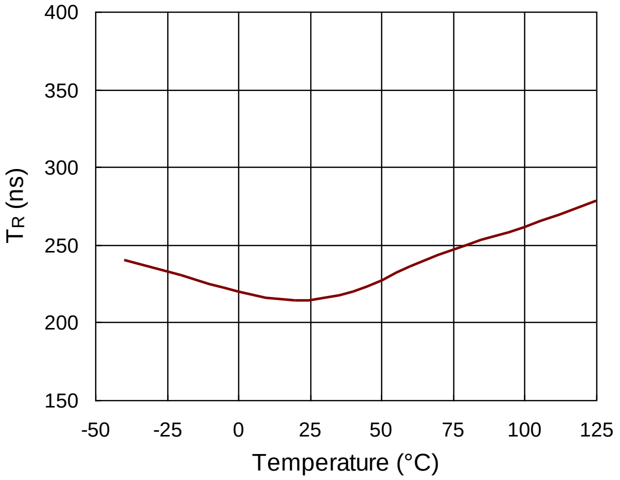

### $V_{SRSP\_TH}$ vs. Temperature



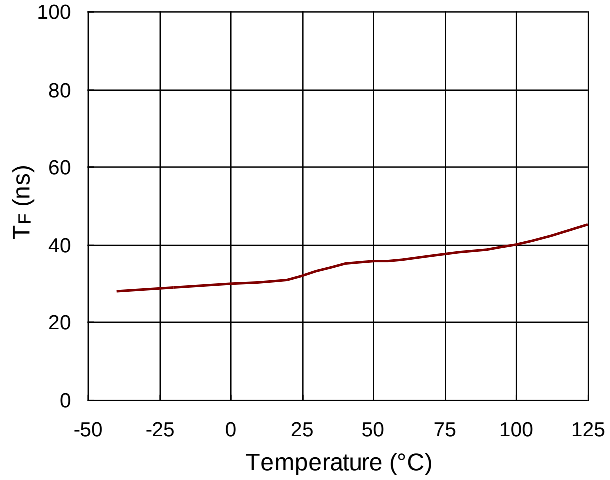

### $V_{OTP\_TH}$ vs. Temperature



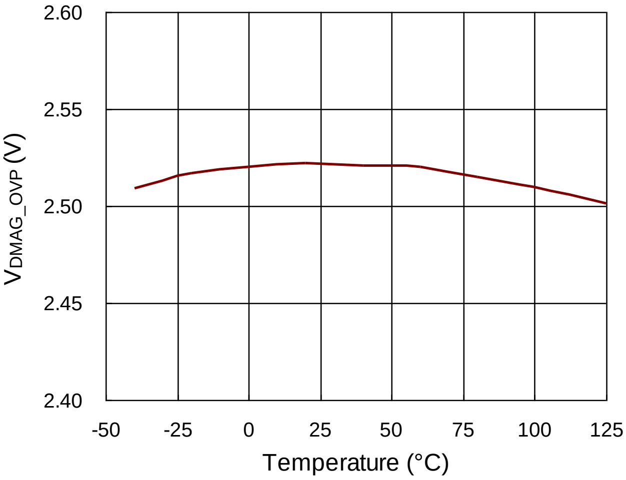

### $T_R$ vs. Temperature



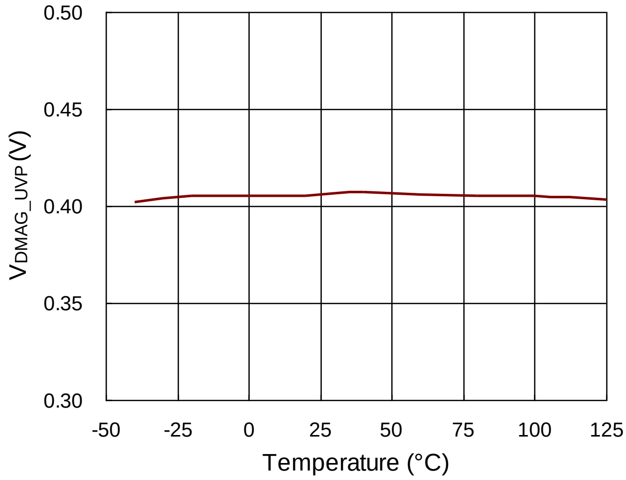

### $T_F$ vs. Temperature



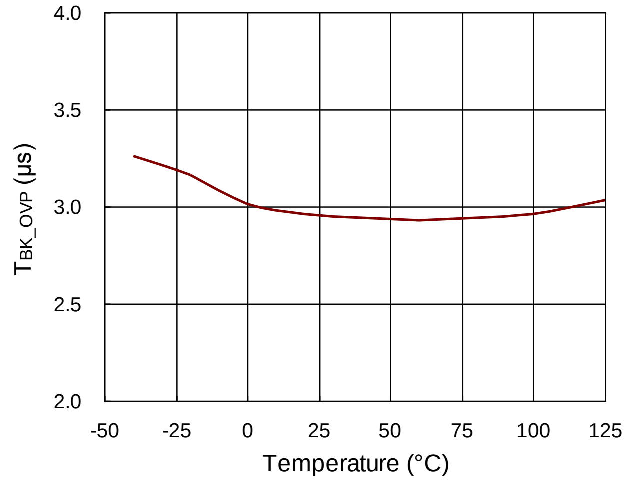
**$V_{DMAG\_OVP}$ vs. Temperature**



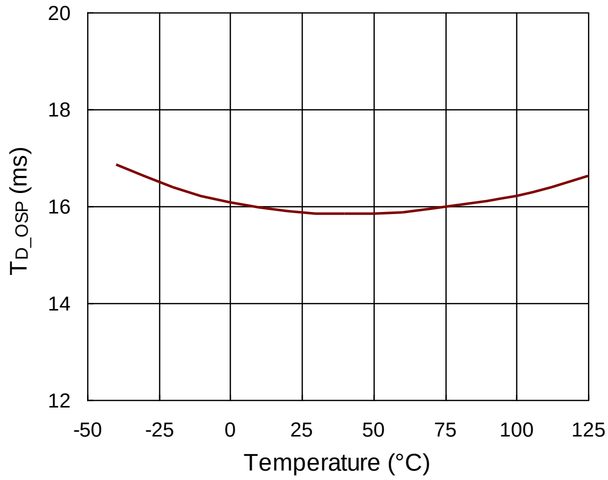

**$V_{DMAG\_UVP}$ vs. Temperature**



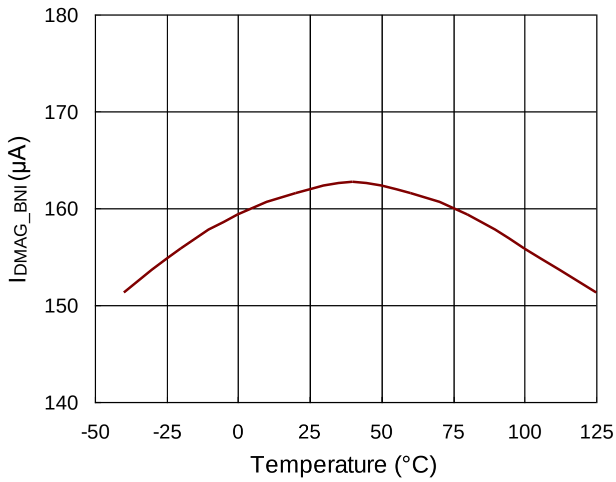

**$T_{BK\_OVP}$ vs. Temperature**



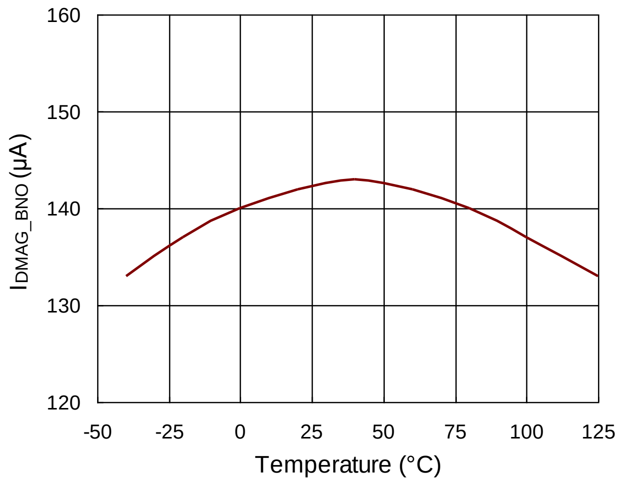

**$T_{D\_OSP}$ vs. Temperature**

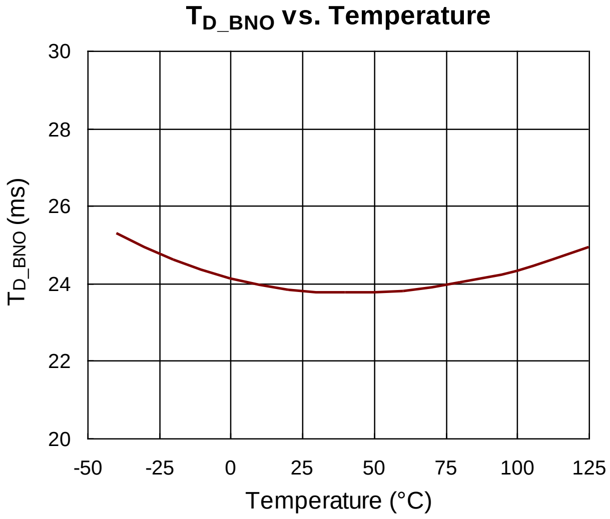



**$I_{DMAG\_BNI}$ vs. Temperature**




**$I_{DMAG\_BNO}$ vs. Temperature**




$T_{D\_BNO}$ vs. Temperature
30
28
26
24
22
20
$T_{D\_BNO}$ (ms)
-50
-25
0
25
50
75
100
125
Temperature (°C)

## Application Information

The RT7738F is a multi-mode PWM flyback controller. The system automatically converts between constant frequency CCM and valley switching mode according to load conditions. As load decreases, the controller enters green mode, burst mode, and VDD holdup mode. The automatic multi-mode switching optimizes the product performance under different load conditions. To meet the stringent trend toward performance, the RT7738F is the best choice for product designers.

### Programmable Propagation Delay Time Compensation Function

The RT7738F provides programmable propagation delay time compensation function, as shown in Figure 1.

The RT7738F outputs a propagation delay time compensation current on the CS pin by gain. Product designers can compensate the propagation delay time differences caused by different input voltages by adjusting the propagation delay time compensation resistor ($R_{PDC}$) to keep the same output current under different input voltages and accurate over-load protection.

In the beginning of propagation delay time compensation function setting, designers could set $R_{PDC}$ = 470Ω, and $C_{RC}$ = 100pF. In Figure 2, the ideal output current should be the same as curve (1). No matter under high line or low line, the output current keeps the same. However, the propagation delay time varies OLP curve under different input voltages according to different designs of transformer inductance, parasitic capacitance of MOSFET, series resistance on the GATE of MOSFET. If the OLP curve is like curve (2), designers should increase the resistance of $R_{PDC}$; if the OLP curve is like curve (3), designers should increase the capacitance of $C_{RC}$. Designers optimize the OLP curve through propagation delay time compensation to keep the same output current under different input voltages.

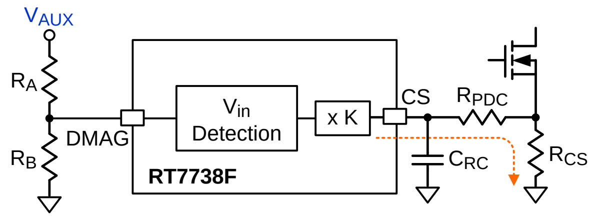



Figure 1. Function Block Diagram of Propagation Delay Time Compensation

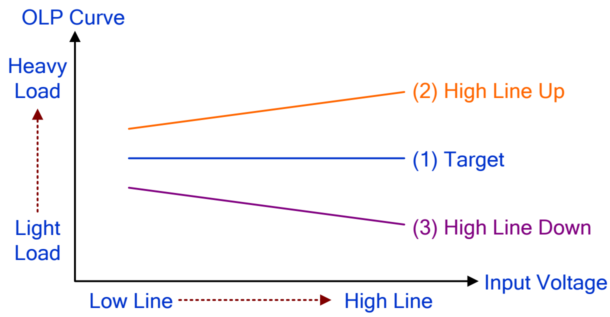



Figure 2. Curve Chart of OLP

### External Over-Temperature Protection

The RT7738F implements external arbitrary over-temperature protection by CS pin. Designer can design arbitrary OTP via constant voltage source ($V_{AUX\_Clamp}$), fast diode and the divided resistors on CS pin, as shown in Figure 3. The constant voltage source is sensing by auxiliary voltage at GATE off, and the divided resistors are NTC resistor ($R_{NTC}$), setting resistor ($R_{SET}$), resistor of propagation delay compensation ($R_{PDC}$) and current sense resistor ($R_{CS}$). When temperature is higher, the resistance of NTC resistor becomes small. The sampling voltage of divided resistors on CS pin during GATE off exceeds the $V_{OTP\_TH}$ trip level, and then after delay time $T_{D\_OTP}$ the controller will be shut down and cease switching. Until the OTP is released, the controller resumes operation. The design equation is :

$$V_{OTP\_TH} = \left[ (V_O + V_F) \times \frac{N_A}{N_S} - V_{F\_OTP} \right] \times \frac{R_{PDC} + R_{CS}}{R_{NTC\_OTP} + R_{SET} + R_{PDC} + R_{CS}}$$

Where $R_{NTC\_OTP}$ is the NTC resistance at over-temperature.

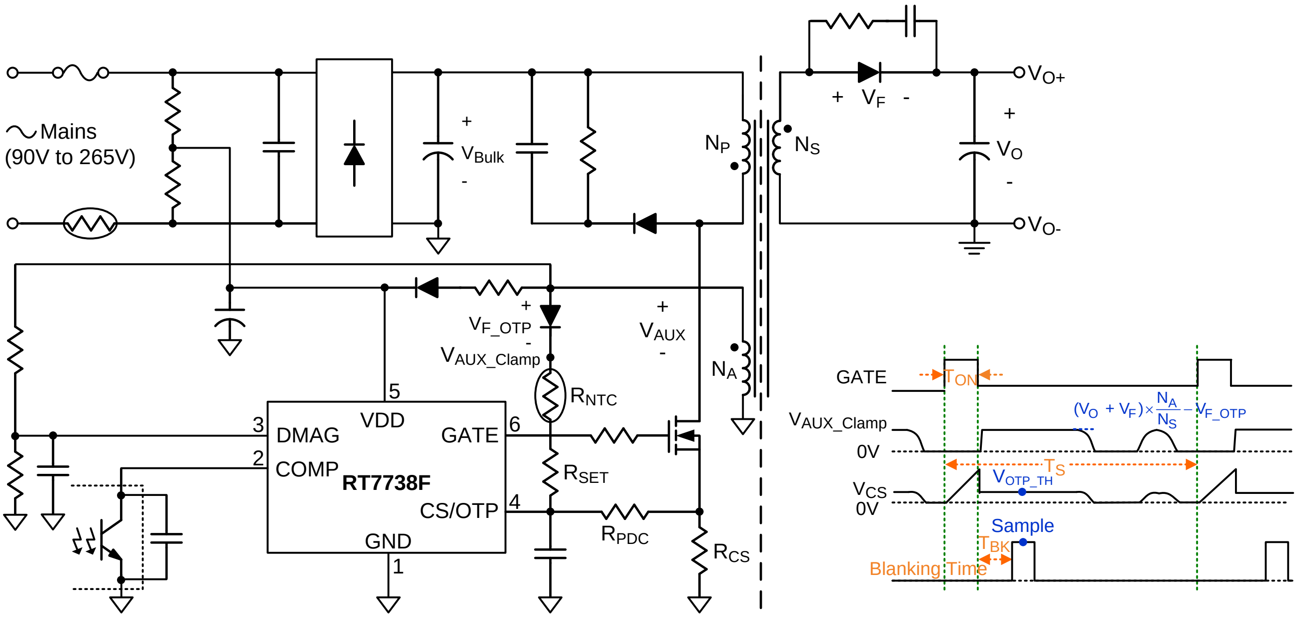



Figure 3. Application Circuit of External Over-Temperature Protection

### SmartJitter™ Technology

The RT7738F applies RICHTEK proprietary SmartJitter™ technology.

In order to reduce switching loss for lower power consumption during light load or no load, general PWM controllers have green mode function.

The output power equation is :

$$P_{O\_DCM}(V_{COMP}) = \frac{1}{2} \times L_p \times \left(\frac{x_1 \times V_{COMP}}{R_{CS}}\right)^2 \times f_S(V_{COMP}) \times \eta$$

Where $L_P$ is the magnetizing inductance of the transformer, $R_{CS}$ is the current sense resistor, $V_{COMP}$ is the feedback voltage of the COMP pin. $f_S$ is the switching frequency of the power switch, $\eta$ is the conversion efficiency, and $x_1$ is a constant coefficient.

Output power is a function of feedback voltage $V_{COMP}$. Frequency jittering technique is typically used to improve EMI problems in general PWM controllers, and the frequency jittering period is based on PWM switching frequency.

When the system enters green mode, a output power relationship is formed between the feedback voltage $V_{COMP}$ and the PWM switching frequency, and a new stable equilibrium point is eventually reached after back-and-forth adjustments. It is mutually-affected by $V_{COMP}$ and PWM switching frequency and limits the frequency jittering. As a result, EMI improvement function worsens, as show in Figure 4.

The innovative SmartJitter™ technology not only helps reduce EMI emissions of SMPS when the system enters green mode, but also eliminates output jittering ripple.

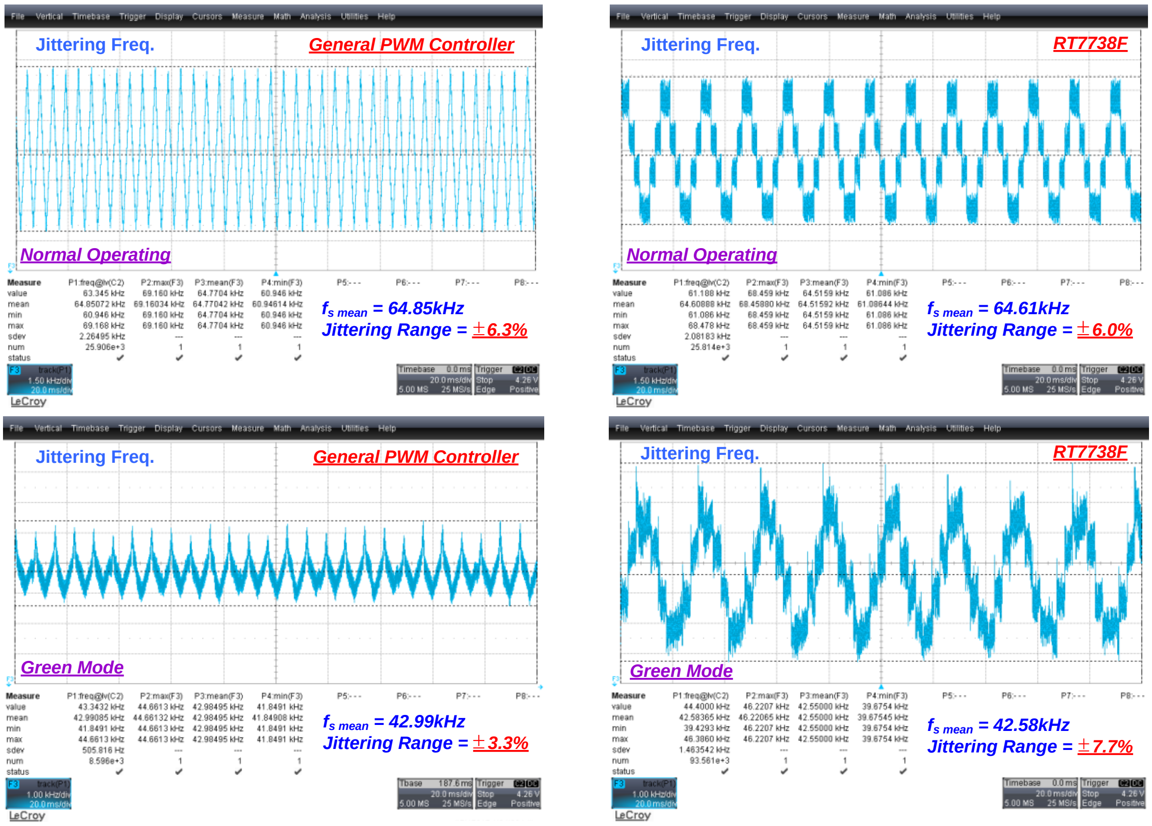



Figure 4. Frequency Jittering Range During Green Mode : General PWM Controller vs. RT7738F

**DMAG Pin Resistance Setting**

When the MOSFET turns on, the voltage of auxiliary winding is negative, and the clamping circuit outputs a clamp current to clamp the DMAG voltage at 0.1V. The clamping current is proportional to the input voltage. The RT7738F features DMAG threshold-on current ($I_{DMAG\_BNI}$), and DMAG under-current protection threshold ($I_{DMAG\_BNO}$). Designers can indirectly design bulk capacitor Brown-in ($V_{Bulk\_Brown\text{-}in}$) and Brown-out ($V_{Bulk\_Brown\text{-}out}$) by adjusting $R_A$ and $R_B$ on the DMAG pin, as shown in Figure 5.

When one of Brown-in and Brown-out is set, others are set proportionally.

The bulk capacitor input voltage Brown-out ($V_{Brown\text{-}out}$) is :

$$V_{Bulk\_Brown\text{-}out} = \frac{V_{Bulk\_Brown\text{-}in} \times I_{DMAG\_BNO}}{I_{DMAG\_BNI}}$$

When the MOSFET turns off, the DMAG pin detects the output voltage according to the ratio of auxiliary and secondary-side turns, and the series resistors, $R_A$ and $R_B$, on the auxiliary winding as shown in Figure 5. The RT7738F provides DMAG over-voltage protection, and designers can indirectly design output OVP ($V_{O\_OVP}$) by DMAG OVP ($V_{DMAG\_OVP}$) :

$$\begin{cases} \dfrac{\dfrac{V_{Bulk\_Brown\text{-}in} \times N_A}{N_P} + 0.1}{R_A} + \dfrac{0.1}{R_B} = I_{DMAG\_BNI} \\[2ex] \dfrac{(V_{O\_OVP} + V_F) \times N_A}{N_S} \times \dfrac{R_B}{R_A + R_B} = V_{DMAG\_OVP} \end{cases}$$

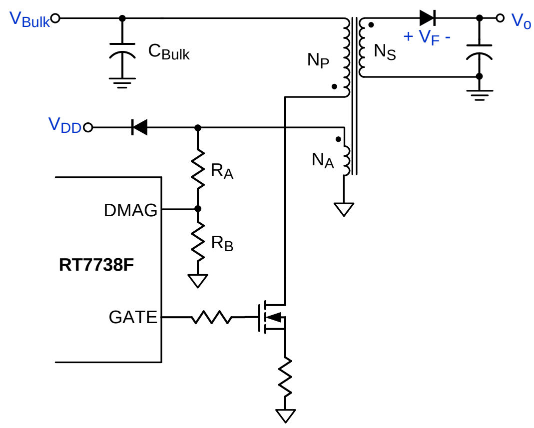



Figure 5. Design DMAG Pin Resistance

### Adaptive Blanking Time

When the MOSFET turns off, the leakage inductance of the transformer and parasitic capacitance ($C_{OSS}$) of MOSFET induce resonance waveform on the DMAG pin, as shown in Figure 6. The resonance waveform makes the controller false trigger the DMAG OVP ($V_{DMAG\_OVP}$) which affects the accuracy of output OVP ($V_{O\_OVP}$), and it may cause the controller operate in unstable condition. As load increases, the resonance time also increases. It is recommended to add 10pF to 47pF bypass capacitor to avoid noise false triggering on DMAG pin. The bypass capacitor should be as close to DMAG pin as possible. The bigger bypass capacitor maybe causes some phase shift on DMAG waveform, so RT7738F maybe doesn't turn on at exact valley point.

The RT7738F provides adaptive blanking time to prevent DMAG OVP from being false triggered. The blanking time ($T_{BK\_OVP}$) varies with maximum current limit of the CS pin ($V_{CS\_PK}$), and the blanking time can be calculated by the following formula :

$$T_{BK\_OVP} = 2\mu s + V_{CS\_PK} \times 2.5\ (\mu s/V)$$

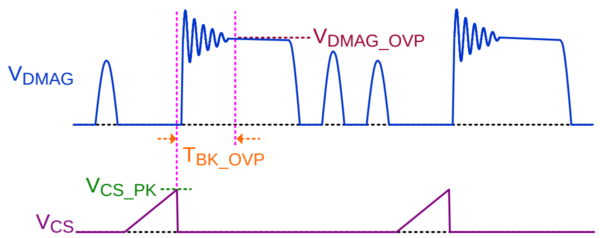



Figure 6. Resonance Waveform on the DMAG Pin

### Start-Up Circuit

To minimize power loss, it's recommended to connect the start-up circuit to the bleeding resistors. It's power saving and also could reset latch mode protection quickly. Figure 7 shows $I_{DD\_Avg}$ vs. $R_{Bleeding}$ curve. Users can apply this curve to design the adequate bleeding resistors.

In order to prolong turn-off period and minimize the power loss and thermal rising during hiccup, the controller is designed to have smaller sinking current during entering auto-recovery protection, $I_{DD\_ARP}$. Therefore, the start-up current at maximum AC line input voltage must be smaller than $I_{DD\_ARP}$ ($I_{DD\_ARP(min)}$ = 400μA). Otherwise, when the controller enters auto-recovery protection, the VDD capacitor won't be dropped down to $V_{TH\_OFF}$ by IC's sinking current and then restart. The controller behaves like latch protection or triggers the SCR of VDD.

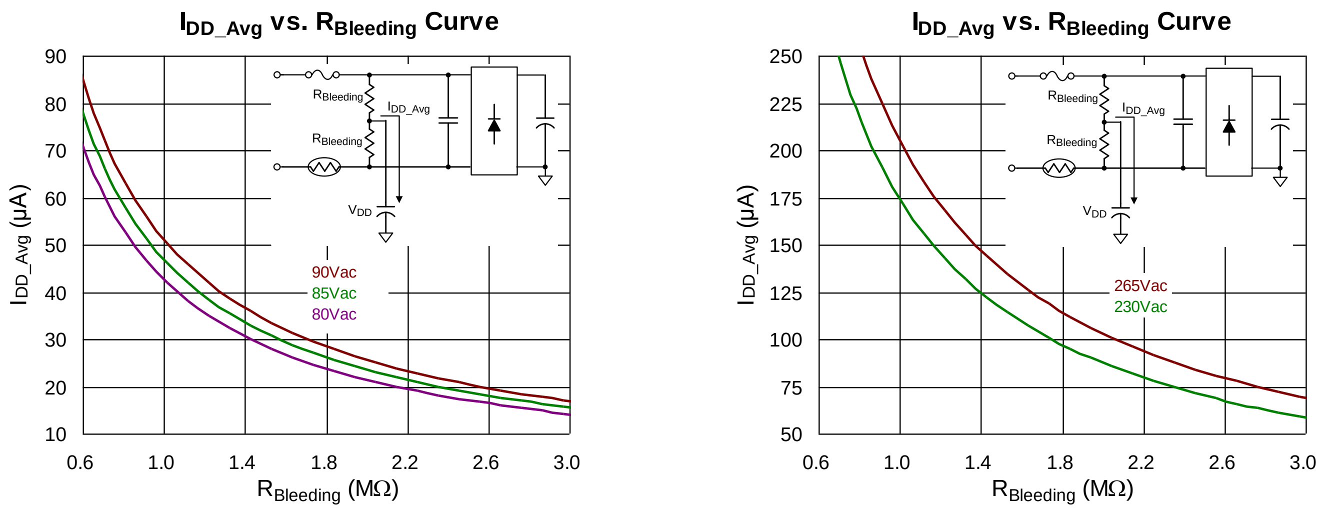



Figure 7. $I_{DD\_Avg}$ vs. $R_{Bleeding}$ Curve

### VDD Discharge Time in Auto Recovery Mode

Figure 8 shows the $V_{DD}$ and $V_{GATE}$ waveforms during an auto recovery protection (e.g., OLP). In this mode, the start-up resistors, VDD sinking current and VDD decoupling capacitor will affect the restart time. The VDD voltage discharge time $t_{D\_Discharge}$ can be calculated by the following equation :

$$t_{D\_Discharge} = \frac{C_{VDD} \times (V_{DD\_DIS} - V_{TH\_OFF})}{I_{DD\_ARP} - I_{ST}}$$

Where the $C_{VDD}$ is the VDD decoupling capacitor, the $V_{DD\_DIS}$ is the initial VDD voltage after entering the auto recovery mode, the $V_{TH\_OFF}$ (9V typ.) is the falling UVLO voltage threshold of the controller, the $I_{DD\_ARP}$ (550μA typ.) is the sinking current of the VDD pin in the auto recovery mode, and $I_{ST}$ is the start-up current of the power system.

Please note that the start-up current at high input voltage must be smaller than the $I_{DD\_ARP}$. Otherwise, the VDD voltage can't reach the $V_{TH\_OFF}$ to activate the next start-up process after an auto recovery protection. Therefore, the system behavior resembles the behavior of latch mode.

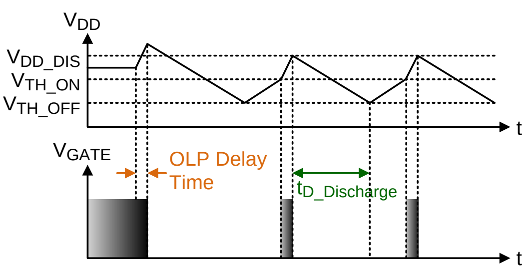



Figure 8. Auto Recovery Mode (e.g., OLP)

### VDD Holdup Mode

The VDD holdup mode is only designed to prevent VDD from decreasing to the turn-off threshold voltage, $V_{TH\_OFF}$, under light load or load transient. Compare to burst mode, the VDD holdup mode brings higher switching. Hence, it is highly recommended that the system should avoid operating at this mode during light load or no load conditions.

### Output Short Protection

The RT7738F implements output short protection by detecting output signal of DMAG pin after delay time ($T_{D\_OSP}$). It can minimize the power loss and temperature during output short, especially at high line input voltage.

### Resistors on GATE Pin

In Figure 9, $R_G$ is applied to alleviate ringing spike of gate drive loop in typical application circuits. The value of $R_G$ must be considered carefully with respect to EMI and efficiency for the system.

The built-in internal discharge resistor $R_{ID}$ in parallel with GATE pin prevents the MOSFET from any uncertain condition. If the connection between the GATE pin and the Gate of the MOSFET is disconnected, the MOSFET will be false triggered by the residual energy through the Gate-to-Drain parasitic capacitor $C_{GD}$ of the MOSFET and the system will be damaged. Therefore, it's highly recommended to add an external discharge-resistor $R_{ED}$ connected between the Gate of MOSFET and GND terminals. The energy through the $C_{GD}$ is discharged by the external discharge-resistor to avoid MOSFET false triggering.

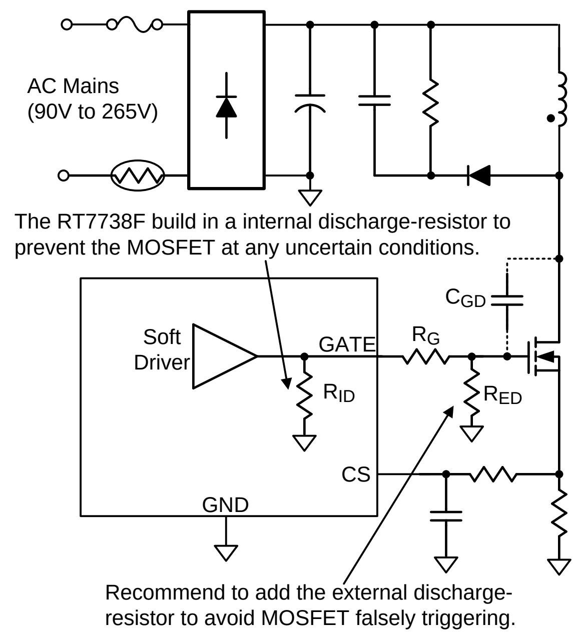



Figure 9. Resistors on Gate Pin

#### Feedback Resistor

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced, as shown in Figure 10. Due to small feedback resistor current, shunt regulator selection (e.g. TL-431) and minimum regulation current design must be considered carefully to make sure it's able to regulate under low cathode current.

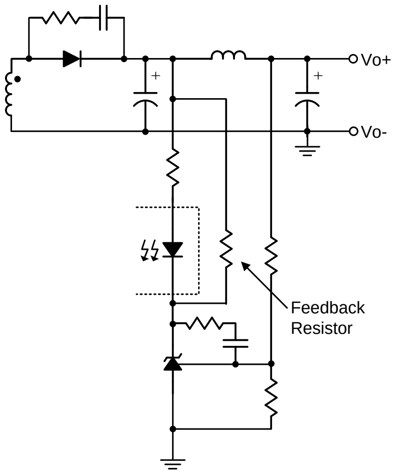



Figure 10. Feedback Resistor

#### Negative Voltage Spike on Each Pin

Negative voltage (<–0.3V) to the controller pins will cause substrate injection and lead to controller damage or circuit false triggering. For example, the negative spike voltage at the CS pin may come from improper PCB layout or inductive current sense resistor. Therefore, it is highly recommended to add an R-C filter to avoid the CS pin damage, as shown in Figure 11. Proper PCB layout and component selection should be considered during circuit design.

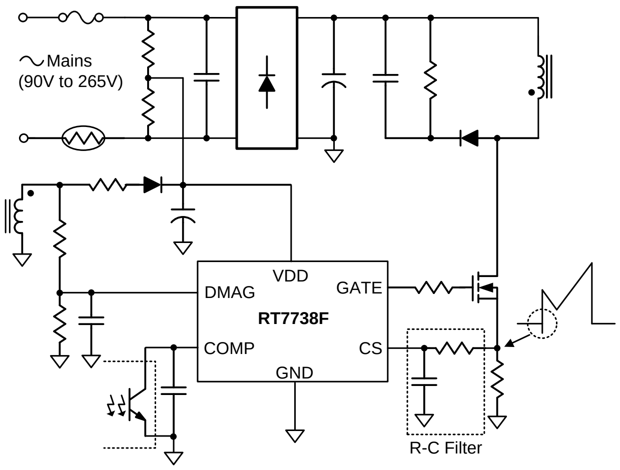



Figure 11. R-C Filter on CS Pin

#### Internal Over-Temperature Protection

The RT7738F provides OTP function to prevent permanent damage. It is not recommended to apply this function to accurate temperature control.

When the IC turns on, the controller detects around temperature before it starts switching. If the temperature is higher than $T_{OTP\_INTH}$ (typ. 130°C), the controller triggers OTP, and there is no output signal. If the temperature is lower than $T_{OTP\_INTH}$, the controller starts operation and the OTP threshold is automatically set to $T_{OTP\_STTH}$ (typ.140°C), which means when the controller starts switching, the OTP threshold is $T_{OTP\_STTH}$.

When the controller triggers OTP, the controller will be shut down and cease switching. At the same time, $V_{DD}$ drops below $V_{DD}$ off threshold $V_{TH\_OFF}$, the controller enters hiccup mode.

#### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For SOT-23-6 package, the thermal resistance, $\theta_{JA}$, is 260.7°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (260.7°C/W) = 0.38W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 12 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

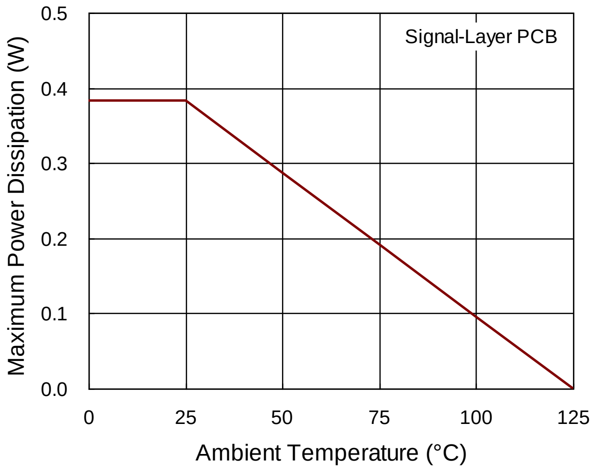



Figure 12. Derating Curve of Maximum Power Dissipation

## Layout Consideration

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply :

- The current path (1) through bulk capacitor, transformer, MOSFET, $R_{CS}$ returns to bulk capacitor is a high frequency current loop. It must be as short as possible to decrease noise coupling and keep away from other low voltage traces, such as IC control circuit paths, especially.
- The path (2) of the RCD snubber circuit is also a high switching loop. Keep it as small as possible.
- Separate the ground traces of bulk capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d) for reducing noise, output ripple and EMI issue. Connect these ground traces together at bulk capacitor ground (a). The areas of these ground traces should be large enough.
- Place the bypass capacitor as close to the controller as possible.
- In order to reduce reflected trace inductance and EMI, minimize the area of the loop connecting the secondary winding, output diode and output filter capacitor. In additional, apply sufficient copper area at the anode and cathode terminal of the diode for heatsinking.

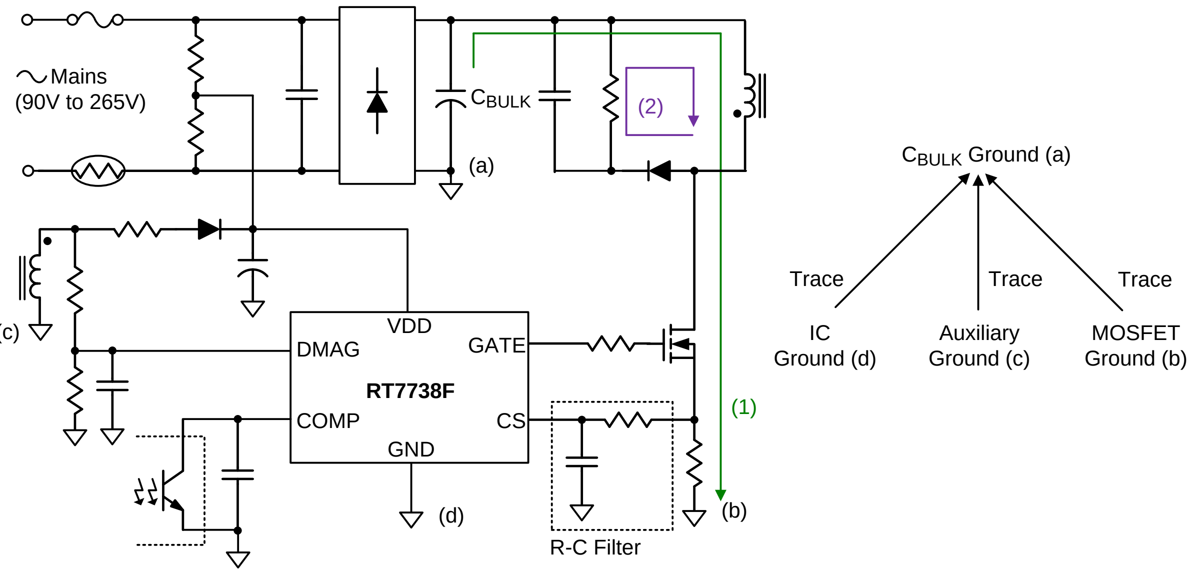
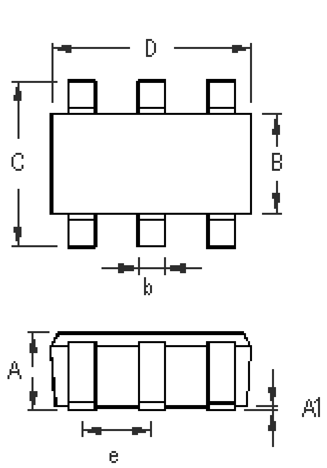



Figure 13. PCB Layout Guide

## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.889 | 1.295 | 0.031 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.250 | 0.560 | 0.010 | 0.022 |
| C | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

**SOT-23-6 Surface Mount Package**

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