PWM Controller for Programmable Power Converter (USBPD)

General Description

The RT7755GEK series is specifically designed to work with controllers, such as the RT7206, to provide a total solution for USB PD or a programmable power adapter. This RT7755GEK not only provides a high power efficiency control scheme, but also gives a 50mW very low standby power control under 5V standby condition.

The RT7755GEK is such a special design to achieve a wide-range of output voltage by utilizing several innovations, including (1) By using DMAG pin, the RT7755GEK senses output voltage to adjust loop gain for system stability, to adjust output over-voltage protection threshold voltage to protect external devices, and to adjust current limit to meet Limited Power Source (LPS) safety requirements; (2) The RT7755GEK is also equipped with comprehensive protection features, including bulk-capacitor brown-in/brown-out protection, VDD over-voltage protection (VDD OVP), output over-voltage/under-voltage protection (Output OVP/UVP), secondary rectifier short-circuit protection (SRSP), and external over-temperature protection (External OTP); (3) For constant output power regulation, a resistor connected to CS pin can be used to achieve accurate line compensation across the universal input voltage range; and (4) The RT7755GEK also provides various features to protect against any failures occurring at the secondary-side component, such as the RT7206 or a shunt regulator.

In applications, it is suggested that the RT7755GEK be used with a secondary controller RT7206 to realize a robust and safe design to prevent all potential fault conditions due to misconnection of various devices, cables, plugs and receptacles.

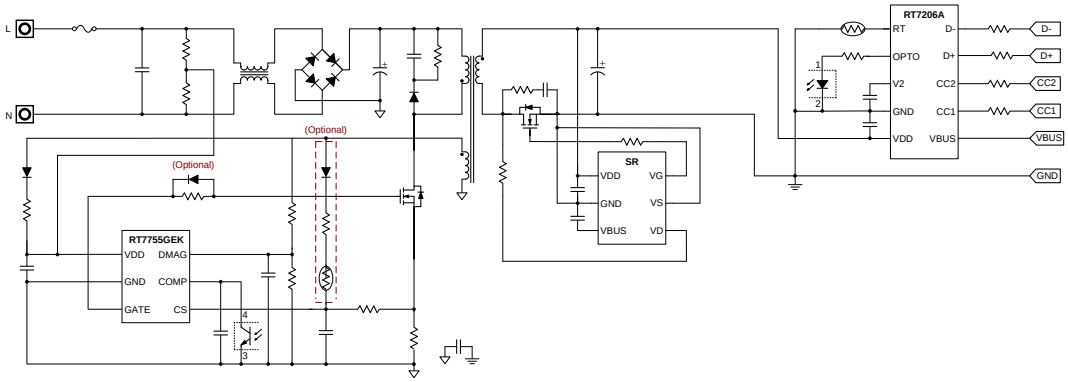
Features

- **Optimized for Adaptive Output Power**
  - **Wide VDD Range : 9V to 64V**
  - **Adaptive Output Over-Voltage Protection**
  - **Adaptive Over-Current Protection**
  - **Adaptive Loop Gain Control for Loop Stability**
- **High Efficiency**
  - **Green Mode Operation at Light Load and No Load**
- **Comprehensive Protection Features**
  - **Bulk-Capacitor Brown-In and Brown-Out Protection**
  - **VDD Over-Voltage Protection**
  - **Output Over-Voltage and Under-Voltage Protection**
  - **External Over-Temperature Protection**
  - **Secondary Rectifier Short-Circuit Protection**
  - **Programmable Line Compensation**
- **Others**
  - **< 50mW in 5V Standby Mode for Power Saving**
  - **Driver Capability : 300mA/–300mA**
  - **SmartJitter™ Technology**

Applications

- USB PD and Programmable Power Adapters

Simplified Application Circuit



Ordering Information

RT7755□□□□□

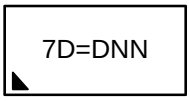
- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green
  (Halogen Free and Pb Free)
- V_{OUT} Application Version
  (Refer to Version Table)
- Protection Mode Version
  (Refer to Version Table)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

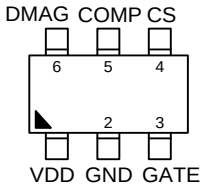
Marking Information



7D= : Product Code
DNN : Date Code

Pin Configuration

(TOP VIEW)



SOT-23-6

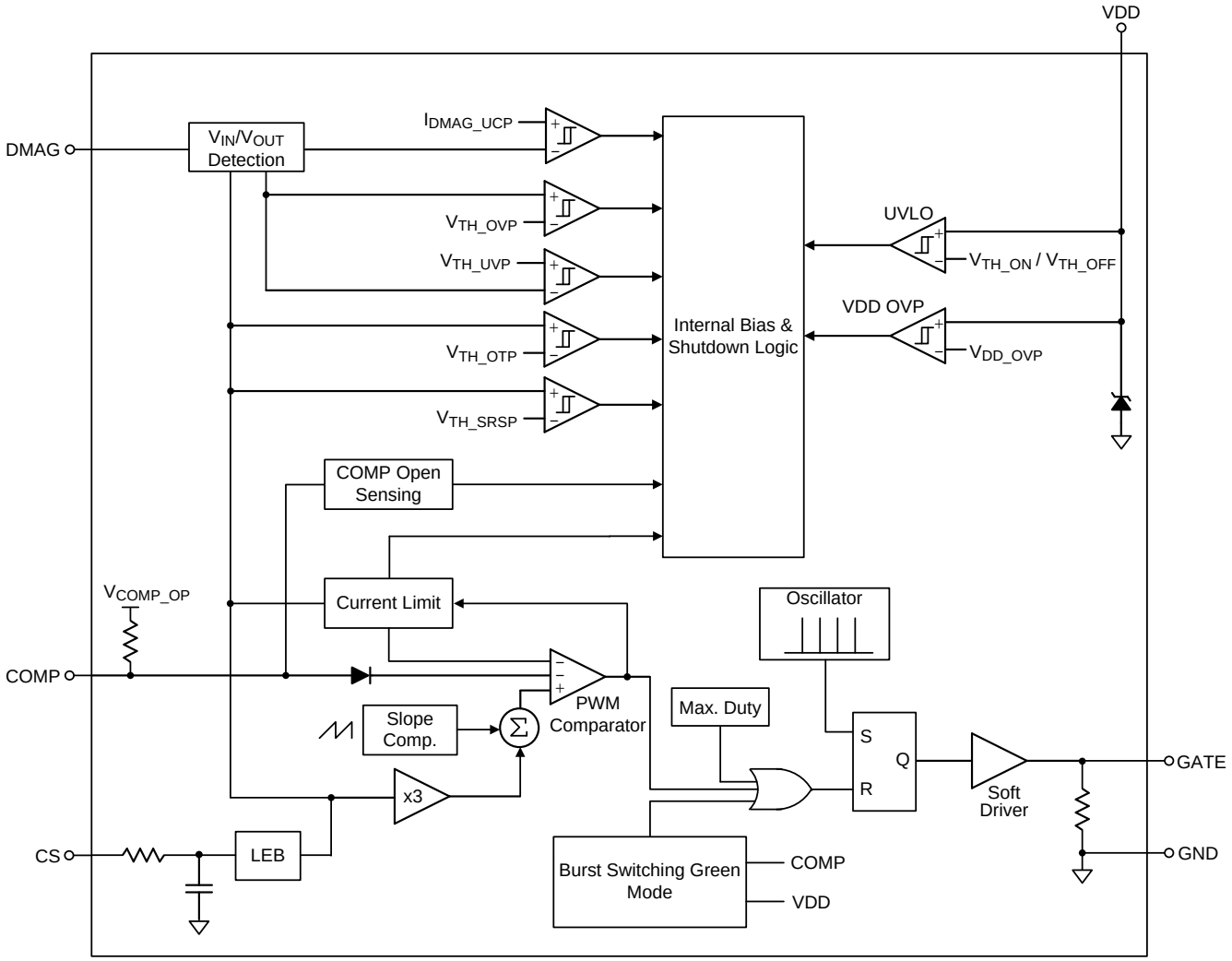
RT7755GEK Version Table

Version	RT7755GEK
Operation Mode	CCM (I_{DMAG} < I_{DMAG_HVSW}) QR Mode (I_{DMAG} > I_{DMAG_HVSW})
Constant Power Application (Disable Adaptive OCP)	X
Maximum Normal Output Voltage, $V_{O\_NOR\_MAX}$	20V
Normal-Mode PWM Frequency	130kHz
Minimum Green-Mode Frequency	25kHz
Minimum QR Frequency	41.3kHz
Adaptive OVP	Auto-Recovery
Start-Up OVP	X
VDD OVP	Auto-Recovery
VDD Over-Voltage Protection Threshold Voltage	67V
Output OVP	Auto-Recovery
Output Voltage Threshold of OVP, V_{O_OVP}	24V
Output UVP	Auto-Recovery
OCP	Auto-Recovery
OCP Delay Time	63ms
SRSP	Auto-Recovery
External OTP	Auto-Recovery
Valley Switching Mode	O
Valley Jitter Function	O

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDD	Supply input voltage. The controller is enabled when the VDD voltage exceeds V_{TH_ON}, and is disabled when the VDD voltage drops below V_{TH_OFF}.
2	GND	Ground of the Controller.
3	GATE	Gate driver output.
4	CS	Current sense input. The current sense resistor, connected from the CS pin to GND, is used to set current limit for the power system.
5	COMP	Feedback input. Connect an opto-coupler from the COMP pin to GND to close the control loop to achieve output voltage regulation.
6	DMAG	Demagnetization input. Input and output voltages are sensed from the auxiliary winding.

Functional Block Diagram



Operation

The RT7755GEK series is specifically designed to work with a USB PD controller or a programmable power adapter controller as a total solution. For applications with wide output voltage range, the RT7755GEK features many innovations, including adaptive output over-voltage protection, adaptive over-current protection and adaptive loop stability control.

Multi-Mode PWM

The RT7755GEK is a PWM controller, which provides a multi-mode control to optimize performance under different load conditions. With an internal oscillator to provide a PWM frequency for system to operate in continuous conduction mode (CCM) or quasi-resonant mode (QR mode), this controller will automatically enter into green mode when in light load or in no load condition.

Gate Driver

A totem-pole gate driver is designed to meet the requirements for both EMI and efficiency in low-power applications. An internal pull-down circuit is included to prevent the external MOSFET from being falsely turned on when VDD is too low and an under-voltage lockout (UVLO) event is triggered.

SmartJitter™ Technology

In general PWM controllers, frequency jittering scheme is usually adopted to spread frequency spectrum in order to alleviate EMI problems. However, due to inherent operating characteristics of the valley switching mode and the green mode, the frequency spectrum in high line conditions or in deeper extended valley switching conditions cannot be spread wide enough as expected, which therefore degrades suppression of the EMI emissions.

The RT7755GEK employs RICHTEK's proprietary SmartJitter™ technology to optimize the frequency jittering range. The innovative SmartJitter™ technology can reduce EMI emissions of a switch-mode power supply as well as output ripple as a consequence of frequency jittering in all operation conditions.

Adaptive Output Over-Voltage Protection

For applications with a wide output voltage range, the RT7755GEK also provides the proprietary adaptive output over-voltage protection. The adaptive output over-voltage protection threshold is automatically adjusted according to the output voltage when activating an output OVP under fault conditions.

Secondary Rectifier Short Protection (SRSP)

When secondary rectifier or secondary MOSFET short-circuit condition occurs during the primary MOSFET on-time, the main transformer becomes saturated and the rising rate of the primary-side current is then limited only by the leakage inductance of the transformer, which is about a few percentage of the primary magnetizing inductance. Therefore, the current slope is much higher than that in normal operation. In high line condition, peak current through the primary MOSFET will become extremely high after over-current protection delay time elapses. To provide a reliable protection, the RT7755GEK is designed to shut down in a few cycles once secondary rectifier short-circuit condition is detected.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD to GND ---------- –0.3V to 70V
- GATE to GND ---------- –0.3V to 16.5V
- DMAG, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 260.7°C/W
  SOT-23-6, θ_{JC} ---------- 135°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 9V to 64V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Over-Voltage Protection Threshold Voltage	V_{DD_OVP}		65	67	69	V
VDD Under-Voltage Protection Threshold Voltage	V_{DD_UVP}	V_{COMP} > 3.0V, V_{DMAG} < V_{TH_UVP}	7	7.5	8	V
Turn-On Threshold Voltage	V_{TH_ON}		14	17	19.5	V
Turn-Off Threshold Voltage	V_{TH_OFF}		6.5	7	7.5	V
VDD Holdup Mode Entry Point	V_{DD_ET}		7	7.5	8	V
VDD Holdup Mode Ending Point	V_{DD_ED}		V_{DD_ET} + 0.1	V_{DD_ET} + 0.5	V_{DD_ET} + 0.9	V
Start-Up Current	I_{DD_ST}	V_{DD} < V_{TH_ON} – 0.1V	--	1.5	3	μA
Operating Supply Current	I_{DD_OP}	V_{DD} = 15V, V_{COMP} = 0V	--	320	450	μA
I_{DD} Sinking Current for Auto-Recovery Mode	I_{DD_ARP}	During entering auto-recovery mode	400	575	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Section						
Normal-Mode PWM Frequency	f_{NOR}	$V_{COMP} > V_{GM\_ET}$	120	130	140	kHz
Minimum Green-Mode Frequency	f_{GM_MIN}	$V_{COMP} < V_{GM\_ED}$	21	25	29	kHz
Minimum QR Frequency	f_{QR_MIN}	$I_{DMAG} > I_{DMAG\_HVSW}$, f_{OSC} = 130kHz	35	41.3	47.6	kHz
Maximum Duty for CCM	D_{MAX}	$I_{DMAG} < I_{DMAG\_HVSW}$ (Note 6)	80	85	90	%
Maximum On-Time for QR Mode	t_{ON_MAX}	$I_{DMAG} > I_{DMAG\_HVSW}$ (Note 6)	12.2	15.2	18.2	μs
PWM Frequency Jittering Range	Δf		±3	±6	±9	%
PWM Frequency Jittering Period	t_{JIT}	f_{OSC} = 130kHz (Note 5)	6.3	7.9	9.5	ms
Frequency Variation Versus VDD Deviation	f_{DV}	V_{DD} = 8.5V to 23V	--	2	3	%
Frequency Variation Versus Temperature Deviation	f_{DT}	T_A = −30°C to 105°C (Note 5)	--	5	6	%
COMP Input Section						
Open-Loop Voltage	V_{COMP_OP}	Comp pin open-circuited	3.2	3.4	3.6	V
COMP Short-Circuit Current	I_{ZERO}	V_{COMP} = 0V	130	170	210	μA
COMP Open-Loop Protection Delay Time	t_{COMP_OP}	f_{OSC} = 130kHz	50.4	63	75.6	ms
Green Mode Entry Voltage	V_{GM_ET}	$I_{DMAG} > I_{DMAG\_HVSW}$, $V_{GM\_ET} = V_{COMP} - V_F$, V_F = 0.7V when T_A = 25°C	1.35	1.41	1.47	V
		$I_{DMAG} < I_{DMAG\_HVSW}$, $V_{GM\_ET} = V_{COMP} - V_F$, V_F = 0.7V when T_A = 25°C	1.15	1.21	1.27	
Green Mode Ending Voltage	V_{GM_ED}	$I_{DMAG} > I_{DMAG\_HVSW}$, $V_{GM\_ED} = V_{COMP} - V_F$, V_F = 0.7V when T_A = 25°C	1	1.06	1.12	V
		$I_{DMAG} < I_{DMAG\_HVSW}$, $V_{GM\_ED} = V_{COMP} - V_F$, V_F = 0.7V when T_A = 25°C	0.8	0.86	0.92	
Zero-Duty Entry Voltage	V_{ZD_ET}	V_{DMAG} > 2.7V $V_{ZD\_ET} = V_{COMP} - V_F$, V_F = 0.7V when T_A = 25°C	0.54	0.6	0.66	V
		V_{DMAG} < 0.9V $V_{ZD\_ET} = V_{COMP} - V_F$, V_F = 0.7V when T_A = 25°C	0.24	0.3	0.36	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Zero-Duty Ending Voltage	V_{ZD_ED}	V_{DMAG} > 2.7V V_{ZD_ED} = V_{COMP} - V_F, V_F = 0.7V when T_A = 25°C	0.565	0.625	0.685	V
		V_{DMAG} < 0.9V V_{ZD_ED} = V_{COMP} - V_F, V_F = 0.7V when T_A = 25°C	0.265	0.325	0.385	
Current Sense Section						
Maximum Current Limit	V_{CS_MAX}	V_{DMAG} = 3V	0.38	0.4	0.42	V
Over-Current Protection Delay Time	t_{D_OCP}	f_{OSC} = 130kHz	50.4	63	75.6	ms
Leading-Edge Blanking Time	t_{LEB}		225	350	475	ns
Secondary Rectifier Short-Circuited Protection Threshold Voltage	V_{TH_SRSP}		1.1	1.2	1.3	V
External Over-Temperature Protection Threshold Voltage	V_{TH_OTP}	V_{DMAG} = 3V	0.75	0.8	0.85	V
External Over-Temperature Protection Delay Time	t_{D_OTP}	f_{OSC} = 130kHz	50.4	63	75.6	ms
GATE Section						
Rising Time	t_R	C_L = 1nF	150	280	410	ns
Falling Time	t_F	C_L = 1nF	10	40	70	ns
GATE Output Clamp Voltage	V_{CLAMP}	V_{DD} = 23V	10	12	14	V
DMAG Section						
Output Over-Voltage Protection Threshold Voltage	V_{TH_OVP}		3.5	3.6	3.7	V
Output Under-Voltage Protection Threshold Voltage	V_{TH_UVP}		0.3	0.35	0.4	V
Output Under-Voltage Protection Delay Time	t_{D_UVP}	f_{OSC} = 130kHz	6.7	7.9	9.1	ms
Blanking Time of DMAG Pin	t_{BLK}	V_{CS_PK} = 0V	0.8	1	1.2	µs
Brown-In Protection Threshold Current	I_{DMAG_BNI}		174	192	210	µA
Brown-Out Protection Threshold Current	I_{DMAG_BNO}		156	174	192	µA
Brown-Out Protection Delay Time	t_{D_BNO}	f_{OSC} = 130kHz	50.4	63	75.6	ms
High Line Input Voltage Entry Level	I_{DMAG_HVSW}		336	396	456	µA
Hysteresis of High Line Input Voltage Entry	I_{DMAG_HVHYS}		0.1	8.4	17	µA
Disable Valley Switching Threshold Voltage	V_{DIS_VALLEY}		0.95	1.05	1.15	V
Enable Valley Switching Threshold Voltage	V_{EN_VALLEY}		1.05	1.15	1.25	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum DMAG Sourcing Current	I_{DMAG_MAX}		1500	--	--	μA
DMAG Under-Current Protection Threshold Current	I_{DMAG_UCP}		13.4	26.4	39.4	μA

Note1. Stresses beyond those listed under ”Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard.

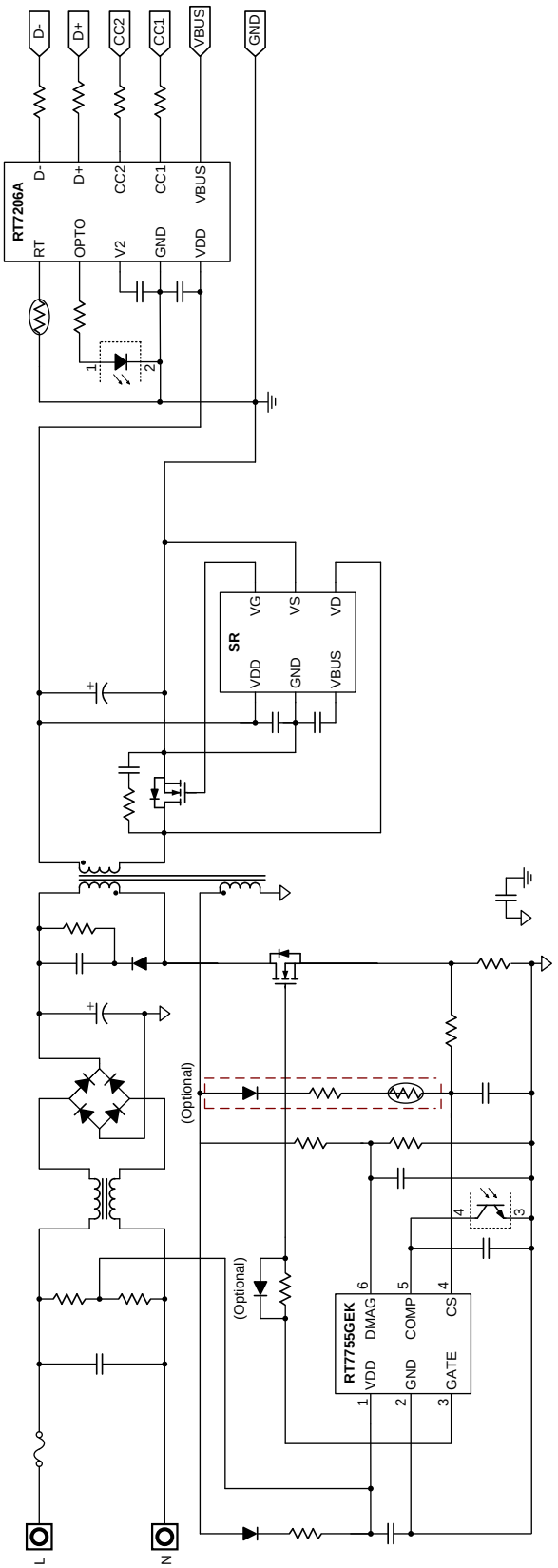
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

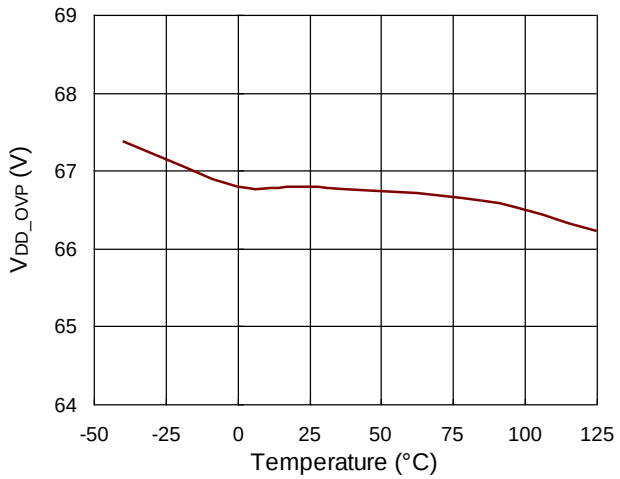
Note 6. For the synchronous rectifier (SR) application, the minimum on-time of SR can not overlap the minimum off-time of PWM controller in any condition. The minimum off-time of PWM controller is affected by the maximum frequency, the maximum duty, the PWM frequency jittering range, and the frequency variation versus temperature deviation.

Typical Application Circuit

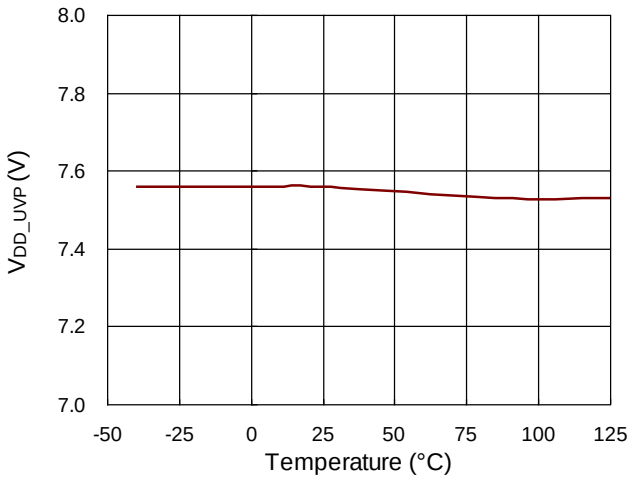


Typical Operating Characteristics

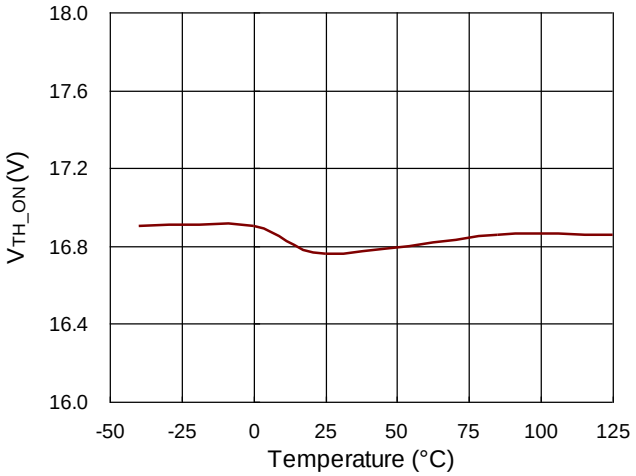
V_{DD_OVP} vs. Temperature



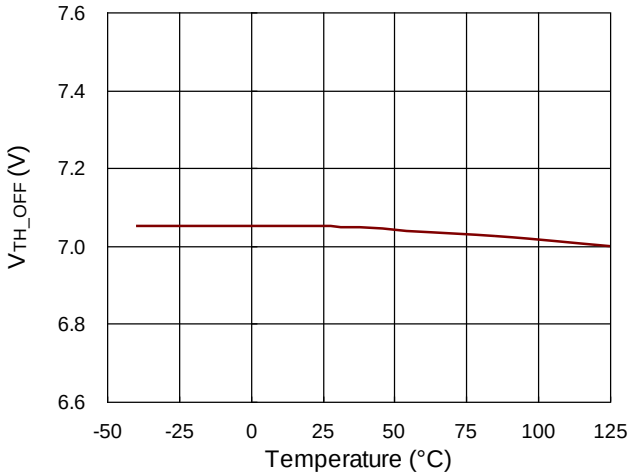
V_{DD_UVP} vs. Temperature



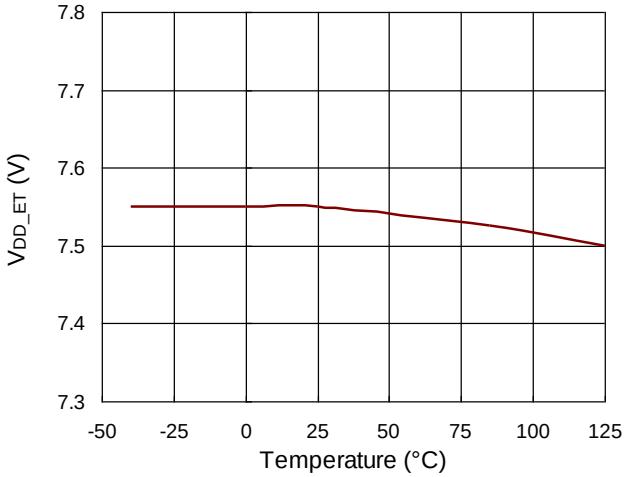
V_{TH_ON} vs. Temperature



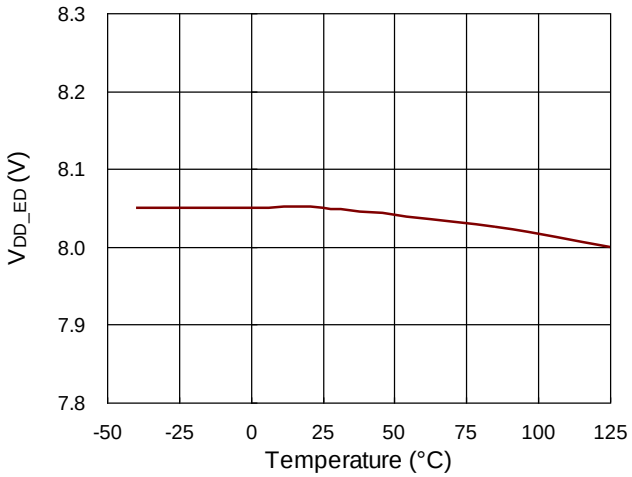
V_{TH_OFF} vs. Temperature

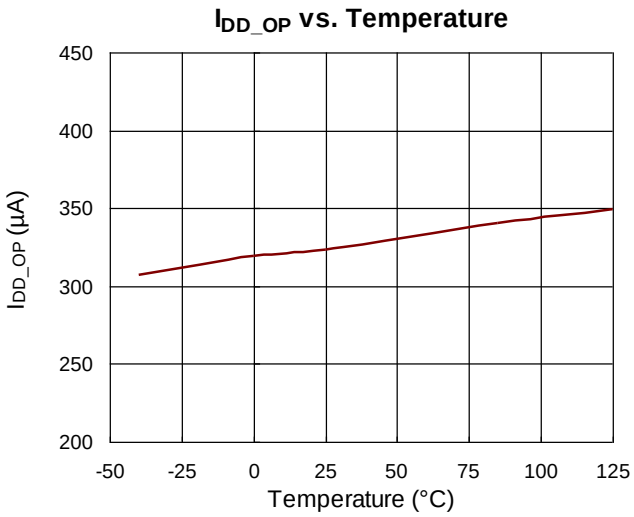


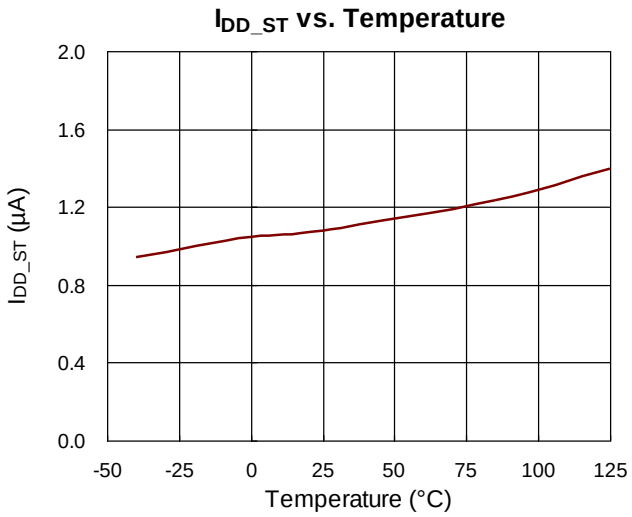
V_{DD_ET} vs. Temperature

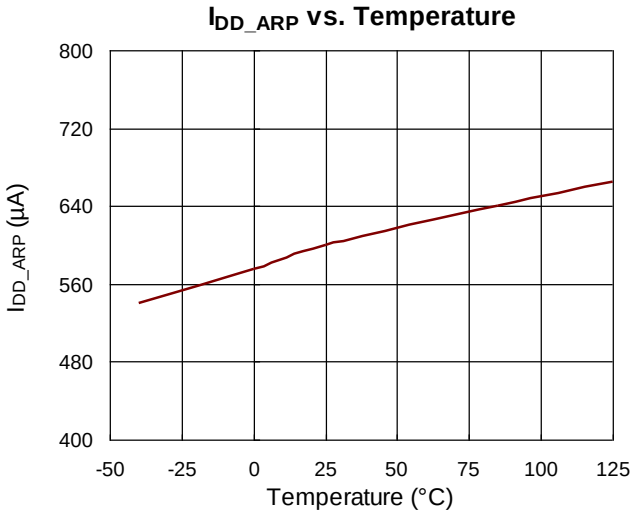


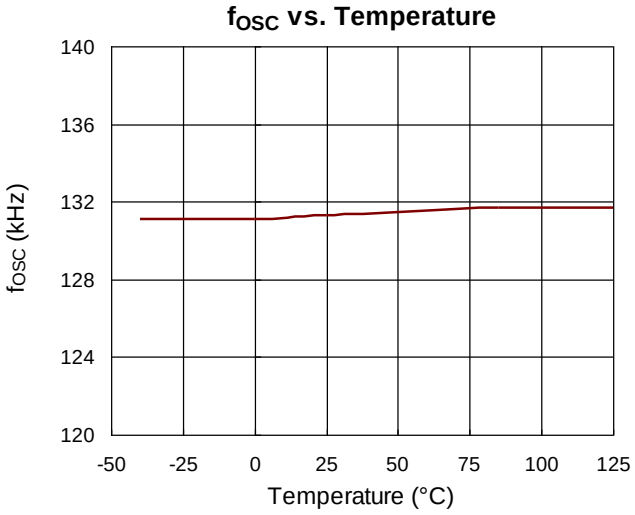
V_{DD_ED} vs. Temperature

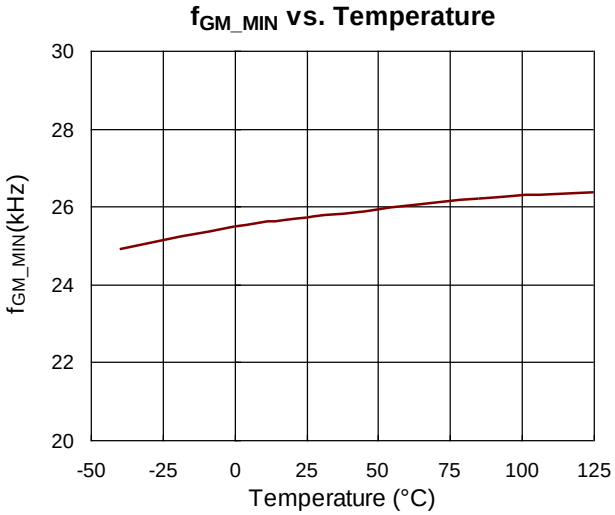


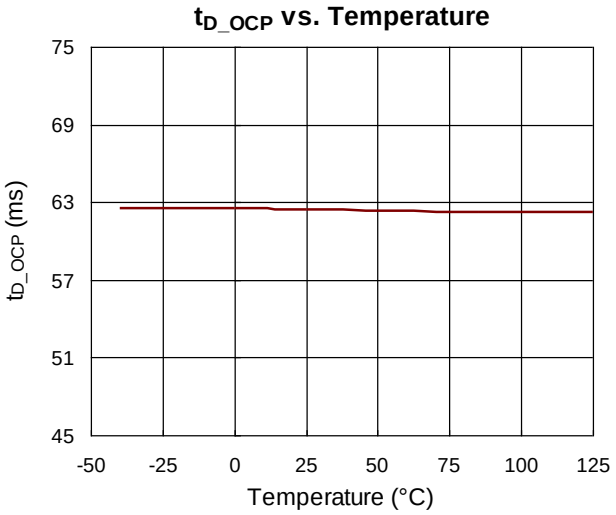


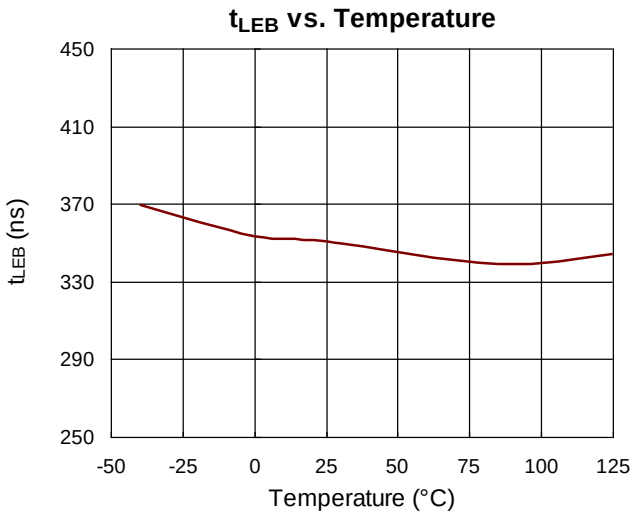


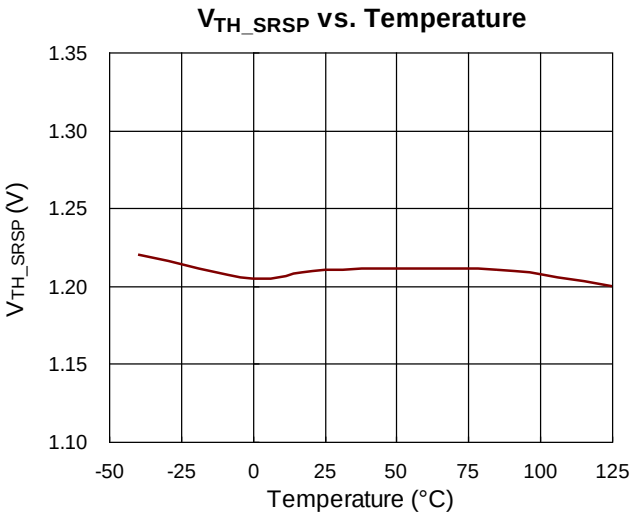


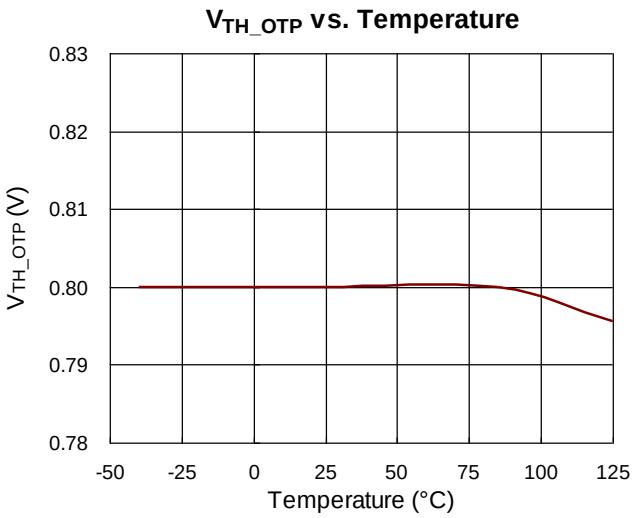


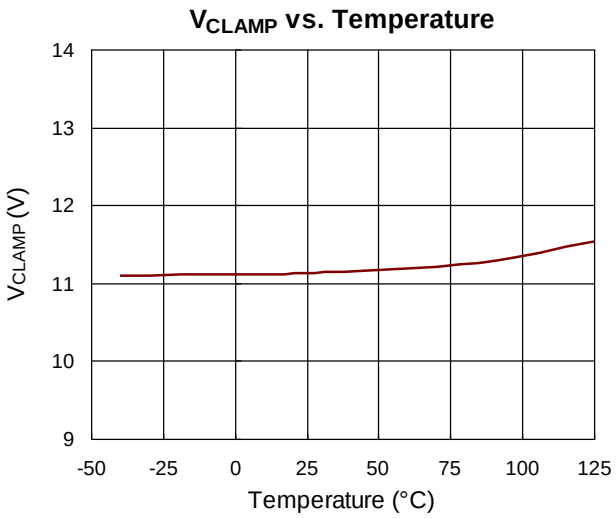


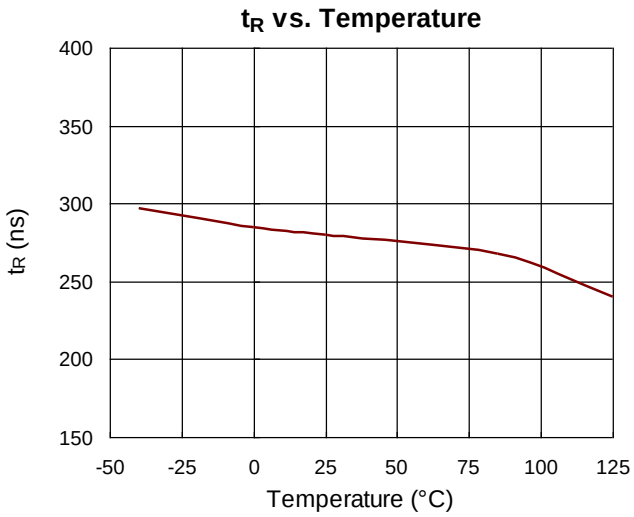


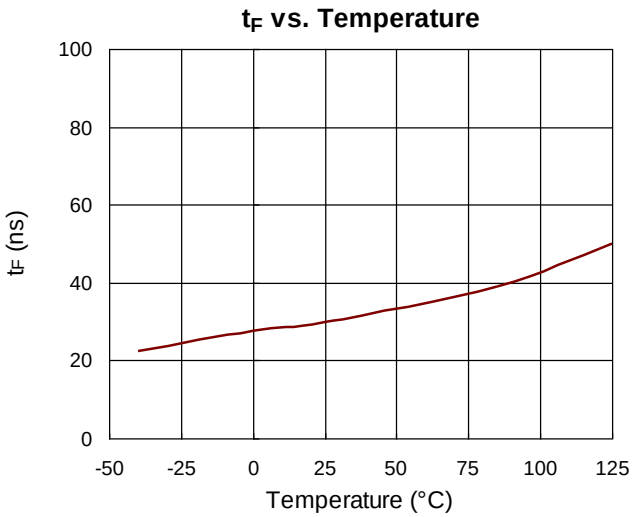


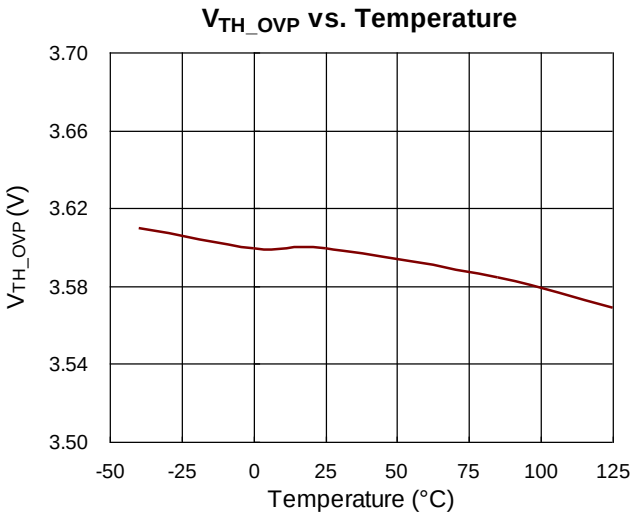


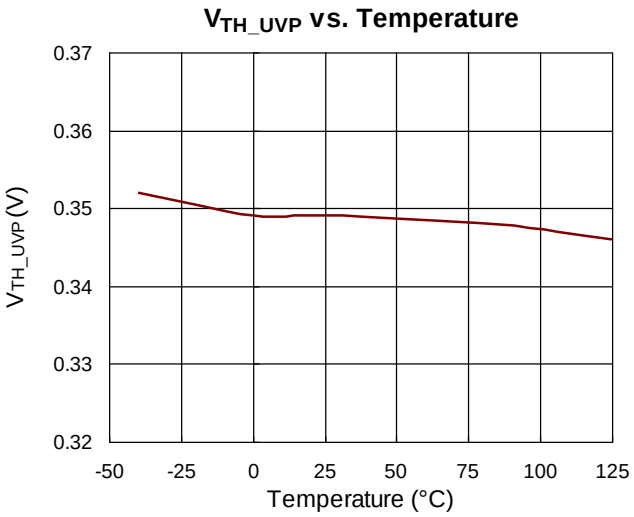


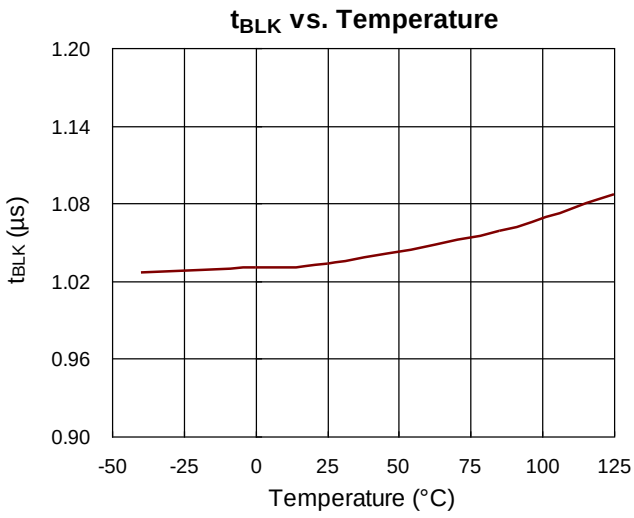


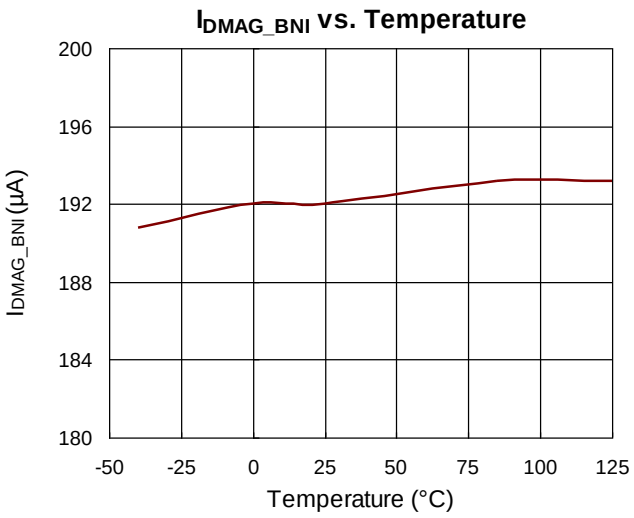


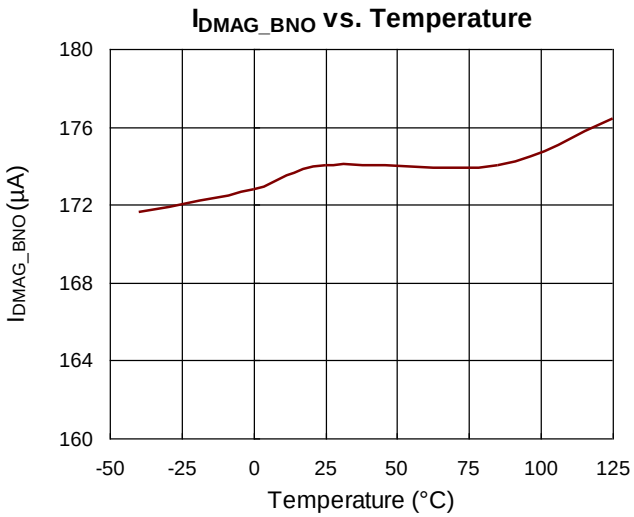


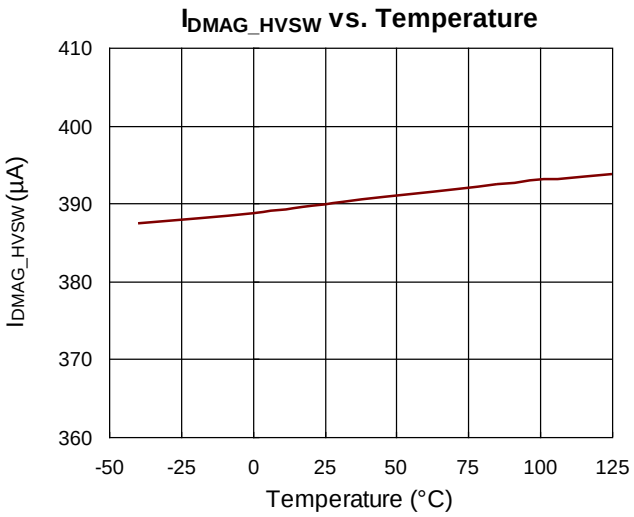




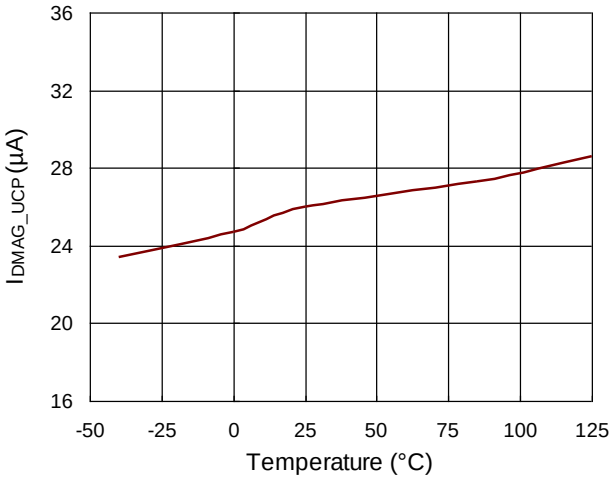




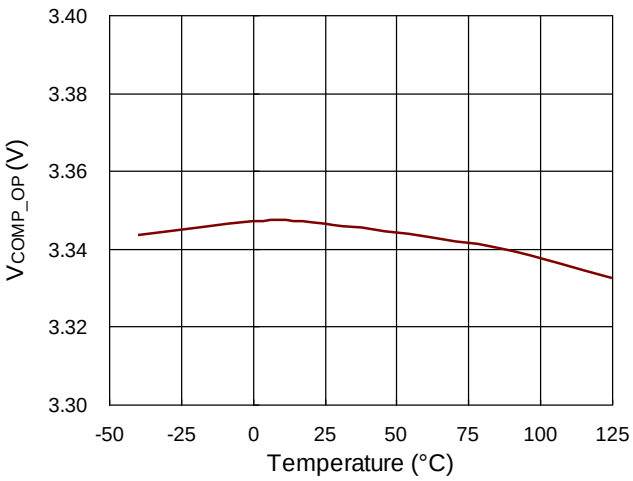




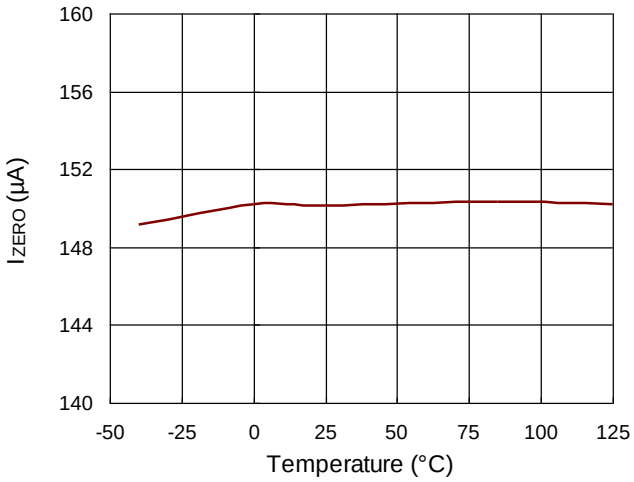
I_{DMAG_UCP} vs. Temperature



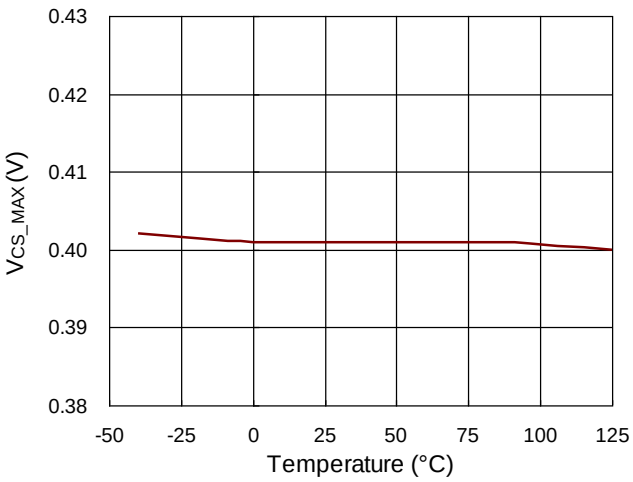
V_{COMP_OP} vs. Temperature



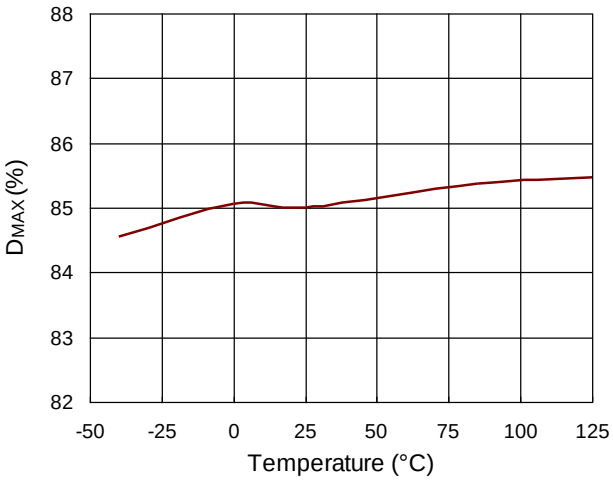
I_{ZERO} vs. Temperature



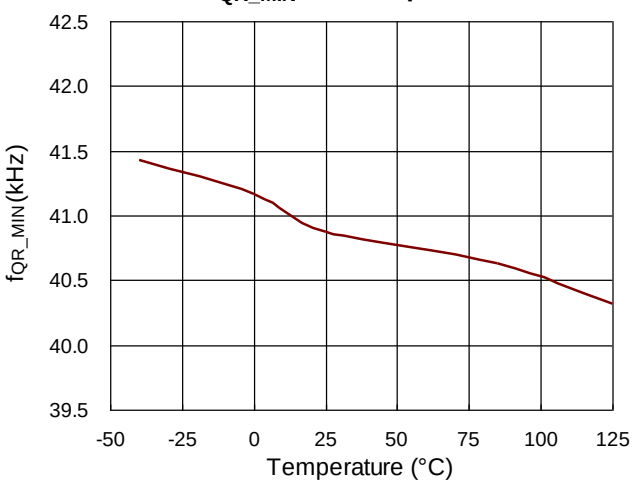
V_{CS_MAX} vs. Temperature

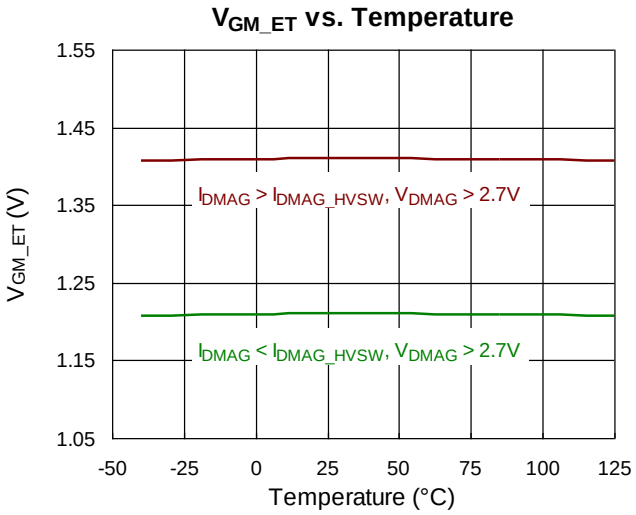


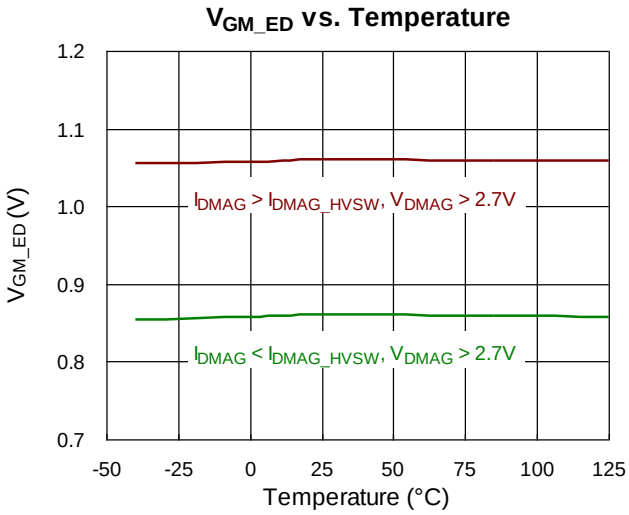
D_{MAX} vs. Temperature



f_{QR_MIN} vs. Temperature







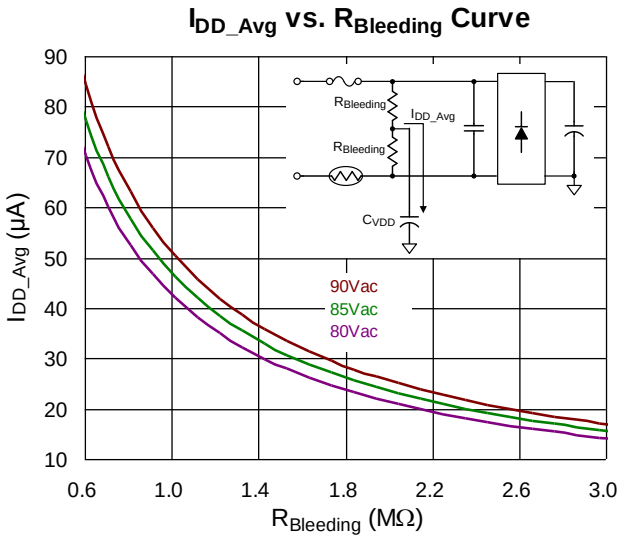
Application Information

The RT7755GEK is a multi-mode PWM flyback controller providing different operational modes, such as the green mode, and the burst mode. The RT7755GEK can automatically switch among several control modes to optimize efficiency for the power system when operating under various load conditions.

Start-Up Circuit

To optimize power efficiency, bleeder resistors can be added to the start-up circuit, which not only reduces power loss but can reset latched-mode protections faster. Figure 1 shows the curve for IDD average current I_{DD_Avg} vs. bleeder resistance ($R_{Bleeder}$). The curve can be used to design bleeder resistance values.

During the hiccup mode, the off-time duration is extended to minimize power loss and heat dissipation. When as the auto-recovery protection mode, the controller sinks a very small sinking current, I_{DD_ARP}. The start-up current at maximum AC line input voltage must be smaller than I_{DD_ARP} (Min). Otherwise, when the controller enters an auto-recovery protection mode, the VDD capacitor cannot be discharged to V_{TH_OFF} by the sinking current I_{DD_ARP} to restart the controller. The controller will then behave as in a latched-protection mode or even trigger the silicon controlled rectifier (SCR) of VDD.



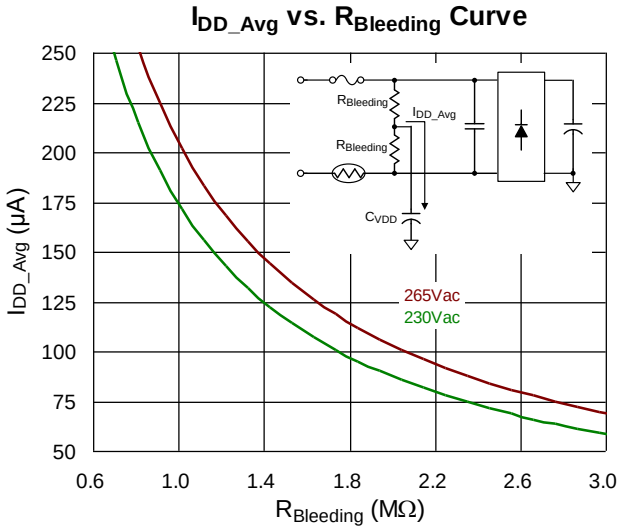


Figure 1. Start-Up Circuit

VDD Discharge Time in Auto-Recovery Mode

Figure 2 shows the V_{DD} and V_{GATE} waveforms during an auto recovery protection (e.g., OCP). In this mode, the start-up resistors, VDD sinking current and VDD decoupling capacitor affect the restart time. The VDD voltage discharge time $t_{D\_Discharge}$ can be calculated by the following equation :

$$t_{D\_Discharge} = \frac{C_{VDD} \times (V_{DD\_DIS} - V_{TH\_OFF})}{I_{DD\_ARP} - I_{ST}}$$

Where the C_{VDD} is the VDD decoupling capacitor; the V_{DD_DIS} is the initial VDD voltage after entering the auto recovery mode; the V_{TH_OFF} (Typ.) is the falling UVLO voltage threshold of the controller; the I_{DD_ARP} (Typ.) is the sinking current of the VDD pin in the auto-recovery mode; and I_{ST} is the start-up current of the power system.

Note that the start-up current at high input voltage must be smaller than the I_{DD_ARP}. Otherwise, the VDD voltage cannot reach the V_{TH_OFF} to activate the next start-up process after an auto-recovery protection. Therefore, the system behavior resembles the behavior of latch mode.

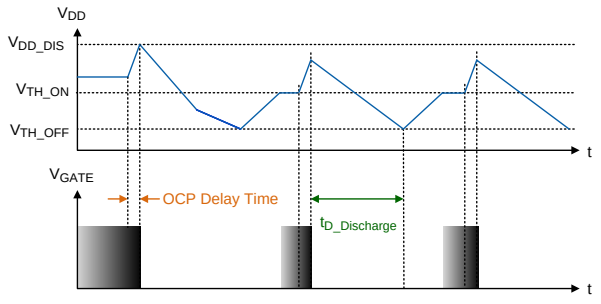


Figure 2. Auto-Recovery Mode (e.g., OCP)

DMAG Pin

During the MOSFET on-time, the auxiliary winding voltage is negative, and the RT7755GEK outputs a clamp current, proportional to the input line voltage, to clamp the DMAG voltage at 0.1V. The RT7755GEK has built-in characteristics for the DMAG pin, namely, a DMAG brown-in protection threshold current I_{DMAG_BNI} and a DMAG brown-out protection threshold current I_{DMAG_BNO}. The bulk-capacitor brown-in and brown-out threshold voltages, V_{BULK_BNI} and V_{BULK_BNO}, can be programmed by adjusting R_{DMAG1} and R_{DMAG2} at the DMAG pin, as shown in Figure 3.

Once one of the brown-in and brown-out threshold voltages is set, the other one can be determined accordingly. The bulk-capacitor brown-out threshold voltage V_{BULK_BNO} can be obtained according to the following equation :

$$V_{BULK\_BNO} = \frac{V_{BULK\_BNI} \times I_{DMAG\_BNO}}{I_{DMAG\_BNI}}$$

When the MOSFET turns off, the DMAG pin senses the output voltage of the power stage across the auxiliary winding, with a ratio equal to the turns ratio of the auxiliary and secondary windings, and then scaled with the resistive divider R_{DMAG2} / R_{DMAG1}, as shown in Figure 3. The voltage divider can be calculated by the following equations :

$$\begin{cases} \dfrac{\dfrac{V_{BULK\_BNI} \times N_A}{N_P} + 0.1}{R_{DMAG2}} + \dfrac{0.1}{R_{DMAG1}} = I_{DMAG\_BNI} \\ \dfrac{R_{DMAG2}}{\dfrac{(V_{O\_OVP} + V_F)}{V_{TH\_OVP}} \times \dfrac{N_A}{N_S} - 1} = R_{DMAG1} \end{cases}$$

where V_{O_OVP} is the output OVP threshold voltage.

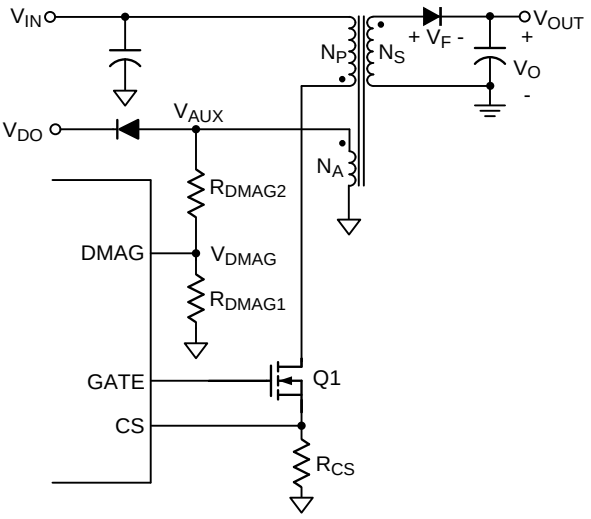


Figure 3. DMAG Pin Resistor

When the secondary-side current reduce to zero during the MOSFET turn-off period, the magnetic inductance (L_P) of the transformer and the equivalent parasitic capacitance (C_{DS}) of the MOSFET induces resonant oscillations on the DMAG pin, as shown in Figure 4.

The RT7755GEK with valley switching version provides valley switching function to save switching loss and improve power supply unit (PSU) efficiency. The valley switching function only works when the resonance period (t_{DCM}) is longer than 1μs and the DMAG voltage is higher than 0.3V. Otherwise DMAG pin can't detect valley signal, and the system will become hard-switching. During circuit design stage, tolerances of magnetic inductance (L_P) and the equivalent parasitic capacitance (C_{DS}) must be considered.

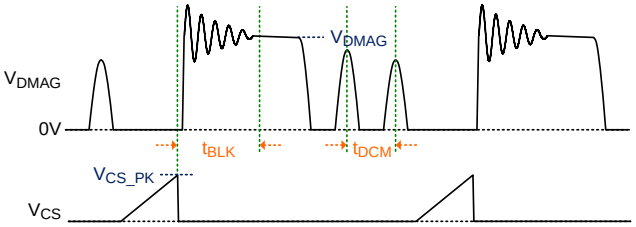


Figure 4. Resonant Oscillations on the DMAG Pin

Adaptive Blanking Time

When the MOSFET just turns off, leakage inductance of transformer and parasitic capacitance (C_{OSS}) of MOSFET induce resonant oscillations on the DMAG pin, as shown in Figure 4. The resonant oscillations may cause the controller to falsely trigger DMAG over-voltage protection ($V_{DMAG} > V_{TH\_OVP}$), which thus fails to reflect actual output over-voltage fault condition ($V_O > V_{O\_OVP}$) so that the controller may not function properly. As load increases, the duration of the resonant oscillation may also increase. A small bypass capacitor, sized from 10pF to 22pF and placed as close to the DMAG pin as possible, is recommended to be added to suppress such noises on the DMAG pin. A larger bypass capacitor may cause the DMAG voltage too much phase-shifted and make the MOSFET unable to switch on at exact valley points.

Correspondingly, the RT7755GEK provides an adaptive blanking time to prevent DMAG over-voltage protection from being falsely triggered. The built-in blanking time for over-voltage protection (t_{BLK}) varies with the system peak current limit (as V_{CS_PK}), and can be calculated by the following equation :

$$t_{BLK} = 1\mu s + 1.829\ (\mu s/V) \times V_{CS\_PK}\ (Typ.)$$

Line Compensation

The RT7755GEK provides line compensation to ensure constant output current limit I_{O_MAX} over a wide range of AC line input voltages, as shown in Figure 5.

For different power stage designs, the propagation delay may vary with the transformer inductances, parasitic capacitances of the MOSFET, or series resistances at the gate of the MOSFET. With the same design, however, the current overshoot caused by the propagation delay may become significant at high line, where the inductor current di/dt is higher. There is a significant difference between the overshoot at high input voltage and that at low input voltage, to the actual peak current.

To compensate such difference to achieve accurate over-current protection under different input line voltages, the RT7755GEK outputs a line compensation current on the CS pin to add an offset voltage proportional to the input voltage by adding a propagation delay resistor (R_{PDC}). The propagation delay differences due to different input line voltages can be compensated by adjusting the propagation delay resistor (R_{PDC}) or the propagation delay capacitor (C_{RC}) to keep output current limit as a constant across different line voltages.

To start with, R_{PDC} = 470Ω and C_{RC} = 100pF can be used as reasonable initial setting for line compensation. In Figure 6, curve (1) is an ideal output current limit curve for over-current protection, which remains constant from low line to high line input voltages. If the output current limit curve is like curve (2), the resistance R_{PDC} should be increased. However, if the output current limit curve is like curve (3), the capacitance C_{RC} should be increased. The output current limit I_{O_MAX} under different line voltages can be optimized by adjusting the propagation delay resistor (R_{PDC}) or the propagation delay capacitor (C_{RC}) to achieve accurate over-current protection.

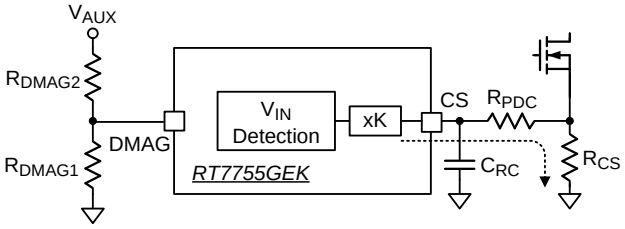


Figure 5. Functional Block Diagram of Line Compensation

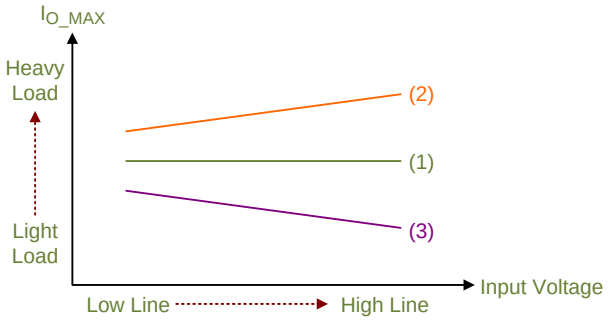


Figure 6. Output Current Limits for Over-Current Protection

External Over-Temperature Protection (Ext-OTP)

The RT7755GEK includes programmable external over-temperature protection (External OTP), implemented with a fast diode and a resistive voltage divider, which consists of an external NTC resistor (R_{NTC}) to sense the power system temperature, as shown in Figure 7. During the MOSFET off-time, the auxiliary winding voltage V_{AUX} is constant, and the CS voltage sampled as a fraction of the clamped voltage V_{AUX_Clamp} and compared with the internal reference voltage to set the over-temperature protection threshold voltage. When the system temperature gets higher, the resistance of the NTC resistor becomes smaller. By adjusting the value of the setting resistor (R_{SET}), the threshold temperature for over-temperature protection can be programmed. During the off-time, if the sampled CS voltage exceeds the external OTP threshold voltage V_{TH_OTP} and sustains for the external OTP delay time t_{D_OTP}, the controller will be shut down and the switching is stopped. If the OTP condition is removed, the controller with auto-recovery option will automatically resume operation.

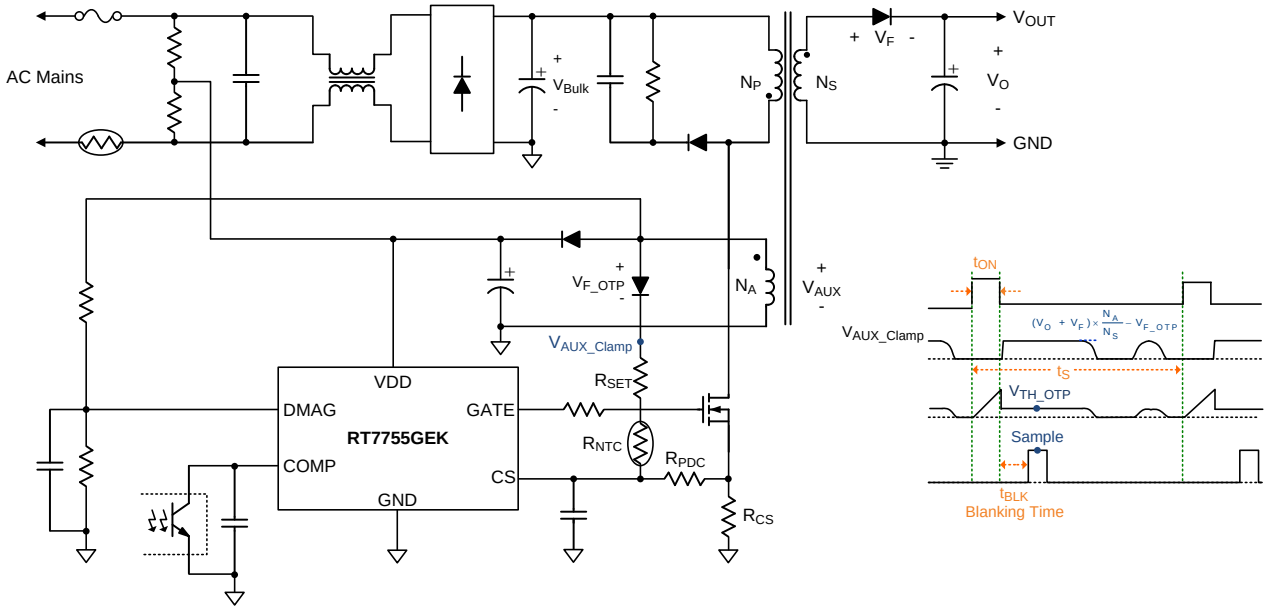


Figure 7. Application Circuit of External Over-Temperature Protection

The design equation for the external OTP threshold voltage is expressed as below :

$$V_{TH\_OTP} = \left[(V_{O\_NOR\_MAX} + V_F) \times \frac{N_A}{N_S} - V_{F\_OTP} \right] \times \frac{R_{PDC} + R_{CS}}{R_{NTC\_OTP} + R_{SET} + R_{PDC} + R_{CS}}$$

where $V_{O\_NOR\_MAX}$ is the maximum normal output voltage; and R_{NTC_OTP} is the NTC resistance at the threshold temperature for external OTP.

It is highly recommended to use a fast diode ($C_T \leq 5pF$ and $t_{rr} \leq 50ns$), ex.1N4148 or BAV21 series, for external OTP application to prevent the CS pin from wrong regulation or being damaged by the negative voltage spikes.

Resistors at the GATE Pin

As the typical application circuit shown in Figure 8, a resistor R_G can be applied to mitigate ringing spikes induced by the gate drive loop. Therefore, the value of the resistor R_G should be chosen carefully to meet the requirements for both EMI and efficiency for applications.

The RT7755GEK has a built-in discharge resistor R_{ID}, internally connected from the GATE pin to GND, to prevent the MOSFET suffering from any uncertain condition. However, if the GATE pin is open-circuited, not connecting to the gate of the MOSFET, the MOSFET may be falsely triggered by the stored charge on the gate-to-drain parasitic capacitor C_{GD} of the MOSFET and then be damaged. Therefore, it is

recommended to add an external discharge resistor R_{ED} between the gate of MOSFET and GND so that the charge stored on the parasitic capacitor C_{GD} can be discharged by the external discharge resistor and the MOSFET can be protected from being falsely triggered even if the RT7755GEK is not in place or GATE pin is open-circuited.

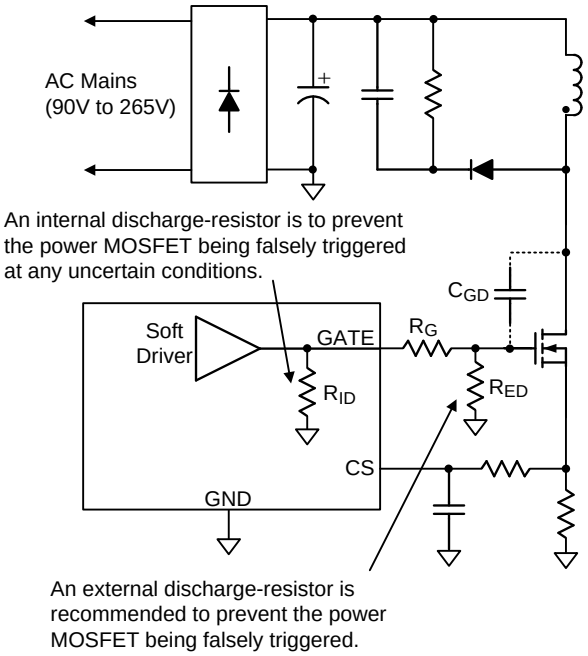


Figure 8. Resistors at the GATE Pin

Feedback Resistor

To enhance efficiency at light load, the power loss caused by the feedback resistor, in parallel with the opto-coupler as shown in Figure 9, must be reduced. Since the current through the feedback resistor is very small, a shunt regulator (e.g. TL431), especially with its minimum regulated current, should be carefully chosen to ensure that the shunt regulator can still regulate the output voltage at such a small cathode current.

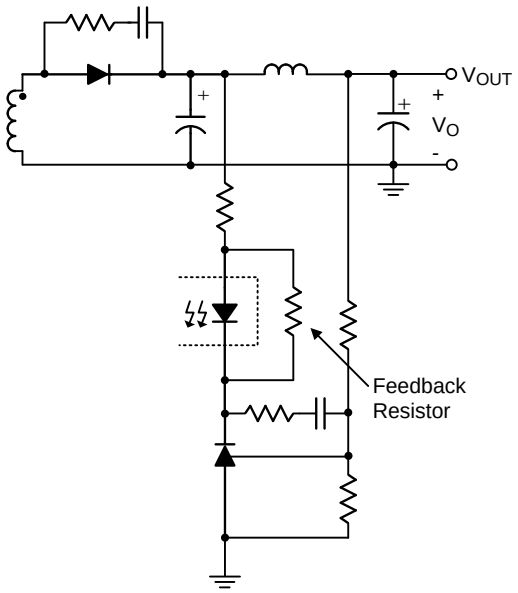


Figure 9. Feedback Resistor

Negative Voltage Spike on Each Pin

Any negative voltage which is less than −0.3V on each controller pin may cause a large injection current into the substrate to damage the controller or to falsely trigger the circuit. For example, the negative voltage spikes at the CS pin may result from poor PCB layout or the inductance of the current sense resistor, and therefore an R-C filter, as shown in Figure 10, is recommended to be added to prevent the CS pin from being damaged by the negative voltage spikes. During circuit design stage, proper PCB layout and component selection must be carefully considered.

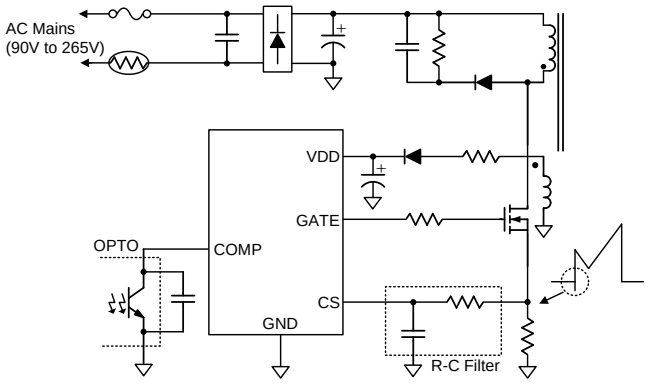


Figure 10. R-C Filter on the CS Pin

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-23-6 package, the thermal resistance, θ_{JA}, is 260.7°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (260.7°C/W) = 0.38W for a SOT-23-6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

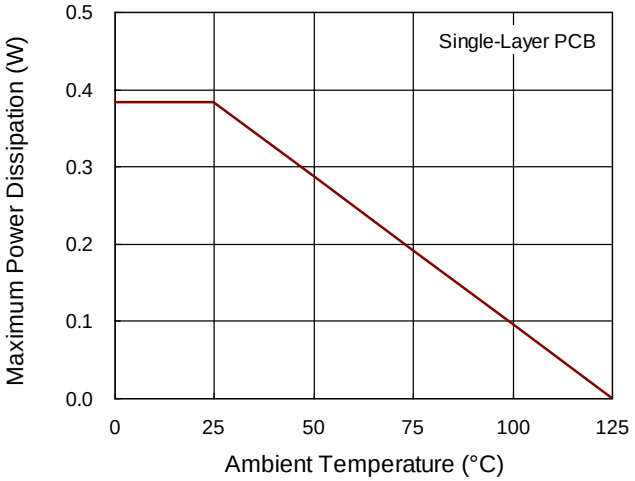


Figure 11. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can alleviate unknown noise interference and EMI emission in a switch-mode power supply (SMPS). It is recommended to follow the following PCB layout guidelines when a switch-mode power supply is to be designed :

- The current path (1), starting from the bulk capacitor, through the transformer, the MOSFET, the resistor R_{CS} and back to the bulk capacitor, is a high-frequency and high-current loop. Another high-frequency and high current loop is the current path (2) which is from the GATE pin, through the MOSFET, the resistor R_{CS} and back to the IC ground. These two paths should be kept as small as possible to decrease noise coupling and kept away from other low-voltage traces, such as IC control circuit paths, especially.
- The path (3), starting from the auxiliary winding, through the resistor, the diode, and the VDD capacitor to the VDD pin, is also recommended to be as short as possible.

  Besides, the VDD capacitor should be placed as close to the VDD pin as possible.
- The path (4) from the RCD snubber circuit to the MOSFET should also be kept short as it is also a loop with high switching frequency.

- The ground traces of the bulk capacitor (a), the MOSFET (b), the VDD capacitor (c), the auxiliary winding (d) and the IC control circuit (e) should be separated to reduce noise, output ripple and EMI emission. The ground traces of the auxiliary winding (d) and the IC control circuit (e) are connected together at the VDD capacitor ground (c). Then the connected ground trace goes through the VDD capacitor ground (c), the MOSFET ground (b), and to the bulk capacitor ground (a) in turn. The area of the bulk capacitor ground trace should be large enough.
- The bypass capacitor should be placed as close to the controller as possible.
- In order to reduce the reflected trace inductance and EMI emissions, the trace connecting the secondary winding, the output diode, and the output filter capacitor should be as short as possible. In addition, the copper areas at the anode and cathode of the diode must be large enough to ease sinking heat from the diode.

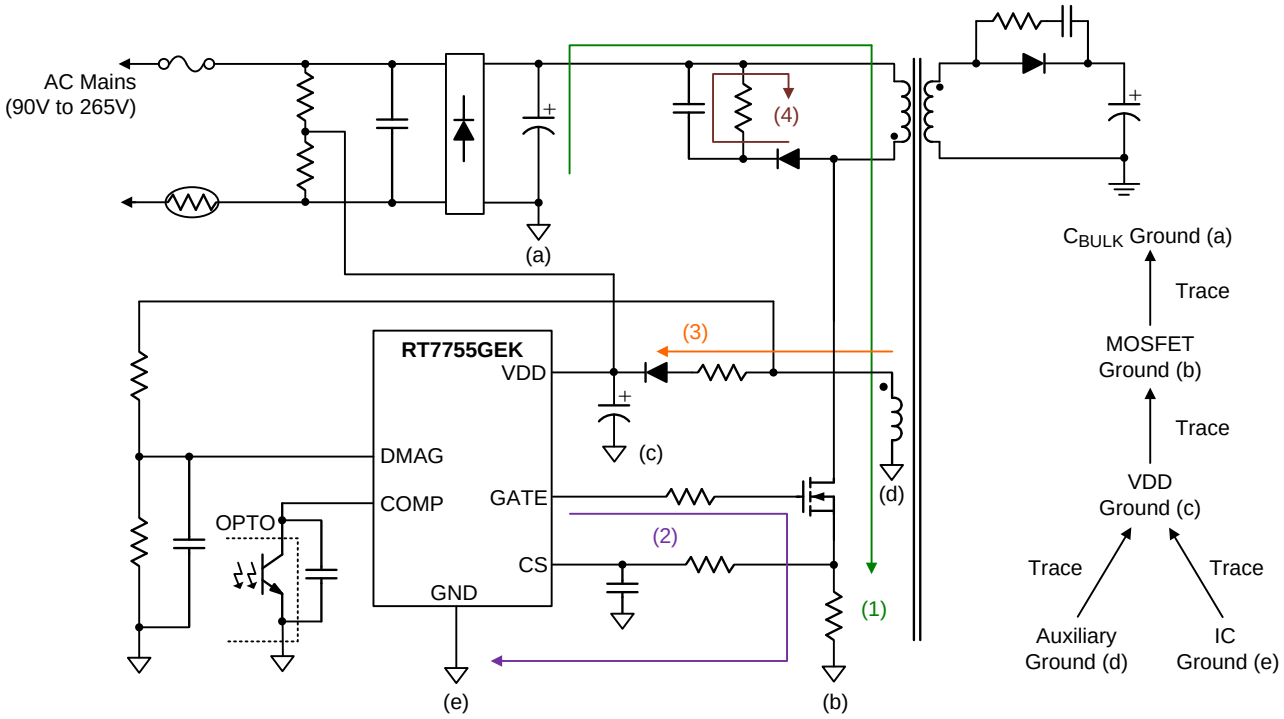
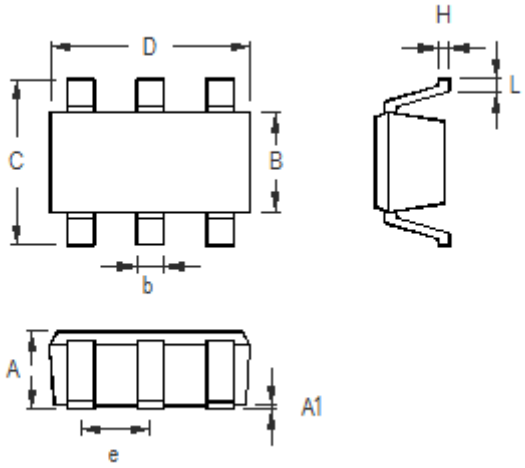


Figure 12. PCB Layout Guide

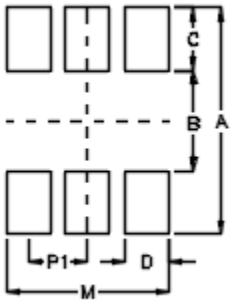
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-26/TSOT-26(FC)/SOT-26	6	0.95	3.60	1.60	1.00	0.70	2.60	±0.10

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