MCU-Integrated USB Type-C Port Controller

General Description

The RT7802 is a USB Power Delivery (USB PD) controller with highly integrated functions for desktop PC, monitor, or any other devices with USB Type-C (USB-C) receptacle. It is designed to embed ARM Cortex™-M0 MCU so as to facilitate various functions of communication protocol, protections and customized requirements.

The RT7802 provide a general USB Type−C port to pass USB2.0 data signal and SBU signal.

Ordering Information

RT7802 □□-□

- □ : Programmed Firmware Code AABBX
  - AA : Customer Code
  - BB : Customer Model Code
  - X : Official Released Firmware Code
- □ : Package Type
  - QW : WQFN-32L 4x4 (W-Type)
- □ : Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

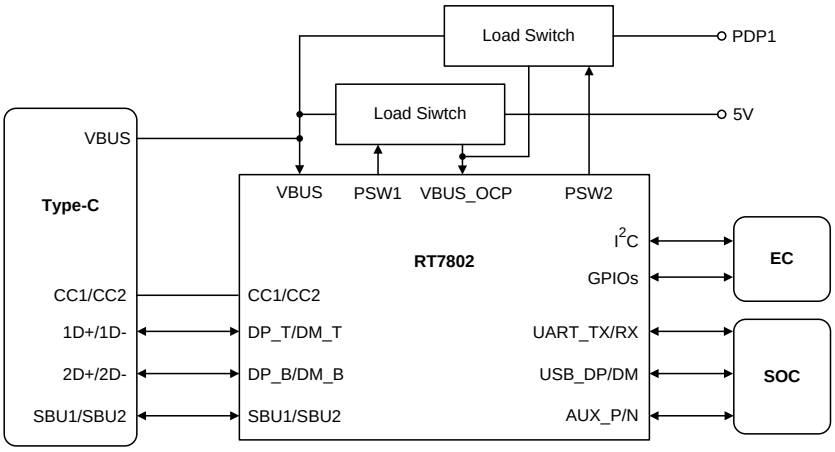
Features

- **Integration MCU**
- **Mode Configuration**
- **CC Logic**
  - **Attach/Detach of USB Port Detection**
  - **Debug Accessory Mode Detection**
- **PD Function**
- **VCONN Support**
- **VBUS/VCONN Monitor**
- **USB 2.0/UART MUX**
- **AUX MUX**
- **VBUS Controller**
  - **Two Power Path Enable Control**
  - **5V and High Voltage On/Off Timing Control**
- **I²C (Slave)**
- **GPIO**
  - **5 port GPIO (I²C Control)**
- **High Voltage Tolerant**
  - **CC Pin and SBU Pin 20V Tolerant**

Applications

- Desktop PC, LCD Monitor, TV, Docking Station

Simplified Application Circuit

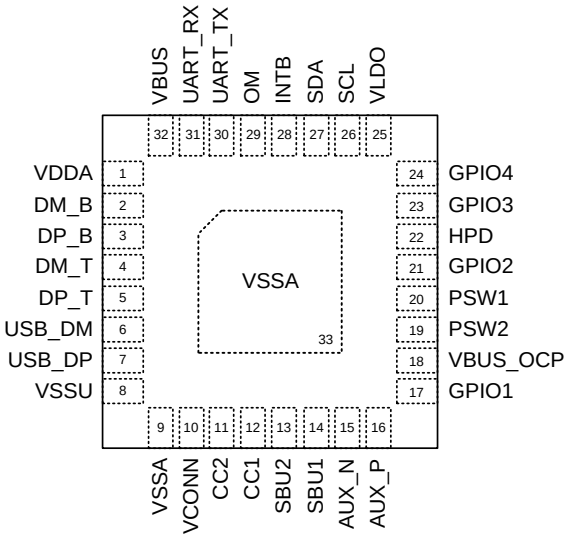


Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

(TOP VIEW)



WQFN-32L 4x4

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDDA	IC bias voltage (3.3V typ.) input pin. Connecting this pin to a 3.3V system voltage via a C filter (1μF) is recommended.
2	DM_B	Input/Output pin of USB/UART MUX. Connect this pin to DM Bottom pin of a USB connector.
3	DP_B	Input/Output pin of USB/UART MUX. Connect this pin to DP Bottom pin of a USB connector.
4	DM_T	Input/Output pin of USB/UART MUX. Connect this pin to DM Top pin of a USB connector.
5	DP_T	Input/Output pin of USB/UART MUX. Connect this pin to DP Top pin of a USB connector.
6	USB_DM	USB 2.0 DM signal from Host.
7	USB_DP	USB 2.0 DP signal from Host.
8	VSSU	GND for USB/UART switch.
9	VSSA	GND pad.
10	VCONN	5V power supply input for VCONN powered accessory with OCP.
11	CC2	Input/Output pin of the second configuration channel. Generally, connect this pin to USB-C CC2 terminal.
12	CC1	Input/Output pin of the first configuration channel. Generally, connect this pin to USB-C CC1 terminal.
13	SBU2	AUX switch between AUX_P/N and SBU1/2. 2000k pull-down is connected.
14	SBU1	AUX switch between AUX_P/N and SBU1/2. 2000k pull-down is connected.

Pin No.	Pin Name	Pin Function
15	AUX_N	AUX N channel from Host. (available for pull-up/down 100kΩ)
16	AUX_P	AUX P channel from Host. (available for pull-up/down 100kΩ)
17	GPIO1	Open-drain with 20V GPIO high voltage NMOS or analog input pin.
18	VBUS_OCP	Input pin for external OCP signal from VBUS power switch. (L : Active, with external pull-up)
19	PSW2	Push-pull GPIO for VBUS load switch2 or analog input pin, 200k pull-down is connected.
20	PSW1	Push-pull GPIO for VBUS load switch1 or analog input pin, 200k pull-down is connected.
21	GPIO2	Input pin for slave address mode selection. (H, L, Hi-Z by external pull-up/down and open)
22	HPD	Hot plug detection for display port with open drain, and initial state is low. (H : Active, with external pull-up)
23	GPIO3	Open-drain/push-pull GPIO or analog input pin.
24	GPIO4	Open-drain/push-pull GPIO or analog input pin.
25	VLDO	Output pin of the internal 1.8V linear regulator which supplies power for digital circuits. Connecting this pin with a 1μF MLCC is recommended.
26	SCL	Open-drain clock signal input/output pin of the slave I^2C interface. This pin can be set as an open-drain or push-pull GPIO pin.
27	SDA	Open-drain data signal input/output pin of the slave I^2C interface. This pin can be set as an open-drain or push-pull GPIO pin.
28	INTB	Interrupt flag output. (L : Active, with external pull-up)
29	OM	OM reset function. (default : keep low state)
30	UART_TX	UART TX from Host.
31	UART_RX	UART RX from Host.
32	VBUS	USB-C VBUS voltage input pin. The voltage at this pin is monitored for programmable USB-C VBUS OVP/UVP.
33	VSSA (Exposed Pad)	Ground pad. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Note :

P : Power Supply

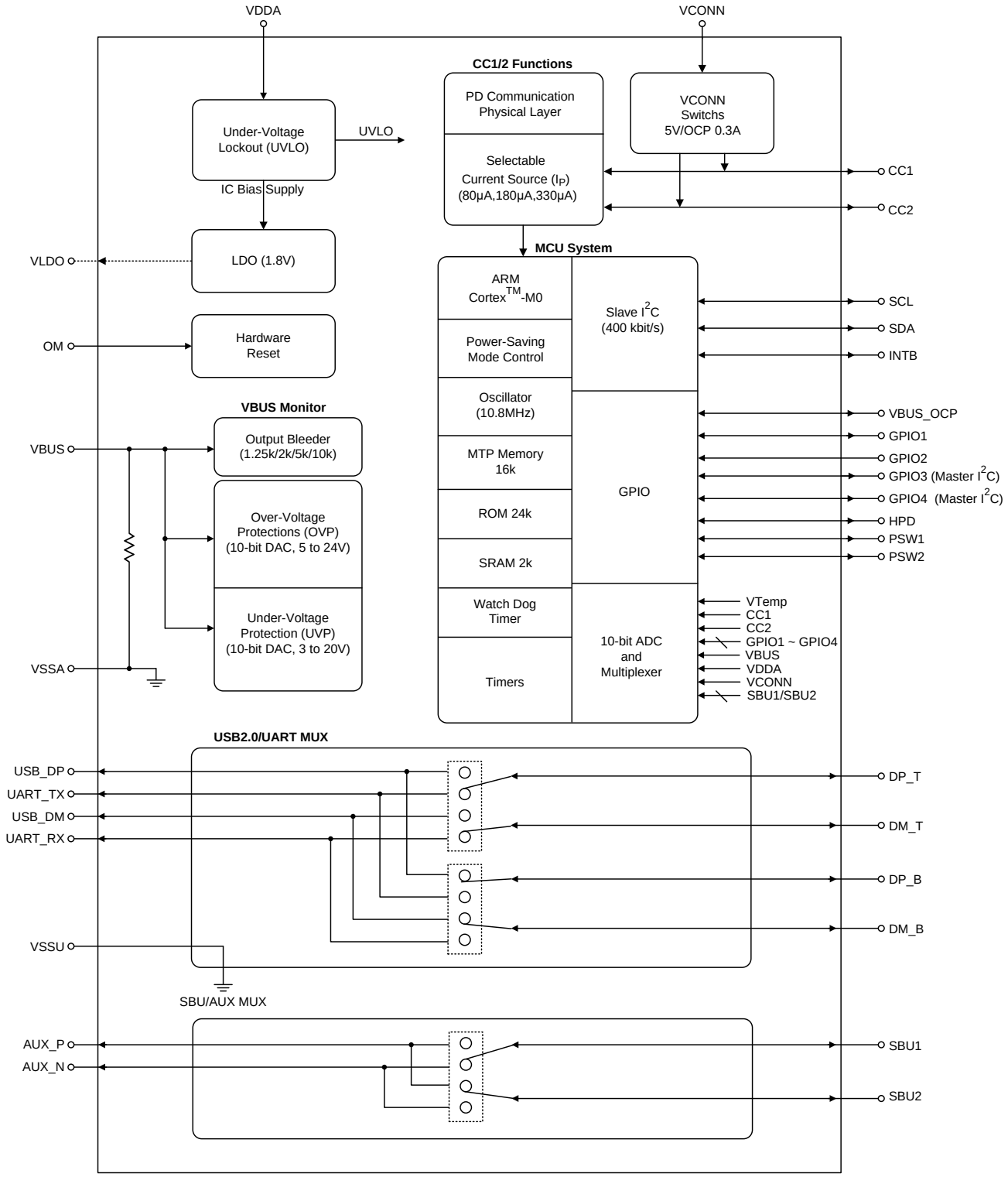
G : Ground

I : Input

O : Output

B : Input and Output

Functional Block Diagram



Operation

The RT7802 is a versatile USB PD controller which can be used in a Provider. It is a highly integrated solution, consisting of four main function blocks: MCU System, MUX, power protections and CC1/2 Functions as shown in the “Functional Block Diagram”.

The MCU System embeds ARM Cortex^{TM}-M0 MCU, multi-time programmable (MTP) memory, ROM, SRAM, a 10-bit ADC (analog to digital converter), two I^2C interfaces (slave and master) and GPIO (General Purpose Input or Output) pins. It can report operating statuses of PD operation to EC and receive commends from EC via the slave I^2C interface.

The “power protections” block consists of VBUS over-voltage protection (VBUS_OVP) and VBUS under-voltage protection (VBUS_UVP). The trip levels and de-bounce time of VBUS OVP/UVP are programmable.

The “CC1/2 Functions” block consists of physical layer, three selectable pull-up current sources (Ip, instead of resistors Rp), and VCONN power-path switches.

VDD Bias Voltage Generation

The LDO (1.8V) supply the voltage for the RT7802 internal circuits, a 1μF MLCC capacitor should be placed between the VLDO pin and GND pin.

Under-Voltage-Lockout (UVLO)

The RT7802 UVLO function continually monitors the bias voltages at the VDDA pin. When the supply voltages VDDA exceed the rising UVLO thresholds, the IC is enabled to work. Otherwise, it will be “Under-Voltage-Lockout” status to prevent any undesirable operations. A 1μF MLCC capacitor should be placed between the VDDA pin and GND pin.

VBUS Over-Voltage Protection (VBUS OVP) and Under-Voltage Protection (VBUS UVP)

The VBUS OVP and UVP function are hardware-based protection which monitors the voltage at the VBUS pin.

When the VBUS voltage exceeds its OVP threshold, the output of the OVP comparator goes high and starts the de-bounce time counting. At the end of the de-bounce time counting, the VBUS OVP will be triggered. The OVP trip voltage is programmable from 5V to 24V (10-bit, 25mV/step typ.) and its de-bounce time is also selectable to meet various application requirements.

When the VBUS voltage under its UVP threshold, the output of the UVP comparator goes high and starts the de-bounce time counting. At the end of the de-bounce time counting, the VBUS UVP will be triggered. The UVP trip voltage is programmable from 3V to 20V (10-bit, 25mV/step typ.) and its de-bounce time is also selectable to meet various application requirements.

Power Output for USB Plug Power (V_{CONN})

The output voltage at one of CC1 and CC2 pins can provide power for an active cable. One of internal MOSFETs between VCONN to CC1 and CC2 pins can be turned on to supply power to CC1 or CC2 pin. The input pin VCONN must be connected to 5V power source.

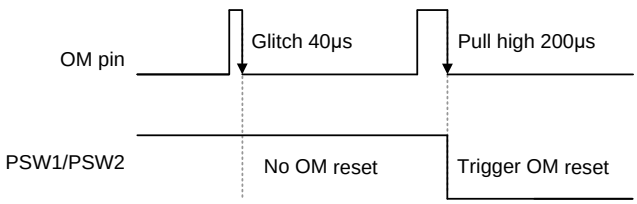
VCONN Over-Current Protection (VCONN OCP)

Because a robust system is very important in USB PD operations, the RT7802 embed VCONN OCP function.

When the current on CC1 or CC2 is higher than 330mA (typ.), VCONN OCP will be triggered. The internal MOSFETs between VCONN to CC1 and CC2 pins will be turned off.

OM Reset

Pull up OM pin 3.3V for 200μs then pull low, OM reset function will be triggered in falling edge. PSW1 and PSW2 turn off, VBUS no output.



Absolute Maximum Ratings (Note 1)

- VLDO to VSSA ---------- –0.3V to 2.5V
- VDDA to VSSA ---------- –0.3V to 6.5V
- VCONN to VSSA ---------- –0.3V to 6.5V
- CC1, CC2 to VSSA ---------- –0.3V to 24V
- SBU1, SBU2 to VSSA ---------- –0.3V to 24V
- VBUS to VSSA ---------- –0.3V to 24V
- GPIO1 to VSSA ---------- –0.3V to 24V
- USB_DP, USB_DM, UART_TX, UART_RX to VSSA ---------- –0.3V to 6.5V
- DP_T, DM_T, DP_B, DM_B to VSSA ---------- –0.3V to 6.5V
- AUX_P, AUX_N to VSSA ---------- –0.3V to 6.5V
- VBUS_OCP, PSW1, PSW2 to VSSA ---------- –0.3V to 6.5V
- GPIO2, GPIO3, GPIO4, HPD to VSSA ---------- –0.3V to 6.5V
- INTB, OM, SCL, SDA to VSSA ---------- –0.3V to 6.5V
- VSSU to VSSA ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-32L 4x4 ---------- 2.87W
- Package Thermal Resistance (Note 2)
  WQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W
  WQFN-32L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VBUS Range in PD Provider Operation, V_{BUS} ---------- 3V to 22V
- VDDA Supply Voltage, V_{VDDA} ---------- 3V to 3.6V
- CC1, CC2 Voltage Range ---------- 0V to VDDA
- SBU1, SBU2 Voltage Range ---------- 0V to VDDA
- Junction Temperature Range ---------- –40°C to 105°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{VDDA} = 3.3V and V_{BUS} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VDDA UVLO and VLDO Linear Regulators							
VDDA Voltage Range	V_{VDDA}			3	3.3	3.6	V
VDDA UVLO Threshold	$V_{VDDA\_UVLO\_H}$	V_{VDDA} rising		--	2.8	--	V
VDDA UVLO Hysteresis	$V_{VDDA\_UVLO\_HYS}$			--	200	--	mV
VLDO Output Voltage	V_{VLDO_REG}			1.62	1.8	1.98	V
VLDO UVLO Voltage Threshold	$V_{VLDO\_UVLO\_H}$	V_{VLDO} rising		--	1.4	--	V
VLDO UVLO Voltage Hysteresis	$V_{VLDO\_UVLO\_HYS}$			--	150	--	mV
VLDO Short-Circuit Current	V_{VLDO_SHORT}			--	60	--	mA
VDDA Input Current in Normal Mode	I_{CC_VDDA1}	MCU = on		--	--	10	mA
VDDA Input Current in Sleep Mode	I_{CC_VDDA2}			--	--	500	μA
VCONN and VCONN Switches							
VCONN Voltage Drop at CC1/CC2	V_{VCONN_DROP}	VCONN = 5V, Output current = 300mA		4.52	4.7	--	V
VCONN to CC1/CC2 Switch RON	R_{VCONN}	VCONN = 5V, Output current = 300mA		--	1	1.6	Ω
VCONN Discharge Resistance	R_{VCONN_BLD}	VCONN = 5V		--	10	--	kΩ
VCONN Current-Limit Threshold	I_{VCONN_OCP}			310	330	350	mA
CC1/2 Voltage Detections, BMC Transmitter/Receiver							
CC1/2 Pull-Up Current Source – 1	Ip1			–20%	80	20%	μA
CC1/2 Pull-Up Current Source – 2	Ip2			–8%	180	8%	μA
CC1/2 Pull-Up Current Source – 3	Ip3			–8%	330	8%	μA
CC1/2 Maximum Output Voltage	--	CC1/2 = open		V_{VDDA} - 1V	--	V_{VDDA}	V
Transmitter High-Level Output Voltage Range	V_{TX_OH}			1.05	--	1.2	V
Transmitter Low-Level Output Voltage Range	V_{TX_OL}			0	--	75	mV
Receiver High-Level Input Voltage Range	V_{RX_IH}	Programmable	00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Receiver Low-Level Input Voltage Range	V_{RX_IL}	Programmable	00	0.4	0.5	0.6	V
			01	0.3	0.4	0.5	
			10	0.2	0.3	0.4	
			11	0.1	0.2	0.3	
Rising Time of the Transmitter Output Voltage	--	From 10% to 90%, C_L = 200 pF to 600pF		300	--	--	ns
Falling Time of the Transmitter Output Voltage	--	From 90% to 10%, C_L = 200 pF to 600pF		300	--	--	ns
10-bit Analog-to-Digital Converter (ADC) for Voltage Detections							
10-bit ADC Input Voltage Range	--	V_{ref_ADC} = 2.048V, LSB = 2mV		0.1	--	2	V
VBUS Voltage Detection Range	--	25mV/step, R_{ratio_VBUS} = 0.08V/V		3	--	22	V
		16mV/step, R_{ratio_VBUS} = 0.125V/V		3	--	16	
CC1/CC2 Voltage Detection Range	--	6mV/step, R_{ratio_CC} = 0.33V/V		0.1	--	5	V
		2mV/step, R_{ratio_CC} = 1V/V		0.1	--	2	
VDD Voltage Detection Range	--	6mV/step, R_{ratio_VDD} = 0.333V/V		3	--	5	V
VCONN Voltage Detection Range	--	8mV/step, R_{ratio_CONN} = 0.25V/V		3	--	5.5	V
SBU1/SBU2 Voltage Detection Range	--	6mV/step, R_{ratio_SBU} = 0.333V/V		0.1	--	5	V
		2mV/step, R_{ratio_SBU} = 1V/V		0.1	--	2	
GPIO1 Voltage Detection Range	--	20mV/step, R_{ratio_GPIO1} = 0.1V/V		1	--	20	V
GPIO2~4 Voltage Detection Range	--	6mV/step, R_{ratio_GPIO} = 0.333V/V		0.1	--	V_{VDDA}	V
		2mV/step, R_{ratio_GPIO} = 1V/V		0.1	--	2	
VBUS Protections – Over-Voltage, Under-Voltage, Voltage -Detection, Bleeder							
VBUS OVP Voltage Threshold Range	V_{TH_OV}	Programmable (10-bit), at VBUS pin R_{ratio_VBUS} = 0.08V/V, 25mV/step		5	--	24	V
		Programmable (10-bit), at VBUS pin R_{ratio_VBUS} = 0.125V/V,16mV/step		5	--	16	
VBUS UVP Voltage Threshold Range	V_{TH_UV}	Programmable (10-bit), at VBUS pin R_{ratio_VBUS} = 0.08V/V, 25mV/step		3	--	20	V
		Programmable (10-bit), at VBUS pin R_{ratio_VBUS} = 0.125V/V, 16mV/step		3	--	16	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VBUS BLD Resistance	R_{BLD_VBUS}	Programmable	0001	--	1.25	--	kΩ
			0010	--	2	--	
			0100	--	5	--	
			1000	--	10	--	
CLK Section							
MCU Clock Frequency	f_{MCU}			–10%	10.8	10%	MHz

Digital Input and Output – I²C Pins (SCL, SDA, INTB) and GPIO Pins

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GPIOA-HV Open Drain (GPIO1)						
GPIOA Voltage Range	--		0	--	20	V
GPIOA High-Level Input Voltage Range	V_{GPIOA_IH}	For the pins configured as input pins	3.75	--	20	V
GPIOA Low-Level Input Voltage Range	V_{GPIOA_IL}	For the pins configured as input pins	0	--	0.75	V
GPIOA Low-Level Output Voltage	V_{GPIOA_OL}	Sinking current = 2mA (Open-drain)	0	--	0.3	V
GPIOA Weak Pull-low Resistance	--		--	30	--	kΩ
GPIOB-LV Open Drain (HPD/SCL/SDA)						
GPIOB Voltage Range	--		0	--	V_{VDDA}	V
GPIOB High-Level Input Voltage Range	V_{GPIOB_IH}	For the pins configured as input pins	1.5	--	V_{VDDA}	V
GPIOB Low-Level Input Voltage Range	V_{GPIOB_IL}	For the pins configured as input pins	0	--	0.4	V
GPIOB Low-Level Output Voltage	V_{GPIOB_OL}	Sinking current = 2mA (Open-drain)	0	--	0.3	V
GPIOB Weak Pull-Low Resistance	--		--	30	--	kΩ
OM Reset						
OM Reset De-bounce Time	t_{OM_DB}	OM fource 3.3V with t_{OM_DB} then immediately goes low, check chip in reset state	40	120	200	μs
OM Reset Enable Threshold Voltage	V_{OM_EN}	When the OM voltage exceeds the threshold voltage, the de-bounce timer starts	1.5	--	V_{VDDA}	V
OM Reset Disable Threshold Voltage	V_{OM_DIS}	OM logic low range	--	--	0.4	V
OM Leakage Current	I_{LEAK_OM}	Pin input voltage = 3.3V	--	--	3	μA
GPIOC-LV PUSH-PULL (GPIO3/GPIO4/VBUS_OCP/PSW1/PSW2/INTB)						
GPIOC Voltage Range	--		0	--	V_{VDDA}	V
GPIOC High-Level Input Voltage Range	V_{GPIOC_IH}	For the pins configured as input pins	1.5	--	V_{VDDA}	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GPIOC Low-Level Input Voltage Range	V_{GPIOC_IL}	For the pins configured as input pins	0	--	0.4	V
GPIOC High-Level Output Voltage	V_{GPIOC_OH}	Sourcing current = 2mA, for the pins configured as push-pull output pins	V_{VDDA} - 0.3	--	V_{VDDA}	V
GPIOC Low-Level Output Voltage	V_{GPIOC_OL}	Sinking current = 2mA	0	--	0.3	V
PSW1/PSW2 Pull-low Resistance	--	Resistor (PSW1/PSW2)	--	200	--	kΩ
GPIOC Weak Pull-low Resistance	--	Resistor	--	30	--	kΩ
GPIOD-LV INPUT only (SBU1/SBU2/AUX_P/AUX_N/UART_TX/UART_RX)						
GPIOD Voltage Range	--		0	--	V_{VDDA}	V
GPIOD High-Level Input Voltage Range	V_{GPIOD_IH}	For the pins configured as input pins	1.5	--	V_{VDDA}	V
GPIOD Low-Level Input Voltage Range	V_{GPIOD_IL}	For the pins configured as input pins	0	--	0.4	V
GPIOD Weak Pull-low Resistance	--	Resistor	--	30	--	kΩ
GPIO2-Slave Address						
GPIO2 Voltage Range	--		0	--	V_{VDDA}	V
GPIO2 High-Level Input Voltage Range	V_{GPIO2_IH}	For the pins configured as input pins	--	0.6 x V_{VDDA}	--	V
GPIO2 Low-Level Input Voltage Range	V_{GPIO2_IL}	For the pins configured as input pins	--	0.4 x V_{VDDA}	--	V
GPIO2 PIN floating Voltage	--	For the pins configured as input pins	--	0.5 x V_{VDDA}	--	V
GPIO2 Pull-High/Pull-Low Resistance	--		--	300	--	kΩ
USB UART MUX						
RON On Resistance of DP/DM to USB_DP/USB_DM	$R_{ON\_USB\_DP/DM}$	DP/DM = 0V, 0.4V, ION = –8mA	--	6	10	Ω
ON Resistance Mismatch within Pair	--	DP/DN = 0V, 0.4V, ION = –8mA	0	--	0.7	Ω
ON Resistance Flatness (RON max – RON min)	--	DP/DN = 0V, 0.4V, ION = –8mA	0	--	0.4	Ω
RON On Resistance of DP/DM to UART	$R_{ON\_UART\_DP/DM}$	DP/DM = 0V, 3.3V, ION = –2mA	--	20	40	Ω
ON Resistance Mismatch within Pair	--	DP/DM = 0V, 3.3V, ION = –2mA	0	--	2	Ω
UART TX/RX Leakage Current	--	Pin input voltage = 3.3V	--	--	3	μA
SBU AUX MUX						
RON On Resistance of SBU to AUX	$R_{ON\_AUX\_SBU}$		--	6	10	Ω
ON Resistance Mismatch within Pair	--		0	--	1.3	Ω
SBU Pull Low Resistance	--		--	2	--	MΩ
AUX Pull High Resistance	--		--	100	--	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AUX Pull Low Resistance	--		--	100	--	kΩ

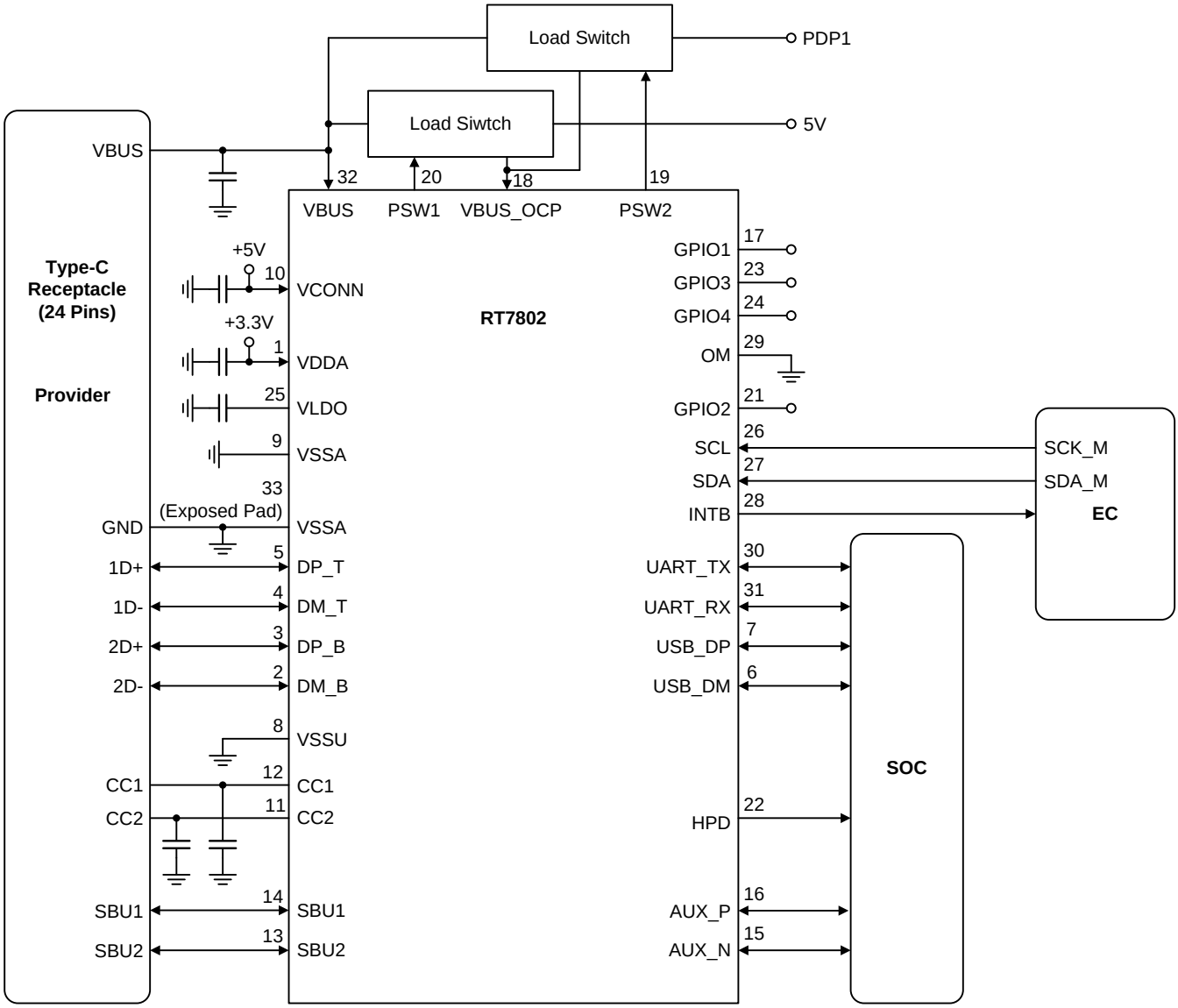
Note1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

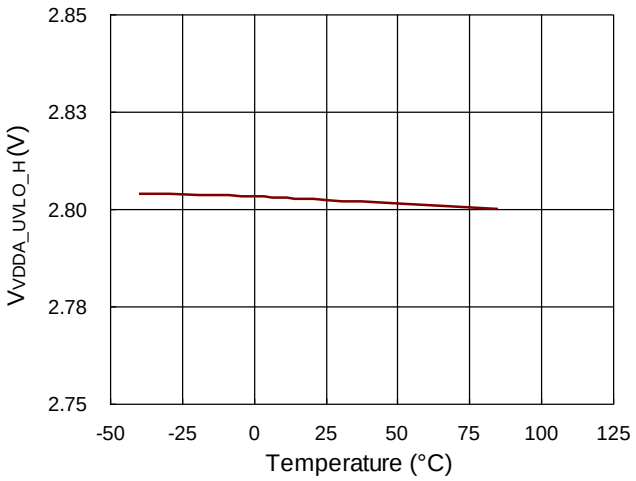
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

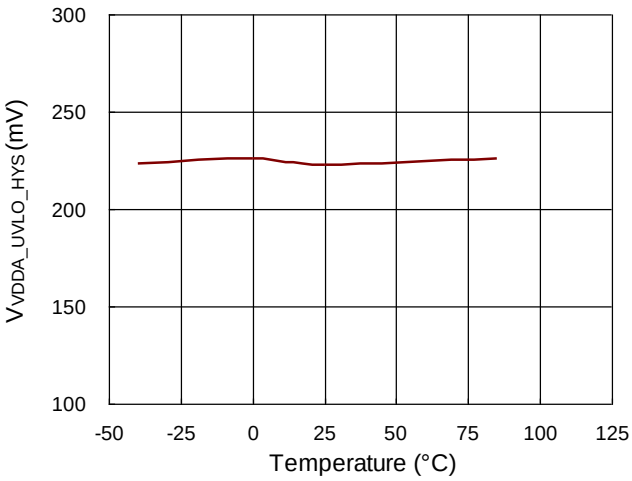


Typical Operating Characteristics

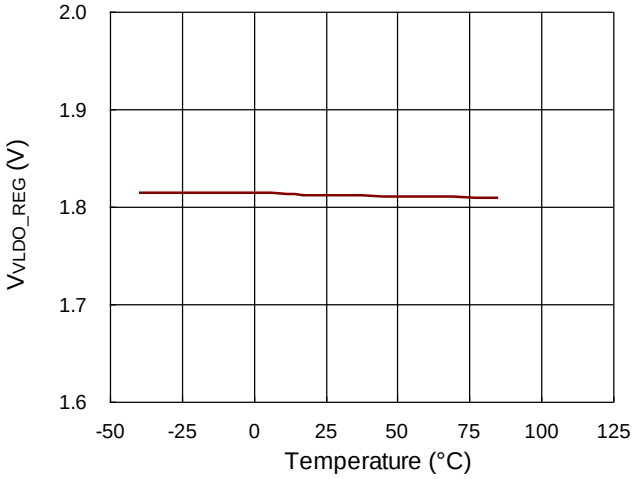
$V_{VDDA\_UVLO\_H}$ vs. Temperature



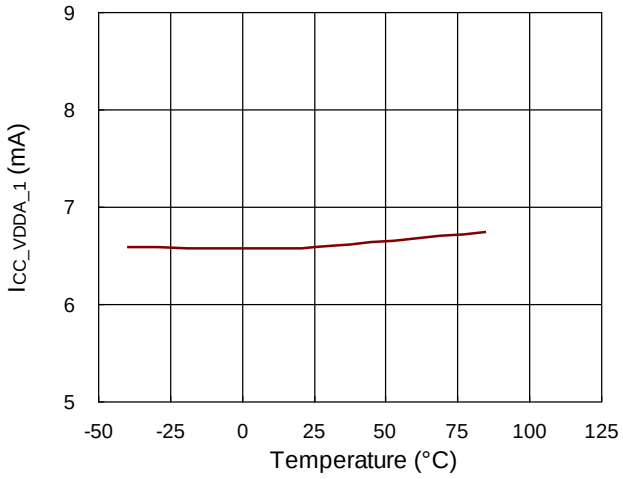
$V_{VDDA\_UVLO\_HYS}$ vs. Temperature



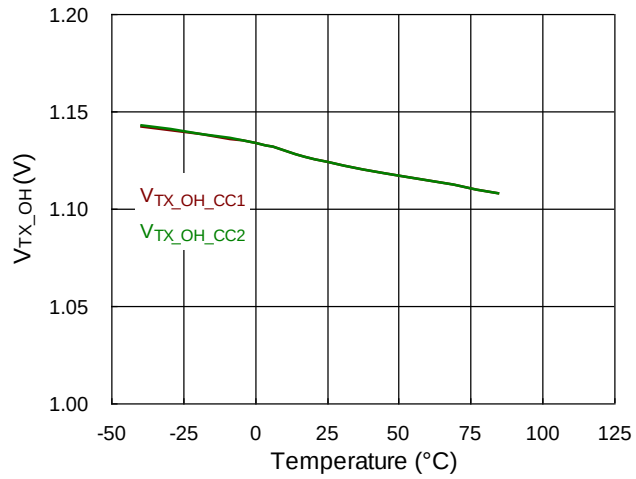
V_{VLDO_REG} vs. Temperature



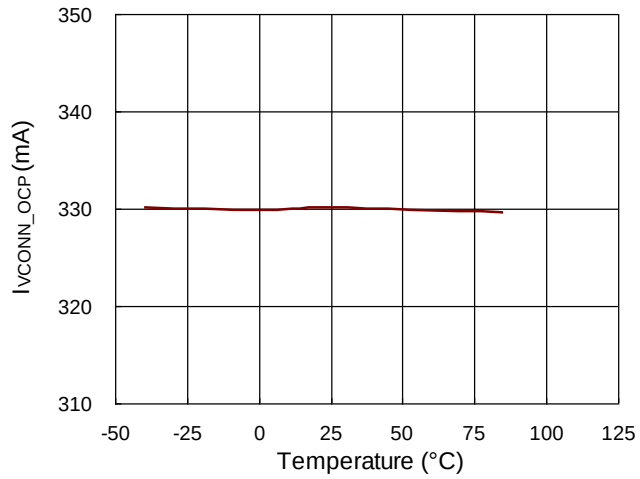
$I_{CC\_VDDA\_1}$ vs. Temperature

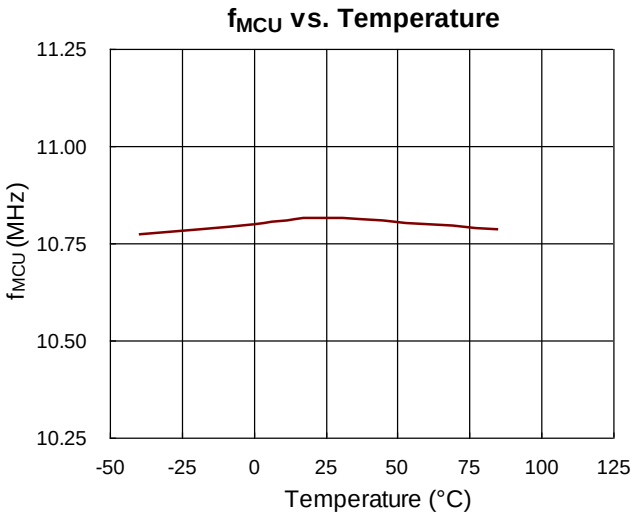


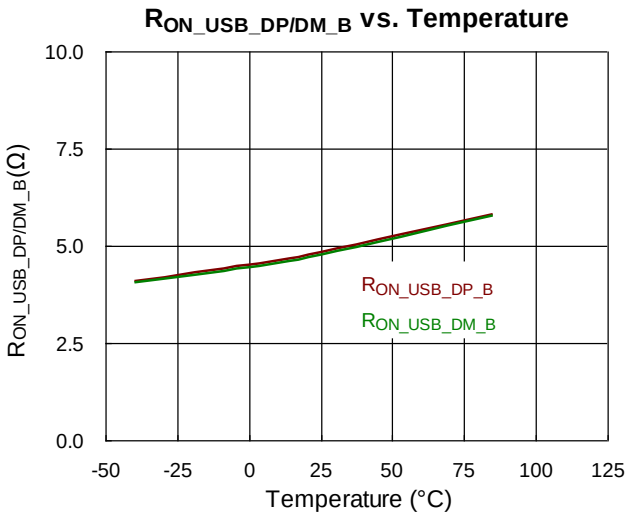
V_{TX_OH} vs. Temperature

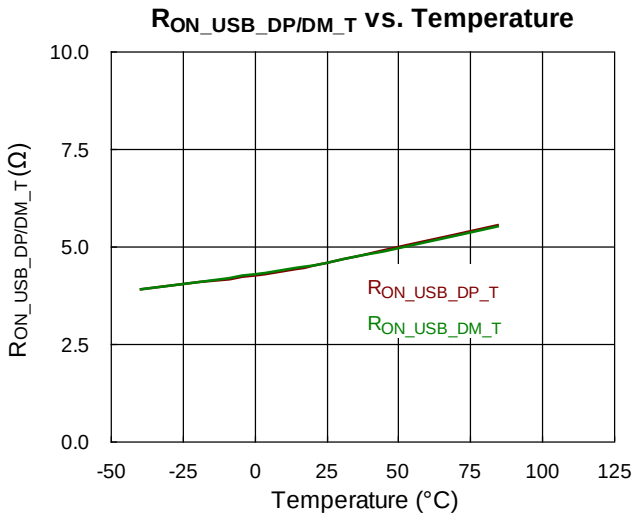


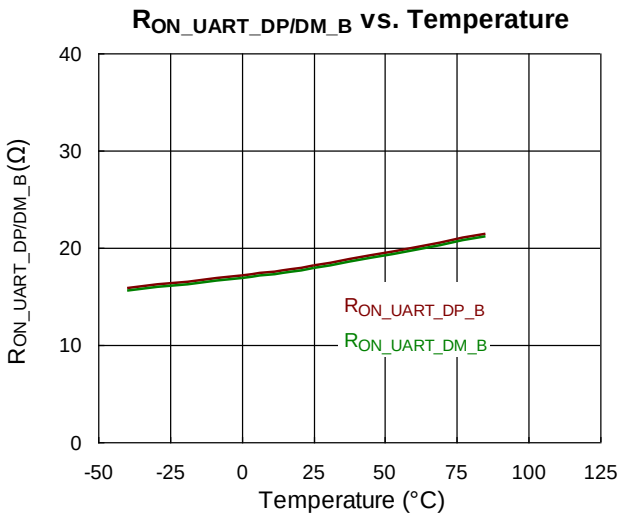
I_{VCONN_OCP} vs. Temperature

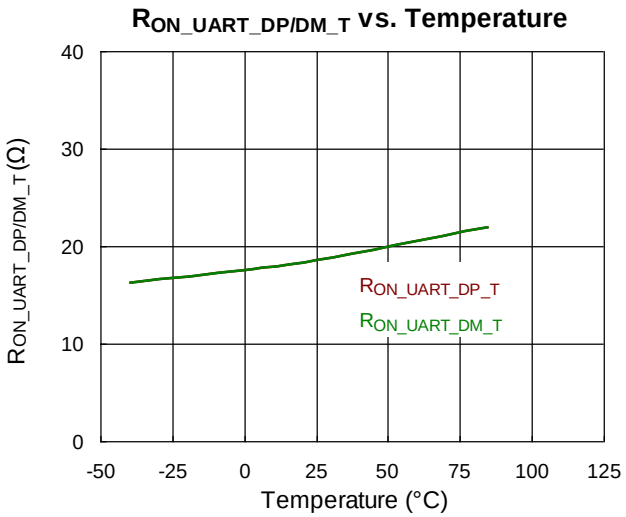


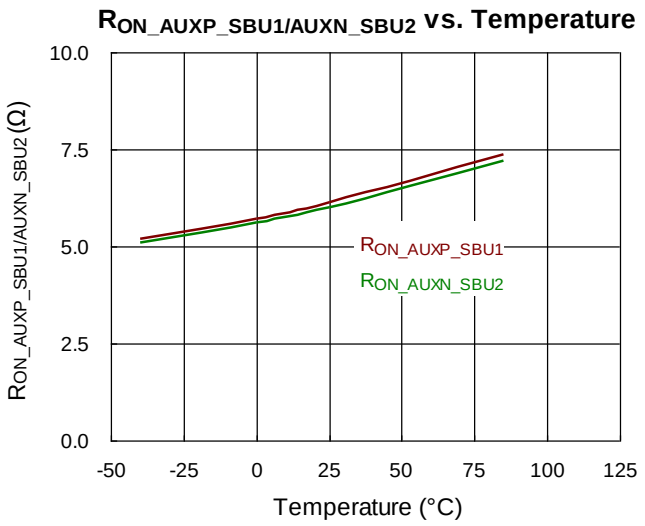


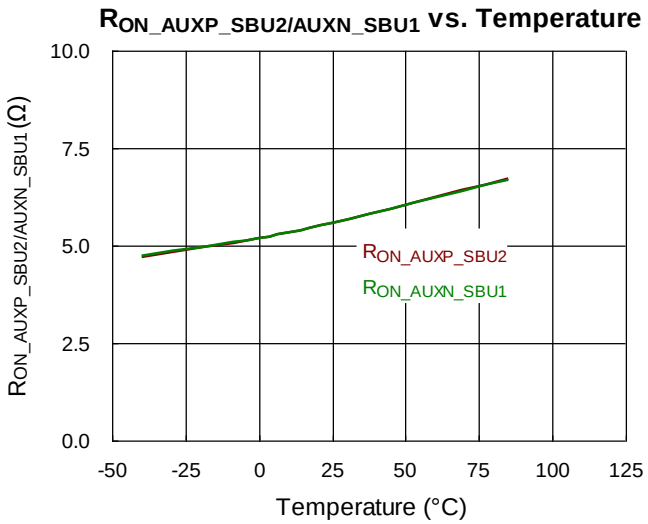












Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

Internet On-line Firmware Update

Due to using MTP memory, the RT7802 firmware can be updated by embedded controller (SCK, SDA, INTB, VDDA and VSSA) or 5-pin connector (SCK, SDA, OM, VDDA and VSSA). Users can easily update firmware without de-soldering/soldering the RT7802 during product development period. In mass production, the RT7802 based products can use same version RT7802 ICs to reduce inventory cost. It also allows updating the RT7802 firmware at end customer site through internet in response to some necessary system software changes.

Calculating Output Discharge Time

Figure 1 is the functional block diagram of the built-in output bleeder. The discharge time (t_{DIS}) is determined by the following equation :

$$t_{DIS} = R_{BLD} \times C_{VBUS} \times \ln\left(\frac{V_{BUS\_OLD}}{V_{BUS\_NEW}}\right)$$

where :

- R_{BLD} is the total internal resistance during on-state of the bleeder.
- C_{VBUS} is the total capacitance of the capacitors coupled to VBUS pin.
- V_{BUS_OLD} is the initial voltage between the capacitors before the discharging.
- V_{BUS_NEW} is the final voltage between the capacitors at end of the discharging.

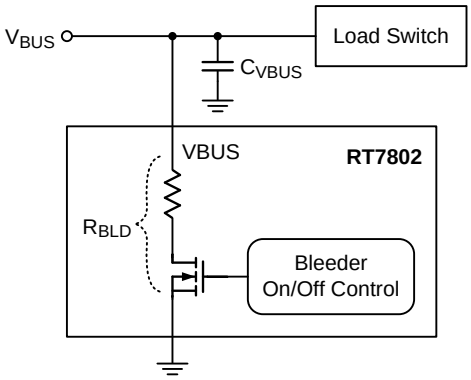


Figure 1. Bleeder Functional Block Diagram

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 105°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (105°C - 25°C) / (27.8°C/W) = 2.87W for a WQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

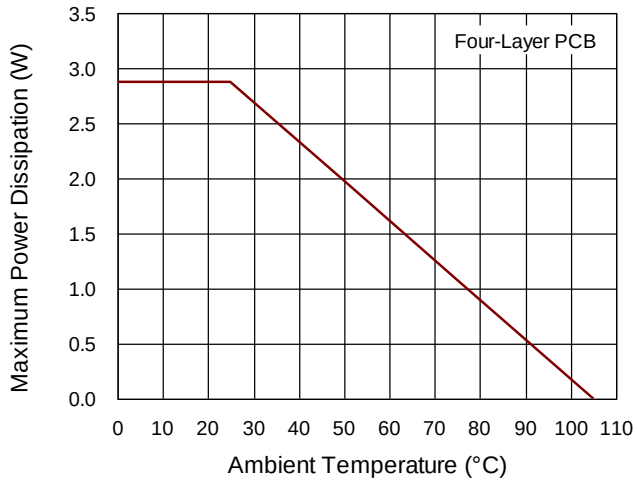


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

Connect the IC GND pins and the exposed pad to a ground plane (IC-ground), and then connect the IC ground to the USB GND terminals via low impedance path. The exposed pad is also applied to dissipate the heat into PCB.

Connect the decoupling MLCCs near to the pins of VDDA, VLDO, VCONN and VBUS. Connect the MLCCs to the pins and IC-ground via low impedance paths.

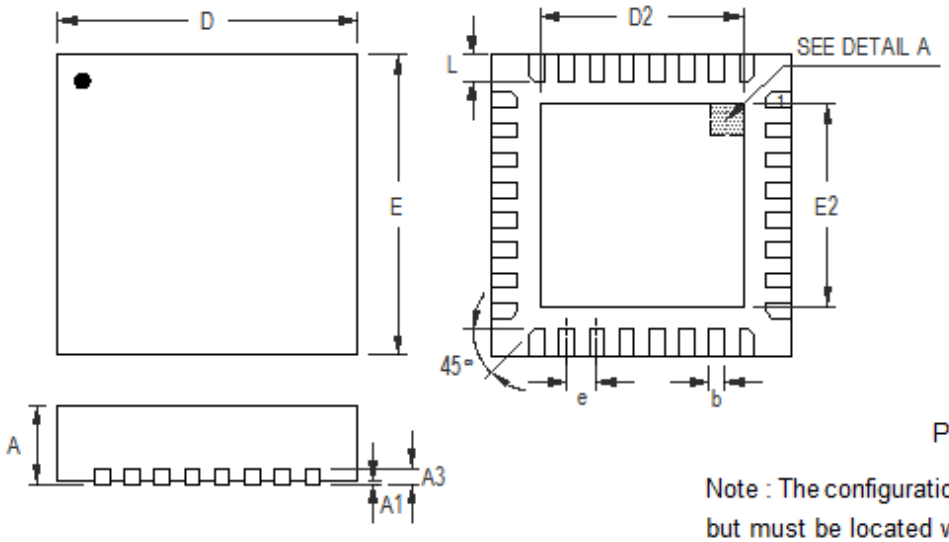
Separate following signals from the switching nodes and the switching-current paths to prevent the noise :

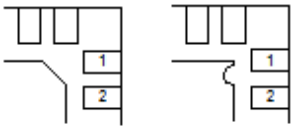
- CC1 and CC2 signals.
- USB 2.0/UART MUX signals
- AUX MUX signals

For improving ESD immunity, connect MLCCs close to the GND and VBUS terminals of USB Type-C connector.

Connect the capacitors to the USB VBUS and GND terminals through the low impedance paths.

Outline Dimension





DETAIL A

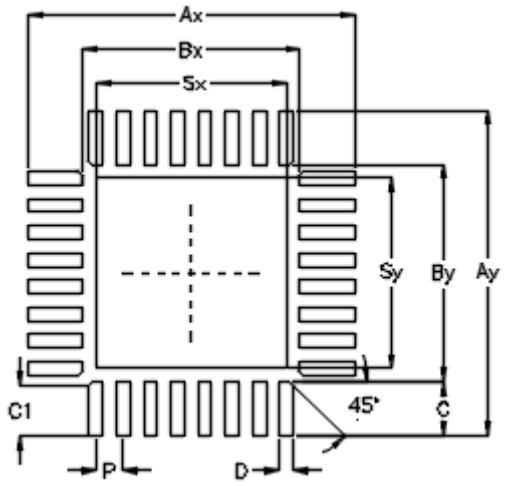
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

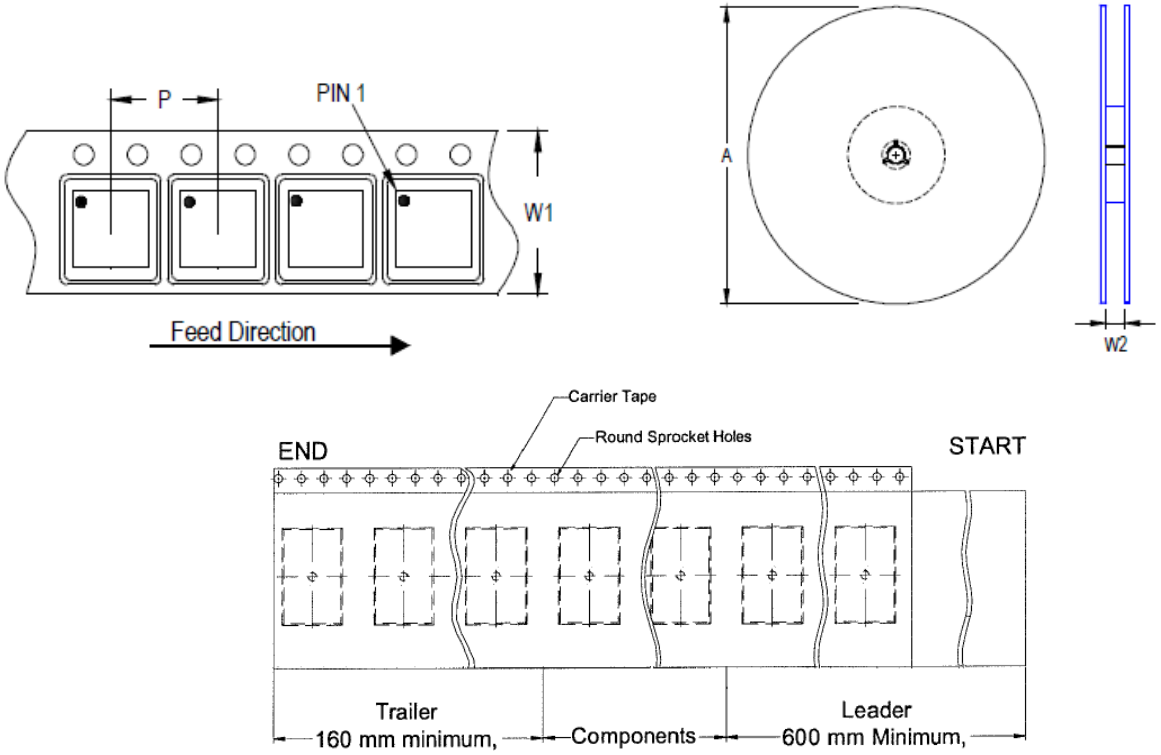
Footprint Information



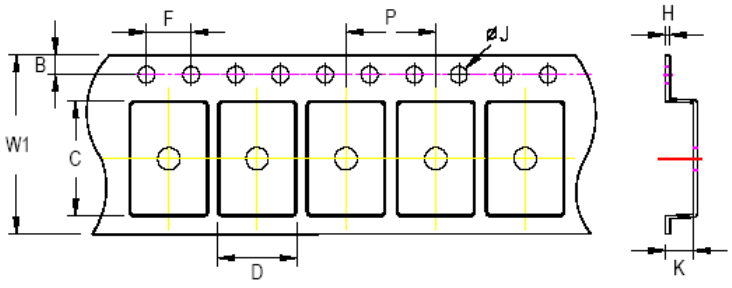
Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*32	C1*8	D	Sx	Sy	
V/W/U/XQFN4*4-32	32	0.40	4.80	4.80	3.20	3.20	0.80	0.75	0.20	2.80	2.80	±0.05

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 4x4	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
01	2023/5/3	Modify	Ordering Information on P1 Marking Information on P2 Functional Pin Description on P2, 3 Functional Block Diagram on P4 Operation on P5 Electrical Characteristics on P9 Application Information on P16 Packing Information on P20, 21, 22