RT7880

USB Type-C PD and PWM Buck-Boost Controller with AnyPower^{TM} and PDsafe^{TM} Features

General Description

The RT7880 is a USB Type-C Power Delivery (USB-C PD) and PWM buck-boost controller with highly integrated functions and flexibility for USB PD provider applications. The IC has an embedded ARM Cortex^{TM}-M0 MCU, which handles various functions of communication protocol, smart control of the PWM converter, firmware-based protections, and customized functions. The IC features hardware-based protections, such as inductor peak current limit, VBUS over-voltage protection (VBUS OVP), VO under-voltage protection (VO UVP), and VCONN current limit protection, so that the protections have faster responses and can still function even when the MCU is not activated. The RT7880 can offer an excellent USB PD solution for a USB-PD Provider application with few external components and simple PCB layout.

Ordering Information

RT7880☐☐

Package Type
QW : WQFN-40L 5x5 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT7880
GQW
YMDNN
●

RT7880GQW : Product Number

YMDNN : Date Code

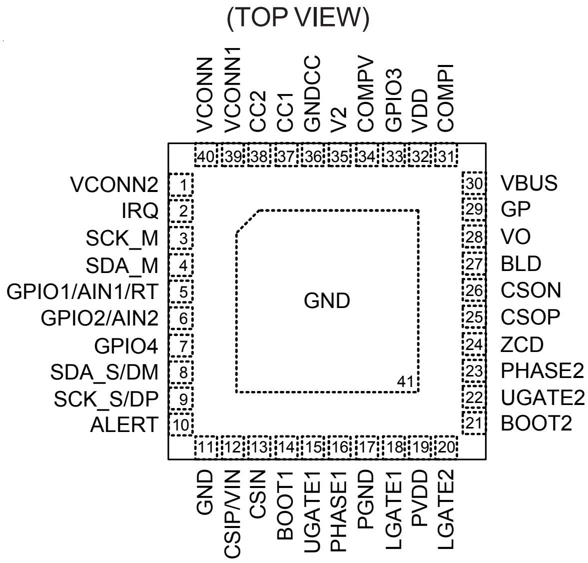
Features

- **Support USB Type-C Power Delivery (PD) Provider Application**
- **Type-C, USB PD and Communication Protocols**
  - **Compliant with USB PD 3.0 Specification, USB Type-C Cable and Connector Specification 1.2**
  - **Alternate Mode and V_{CONN} Output**
  - **Support Other Proprietary Communication Protocols through Internal MCU, DP and DM Pins**
- **Integrated PWM Buck-Boost Controller**
  - **Wide Input Voltage Range : 4V to 36V**
  - **Peak-Current Mode PWM Operation**
  - **Programmable PWM Switching Frequency (200kHz to 600kHz)**
  - **Pulse-Skipping Mode for Light-Load Efficiency; Selectable Forced CCM Operation**
- **AnyPower^{TM} for Constant Voltage Output (15.6 or 23.4mV/step, typ.) and Constant Current (in 9-Bit Resolution) Output Settings**
- **PDsafe^{TM}**
  - **Adjustable Converter Input Current Limit**
  - **Programmable VBUS OVP and VO UVP**
  - **Adjustable External OTP**
  - **VCONN1/2 Output Current Limit**
- **Cable Voltage Drop Compensation for V_{BUS}**
- **Master and Slave I^2C Interfaces**
- **GPIOs for MUX Control or Customized Functions**
- **Built-in Output Bleeders for Quick V_{BUS} Discharge**
- **Built-in Charge Pump for Driving Cost-Effective N-MOSFETs**
- **Available in WQFN-40L 5x5 Package**
- **Online Firmware Update via Slave I^2C Interface**

Applications

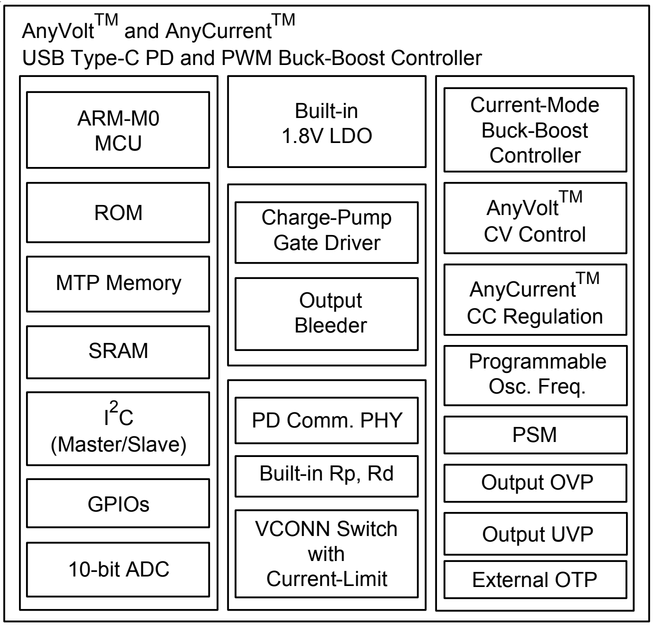
- Desktop PC, LCD Monitor, LCD TV
- Docking Station, Portable Hard Disk
- USB Car Charger, USB Power Bank

Pin Configuration

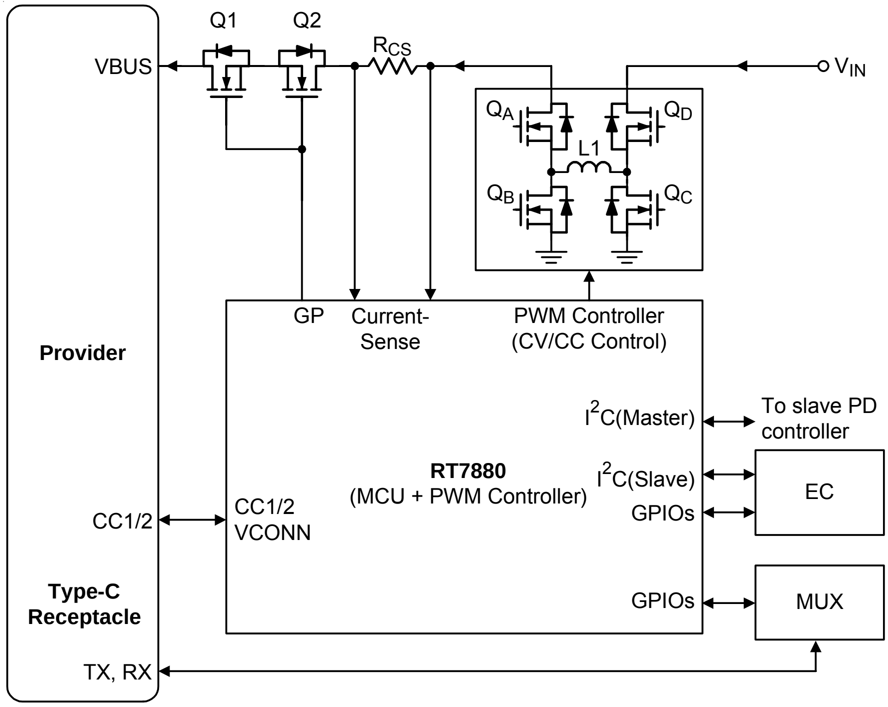


WQFN-40L 5x5

Simplified Functional Block Diagram



Simplified Application Circuit



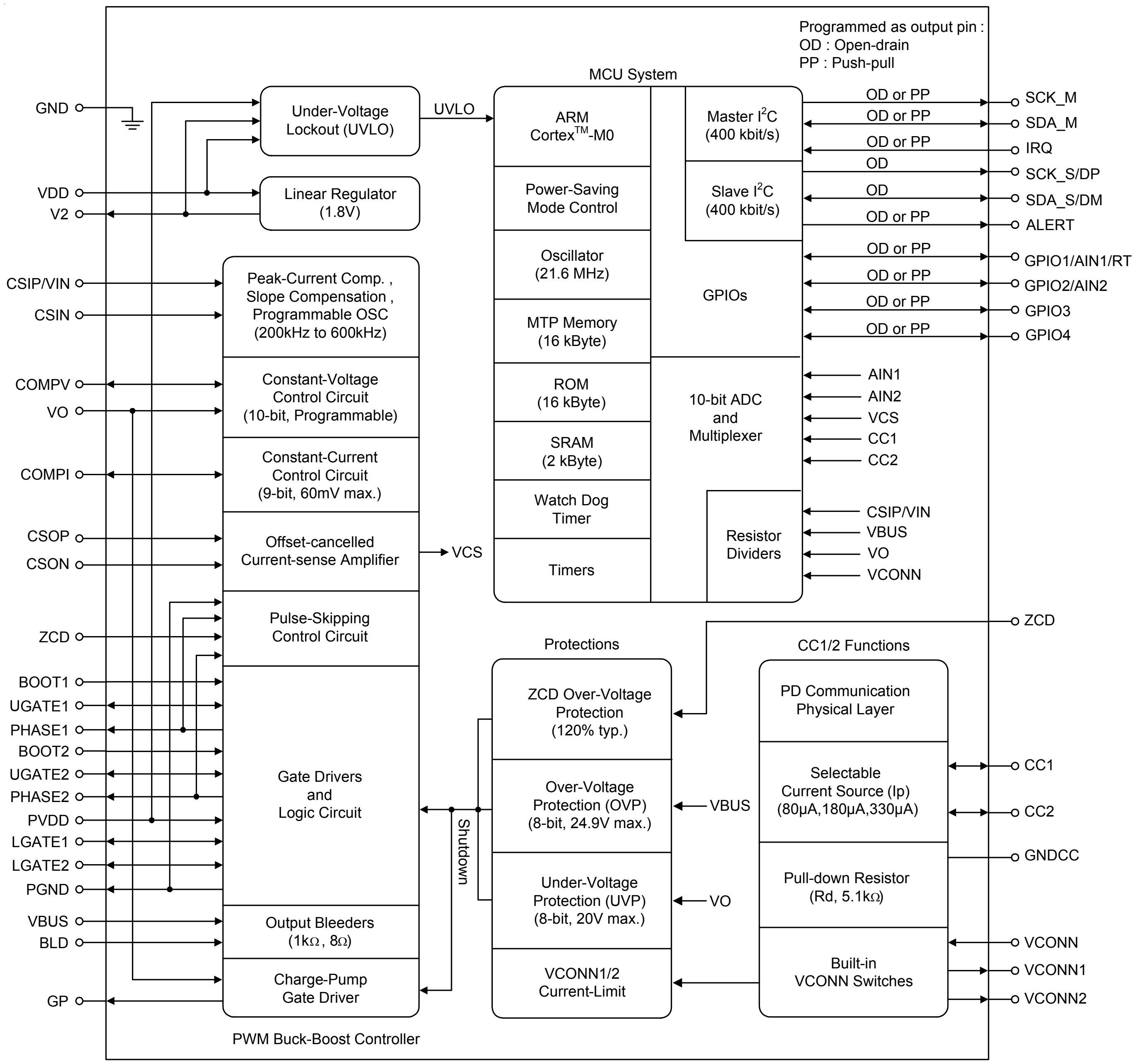
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCONN2	Power output to supply USB plug power (V_{CONN}) through USB Type-C connector CC2 terminal. A MOSFET is built in to turn on/off the power path from VCONN to VCONN2. This pin is usually connected to USB Type-C connector CC2 terminal via a Schottky diode.
2	IRQ	Interrupt input. The RT7880 will do emergency control when it receives a low-level signal via this pin. This pin can be set as an open-drain or push-pull GPIO pin.
3	SCK_M	Open-drain clock signal output from the master I^2C interface. This pin can be set as an open-drain or push-pull GPIO pin.
4	SDA_M	Open-drain data signal input / output for the master I^2C interface. This pin can be set as an open-drain or push-pull GPIO pin.
5	GPIO1/AIN1/RT	Open-drain/push-pull GPIO, analog input or input for external over-temperature protection (EOTP). An NTC is connected from this pin to GND for the EOTP.
6	GPIO2/AIN2	Open-drain/push-pull GPIO or analog input. Connect this pin to GND if it is not used.
7	GPIO4	Open-drain/push-pull GPIO.
8	SDA_S/DM	Open-drain data signal input / output for the slave I^2C interface or USB D- data line input / output. This pin can be set as an open-drain GPIO or connected to USB D- terminal for special communication protocol.
9	SCK_S/DP	Clock signal input for the slave I^2C or USB D+ data line input / output. This pin can be set as an open-drain GPIO or connected to USB D+ terminal for special communication protocol.
10	ALERT	Open-drain Interrupt signal output. An external MCU can check the slave I^2C registers to do emergency control when it receives a low-level signal from this pin. This pin can be set as an open-drain or push-pull GPIO.
11	GND	Analog ground.
12	CSIP/VIN	Positive input for input current sensing or voltage-sense input for input voltage of the converter.
13	CSIN	Negative input for input current sensing.
14	BOOT1	Bootstrap capacitor connection node. Connect a 0.1μF ceramic capacitor from this pin and the PHASE1 pin to power the internal 1st high-side gate driver.
15	UGATE1	1st High-side gate driver output.
16	PHASE1	Negative power-rail pin of the 1st high-side gate driver.
17	PGND	Ground of the low-side gate drivers and one input pin of zero-current detection at the MOSFET controlled by LGATE1. It is recommended to connect this pin to the source of the MOSFET via a dedicated trace.
18	LGATE1	1st Low-side gate driver output.
19	PVDD	Bias voltage (5V typ.) supply for the low-side gate drivers. It is recommended to connect an external MLCC (1μF) from this pin to PGND pin.
20	LGATE2	2nd Low-side gate driver output.
21	BOOT2	Bootstrap capacitor connection node. Connect a 0.1μF ceramic capacitor from this pin and the PHASE2 pin to power the internal 2nd high-side gate driver.

Pin No.	Pin Name	Pin Function
22	UGATE2	2nd High-side gate driver output.
23	PHASE2	Negative power-rail pin of the 2nd high-side gate driver.
24	ZCD	One input pin of zero-current detection (at the MOSFET controlled by LGATE1) and Output over-voltage protection input pin.
25	CSOP	Positive input of an offset-cancelled current-sense amplifier to sense the output current for constant current regulation and also through an ADC to the MCU. It is necessary to connect this pin to the positive terminal of output current-sense resistor via an RC filter and a dedicated PCB trace.
26	CSON	Negative input of an offset-cancelled current-sense amplifier to sense the output current for constant-current regulation and also through an ADC to the MCU. It is necessary to connect this pin to the negative terminal of output current-sense resistor via an RC filter and a dedicated PCB track.
27	BLD	Bleeder connection node. An output bleeder, comprising a pull-low NMOS, is built in to provide another path to discharge the output capacitor of the PWM converter. Connect this pin to the converter output through an external resistor.
28	VO	Input of feedback voltage from converter output. The voltage at this pin is monitored for output under-voltage protection with an 8-bit programmable threshold voltage.
29	GP	Charge-pump gate diver output. It drives N-channel power MOSFET(s) to turn on / off the output power path.
30	VBUS	USB-C VBUS voltage input. The voltage at this pin is monitored for USB-C VBUS over-voltage protection with an 8-bit programmable threshold voltage.
31	COMPI	Constant-current (CC) loop error amplifier output. Connect an external RC network between this pin and GND for constant-current loop feedback compensation.
32	VDD	IC bias voltage (5V typ.) input. It is recommended to connect this pin to a 5V system voltage via an RC filter of 1μF and 4.7Ω.
33	GPIO3	Open-drain / push-pull GPIO.
34	COMPV	Constant-voltage (CV) loop error amplifier output. Connect an external RC network between this pin and GND for constant-voltage (CV) loop feedback compensation.
35	V2	Internal 1.8V linear regulator output to supply power for internal circuitry. An MLCC (1μF typ. or greater) must be connected from this pin to ground.
36	GNDCC	Ground for Configuration Channel (CC) circuitry.
37	CC1	Type-C connector Configuration Channel (CC) 1. Generally, this input/output pin is connected to USB Type-C connector CC1 terminal.
38	CC2	Type-C connector Configuration Channel (CC) 2. Generally, this input/output pin is connected to USB Type-C connector CC2 terminal.
39	VCONN1	Power output to supply USB plug power (V_{CONN}) through USB Type-C connector CC1 terminal. A MOSFET is built in to turn on / off the power path, from VCONN to VCONN1. This pin is usually connected to USB Type-C connector CC1 terminal via a Schottky diode.
40	VCONN	Power input for sourcing V_{CONN} through the power path from VCONN to VCONN1, or VCONN2 pin. This pin is usually connected to a regulated 5V voltage source.

Pin No.	Pin Name	Pin Function
41 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT7880 is a versatile USB Type-C Power Delivery (USB-C PD) and PWM Buck-Boost controller especially designed for applications as Providers. It's a highly integrated solution, comprising four main functional blocks : MCU System, PWM Buck-Boost Controller, Protections and CC1/2 Functions as shown in the "Functional Block Diagram".

The MCU System embeds an ARM Cortex^{TM}-M0 MCU, multi-time programming (MTP) memory, ROM, SRAM, a 10-bit ADC (analog to digital converter), two I^2C interfaces (slave and master) and GPIO (general purpose input or output) pins. The MCU System is programmed to perform power controls, customized functions, as a policy engine and a device policy manager. It reports the operating status of PD operation, such as present input/output voltage, output current and external temperature to an EC (embedded controller) or AP (application processor) and receives commands from the EC/AP, as a system policy manager, via the slave I^2C interface. The GPIO pins can be used to control high-speed multiplexers or other customized functions.

The "PWM Buck-Boost controller" consists of an AnyVolt^{TM} constant-voltage (CV) control circuit (15.6 or 23.4mV/step, typ.), an AnyCurrent^{TM} constant-current (CC) control circuit, an offset-cancelled output current-sense amplifier (23.5mA to 47mA/step, depending on current-sense resistor), built-in gate drivers, one charge-pump gate driver and output bleeders (at BLD and VBUS pins). Generally, either the CV or the CC control circuit regulates the output voltage or current through peak-current mode PWM operation. Diode emulation function and pulse-skipping mode (PSM) are built in to improve power efficiency at light loads. The output current-sense amplifier (OCS-AMP) allows current-sense resistors as low as 5mΩ to 15mΩ for reducing power loss. The charge-pump driver drives N-channel MOSFETs for on/off control of output power-path, instead of P-channel MOSFET with higher cost. The output bleeders at BLD and VBUS pins can be turned on to discharge output voltage (V_{BUS}) during V_{BUS} negative transition or hard reset process, or after the removal of the USB-C connector.

The PDsafe^{TM} power delivery operation consists of over-voltage protection (OVP) at the VBUS pin, under-voltage protection at the VO pin, output CC regulation and VCONN1/2 output current-limit function. The OVP and UVP trip levels can be set dynamically for each output voltage target. The CC regulation level is also adaptively programmed according to full load current level.

The "CC1/2 Functions" block consists of the physical layer, three selectable levels of the pull-up current sources Ip (instead of resistors Rp), a controllable pull-down resistor Rd and programmable V_{CONN} power-path switches.

Under-Voltage Lockout (UVLO)

The RT7880 UVLO function continuously monitors bias voltages at the VDD and V2 pins. When both of the supply voltages (V_{DD} and V_{V2}) rise above the respective rising UVLO thresholds, the internal UVLO signals will go low to activate the MCU. The IC also monitors the bias voltage at the PVDD pin for UVLO function. Only when all of the UVLO signals go low, the PWM Buck-Boost controller will be activated; otherwise the MCU or PWM controllers will be in "Under-Voltage Lockout" state to prevent any undesirable operation.

Pulse-Skipping Mode (PSM) with Diode Emulation

When a switch-mode converter operates in light load condition, most power loss is caused by switching losses. To reduce switching loss in light load condition, the switching frequency needs to be reduced, and this can be accomplished by entering pulse-skipping mode (PSM) and discontinuous conduction mode (DCM). An internal compensation voltage V_{COMP} is compared by a PSM comparator, which has a programmable PSM threshold. When the compensation voltage V_{COMP} (which follows the voltage at COMPV, or COMPI pin) is above the PSM threshold, the converter works in normal fixed-frequency PWM mode. But when the V_{COMP} drops below the PSM threshold, the converter will enter pulse-skipping mode to reduce switching frequency and thus switching losses. The PSM threshold also defines the minimum inductor peak current in PSM operation. Setting a larger PSM threshold will give a higher minimum peak current which in turn gives a lower switching frequency at light load for better light load efficiency at the cost of increased output voltage ripple. Conversely, a lower PSM threshold gives lower peak current and lower PSM ripple at the cost of worse light load efficiency.

A Diode Emulation Mode (DEM) is also a necessary function to avoid delivering energy from converter output to converter input during dynamic output voltage control. The DEM function is equipped with two zero-current detection (ZCD) circuits for the low-side and high-side MOSFETs respectively controlled by the LGATE1 and UGATE2 pins: The Source-to-Drain voltage (V_{SDB}, detected via PGND and PHASE1 pins) of the low-side MOSFET is compared with a zero-current threshold (V_{TH_ZCDB}). When the V_{SDB} drops below the V_{TH_ZCDB} voltage, the RT7880 turns off the low-side MOSFET thereby avoiding reverse inductor current. In DEM operation, the behavior of the low-side MOSFET resembles a diode. The second ZCD circuit compares the Source-to-Drain voltage (V_{SDD}, detected via PHASE2 and ZCD pins) of the high-side MOSFET with a zero-current threshold (V_{TH_ZCDD}) to achieve the DEM function.

Cable Voltage Drop Compensation (CDC)

In a power delivery system with both a Provider and a Consumer, the Provider with the RT7880 AnyVolt^{TM} feature can slightly adjust its CV output voltage to compensate voltage drop across the USB cable. A PD controller of the Consumer can request higher VBUS voltage from the Provider through PD communication to achieve an accurate application voltage.

There is another method to implement the CDC function without PD communication. The RT7880 can use the ADC to detect the output current-sense voltage (V_{CSO}) between CSOP and CSON pins and adaptively add a proper output voltage offset (V_{CDC}) to compensate the cable voltage drop. The output voltage offset (V_{CDC}) is gradually added by adjusting the CV regulated output voltage (V_{REG_VO}) and is approximately proportional to the converter output current (I_{OUT}). The V_{CDC} is approximately determined by the following equation :

$$V_{CDC} = I_{OUT} \times R_{CABLE}$$

where :

R_{CABLE} is a preset value of parasitic resistance of USB cable.

VBUS Over-Voltage Protection (VBUS OVP)

In Figure 1, the VBUS OVP function is a hardware-based protection which monitors the voltage at the VBUS pin via a built-in resistor-divider. When the VBUS voltage exceeds its OVP threshold, the output of the OVP comparator goes high and starts the debounce time counting. At the end of the debounce time counting. At the end of the debounce time, the signal VBUS OVP goes high to turn off the PWM controller. The OVP trip voltage is programmable from 3V to 24.9V (8-bit, 97.66mV/step typ.) and its debounce time is also selectable to meet various application requirements.

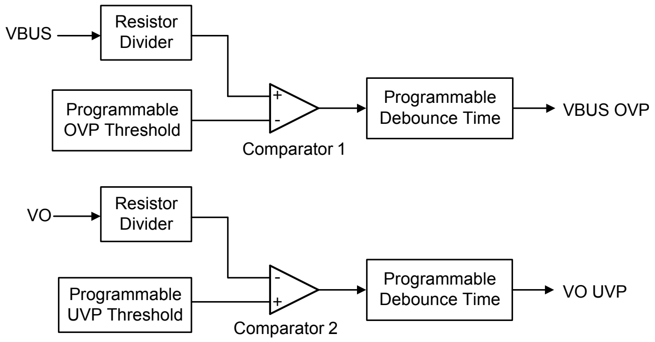


Figure 1. Functional diagram of VBUS OVP and VO UVP

VO Under-Voltage Protection (VO UVP)

In Figure 1, the VO UVP function is a hardware-based protection which monitors the voltage at the VO pin via a built-in resistor-divider. When the VO voltage falls below its UVP threshold, the output of the UVP comparator goes high and starts the debounce time counting. At end of the debounce time, the signal VO UVP goes high to turn off PWM controller. The UVP trip voltage is programmable from 3V to 20V (8-bit, 93.75mV/step typ.) and its debounce time is also selectable to avoid false triggering and to meet various application requirements.

AnyCurrent^{TM} Constant-Current (CC) Regulation

Because a robust system is very important in USB PD operations, the AnyCurrent^{TM} CC regulation allows setting the most suitable CC level for a negotiated PD system. The RT7880 integrates a current-sense amplifier to sense output current for CC regulation and also through an ADC to the MCU for the output current to be recorded. The amplifier is embedded with offset cancellation function to accurately sense the current-sense voltage (i.e., V_{CS} = output current x current-sense resistor) between the CSOP and CSON pins. The recommended current-sense voltage range for CC regulation is from 10mV to 60mV which is programmed by an internal 9-bit DAC (digital-to analog converter) with 0.1174mV/step resolution.

Power-Path Gate Driver for Driving N-Channel MOSFETs

The RT7880 integrates a power-path gate driver to control external output blocking MOSFETs between the output of the PWM converter and the USB-C VBUS terminal. A built-in charge pump is included to supply the gate driver to turn on the external N-channel power MOSFETs, which allow power systems to be more cost-effective, compared to the counterpart, P-channel power MOSFETs.

Power Output for USB Plug Power (V_{CONN})

In Figure 2, either one of the VCONN1 and VCONN2 pins is selected to power an external electrically marked (E-mark) or active cable. Two internal MOSFETs, between VCONN to VCONN1 and VCONN2 pins, are used to control the VCONN power path to VCONN1 or to VCONN2. Connect the VCONN1/2 pins to USB-C CC1/2 terminals via Schottky diodes (D1/2) to prevent reverse current. The input pin VCONN must be connected to an external 5V power source.

Online Firmware Update via Slave I^2C Interface

The embedded MTP memory allows the RT7880's firmware to be updated by an EC (Embedded Controller) or AP (Application Processor) through the I^2C slave interface. The RT7880 provides some firmware- programmable design features, which greatly eases the design efforts during product development stage. End users are also allowed to update the firmware through internet to make software changes based on the needs.

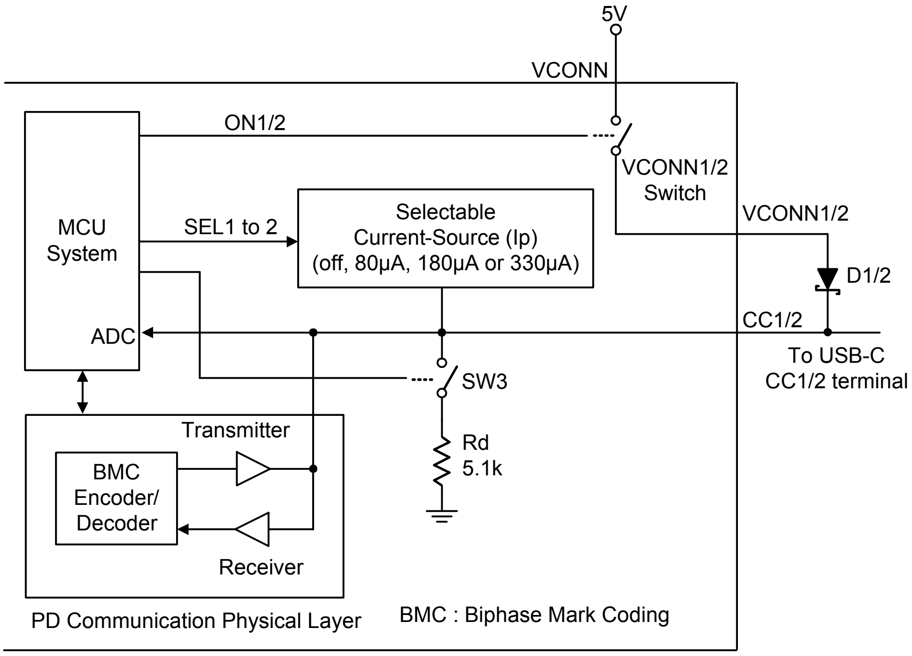


Figure 2. Functional diagram of VCONN and CC1/2 functions

Absolute Maximum Ratings (Note 1)

V2 to GND	–0.3V to 2.5V
VDD, PVDD, VCONN to GND	–0.3V to 6.5V
COMPV, COMPI to GND	–0.3V to 6.5V
VCONN1, VCONN2 to GND	–0.3V to V_{VCONN} + 0.3V
VBUS, CSOP, CSON, VO, BLD, ZCD to GND	–0.3V to 25V
CSOP to CSON Voltage	–5V to 5V
GP to GND	–0.3V to 33V
CSIP/VIN, CSIN to GND	–0.3V to 40V
CSIP/VIN to CSIN Voltage	–5V to 5V
I^{2}C Pins (SCK_S/DP, SDA_S/DM, ALERT, SCK_M, SDA_M, IRQ) to GND	–0.3V to 6.5V
GPIO Pins (GPIO1/AIN1/RT, GPIO2/AIN2, GPIO3, GPIO4) to GND	–0.3V to 6.5V
CC1, CC2 to GND	–0.3V to 25V
BOOT1/2 to PHASE1/2 ($V_{BOOT-PHASE}$)	–0.3V to 6.5V
UGATE1/2 to PHASE1/2	–0.3V to $V_{BOOT-PHASE}$ + 0.3V
PHASE1 to GND (DC)	–0.3V to 40V
< 20ns	–5V to 45V
PHASE2 to GND (DC)	–0.3V to 25V
< 20ns	–5V to 30V
LGATE1/2 to PGND	–0.3V to V_{PVDD} + 0.3V
PGND, GNDCC to GND	–0.3V to 0.3V
Power Dissipation, P_D @ T_A = 25°C	
WQFN-40L 5x5	3.63W
Package Thermal Resistance (Note 2)	
WQFN-40L 5x5, θ_{JA}	27.5°C/W
WQFN-40L 5x5, θ_{JC}	6°C/W
Junction Temperature	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Storage Temperature Range	–65°C to 150°C
ESD Susceptibility (Note 3)	
HBM (Human Body Model)	2kV

Recommended Operating Conditions (Note 4)

PWM Converter Input Voltage, V_{IN}	4V to 36V
PWM Converter Ouput Voltage, V_{OUT}	3V to 22V
VDD Supply Voltage	4.25V to 5.5V
PVDD Supply Voltage	4.5V to 5.5V
Junction Temperature Range	–40°C to 125°C
Ambient Temperature Range	–40°C to 85°C
Minimum MTP Memory Write/Erase Cycles	100cycles

Electrical Characteristics

(V_{DD} = V_{PVDD} = V_{VCONN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Currents and V2 Linear Regulator						
VDD Normal Operating Current	I_{OP_VDD}	PWM = MCU = on, digital output pins = open	--	10	15	mA
VDD Operating Current in Green-Mode (GM)	I_{GM_VDD}	PWM = on, MCU = off, GP = on, digital output pins = open	--	5	8	mA
VDD Operating Current in Deep Green-Mode (DGM)	I_{DGM_VDD}	PWM = MCU = off, digital output pins = open	--	75	150	μA
V2 Output Voltage	V_{REGV2}	I_{V2} = 0A	1.58	1.76	1.94	V
V2 Short-Circuit Current			30	50	80	mA
PVDD Input Current in PWM Shutdown			--	--	3	μA
VCONN Input Current		Resistor-divider and switches are off	--	--	3	μA
BOOT Input Current in PWM Shutdown		V_{BOOT} = 4.5V	--	--	3	μA
Under-Voltage Lockout (UVLO), Over/Under-Voltage Protection (OVP/UVP) and Max. On-Time Protection						
VDD UVLO Voltage Threshold		V_{DD} rising	3.8	4.0	4.2	V
VDD UVLO Voltage Hysteresis			--	0.25	--	V
V2 UVLO Voltage Threshold		V_{V2} rising	--	1.4	--	V
V2 UVLO Voltage Hysteresis			--	0.2	--	V
PVDD UVLO Threshold		V_{PVDD} rising	3.8	4.0	4.2	V
PVDD UVLO Hysteresis			--	0.2	--	V
CSIP/VIN UVP Threshold		Enabled by firmware, $V_{CSIP/VIN}$ rising	2.7	2.9	3.1	V
CSIP/VIN UVP Hysteresis			--	0.25	--	V
VBUS OVP Voltage Threshold Range	V_{TH_VBUSOV}	Programmable(8-bit), 97.66mV/step at V_{VBUS} pin	3.03	--	24.90	V
VBUS OVP Voltage Threshold Accuracy		Setting of V_{TH_VBUSOV} = 5.96V/24.0V, V_{VBUS} rising	−5	--	5	%
VBUS OVP Debounce Time	t_{DB_VBUSOV}	Programmable, V_{VBUS} rising	--	4.5 7 12 22	6.6 9.6 15.6 27.6	μs
VO UVP Voltage Threshold Range	V_{TH_VOUV}	Programmable (8-bit), 93.75mV/step (typ.)	3.00	--	19.97	V
VO UVP Voltage Threshold Accuracy		Nominal V_{TH_VOUV} = 3.0V/15.0V, V_{VO} falling	−5	--	5	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VO UVP Debounce Time		V_{VO} falling, programmable	--	8 10.5 15.5 25.5	13.6 16.6 22.6 34.6	μs
VO UVP Blanking Time during Start-Up		Programmable	4 8 16 32	5 10 20 40	6 12 24 48	ms
CC1/2 Voltage Detections, BMC Transmitter/Receiver and VCONN Switches						
CC1/2 Voltage Detection Range		Using the 10-bit ADC	0	--	2.7	V
CC1/2 Voltage Detection Accuracy		Using the 10-bit ADC, $V_{CC1/2}$ = 0.1 to 2.7V	−40	--	40	mV
CC1/2 Pull-Up Current Source – 1	Ip1	For default USB power	64	80	96	μA
CC1/2 Pull-Up Current Source – 2	Ip2	For 1.5A and 5V	165.6	180	194.4	μA
CC1/2 Pull-Up Current Source – 3	Ip3	For 3.0A and 5V	303.6	330	356.4	μA
CC1/2 Pull-Down Resistor	Rd	Reserved	4.6	5.1	5.6	kΩ
CC1/2 Maximum Output Voltage		CC1/2 = open	--	V_{DD}-0.7V	--	V
Transmitter High-Level Output Voltage Range			1.05	--	1.2	V
Transmitter Low-Level Output Voltage Range			0	--	75	mV
Receiver High-Level Input Voltage Range			0.67	--	1.45	V
Receiver Low-Level Input Voltage Range			−0.25	--	0.43	V
Rising Time of the Transmitter Output Voltage		From 10% to 90%, C_L=200pF to 600pF	300	--	--	ns
Falling Time of the Transmitter Output Voltage		From 90% to 10%, C_L=200pF to 600pF	300	--	--	ns
On-Resistance of VCONN-to-VCONN1/2 MOSFET			--	0.4	0.8	Ω
VCONN1/2 Output Voltage Accuracy		Output current = 0 to 200mA	4.70	--	--	V
VCONN1/2 Current-Limit Threshold		VCONN1/2 = GND	350	500	650	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MCU Section						
MCU Clock Frequency	f_{MCU}		19.4	21.6	23.8	MHz
MCU Clock Frequency in Deep Green-Mode	f_{MCU_DGM}		--	80	--	kHz
Charge-Pump Gate Driver (GP), I^{2}C Pins (SCK_S, SDA_S, ALERT, SCK_M, SDA_M, IRQ) and GPIO Pins (GPIO1/2/3/4)						
GP Pull-Low MOSFET On-Resistance			--	100	--	Ω
Maximum GP Voltage		V_{VO} = 20V, $R_{GP\text{-}to\text{-}GND}$ = 50MΩ	$V_{VO}+V_{DD}$	$V_{VO}+2 \cdot V_{DD}-3V$	$V_{VO}+2 \cdot V_{DD}-1V$	V
I^{2}C/GPIO High-Level Input Voltage Range	V_{IH}	For the pins configured as input pins	1.5	--	--	V
I^{2}C/GPIO Low-Level Input Voltage Range	V_{IL}	For the pins configured as input pins	--	--	0.4	V
I^{2}C/GPIO High-Level Output Voltage	V_{OH}	Sourcing current = 2mA, for the pins configured as push-pull output pins	--	$V_{DD}-0.8V$	--	V
I^{2}C/GPIO Low-Level Output Voltage	V_{OL}	Sinking current = 2mA	--	--	0.3	V
I^{2}C/GPIO Leakage Current		Pin input voltage = 5V	--	--	1	μA
Internal DP-to-DM On-Resistance	R_{ON_DPDM}		--	12	30	Ω
RT Current Source		V_{RT} < 2.7V	95	100	105	μA
PWM Controller – Programmable Oscillator						
Oscillator Frequency Range	f_{OSC}	Programmable	200	--	600	kHz
Oscillator Frequency Accuracy		T_A = 25°C	−6	--	6	%
		T_A = −40 to 85°C (Note 5)	−10	--	10	
Maximum On-Time Range	t_{ON_MAX}	Programmable	0.32	--	5.88	μs
PWM Controller – Constant-Voltage (CV) Control Loop						
CV Regulated Voltage Range at VO	V_{REG_VO}	Programmable (10-bit), 15.625 or 23.438mV/step	3.00	--	15.98 23.98	V
Output Voltage Accuracy (at VO Pin)		V_{OUT} = 5V/9V/12V/15V/20V, 23.438mV/step, T_A = 25°C	−2	--	2	%
		T_A = −40 to 85°C (Note 5)	−3	--	3	
Trans-Conductance of COMPV Amplifier	Gmv	I_{COMPV} = ±20μA	412	550	688	μA/V
COMPV Maximum Output Voltage		COMPV = open	3.2	3.5	--	V
COMPV Voltage Offset	V_{OFS1}	(Note 5)	--	0.35	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller – Constant-Current (CC) Control Loop and Output Current-Sense Amplifier (OCS-AMP)						
CSON and CSOP Operating Voltage Range			3	--	22	V
CC Regulated Voltage Range between CSOP and CSON Pins	V_{REF_CC}	Programmable (9-bit), 0.1174mV/step (typ.), V_{CSON} and V_{CSOP} > 3V	10	--	60	mV
CC Reference Voltage Accuracy		Nominal V_{REF_CC} = 20mV/60mV	–3.0	--	3.0	mV
Trans-conductance of COMPI Amplifier	Gmi	I_{COMPI} = ±20μA	412	550	688	μA/V
COMPI Maximum Output Voltage		COMPI = open	3.2	3.5	--	V
COMPI Voltage Offset	V_{OFS2}	(Note 5)	--	0.35	--	V
PWM Controller – Input Current Comparison and Slope Compensation						
Maximum Input Current-Sense Voltage Threshold Range	V_{TH_CSMAX}	Programmable	--	--	140	mV
Maximum Input Current-Sense Voltage Threshold Accuracy		V_{TH_CSMAX} = 50mV, 100mV, 140mV	–15	--	15	mV
Leading Edge Blanking (LEB) Time of Input Peak/Over-Current Comparator	t_{LEBA}	From V_{UGATE1} rising edge, programmable	--	100 150 200 250	--	ns
LEB Time of Input Peak/Over-Current Comparator	t_{LEBC}	From V_{LGATE2} rising edge, programmable	--	100 150 200 250	--	ns
Voltage Rate Range of Slope Compensation		Programmable	0	--	92	mV/μs
PWM Controller – Pulse-Skipping Mode (PSM) Operation with Zero-Current Detection (ZCD)						
PSM Voltage Threshold Range at COMPV or COMPI Pin	V_{TH_PSM}	Programmable	--	--	1.969	$+V_{OFS1/2}$
MOS-D ZCD Voltage Threshold between PHASE2 and ZCD pins	V_{TH_ZCDD}	To compare the PHASE2-to-ZCD voltage	--	4	--	mV
MOS-B ZCD Voltage Threshold between PGND and PHASE1 pins	V_{TH_ZCDB}	To compare the PGND-to-PHASE1 voltage	--	4	--	mV
MOS-D ZCD Leading-Edge Blanking (LEB) Time	t_{LEBD}	Programmable, from V_{UGATE2} rising edge	--	150 225 300 375	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MOS-B ZCD LEB Time	t_{LEBB}	Programmable, from V_{LGATE1} rising edge	--	100 150 200 250	--	ns
PWM Controller – Gate Drivers						
UGATE1/2 Pull-High Resistance		$V_{BOOT1/2-PHASE1/2}$ = 5V, $V_{BOOT1/2-UGATE1/2}$ = 0.1V	--	1.7	--	Ω
UGATE1/2 Pull-Low Resistance		$V_{UGATE1/2-PHASE1/2}$ = 0.1V	--	0.8	--	Ω
LGATE1/2 Pull-High Resistance		V_{PVDD}-$V_{LGATE1/2}$ = 0.1V	--	1.7	--	Ω
LGATE1/2 Pull-Low Resistance		$V_{LGATE1/2}$ = 0.1V	--	0.8	--	Ω
Dead-Time before UGATE1/2 Rising Edge			--	20	--	ns
Dead-Time after UGATE1/2 Falling Edge			--	20	--	ns
PWM Controller – Output Bleeders						
On-Resistance of BLD Pull-Low MOSFET		Pull-low NMOS is on, sinking I_{BLD} = 10mA	--	8	16	Ω
BLD Leakage Current		V_{BLD} = 20V, pull-low NMOS is off	--	--	1	μA
VBUS Pull-Low Resistor		Pull-low NMOS is on	--	1.1	1.5	kΩ

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package. The copper area is 70mm^2 connected with IC exposed pad.

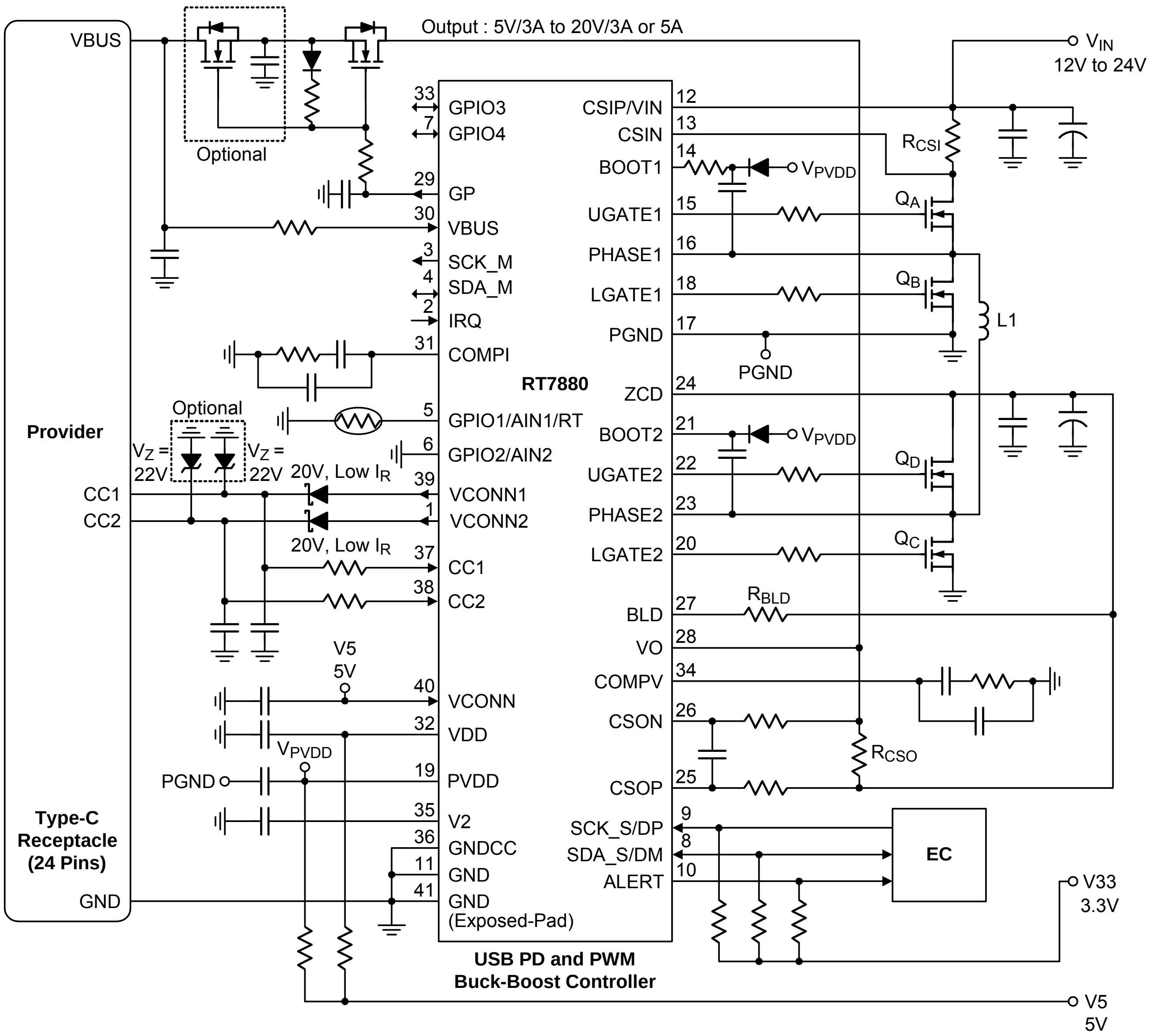
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

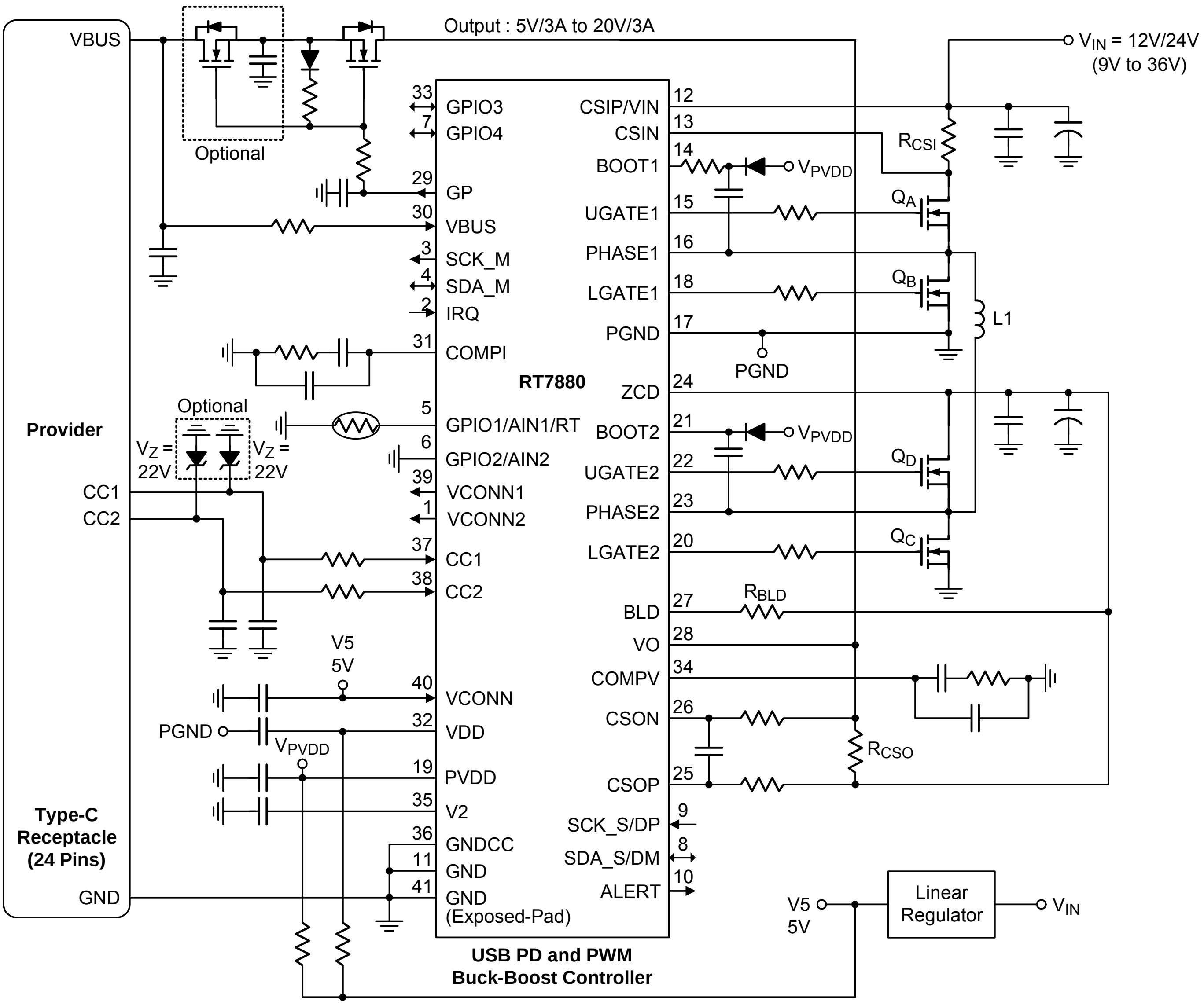
Note 5. Guaranteed by design.

Typical Application Circuit

(1) Provider Circuit with Buck-Boost Converter for Desktop PC, TV and Monitor Applications

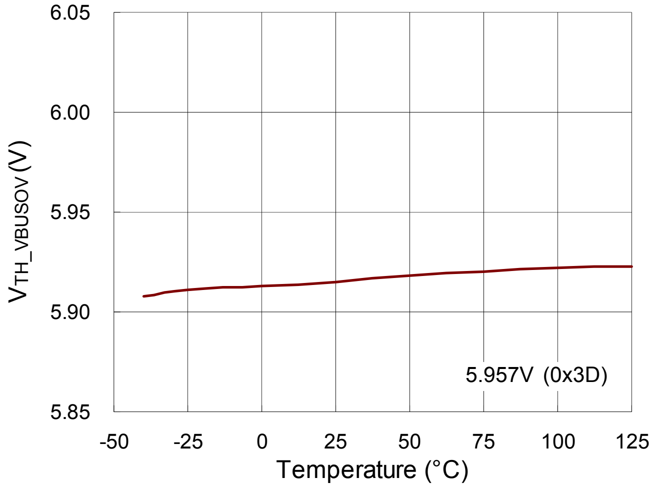


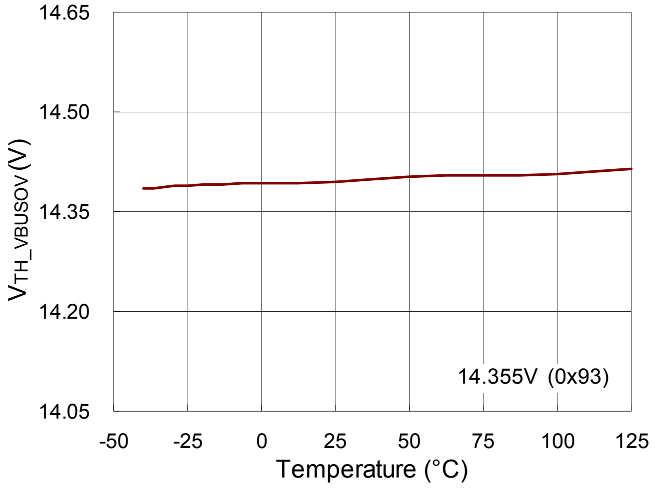
(2) Provider Circuit with Buck-Boost Converter for USB Car Charger Applications

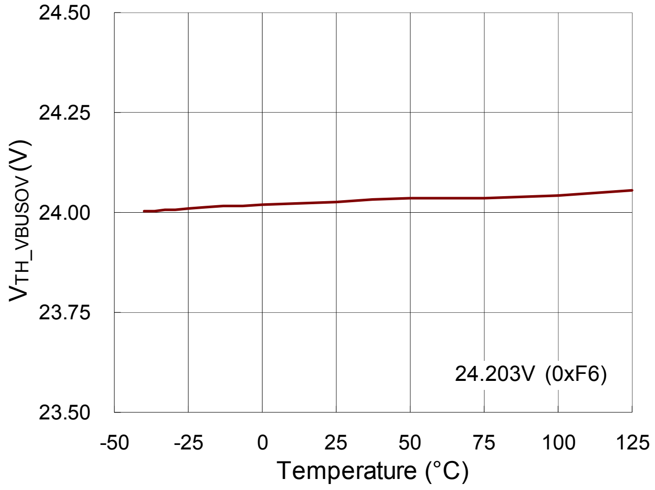


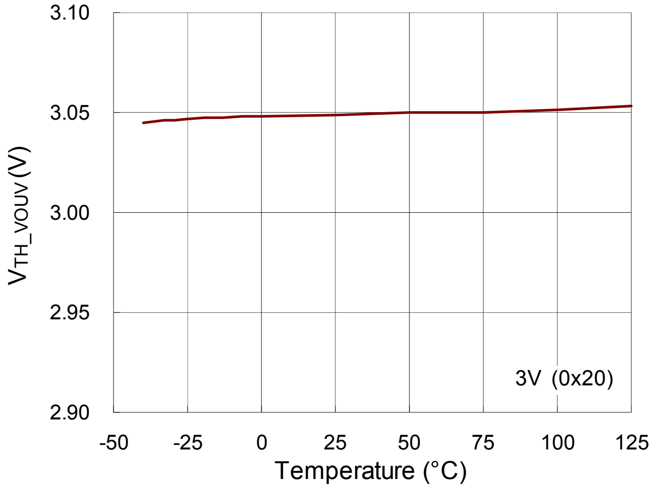
USB PD and PWM
Buck-Boost Controller

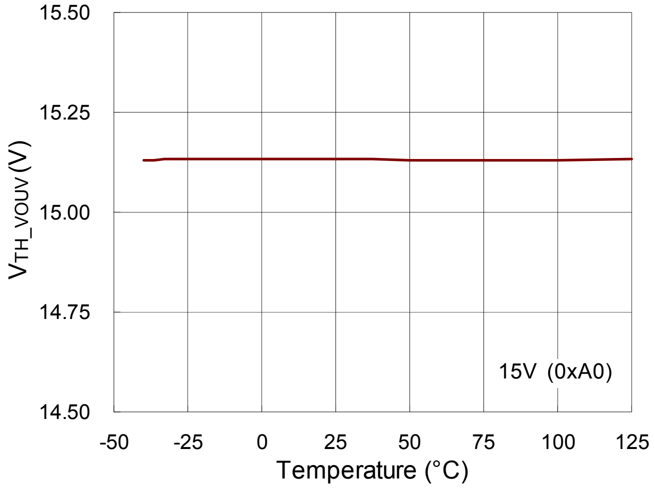
Typical Operating Characteristic

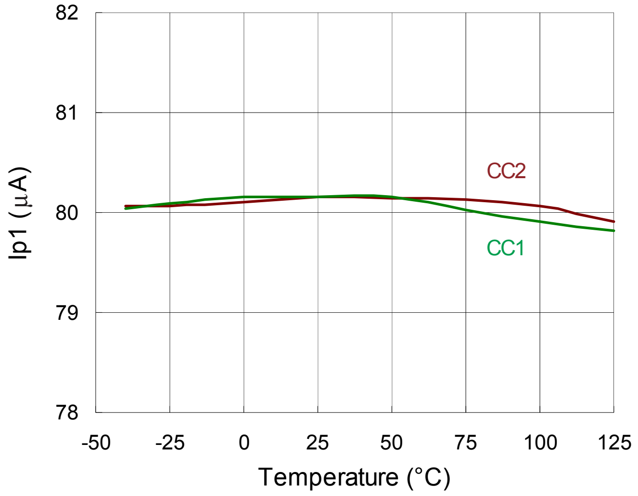

V_{TH_VBUSOV} vs. Temperature

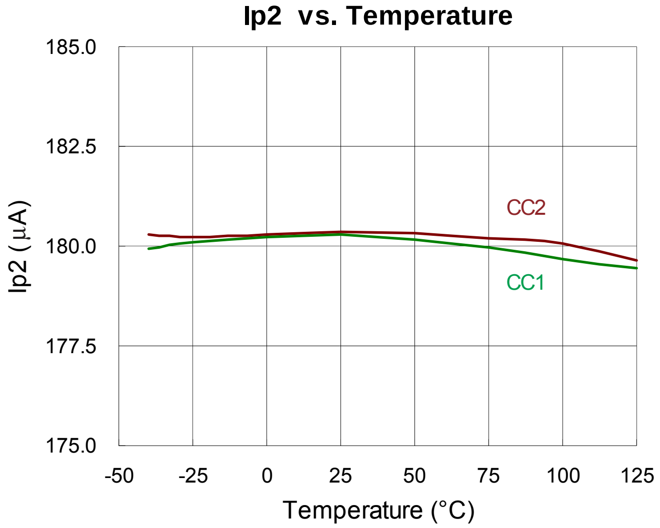

V_{TH_VBUSOV} vs. Temperature

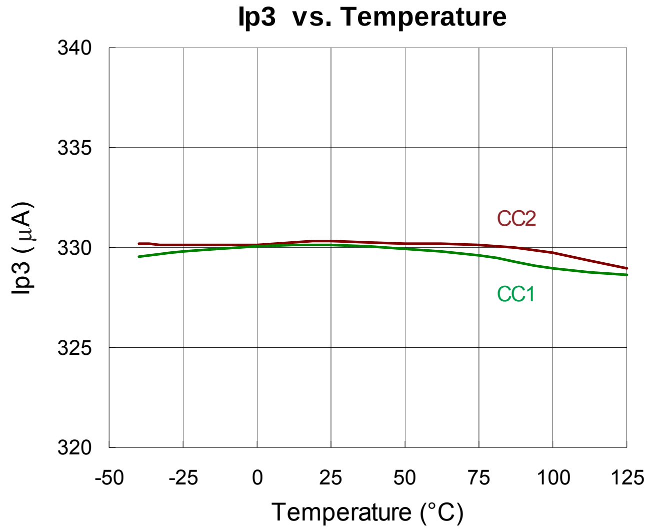

V_{TH_VBUSOV} vs. Temperature

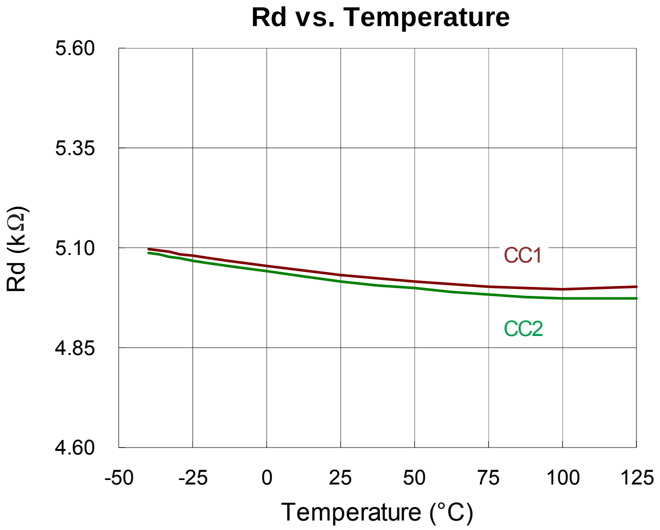

V_{TH_VOUV} vs. Temperature

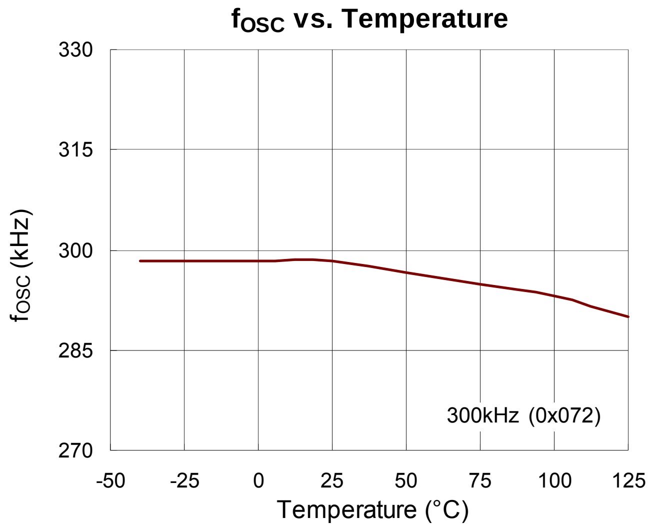

V_{TH_VOUV} vs. Temperature

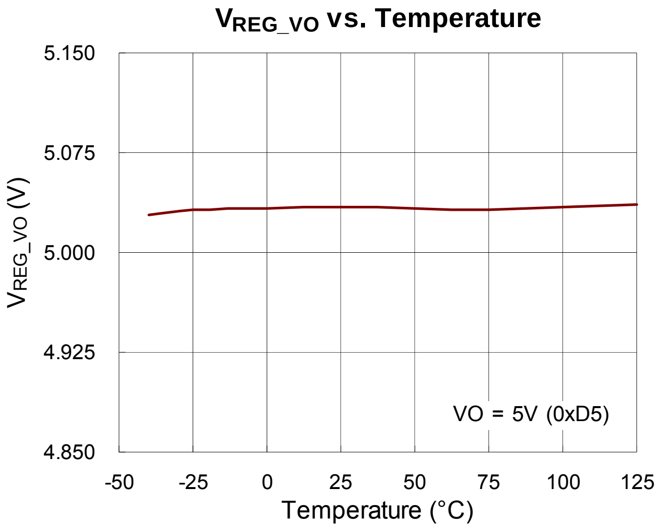

Ip1 vs. Temperature

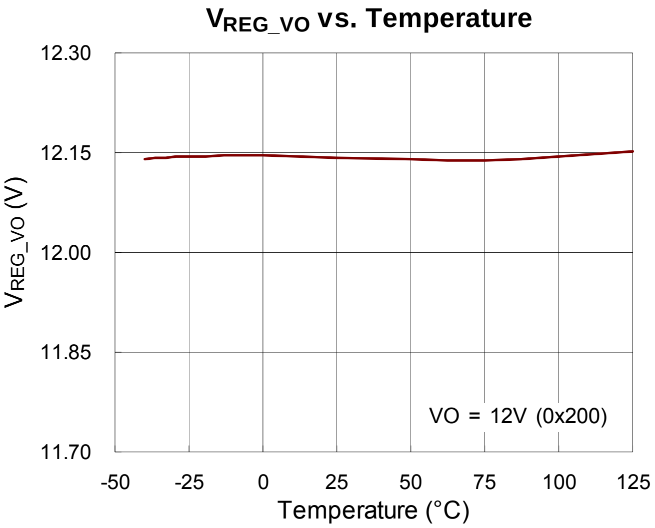

Ip2 vs. Temperature

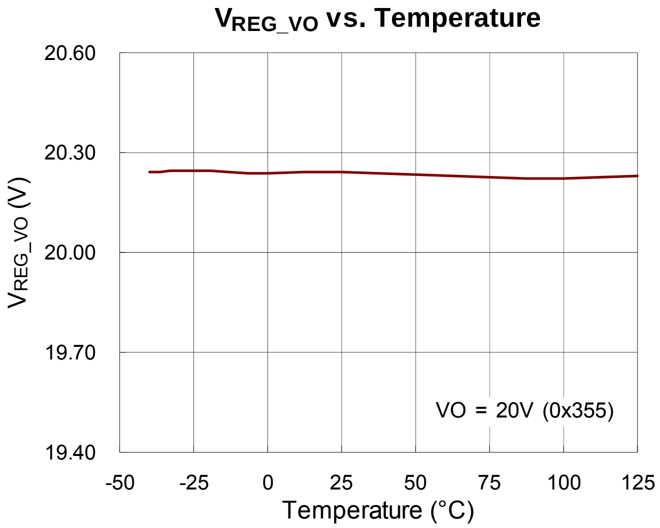

Ip3 vs. Temperature

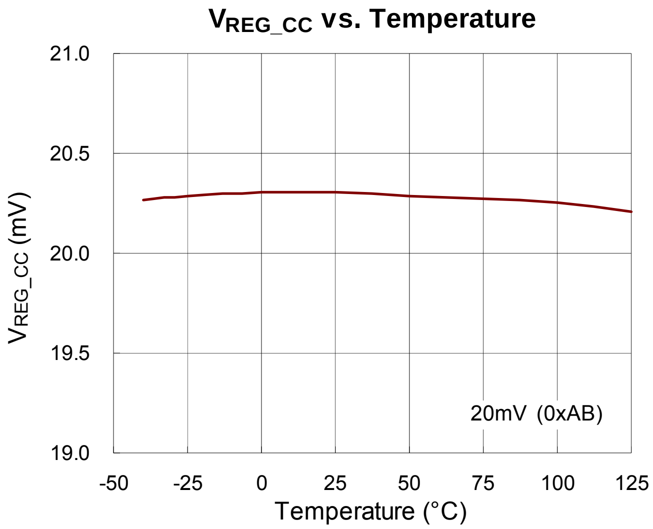

Rd vs. Temperature

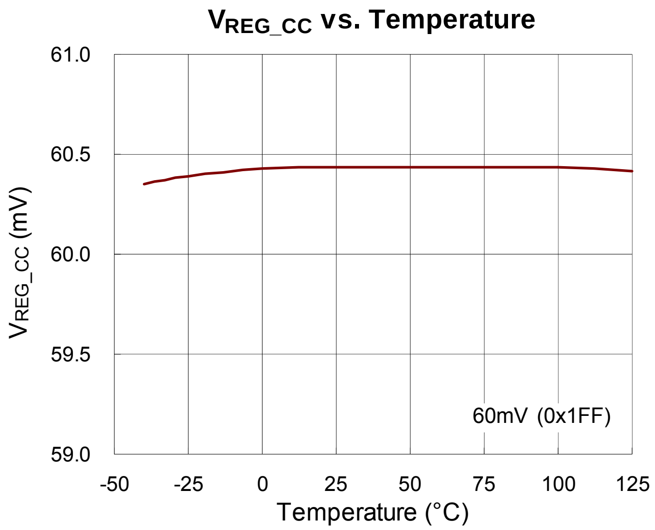

f_{OSC} vs. Temperature

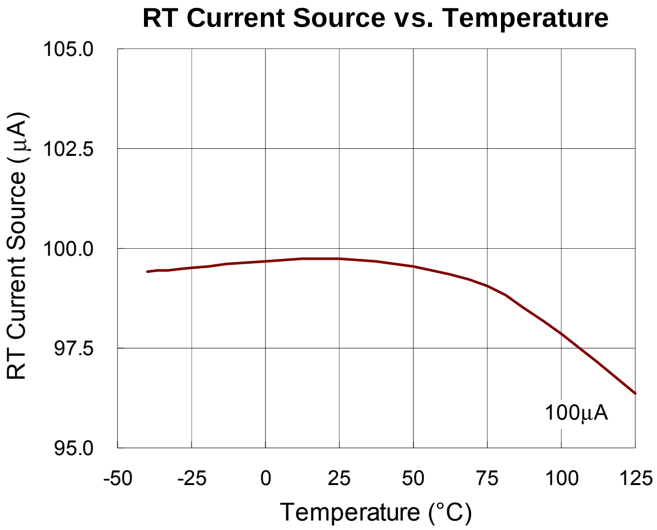

V_{REG_VO} vs. Temperature


V_{REG_VO} vs. Temperature


V_{REG_VO} vs. Temperature
20.60
20.30
20.00
19.70
19.40
V_{REG_VO} (V)
VO = 20V (0x355)
-50
-25
0
25
50
75
100
125
Temperature (°C)


V_{REG_CC} vs. Temperature
21.0
20.5
20.0
19.5
19.0
V_{REG_CC} (mV)
20mV (0xAB)
-50
-25
0
25
50
75
100
125
Temperature (°C)


V_{REG_CC} vs. Temperature
61.0
60.5
60.0
59.5
59.0
V_{REG_CC} (mV)
60mV (0x1FF)
-50
-25
0
25
50
75
100
125
Temperature (°C)


RT Current Source vs. Temperature
105.0
102.5
100.0
97.5
95.0
RT Current Source (μA)
100μA
-50
-25
0
25
50
75
100
125
Temperature (°C)

Application Information

Calculating Output Discharge Time

Figure 3 shows the functional block diagram of two built-in output bleeders at VBUS and BLD pins. The VBUS bleeder consists of an internal resistor (1.1kΩ typ.) and a pull-low MOSFET (Q_{BLD2}) for discharging the capacitors at VBUS side; the BLD bleeder consists of an external resistor (R_{BLD_EXT}) and a pull-low MOSFET (Q_{BLD1}) for discharging the capacitors at the output of the PWM converter. If the blocking MOSFETs (Q1A and Q1B) are on during discharging, the BLD bleeder with larger current capability dominates the discharge time. If the blocking MOSFETs are off, the discharge time (t_{DIS_CVBUS}) of the capacitor connected to the VBUS pin is determined by the following equation :

$$t_{DIS\_CVBUS} = R_{BLD\_INT} \times C_{VBUS} \times \ln\left(\frac{V_{BUS\_INI}}{V_{BUS\_FINAL}}\right)$$

where :

- R_{BLD_INT} is total internal resistance during on-state of the internal MOSFET Q_{BLD2}.
- C_{VBUS} is the total capacitance, coupled to the VBUS pin.
- V_{BUS_INI} is the initial bus voltage before the discharging.
- V_{BUS_FINAL} is the final bus voltage at end of the discharging.

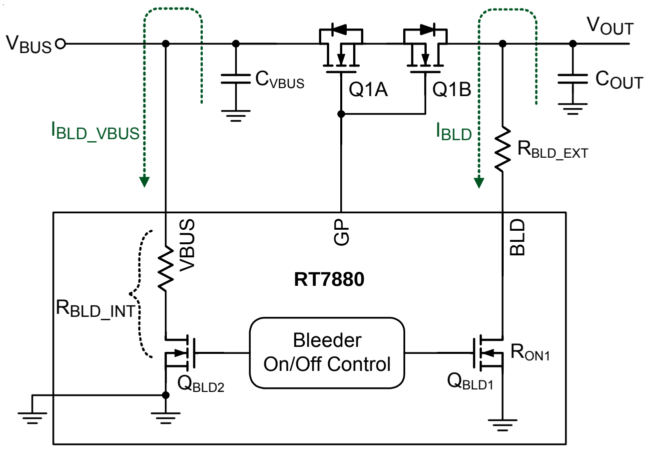


Figure 3.Functional diagram of the output bleeders

Similar to the operation of the VBUS bleeder, the discharge time (t_{DIS_COUT}) of the capacitor connected to the output of the PWM converter is determined by the following equation :

$$t_{DIS\_COUT} = (R_{BLD\_EXT} + R_{ON1}) \times C_{OUT} \times \ln\left(\frac{V_{OUT\_INI}}{V_{OUT\_FINAL}}\right)$$

where :

- R_{BLD_EXT} is resistance of the external resistor.
- R_{ON1} is on-resistance of the internal MOSFET Q_{BLD1}.
- C_{OUT} is the total capacitance connected to the output of the PWM converter.
- V_{OUT_INI} is the initial voltage of the PWM converter output before discharging.
- V_{OUT_FINAL} is the final voltage of the PWM converter output at end of discharging.

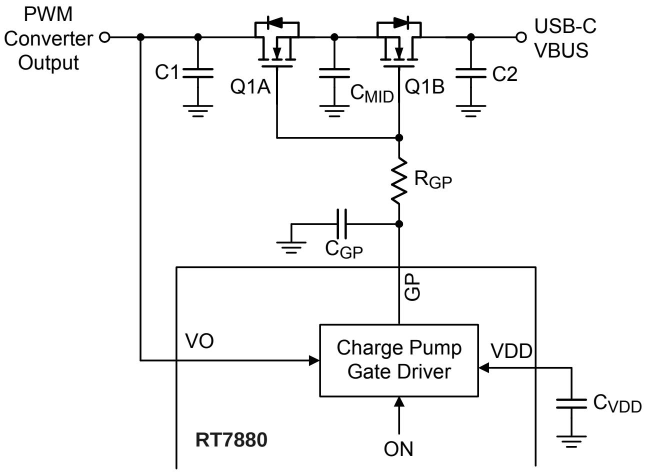


Figure 4. Functional diagram of the power-path control

Using Charge-Pump Gate Driver for Power-Path On/Off Control

Figure 4 shows the application schematic of a power-path on/off control. In this schematic, two N-channel MOSFETs of low on-resistance driven by a built-in gate driver, supplied by the charge pump, are employed to turn on or off the power-path between the PWM converter output and the USB-C VBUS terminal. If the internal control signal “ON” goes high, the GP voltage (V_{GP}) will be pulled high to turn on the power MOSFETs (Q1A and Q1B) and connect the power-path. If "ON" goes low, V_{GP} will be pulled low by a built-in MOSFET to disconnect the power-path.

Two power inputs (VO and VDD) are needed for the charge pump, and the VO pin must be connected the PWM converter output to ensure the power MOSFETs can be turned on successfully.

An optional MLCC capacitor (C_{GP}) can be used to reduce the V_{GP} rising rate and surge current in the power path when the power MOSFETs being switched on. When the power MOSFETs being switched off, the parasitic inductor and capacitors, C1 or C2, on the power path may cause voltage ringing at the drain of the Q1A or Q1B. An optional gate resistor (R_{GP}) can be added to reduce the falling rate of the power-path current and prevent voltage spikes. A 1μF MLCC capacitor (C_{MID}) between the source terminals to ground is necessary in order to prevent oscillation due to such dual-MOSFET connection.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (27.5°C/W) = 3.63W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

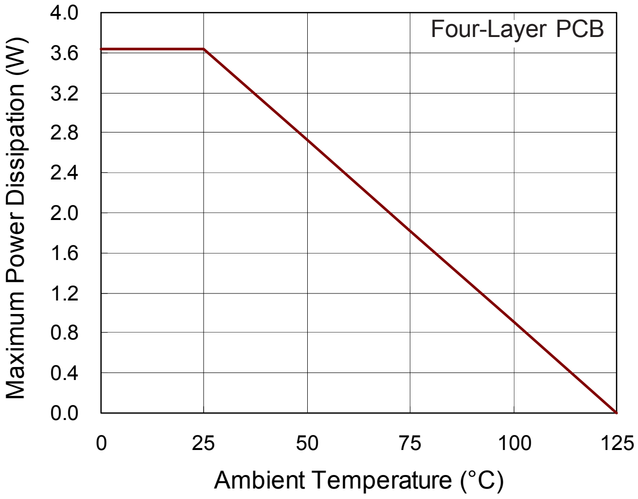


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

- Connect the IC GND pin and the exposed pad to a ground plane (IC-ground), and then connect the IC-ground to the USB GND terminals via a low-impedance path. The exposed pad is also used to dissipate the heat into PCB.
- Connect the decoupling MLCCs near the pins of VCONN, VDD, V2, PVDD and VBUS. Connect the MLCCs to the pins and IC-ground via low impedance paths.
- Connect the decoupling MLCC from the BOOT1/2 pin to the PHASE1/2 pin via a short and low-impedance path.
- Connect the PGND and PHASE1 pins to Source and Drain of low-side power MOSFET (controlled by LGATE1) via dedicated and low-impedance paths.
- Connect the PHASE2 and ZCD pins to Source and Drain of high-side power MOSFET (controlled by UGATE2) via dedicated and low-impedance paths.
- Connect the GNDCC pin to GND terminals of the USB Type-C connector via dedicated and low-impedance path.

- Connect the capacitor (between the CSOP and CSON pins) close to these pins. The paths of CSOP and CSON must be directly connected to the terminals of current-sense resistor (R_{CSO}) using Kelvin connections as shown in the layout in Figure 6.

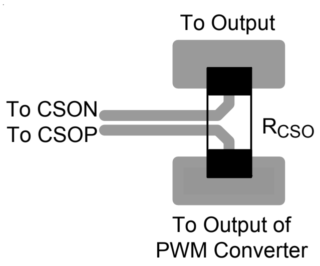


Figure 6. Kelvin connections for the R_{CSO}

- Figure 7 is a recommended placement of the PWM Buck-Boost power-stage. Two critical current-loop paths "from C_{IN1}→R_{CSI}→Q_A→Q_B to C_{IN1}" and "from C_{O1}→Q_D→Q_C to C_{O1}" must be as short as possible to minimize the switching noise at CSIP/VIN, CSIN, PHASE1, PHASE2 and ZCD pins. The short paths also reduce radiated EMI. It's necessary to use an MLCC (10µF/50V, X5R/X7R) for the input capacitor (C_{IN1}) and output capacitor (C_{O1}). For reducing input and output voltage ripples during heavy load operation, it is recommended to add more MLCCs or solid input and output capacitors. To improve heat dissipation, increase the PCB areas for Drains of high-side and low-side MOSFETs.
- Place the CV/CC loop compensation networks near the COMPV/COMPI pins and the IC-ground.

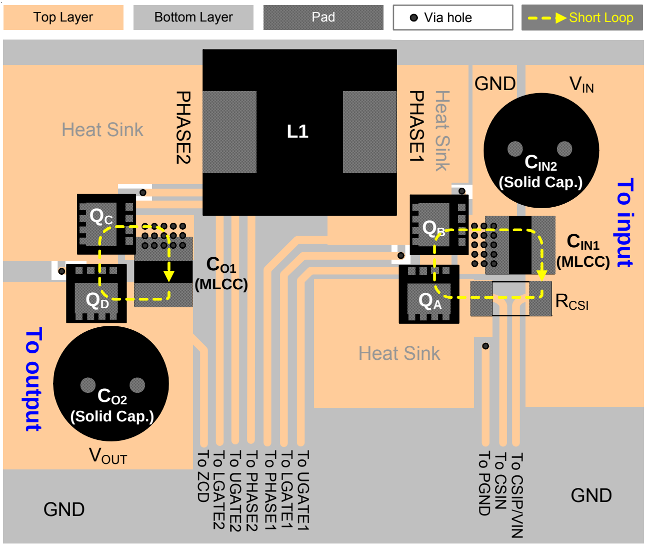


Figure 7. Recommended PCB layout of the power stage

- To prevent the switching noises, separate the following signals from the switching nodes and the switching-current paths connected with PHASE pin :
  - Input and output current-sense signals;
  - CC1 and CC2 signals;
  - CV-loop feedback signal;
  - CV and CC compensation networks.
- For improving ESD immunity, connect MLCCs close to the GND and VBUS terminals of the USB Type-C connector. Connect the capacitors to the USB VBUS and GND terminals through the low-impedance paths.

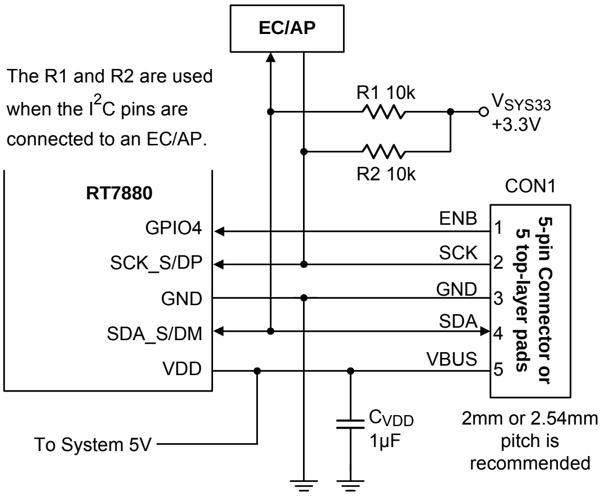


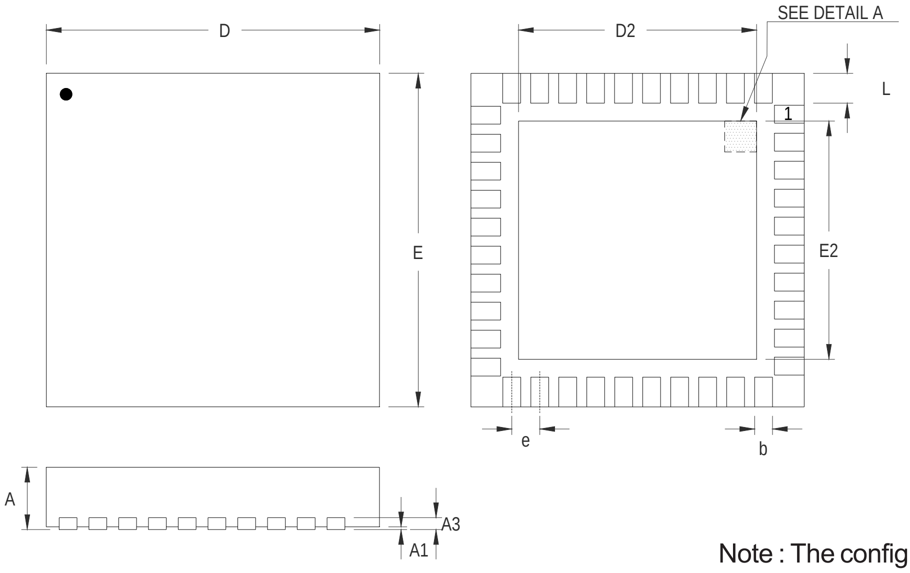
Figure 8. Connections for manual firmware updates

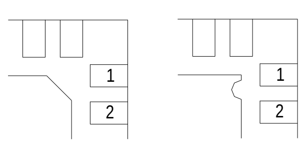
Manual Firmware Update

During product development stage, users might need to download or update the RT7880 firmware. This can be done by add a 5-pin connector (CON1) or five test pads on PCBs for updating the RT7880 firmware manually as shown in Figure 8. This connector is then connected to a "RT7800 firmware update fixture" by a 5-pin cable. The fixture is also connected to a PC via a Micro USB cable and acts as a bridge between the RT7880 and the PC. Therefore, users can download firmware to the RT7880 by using the RT7880 graphic user interface (GUI) installed in the PC. During the firmware update process, the fixture can supply current (up to 40mA) to the RT7880 and the system 5V via the VBUS pin of the 5-pin cable.

If the power from the fixture is enough to power the RT7880 and the system 5V, it's not necessary to use the input voltage of the system 5V; If the system 5V consumes more current than the fixture capability, please use the system input voltage.

Outline Dimension





DETAIL A

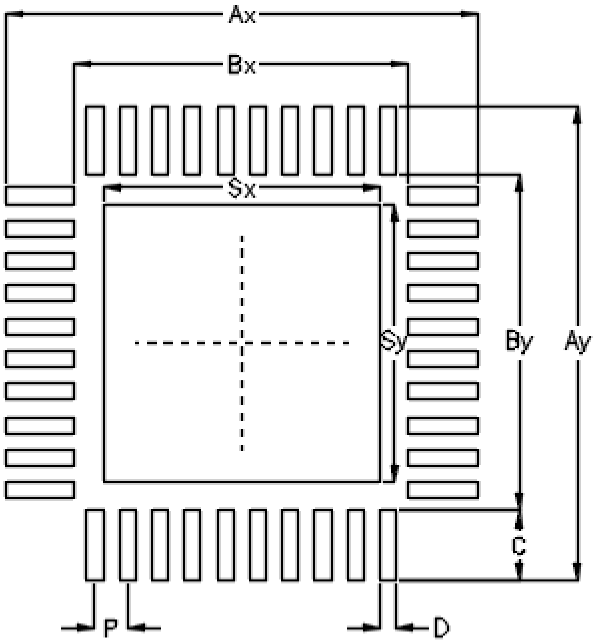
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-40	40	0.40	5.80	5.80	4.10	4.10	0.85	0.20	3.40	3.40	±0.05

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789