One Step Down DC/DC Converter and Four Linear Regulators with Individual On/Off Control

General Description

The RT8036 is an integrated power management unit which integrates one 600mA high efficiency step down DC/DC converter and four low dropout voltage regulators with 300mA current capability for each regulator.

The RT8036 is optimized for sub block power requirement solution. The individual on/off control for each device can provide flexibility for different power on sequence. Four linear regulators provide high PSRR output and are suitable for both analog and digital power.

The RT8036 is available in the WQFN-20L 3x3 package that is suitable for portable device.

Ordering Information

RT8036□□□

Package Type
QW : WQFN-20L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Output Voltage :
A : Buck : 1V
LDO1/2/3/4 : 1V/2.6V/3V/3.3V
B : Buck : 1.2V
LDO1/2/3/4 : 1.8V/2.8V/2.8V/2.8V
C : Buck : 1.3V
LDO1/2/3/4 : 1.8V/2.8V/2.8V/2.8V
D : Buck : 1.3V
LDO1/2/3/4 : 1.8V/2.8V/2.8V/3.0V
E : Buck : 1.3V
LDO1/2/3/4 : 1.8V/2.8V/2.8V/3.3V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

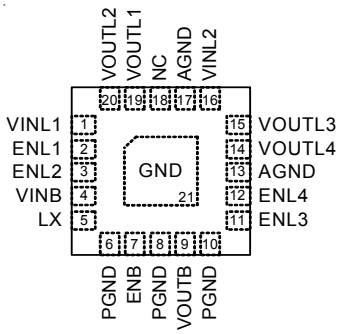
- **Four Low Noise LDOs for Up to 300mA**
- **One High Efficiency Synchronous Buck Up to 600mA Output**
- **Individual On/Off Control for Each Output**
- **Small 20-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Smart Handheld device
- Cellular phone

Pin Configurations

(TOP VIEW)

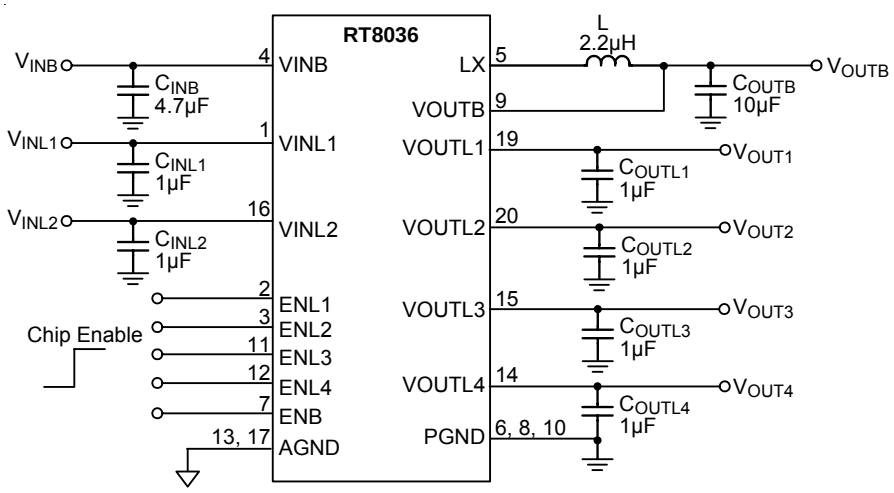


WQFN-20L 3x3

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

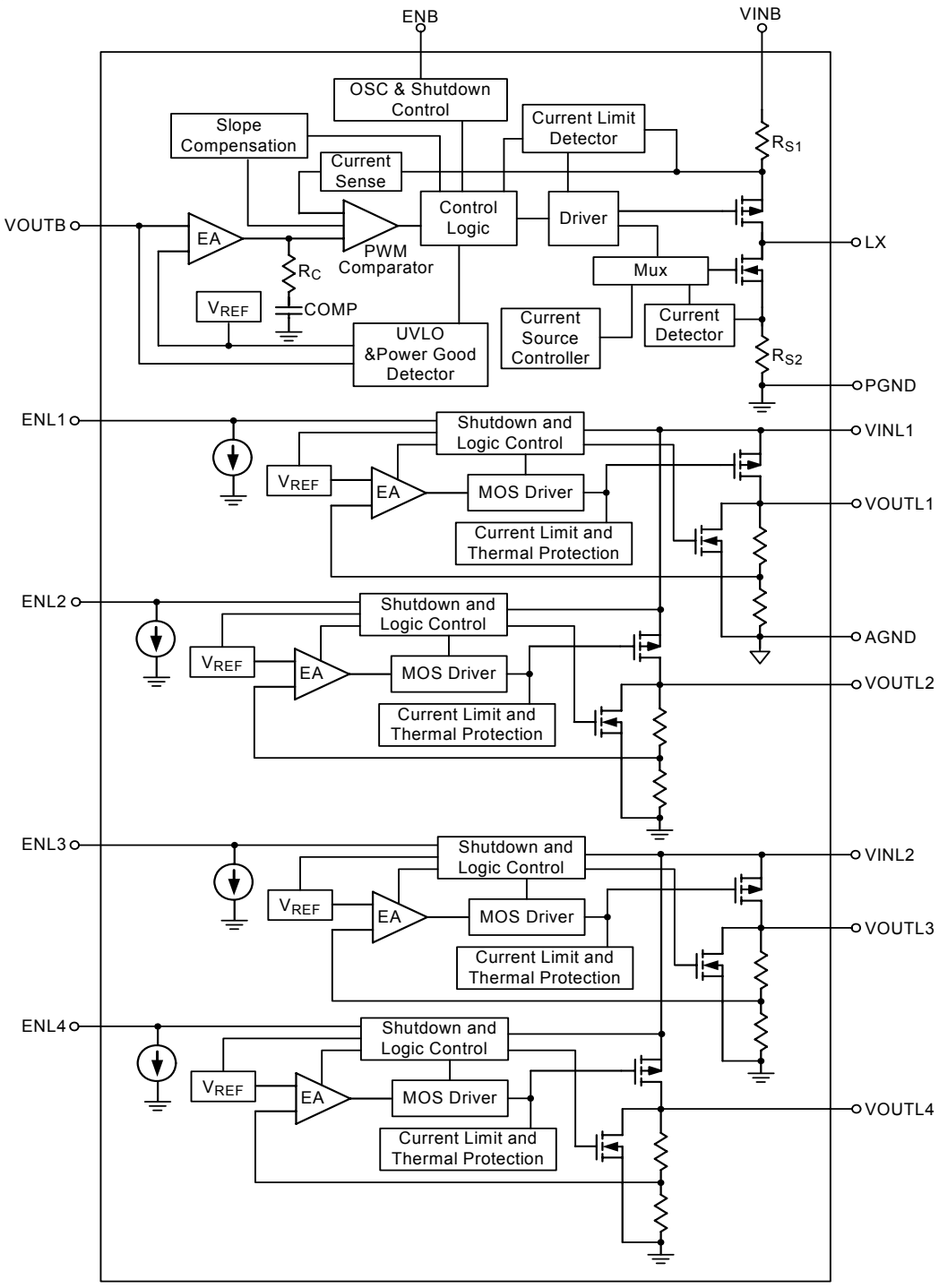
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VINL1	Supply Input for LDO1 and LDO2.
2	ENL1	Chip Enable for LDO1 (Active High).
3	ENL2	Chip Enable for LDO2 (Active High).
4	VINB	Supply Input for Buck Converter.
5	LX	Power Switching Output.
6, 8, 10	PGND	Power Ground.
7	ENB	Chip Enable for Buck Converter (Active High).
9	VOUTB	Feedback Input of Buck Converter.
11	ENL3	Chip Enable for LDO3 (Active High).
12	ENL4	Chip Enable for LDO4 (Active High).
13, 17	AGND	Analog Ground.
14	VOUTL4	LDO4 Output.
15	VOUTL3	LDO3 Output.
16	VINL2	Supply Input for LDO3 and LDO4.
18	NC	No Internal Connection.
19	VOUTL1	LDO1 Output.
20	VOUTL2	LDO2 Output.
21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Buck Supply Input Voltage, V_{INB} ---------- –0.3V to 6.5V
- ENB, VOUTB Voltage ---------- –0.3V to V_{INB}
- LDO1, LDO2 Supply Input Voltage, V_{INL1}, V_{INL2} ---------- –0.3V to 6V
- ENL1 to ENL4, VOUT1 to VOUT4 Voltage ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN–20L 3x3 ---------- 1.471W
- Package Thermal Resistance (Note 2)
  WQFN–20L 3x3, θ_{JA} ---------- 68°C/W
  WQFN–20L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 165°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{INB}, V_{INL1}, V_{INL2} ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{INB} = 3.6V, V_{INLx} = V_{OUTLx} + 0.7V, V_{ENLx} = V_{INLx}, C_{INB} = 4.7µF, C_{OUTB} = 10µF, C_{INLx} = C_{OUTLx} = 1µF, L = 2.2µH, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Buck Converter						
Input Voltage Range	V_{INB}		2.5	--	5.5	V
Quiescent Current	I_{QB}	I_{OUTB} = 0mA,	--	40	60	µA
Shutdown Current	I_{SHDNB}	ENB = GND	--	0.1	0.9	µA
Output Voltage Accuracy	ΔV_{OUTB}	V_{INB} = V_{OUTB} + ΔV to 5.5V V_{IN} > 2.5V which ever is larger. (Note 5)	–3	--	3	%
VOUTB Pin Input Current	I_{OUTB}	V_{OUTB} = V_{INB}	–50	--	50	nA
$R_{DS(ON)}$ of P-MOSFET	$R_{DS(ON)\_P}$	I_{OUTB} = 200mA, V_{INB} = 3.6V	0.1	0.28	0.6	Ω
		I_{OUTB} = 200mA, V_{INB} = 2.5V	0.1	0.38	0.6	Ω
$R_{DS(ON)}$ of N-MOSFET	$R_{DS(ON)\_N}$	I_{OUTB} = 200mA, V_{INB} = 3.6V	0.1	0.25	0.55	Ω
		I_{OUTB} = 200mA, V_{INB} = 2.5V	0.1	0.35	0.55	Ω
P-Channel Current Limit	I_{LIM_P}	V_{INB} = 2.5V to 5.5V	600	1800	2500	mA
ENB High-Level Input Voltage	V_{ENB_H}	V_{INB} = 2.5V to 5.5V	1.5	--	VINB	V
ENB Low-Level Input Voltage	V_{ENB_L}	V_{INB} = 2.5V to 5.5V	--	--	0.4	V
Under Voltage Lock Out	UVLO		--	1.8	--	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Lockout Hysteresis	UVLO_Hys		0.05	0.1	0.35	V
Oscillator Frequency	f_{OSC}	V_{INB} = 3.6V, I_{OUTB} = 100mA	--	1.5	--	MHz
Thermal Shutdown Temperature	T_{SDB}		--	160	--	°C
Maximal Duty Cycle			100	--	--	%
LX Leakage Current		V_{INB} = 3.6V, V_{LX} = 0V or V_{LX} = 3.6V	1	--	100	μA
LDO						
LDO Input Voltage		V_{INL} = 2.5V to 5.5V	2.5	--	5.5	V
Quiescent Current	I_{QL}	V_{ENL} > 1.5V	--	50	80	μA
Shutdown Current	I_{QL_SD}	V_{ENL} < 0.4V	--	0.1	0.8	μA
Dropout Voltage (Note 5)	V_{DROP}	I_{OUTL} = 300mA	--	330	500	mV
VOUTL Accuracy	ΔV	I_{OUTL} = 1mA	−3	--	3	%
Line Regulation	ΔV_{LINE}	V_{IN} = 2.5V to 5.5V	0	0.02	0.2	%/V
Load Regulation	ΔV_{LOAD}	1mA < I_{OUTL} < 300mA	0	0.1	0.6	%
Current Limit	I_{LIM}	R_{LOAD} = 1Ω	330	430	600	mA
ENL Threshold	V_{IHL}	V_{INL} = 2.5V to 5.5V, Power On	1.5	--	--	V
	V_{ILL}	V_{INL} = 2.5V to 5.5V, Shutdown	--	--	0.4	V
Output Voltage TC			--	100	--	ppm/°C
VOUTL Discharge Resistance in Shutdown		V_{IN} = 5V, EN1 = EN2 = GND	--	20	--	Ω
Thermal Shutdown	T_{SDL}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SDL}		--	30	--	°C
PSRR V_{INL} = V_{OUTL} + 1V C_{OUTL} = 2.2μF I_{LOAD} = 50mA	PSRR	f = 100Hz, I_{LOAD} = 10mA	--	65	--	dB
		f = 1kHz, I_{LOAD} = 10mA	--	60	--	
		f = 10kHz, I_{LOAD} = 10mA	--	50	--	
		f = 100Hz, I_{LOAD} = 150mA	--	65	--	
		f = 1kHz, I_{LOAD} = 150mA	--	50	--	
		f = 10kHz, I_{LOAD} = 150mA	--	50	--	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

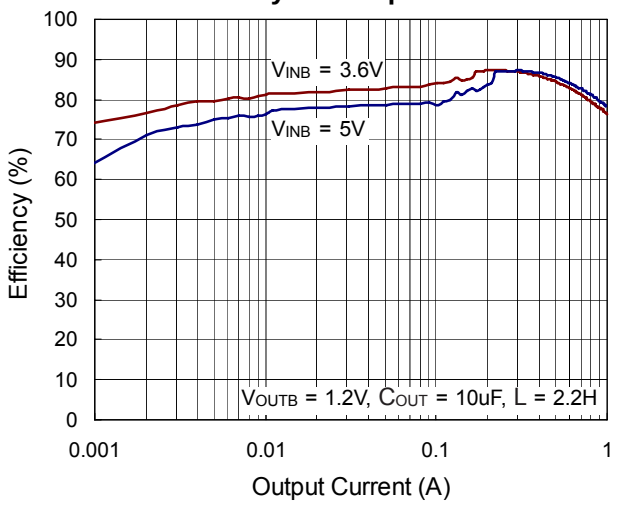
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. $\Delta V = I_{OUT} \times R_{DS(ON)\_P}$

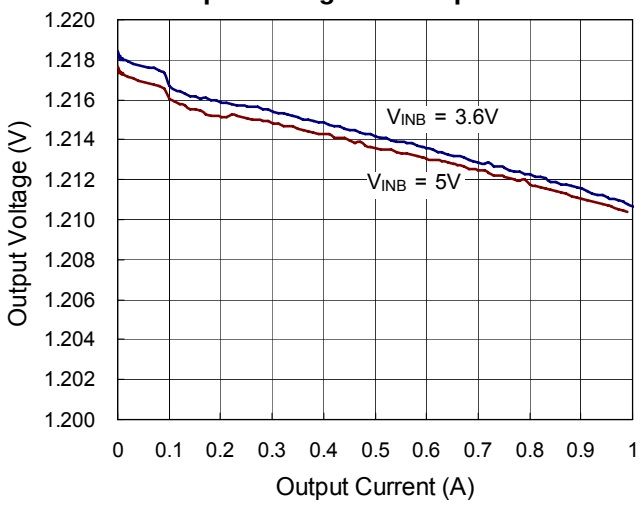
Typical Operating Characteristics

For Buck

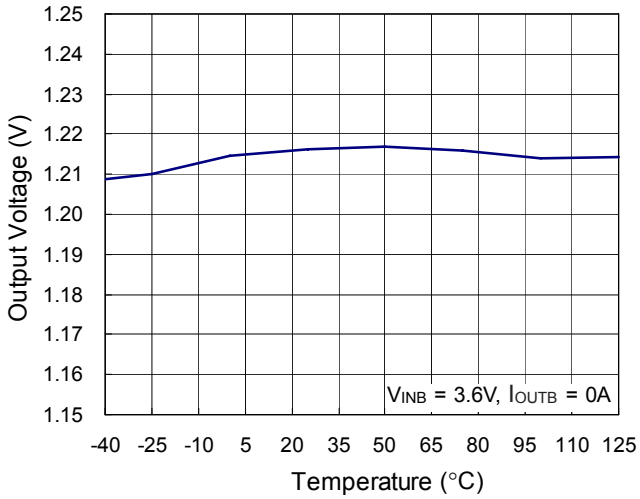
Efficiency vs. Output Current



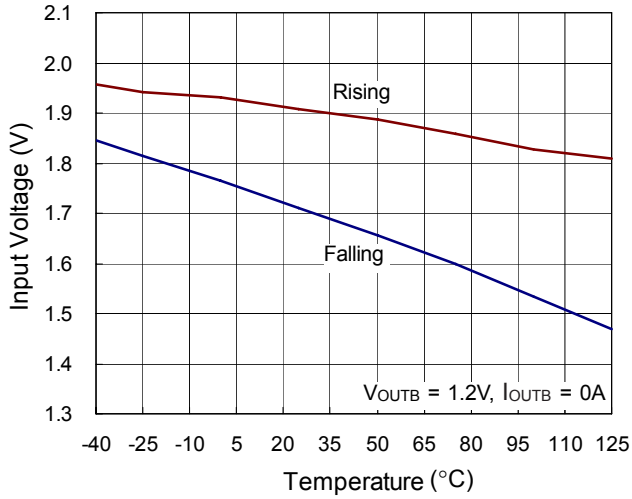
Output Voltage vs. Output Current



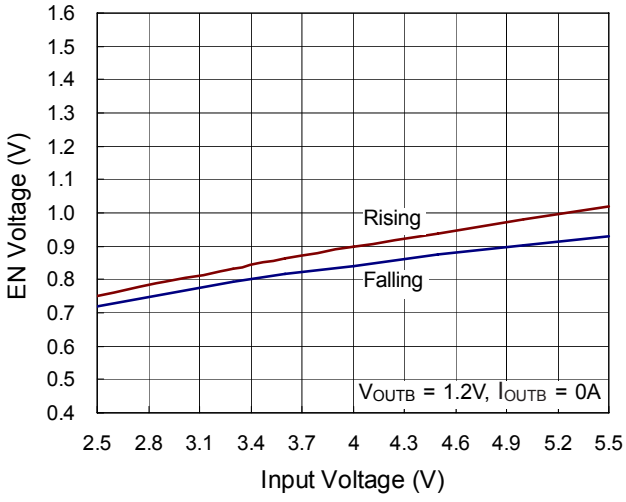
Output Voltage vs. Temperature



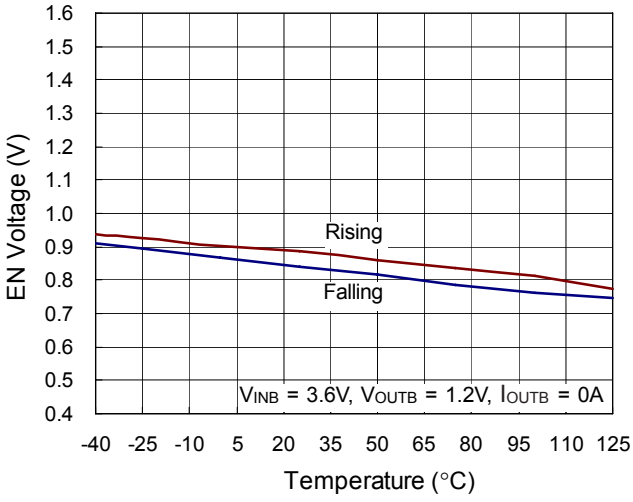
UVLO Threshold vs. Temperature



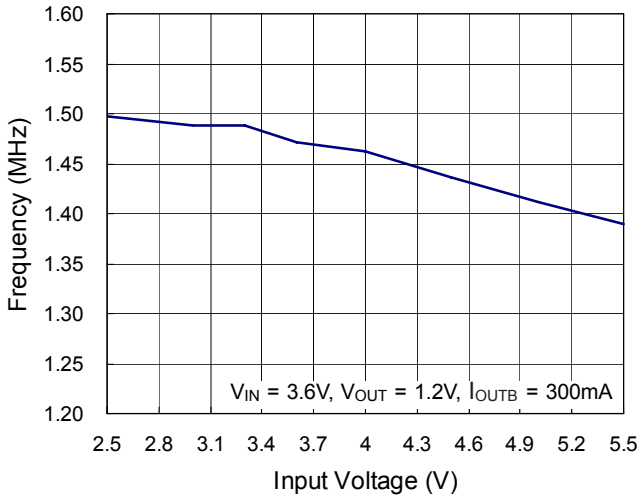
EN Threshold vs. Input Voltage



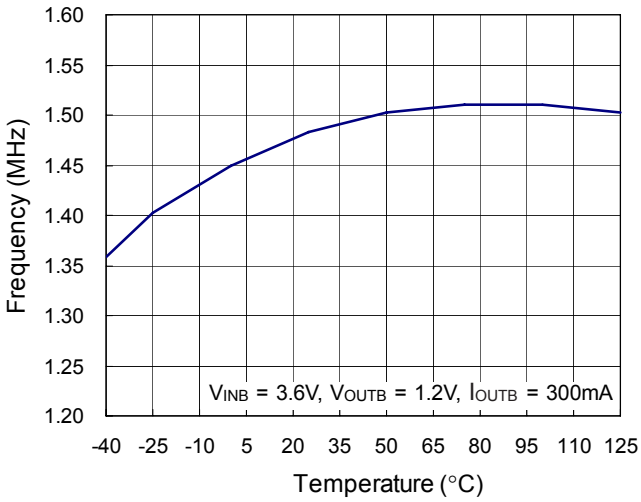
EN Threshold vs. Temperature



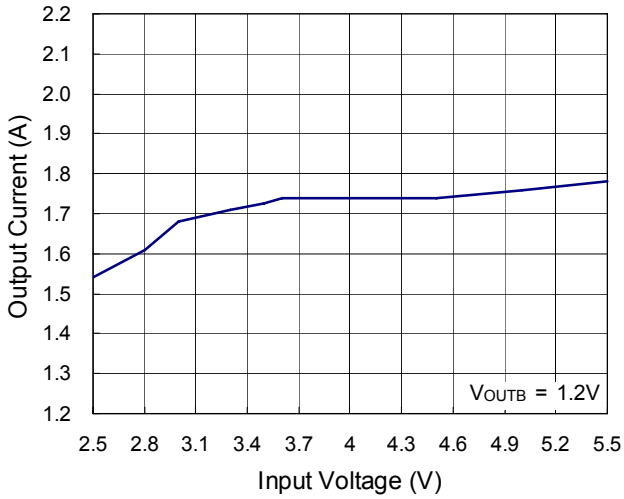
Frequency vs. Input Voltage



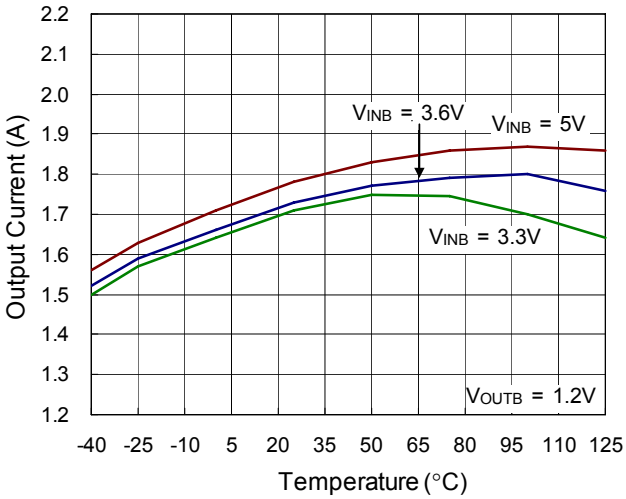
Frequency vs. Temperature



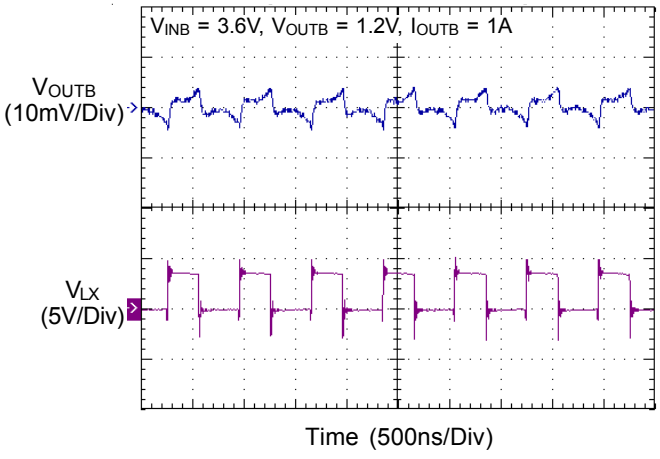
Current Limit vs. Input Voltage



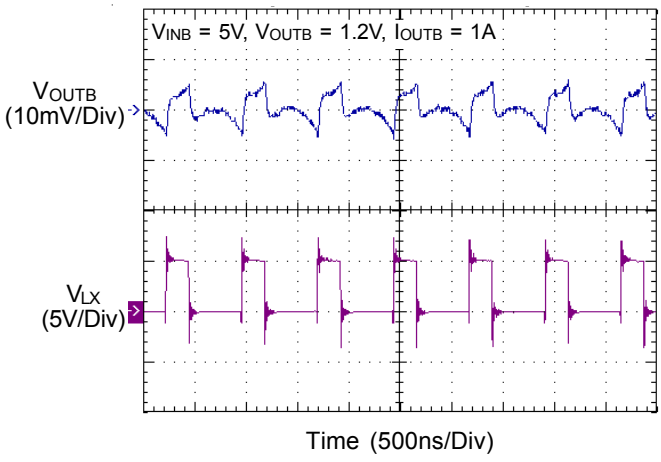
Current Limit vs. Temperature



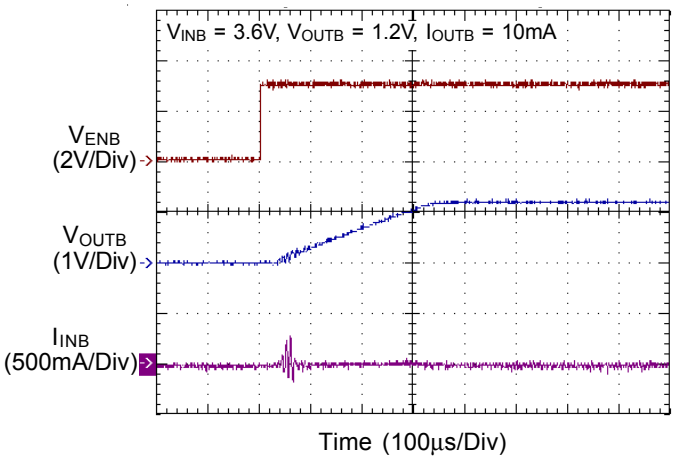
Output Ripple Voltage



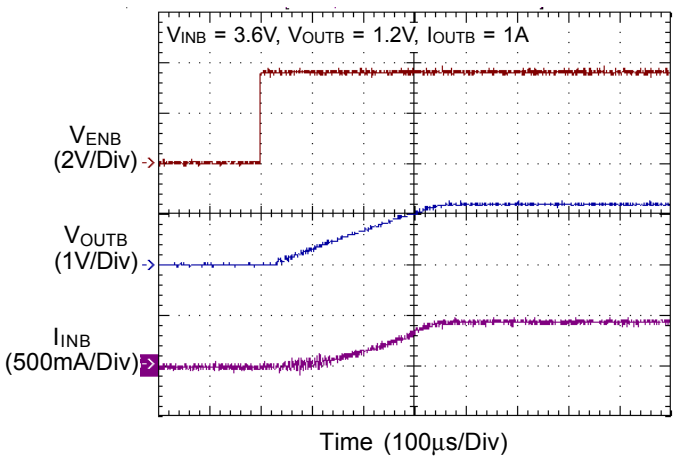
Output Ripple Voltage



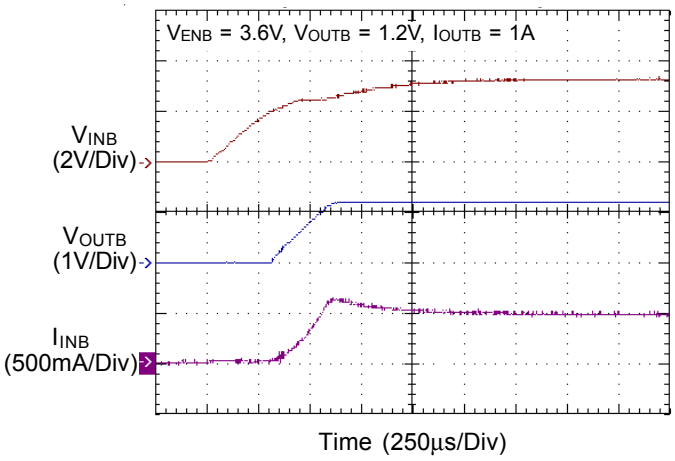
Power On from EN



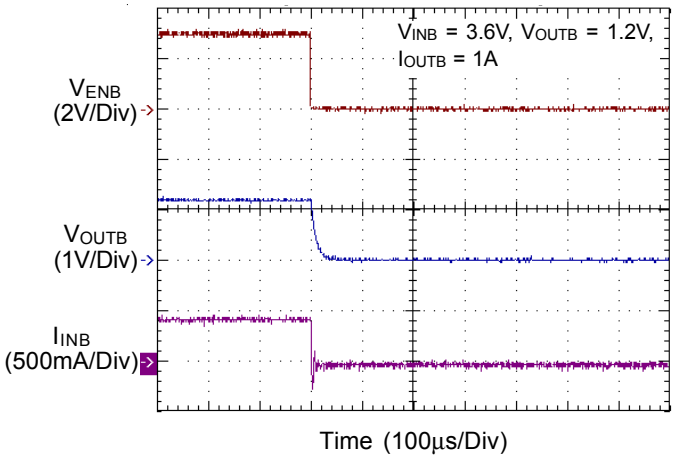
Power On from EN



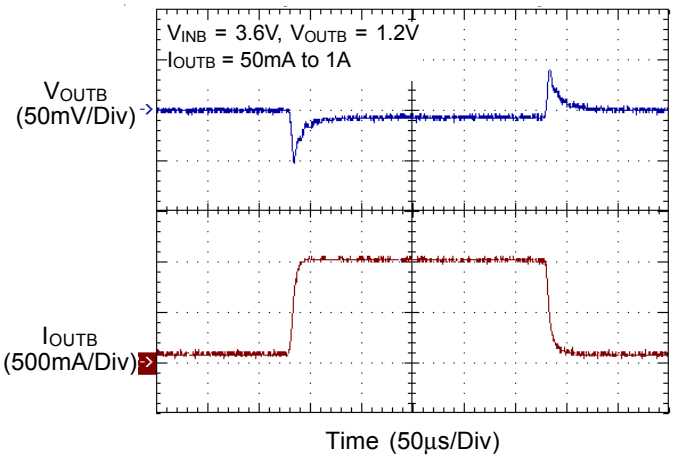
Power On from VIN



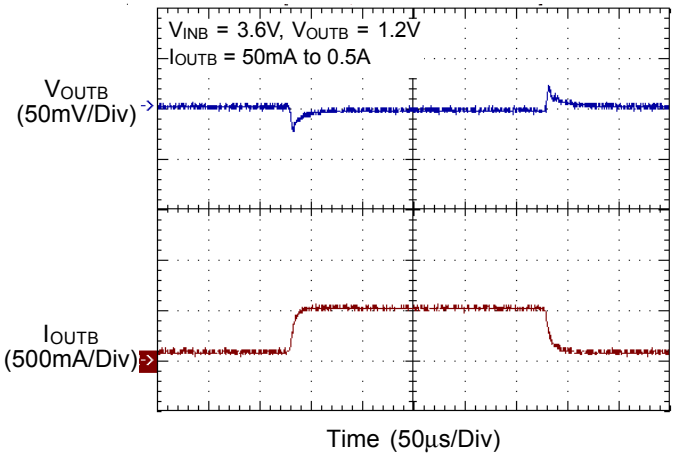
Power Off from EN



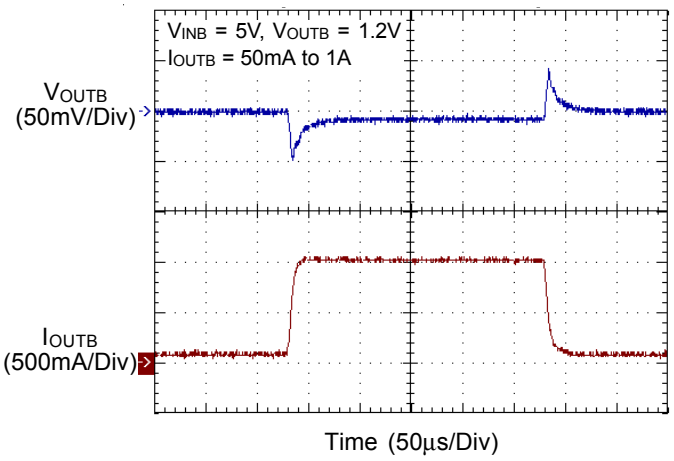
Load Transient Response



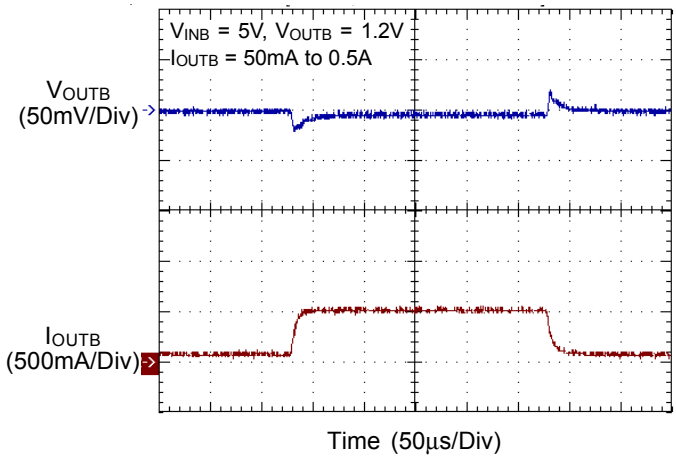
Load Transient Response



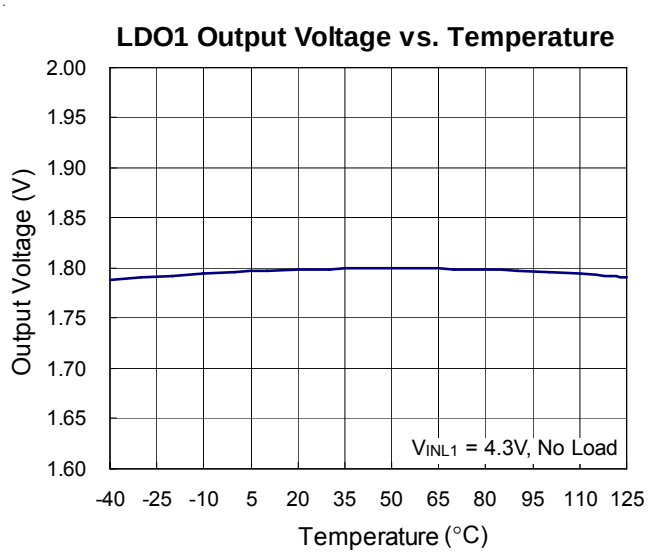
Load Transient Response

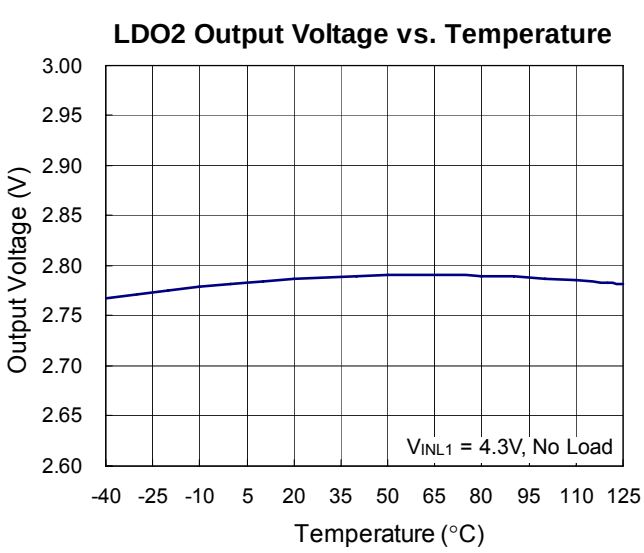


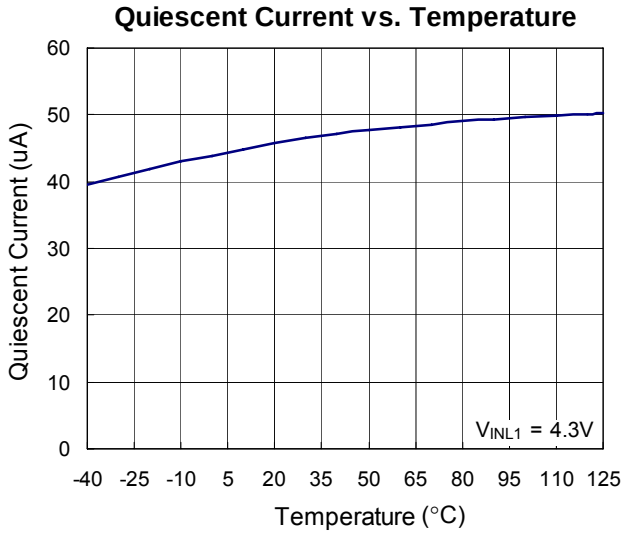
Load Transient Response

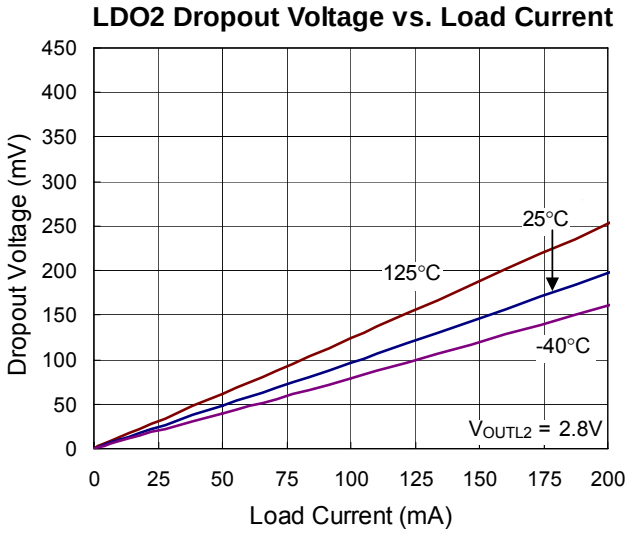


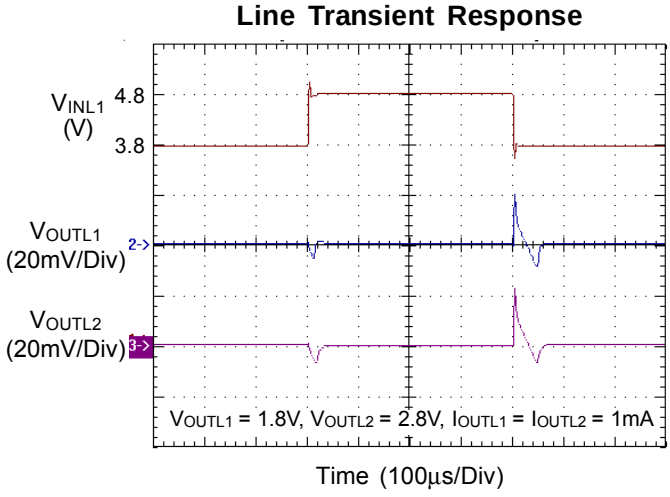
For LDO

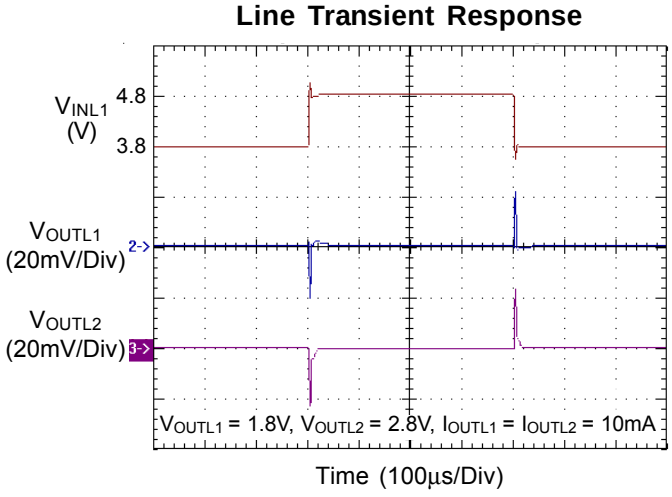

LDO1 Output Voltage vs. Temperature
Output Voltage (V)
2.00
1.95
1.90
1.85
1.80
1.75
1.70
1.65
1.60
VINL1 = 4.3V, No Load
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)


LDO2 Output Voltage vs. Temperature
Output Voltage (V)
3.00
2.95
2.90
2.85
2.80
2.75
2.70
2.65
2.60
VINL1 = 4.3V, No Load
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)

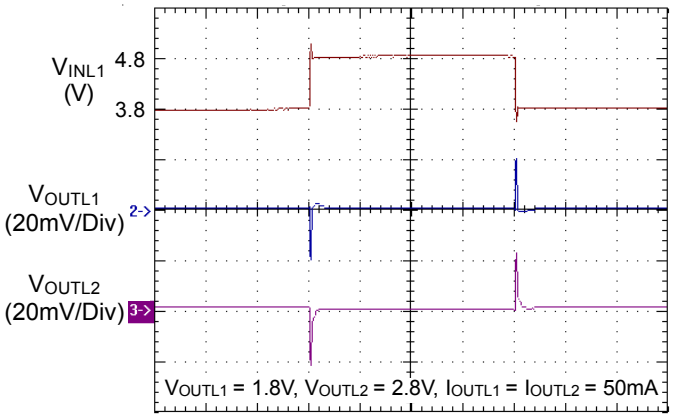

Quiescent Current vs. Temperature
Quiescent Current (uA)
60
50
40
30
20
10
0
VINL1 = 4.3V
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)


LDO2 Dropout Voltage vs. Load Current
Dropout Voltage (mV)
450
400
350
300
250
200
150
100
50
0
25°C
125°C
-40°C
VOUTL2 = 2.8V
0 25 50 75 100 125 150 175 200
Load Current (mA)

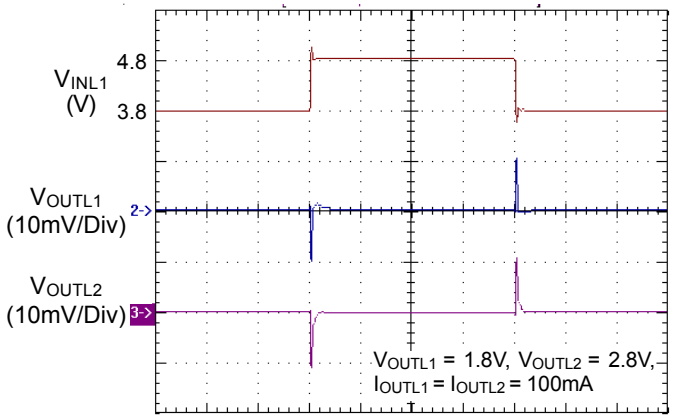

Line Transient Response
VINL1 (V)
4.8
3.8
VOUTL1 (20mV/Div)
VOUTL2 (20mV/Div)
VOUTL1 = 1.8V, VOUTL2 = 2.8V, IOUTL1 = IOUTL2 = 1mA
Time (100µs/Div)


Line Transient Response
VINL1 (V)
4.8
3.8
VOUTL1 (20mV/Div)
VOUTL2 (20mV/Div)
VOUTL1 = 1.8V, VOUTL2 = 2.8V, IOUTL1 = IOUTL2 = 10mA
Time (100µs/Div)

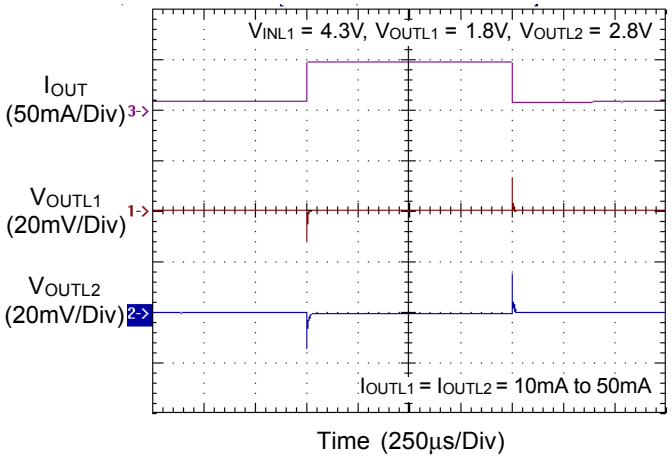
Line Transient Response



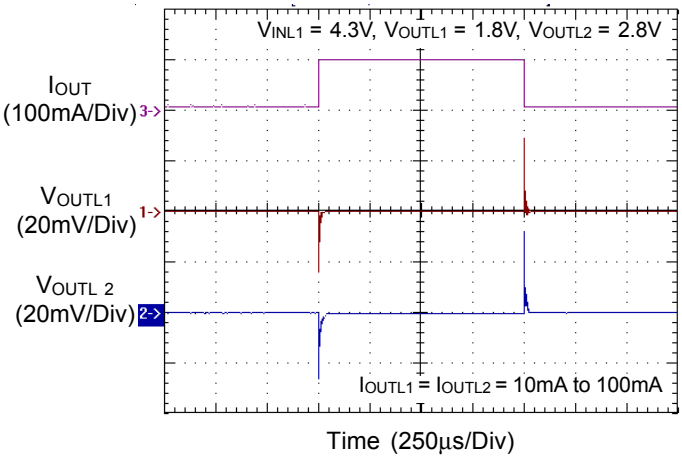
Line Transient Response



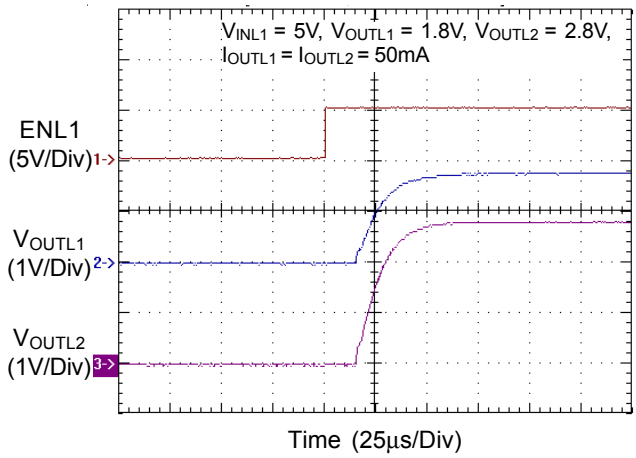
Load Transient Response



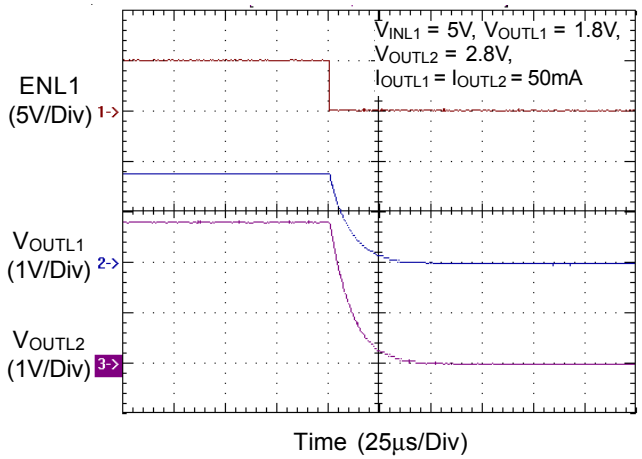
Load Transient Response



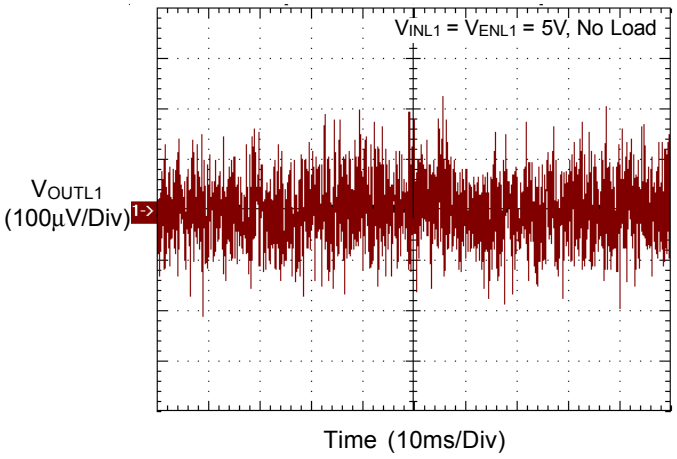
Power On from ENL1



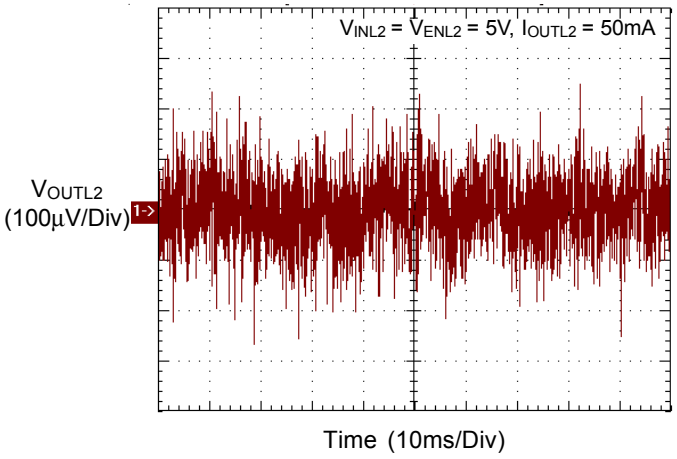
Power Off from ENL1



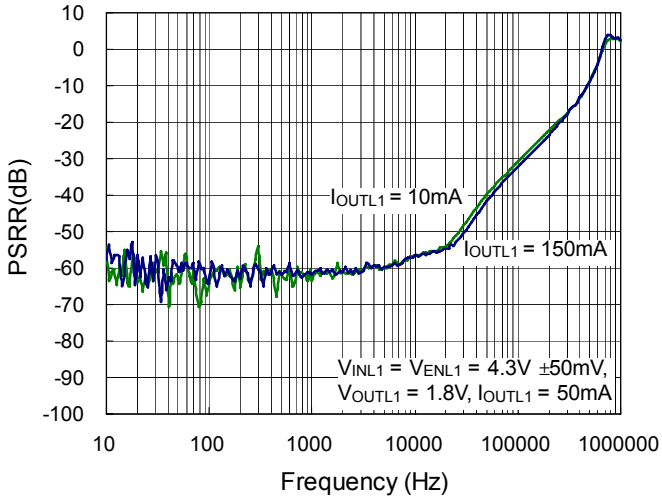
Noise



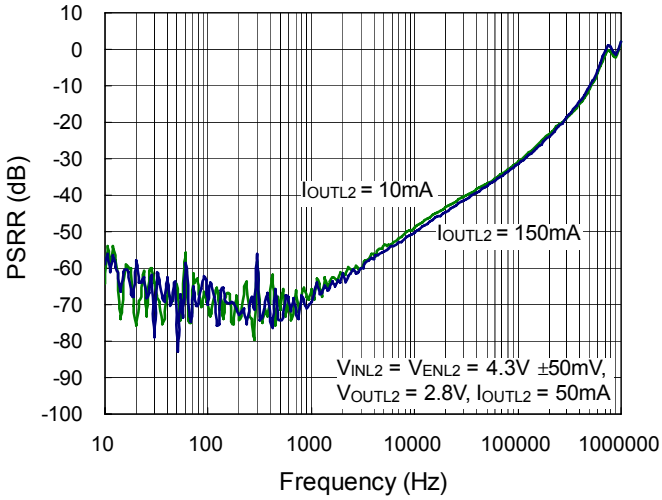
Noise



VOUTL1 PSRR



VOUTL2 PSRR



Application Information

The RT8036 is an integrated power management IC including one Buck converter and four linear regulators.

The RT8036 features a fixed output voltage to eliminate the need of external feedback resistors and simplify the PCB layout. The RT8036 fix the output voltage by internal resistor and keep the output voltage between -3% to 3%. Please refer to the ordering information for detailed output voltage setting.

Buck Enable Control

Pull the ENB pin (>1.5V) to turn on the buck converter and to pull low the ENB pin (<0.4V) to turn off the buck converter.

Soft-Start

The RT8036 has a soft-start to control the output voltage rise time and limit the current surge at the startup. The soft-start will begin while EN rises above high threshold.

Buck Current Limiting

A current limit feature allows the RT8036 to protect itself and external components during overload conditions. In operating mode, the inductor peak current under 600mA is normally used. The current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current, ΔI_L, increases with higher V_{INB} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is ΔI_L = 0.4 (I_{MAX}). The largest ripple current occurs at the highest VINB. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements.

C_{INB} and C_{OUTB} Selection

The input capacitance, C_{INB}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUTB(MAX)} \frac{V_{OUTB}}{V_{INB}} \sqrt{\frac{V_{INB}}{V_{OUTB}} - 1}$$

This formula has a maximum at V_{INB} = 2V_{OUTB}, where I_{RMS} = I_{OUTB}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUTB} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUTB}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since DIL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VINB. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VINB large enough to damage the part.

LDO Capacitor Selection

Like any low-dropout regulator, the external capacitors used with the RT8036 must be carefully selected for regulator stability and performance. Using a capacitor whose value is >1μF on the RT8036 input and the amount of capacitance can be increased without limit. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT8036 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 20mΩ on the RT8036 output ensures stability. The RT8036 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the output pin of the RT8036 and returned to a clean analog ground.

LDO Enable

The LDO of RT8036 goes into shutdown mode when the ENL1, ENL2, ENL3 and ENL4 pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to be lower than 1μA. The ENL1, ENL2, ENL3 and ENL4 pin can be directly tied to VINL1 and VINL2 to keep the part on.

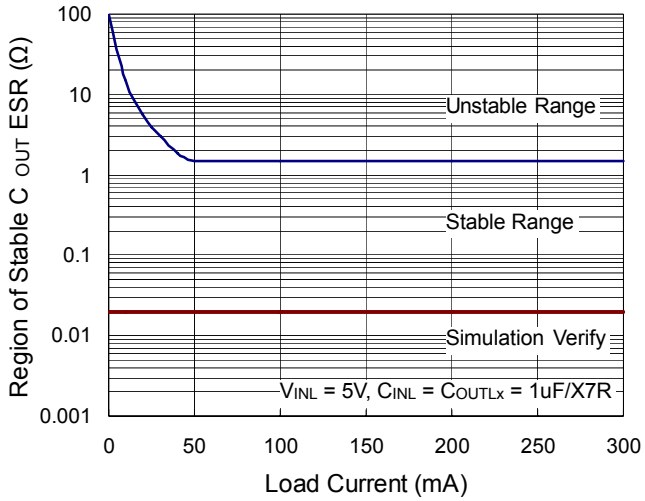


Figure 1. Stable Region of Output Capacitor ESR

LDO Current limit

The RT8036 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 460mA (typ.). The output can be shorted to ground indefinitely without damaging the part.

Thermal Shutdown Protection

As the die temperature reaches a certain thermal shutdown threshold, the chip will enter protection mode. The power MOSFET will turn-off during protection mode to prevent abnormal operation.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8036, The maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-20L 3x3 packages, the thermal resistance θ_{JA} is 68°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) =1.471W for WQFN-20L 3x3 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . For RT8036 packages, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

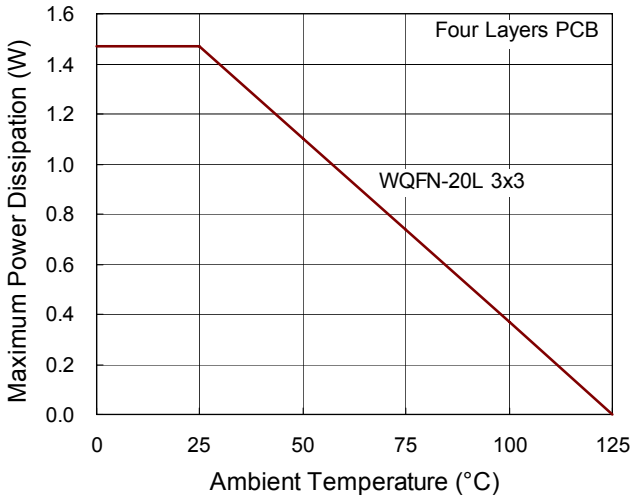


Figure 2. Derating Curves for RT8036 Packages

Layout Consideration

The RT8036 is an integrated power management unit which integrates one 1A high efficiency step down DC/DC converter and four low dropout voltage regulators with 300mA current capability for each regulator. Careful PCB layout is necessary. For best performance, place all peripheral components as close to the IC as possible. A short connection is highly recommended. The following guidelines should be strictly followed when designing a PCB layout for the RT8036.

- Input capacitor should be placed close to IC and connected to ground plane. The trace of input in the PCB should be placed far away from the sensitive devices or shielded by the ground.

- The GND should be connected to a strong ground plane for heat sinking and noise protection.
- The inductor should be placed close to LX pin and connected to output capacitor. The trace of input in the PCB should be placed far away from the sensitive devices or shielded by the ground.
- Output capacitor should be placed close to inductor and connected to ground plane to reduce noise coupling.

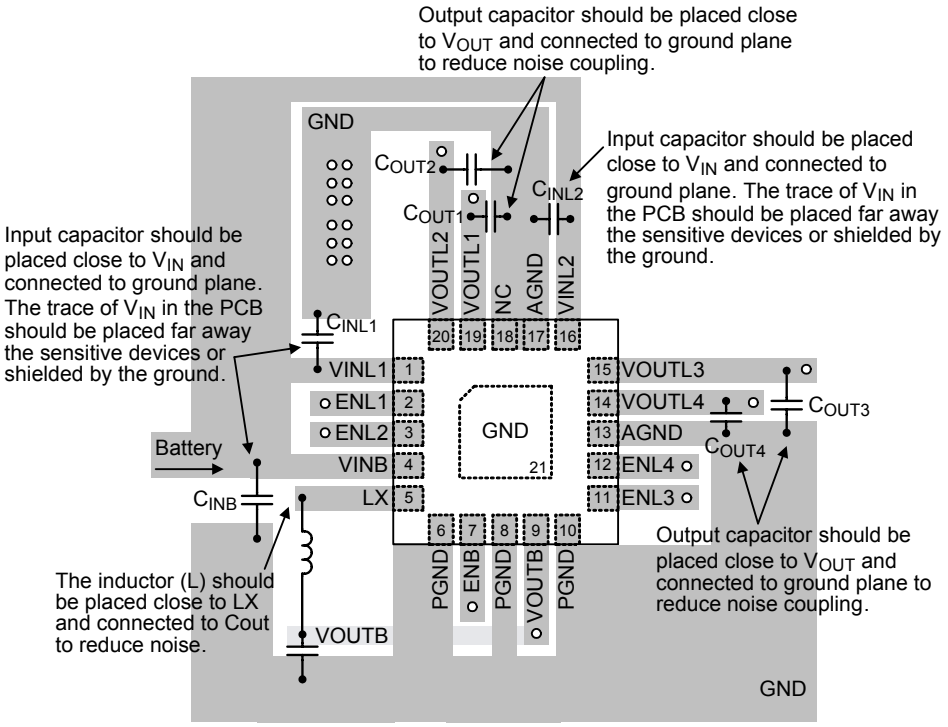
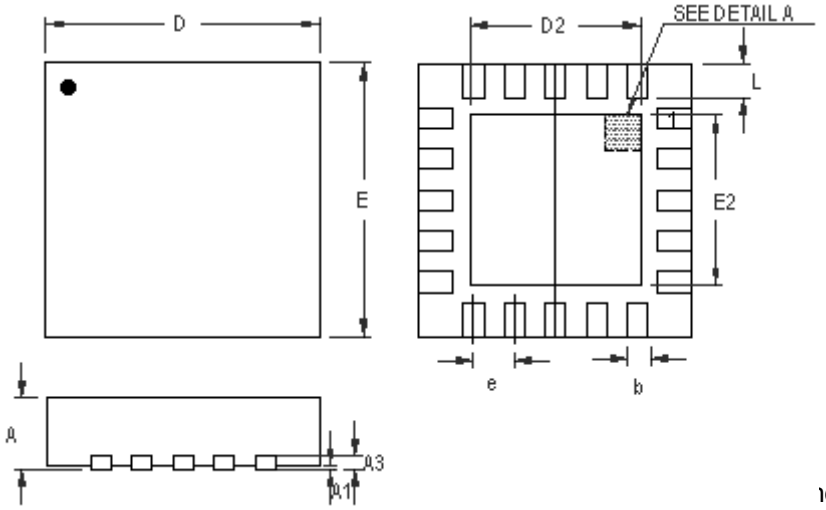
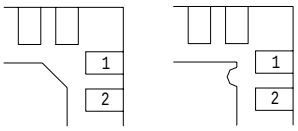


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

ıe configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
D2	1.650	1.750	0.065	0.069
E	2.950	3.050	0.116	0.120
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

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