Single Phase VR11.1 PWM Controller with 7-bit VID

General Description

The RT8113 is a single-phase PWM buck controller with one integrated MOSFET driver for advanced microprocessor applications such as Atom V_{CORE} or Ibexpeak Graphic Power. This controller maintains the same features as the multi-phase product family. However, it reduces the output to one phase for lower current systems. Features of this controller include adjustable operation frequency, power good indication, external error amplifer compensation, over voltage protection, over current protection, droop enable/disable capability, externally adjustable offset voltage, load transient enhancement (quick response), and enable/shutdown pin to achieve optimal power management solution for various applications. The RT8113 comes in a WQFN-24L 4x4 package.

Ordering Information

RT8113 □ □

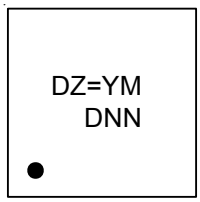
- Package Type
  QW : WQFN-24L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



DZ= : Product Code

YMDNN : Date Code

Features

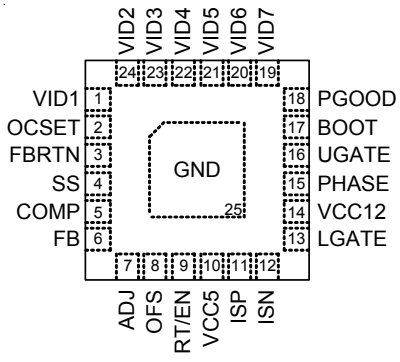
- **Single-Phase Power Conversion**
- **One Embedded MOSFET Driver with Internal Bootstrap Diode**
- **VID Table for Intel VR11.1**
- **Continuous Differential Inductor DCR Current Sense**
- **Droop Enable/Disable Capability**
- **Adjustable Soft-Start**
- **Adjustable Frequency Typically at 200kHz**
- **Power Good Indication**
- **Adjustable Over Current Protection**
- **Over Voltage Protection**
- **Over Temperature Protection**
- **Small 24-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Atom V_{CORE} Power
- Ibexpeak Graphic Power
- Low Voltage, High Current DC/DC Converter

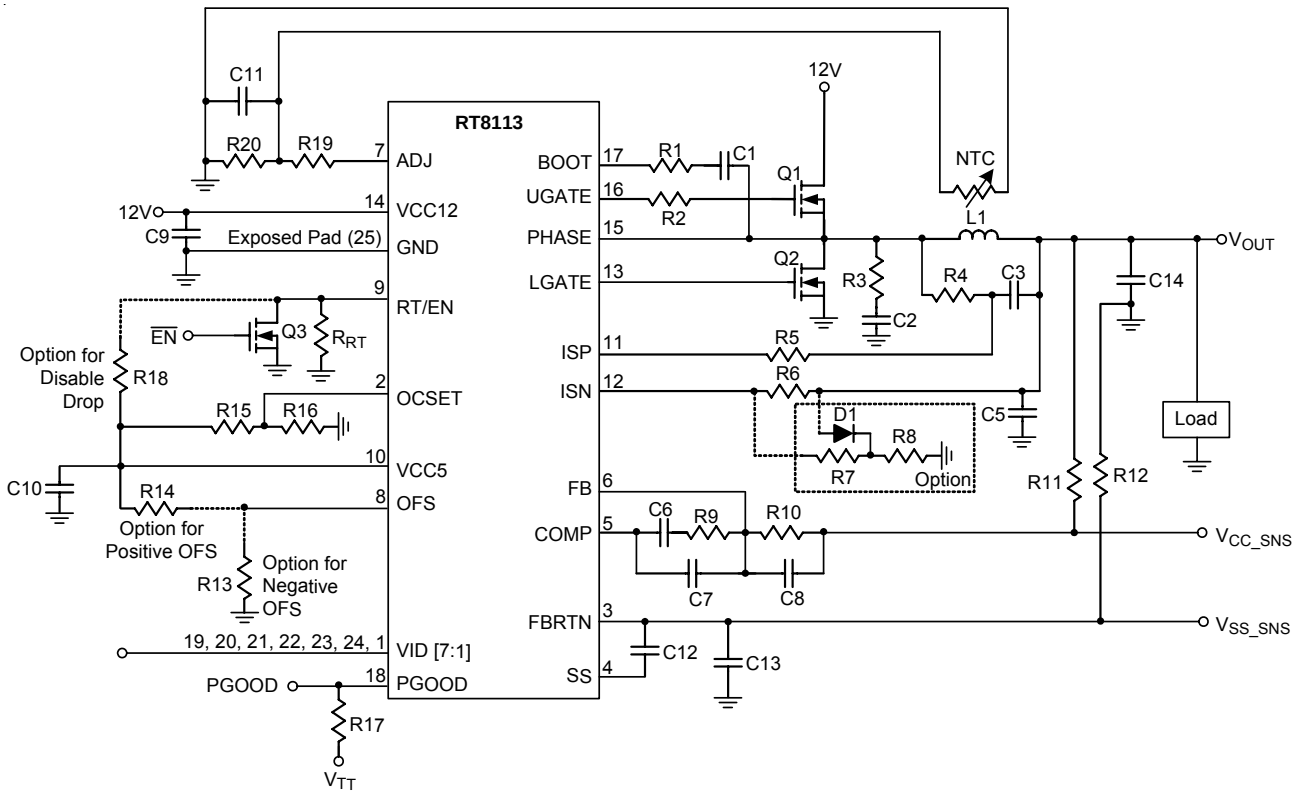
Pin Configurations

(TOP VIEW)

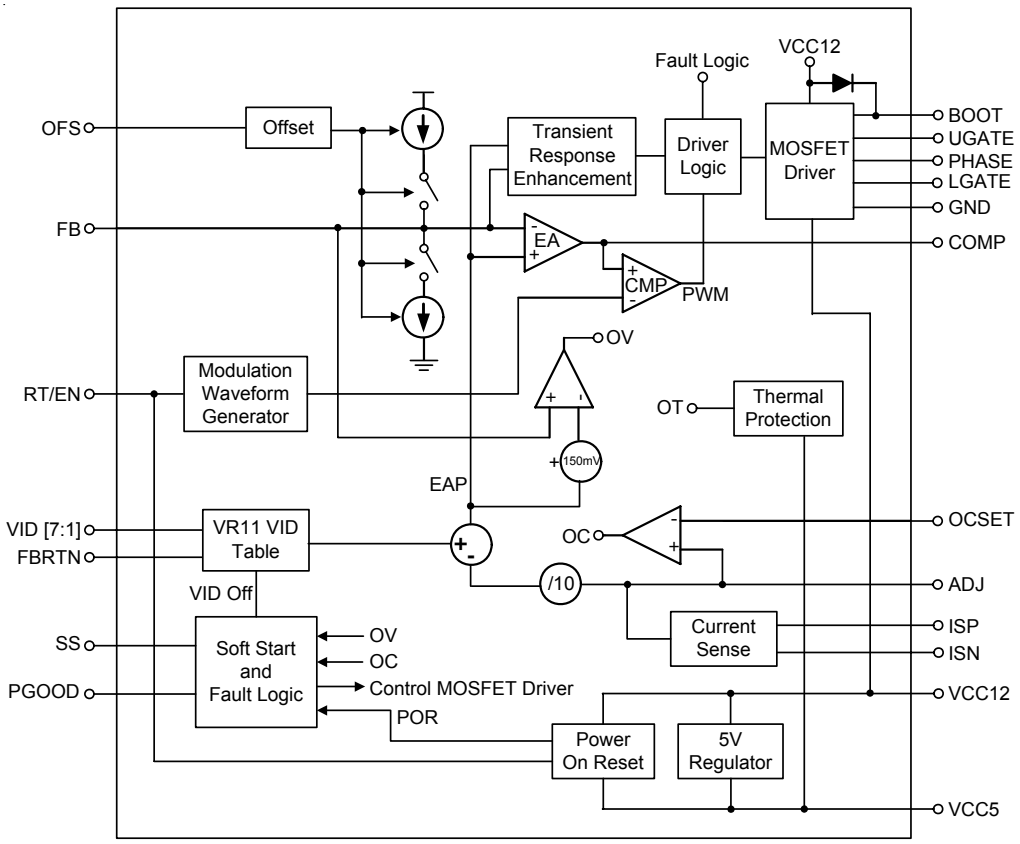


WQFN-24L 4x4

Typical Application Circuit



Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
2	OCSET	Over Current Protection Threshold Set Pin.
3	FBRTN	Return Ground. This pin is Negative Node of the differential Remote Voltage sending.
4	SS	Soft-Start Ramp Slope Set Pin. Connect this pin to FBRTN by a Capacitor to Adjust soft-start slew rate.
5	COMP	Compensation Pin. Output of Error Amplifier and Input of PWM comparator.
6	FB	Inverting Input of Error Amplifier.
7	ADJ	Droop Set Pin. Connect a resistor from this pin to GND sets the load line slope.
8	OFS	Voltage Offset Pin. This pin sets No-Load Output Voltage Offset. Connect a resistor from this Pin to VCC5 or GND to bidirection set the output voltage no-load offset.
9	RT/EN	Switching Frequency Set Pin. Connect this pin to GND via a resistor to adjust switching frequency and operate with droop function. Connect this pin to VCC5 via a resistor to adjust switching frequency and operate without droop function.
10	VCC5	Internal 5V Regulator Output.
11	ISP	Non-Invertering Input of Current Sense Amplifier.
12	ISN	Invertering Input of Current Sense Amplifier.
13	LGATE	Lower Gate Driver. This pin drives the gate of low side MOSFETs.
14	VCC12	12V Power Supply Input Pin.
15	PHASE	Switch Node of High side Driver. Connect this pin to high-side MOSFETs sources together with the low side MOSFETs drains and inductor.
16	UGATE	Upper Gate Driver. This pin drives the gate of the high-side MOSFETs.
17	BOOT	Bootstrap Power Pin. This pin powers the high-side MOSFETs drivers. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode.
18	PGOOD	Power Good Indicator.
19 to 24,1	VID7 to VID1	DAC Voltage Identification Inputs.
25 (Exposed Pad)	GND	Ground Pin. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.

Table 1. Output Voltage Program

Pin Name							Nominal Output Voltage DACOUT
VID7	VID6	VID5	VID4	VID3	VID2	VID1	
0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	1	1.60000V
0	0	0	0	0	1	0	1.58750V
0	0	0	0	0	1	1	1.57500V
0	0	0	0	1	0	0	1.56250V
0	0	0	0	1	0	1	1.55000V
0	0	0	0	1	1	0	1.53750V
0	0	0	0	1	1	1	1.52500V
0	0	0	1	0	0	0	1.51250V
0	0	0	1	0	0	1	1.50000V
0	0	0	1	0	1	0	1.48750V
0	0	0	1	0	1	1	1.47500V
0	0	0	1	1	0	0	1.46250V
0	0	0	1	1	0	1	1.45000V
0	0	0	1	1	1	0	1.43750V
0	0	0	1	1	1	1	1.42500V
0	0	1	0	0	0	0	1.41250V
0	0	1	0	0	0	1	1.40000V
0	0	1	0	0	1	0	1.38750V
0	0	1	0	0	1	1	1.37500V
0	0	1	0	1	0	0	1.36250V
0	0	1	0	1	0	1	1.35000V
0	0	1	0	1	1	0	1.33750V
0	0	1	0	1	1	1	1.32500V
0	0	1	1	0	0	0	1.31250V
0	0	1	1	0	0	1	1.30000V
0	0	1	1	0	1	0	1.28750V
0	0	1	1	0	1	1	1.27500V
0	0	1	1	1	0	0	1.26250V
0	0	1	1	1	0	1	1.25000V
0	0	1	1	1	1	0	1.23750V
0	0	1	1	1	1	1	1.22500V
0	1	0	0	0	0	0	1.21250V
0	1	0	0	0	0	1	1.20000V
0	1	0	0	0	1	0	1.18750V
0	1	0	0	0	1	1	1.17500V
0	1	0	0	1	0	0	1.16250V
0	1	0	0	1	0	1	1.15000V
0	1	0	0	1	1	0	1.13750V
0	1	0	0	1	1	1	1.12500V

To be continued

Table 1. Output Voltage Program

Pin Name							Nominal Output Voltage DACOUT
VID7	VID6	VID5	VID4	VID3	VID2	VID1	
0	1	0	1	0	0	0	1.11250V
0	1	0	1	0	0	1	1.10000V
0	1	0	1	0	1	0	1.08750V
0	1	0	1	0	1	1	1.07500V
0	1	0	1	1	0	0	1.06250V
0	1	0	1	1	0	1	1.05000V
0	1	0	1	1	1	0	1.03750V
0	1	0	1	1	1	1	1.02500V
0	1	1	0	0	0	0	1.01250V
0	1	1	0	0	0	1	1.00000V
0	1	1	0	0	1	0	0.98750V
0	1	1	0	0	1	1	0.97500V
0	1	1	0	1	0	0	0.96250V
0	1	1	0	1	0	1	0.95000V
0	1	1	0	1	1	0	0.93750V
0	1	1	0	1	1	1	0.92500V
0	1	1	1	0	0	0	0.91250V
0	1	1	1	0	0	1	0.90000V
0	1	1	1	0	1	0	0.88750V
0	1	1	1	0	1	1	0.87500V
0	1	1	1	1	0	0	0.86250V
0	1	1	1	1	0	1	0.85000V
0	1	1	1	1	1	0	0.83750V
0	1	1	1	1	1	1	0.82500V
1	0	0	0	0	0	0	0.81250V
1	0	0	0	0	0	1	0.80000V
1	0	0	0	0	1	0	0.78750V
1	0	0	0	0	1	1	0.77500V
1	0	0	0	1	0	0	0.76250V
1	0	0	0	1	0	1	0.75000V
1	0	0	0	1	1	0	0.73750V
1	0	0	0	1	1	1	0.72500V
1	0	0	1	0	0	0	0.71250V
1	0	0	1	0	0	1	0.70000V
1	0	0	1	0	1	0	0.68750V
1	0	0	1	0	1	1	0.67500V
1	0	0	1	1	0	0	0.66250V
1	0	0	1	1	0	1	0.65000V
1	0	0	1	1	1	0	0.63750V
1	0	0	1	1	1	1	0.62500V

To be continued

Table 1. Output Voltage Program

Pin Name							Nominal Output Voltage DACOUT
VID7	VID6	VID5	VID4	VID3	VID2	VID1	
1	0	1	0	0	0	0	0.61250V
1	0	1	0	0	0	1	0.60000V
1	0	1	0	0	1	0	0.58750V
1	0	1	0	0	1	1	0.57500V
1	0	1	0	1	0	0	0.56250V
1	0	1	0	1	0	1	0.55000V
1	0	1	0	1	1	0	0.53750V
1	0	1	0	1	1	1	0.52500V
1	0	1	1	0	0	0	0.51250V
1	0	1	1	0	0	1	0.50000V
1	1	1	1	1	1	1	OFF

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VCC12 ---------- –0.3V to 15V
- BOOTx to GND
  - DC ---------- –0.3V to 30V
  - < 200ns ---------- –0.3V to 42V
- PHASEx to GND
  - DC ---------- –2V to 15V
  - < 200ns ---------- –5V to 30V
- UGATEx to GND ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 200ns ---------- (V_{PHASE} – 5V) to (V_{BOOT} + 5V)
- LGATEx to GND ---------- (GND – 0.3V) to (V_{CC} + 0.3V)
  - < 200ns ---------- (GND – 5V) to (V_{CC} + 5V)
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-24L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 2)
  - WQFN-24L 4x4, θ_{JA} ---------- 52°C/W
  - WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VCC12 ---------- 12V ±10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC12 Supply Input						
VCC12 Supply Current	I_{CC}		--	6	--	mA
VCC5 Power						
VCC5 Output Voltage	V_{CC5}	I_{LOAD} = 10mA	4.9	5	5.1	V
VCC5 Output Sourcing	I_{VCC5}		10	--	--	mA
Power-On Reset						
VCC12 Rising Threshold	V_{CC12_TH}	VCC12 Rising	9.2	9.7	10.2	V
VCC12 Hysteresis	V_{CC12_HY}	VCC12 Falling	--	0.9	--	V
VCC5 Rising Threshold	V_{CC5_TH}	VCC5 Rising	4.4	4.6	4.8	V
VCC5 Hysteresis	V_{CC5_HY}	VCC5 Falling	--	0.4	--	V

To be continued

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
RT/EN							
Chip Disable Threshold		V_{DIS}		--	--	0.4	V
Running Frequency		f_{OSC}	R_{RT} = 60kΩ	180	200	220	kHz
RT Pin Voltage		$V_{RT, GND}$	R_{RT} = 60kΩ, connected between RT/EN and GND	1.52	1.6	1.68	V
RT Pin Voltage		$V_{RT, VDD}$	R_{RT} = 60kΩ, connected between RT/EN and V_{CC5}	V_{CC5}– 1.68	V_{CC5}– 1.6	V_{CC5}– 1.52	V
Modulation Gain		A_{RAMP}	R_{RT} = 60kΩ	--	22	--	%/V
Reference Voltage Accuracy							
DAC Accuracy			1V to 1.6V	–0.5	--	0.5	%
			0.8V to 1V	–5	--	5	mV
			0.5V to 0.8V	–8	--	8	mV
VID Threshold Voltage	Logic-Low	V_{IL}	VID [7:1]	--	--	0.4	V
	Logic-High	V_{IH}	VID [7:1]	0.8	--	--	V
Error Amplifier							
DC Gain		A_{DC}	No Load	--	80	--	dB
Gain-Bandwidth		GBW	C_{LOAD} = 10pF	--	10	--	MHz
Slew Rate		SR	C_{LOAD} = 10pF	10	--	--	V/μs
Output Voltage Range		V_{COMP}		0.5	--	3.6	V
Maximum Current		I_{EA_SLEW}	Slew	300	--	--	μA
Power Sequence							
PGOOD Low Voltage		V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
Soft-Start Delay		t_{D1}	After POR, from EN = High to V_{OUT} Rising	0	--	5	ms
V_{BOOT} Duration		t_{D3}		0.05	--	3	ms
PGOOD Delay		t_{D5}	Measured from final V_{OUT} value to PGOOD = High	0.05	--	3	ms
Current Sense Amplifier							
Maximum Current		I_{GMMAX}	V_{CSP} = 1.3V, sink current from CSN	100	--	--	μA
Input Offset Voltage		V_{OSCS}		–1.5	0	1.5	mV
Soft Start							
Soft Start Current		I_{SS1}	Slew	12	16	20	μA
VID Change Current		I_{SS2}	Slew	120	160	200	μA
Gate Driver							
UGATE Drive Source		$I_{UGATEsr}$	BOOT – PHASE = 12V, UGATE – PHASE = 6V	0.6	1	--	A
UGATE Drive Sink		$R_{UGATEsk}$	BOOT – PHASE = 8V, 250mA Source Current	--	1	--	Ω
LGATE Drive Source		$I_{LGATEsr}$	V_{CC12} = 12V, V_{LGATE} = 6V	0.6	1	--	A
LGATE Drive Sink		$R_{LGATEsk}$	250mA Sink Current	--	0.8	--	Ω
Protection							
Over-Voltage Threshold		V_{OVP}	Sweep FB Voltage, V_{FB} – V_{EAP}	125	150	175	mV
OCP Input Offset Voltage		V_{OCOFS}		–10	--	10	mV

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over Temperature Shutdown Setpoint	T_{SD}		--	160	--	°C
Dynamic Characteristic						
UGATE Rise Time	t_{rUGATE}	C_{iss} = 3000pF	-	15	-	ns
UGATE Fall Time	t_{fUGATE}		-	10	-	ns
LGATE Rise Time	t_{rLGATE}		-	15	-	ns
LGATE Rise Time	t_{fLGATE}		-	10	-	ns

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

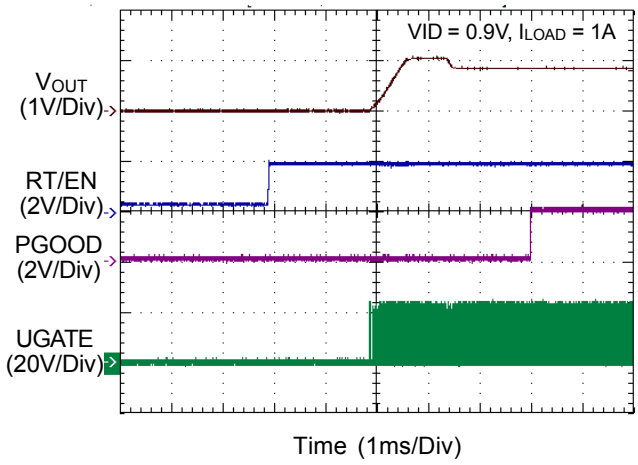
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

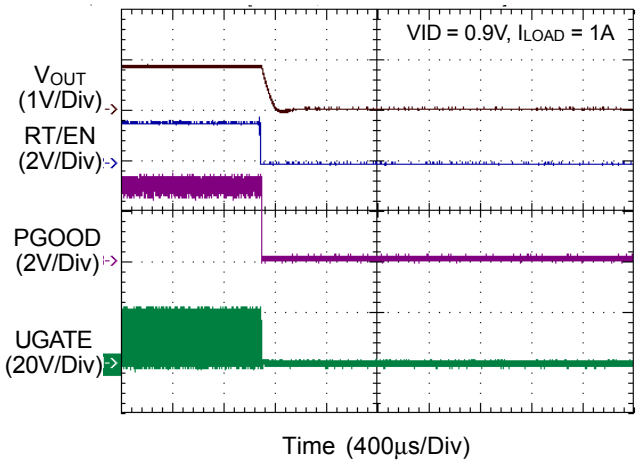
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

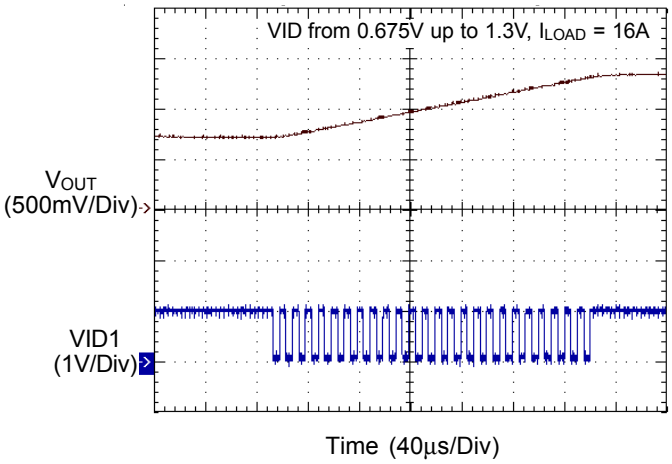
Start Up from RT/EN



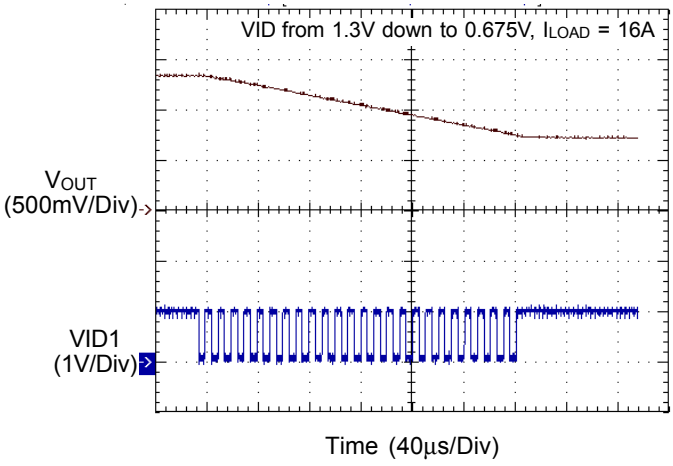
Power Off from RT/EN



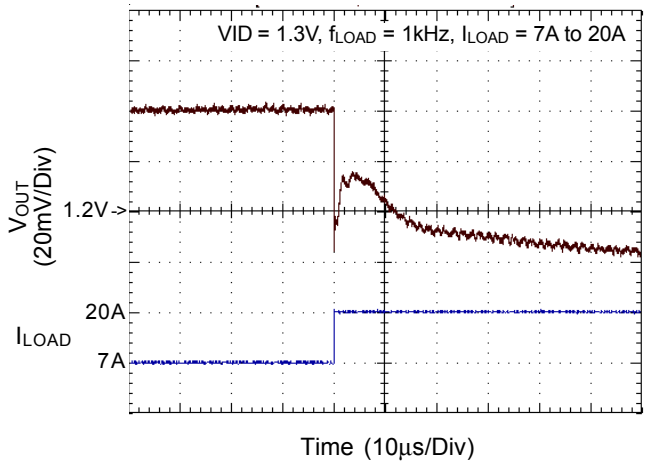
Dynamic VID Up



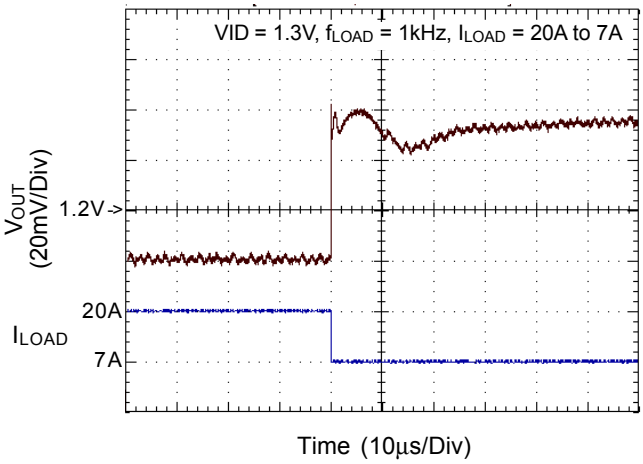
Dynamic VID Down



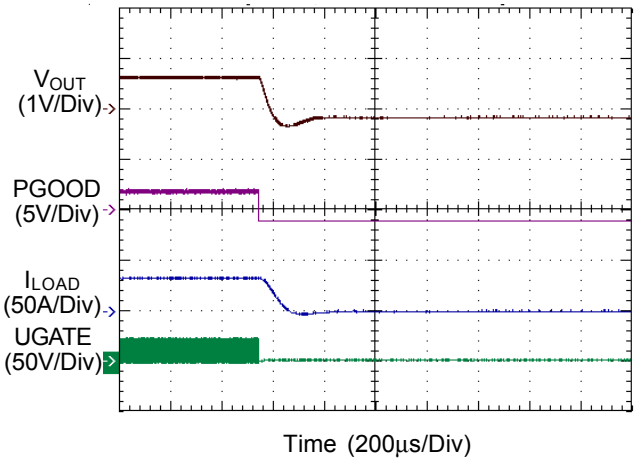
Load Transient Response



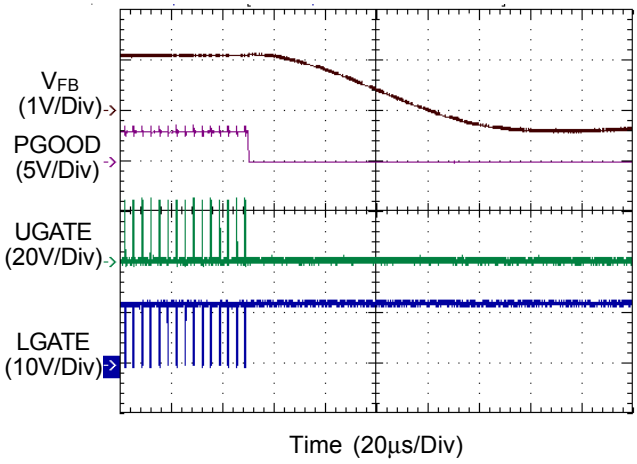
Load Transient Response



Over Current Protection



Over Voltage Protection



Applications Information

The RT8113 is a single-phase synchronous buck DC/DC converter with embedded MOSFET driver. The internal VID DAC is designed to interface with the Intel 7-bit VR11.X compatible VID table for Ibexpeak platform CPU's AXG VR application.

Supply voltage, VCC5 regulation and POR

There are two supply voltage pins built-in in the RT8113, VCC12 and VCC5. VCC12 is a power input pin which receives external 12V voltage for embedded driver logic operation. VCC5 is a power output pin which is the output of an internal 5V LDO regulator. The mentioned 5V LDO regulator regulates VCC12 to generate a 5V voltage source for internal gate logic and external circuit biasing, e.g., OCP biasing. Since the VCC5 voltage is regulated, the variation of VCC5 (2%) will be much smaller than Platform ATX +5V (5%~7%). The maximum supply current of VCC5 is 10mA, which is designed only for controller circuit biasing. The recommended configuration of the RT8113 supply voltages is as follows: Platform ATX +12V to the VCC12 pin, and decoupling capacitors on the VCC12 and VCC5 pins (minimum 0.1μF).

The initialization of the RT8113 requires both the voltage on the VCC12 and VCC5 to be ready. Since VCC5 is regulated internally from VCC12, the VCC5 voltage will be ready (>4.6V) after VCC12 reaches about 7V, so there is no power sequence problem between VCC12 and VCC5. After VCC5 > 4.6V and VCC12 > 9.6V, the internal power-on-reset (POR) signal goes high. This POR signal indicates the power supply voltages are all ready and initiates soft-start sequence. When POR = low, The RT8113 will try to turn off both high-side and low-side MOSFETs to prevent catastrophic failure.

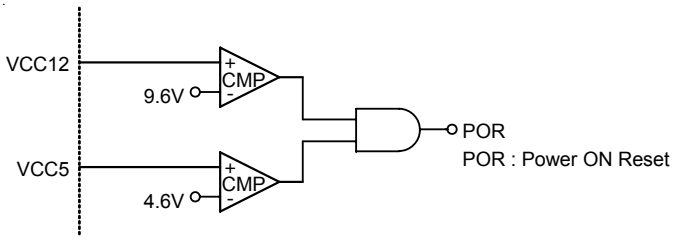


Figure 1. Circuit for Power Ready Detection

Switching Frequency

The switching frequency of the RT8113 is set by an external resistor connected from the RT/EN pin either to GND or to VCC5. If the resistor is connected from RT/EN to GND, the load line function will be enabled as well. More details will be described in the Load Line section. The frequency follows the graph in Figure 2.

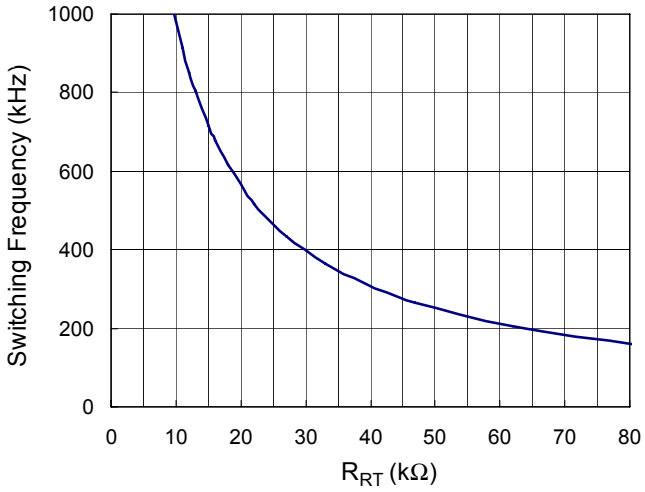


Figure 2. Switching Frequency vs. R_{RT} Resistance

Chip Enable

The enable function of the RT8113 is combined in the RT/EN pin. Besides frequency setting function, pulling the RT/EN pin to GND can also force the RT8113 to enter soft shutdown sequence. It is recommended to connect a control switch from the RT/EN pin to GND in parallel with RT setting resistors. The RT8113 will enter soft shutdown sequence when the control switch is turned on.

Soft-Start

The V_{OUT} soft-start slew rate is set by a capacitor from the SS pin to FBRTN. Before power on reset (POR = low), the SS pin is held at GND. After power on reset (POR = high) and an extra delay of 1600μs (t_{D1}), the controller initiates ramping up. V_{OUT} will always trace V_{EAP} during normal operation of the RT8113, where V_{EAP} is the positive input of compensation error amplifier, which can be described as $V_{EAP} = V_{DAC} – V_{ADJ}$ (The definition of V_{ADJ} will be described later in the Load Line section). The first ramping up duration of V_{OUT} (t_{D2}) ramps V_{OUT} to V_{BOOT}.

After V_{OUT} ramps to V_{BOOT}, the RT8113 stays in this state for 800μs (t_{D3}) waiting for valid VID code sent by CPU. After receiving valid VID code, V_{OUT} continues ramping up or down to the voltage specified by VID code. After V_{OUT} ramps to $V_{EAP} = V_{DAC} – V_{ADJ}$, the RT8113 stays in this state for 1600μs (t_{D5}) and then asserts PGOOD = high. The ramping slew rate of t_{D2} and t_{D4} is controlled by the external capacitor connected to SS pin. The voltage of the SS pin will always be V_{EAP}+0.7V, where the mentioned 0.7V is the typical turn-on threshold of an internal power switch. Before PGOOD = high, the slew rate of V_{EAP} is limited to 16μA/C_{SS}. When PGOOD = high, the slew rate of V_{EAP} is limited to 160μA/C_{SS}, which is 10 times faster than soft start slew rate for dynamic VID feature. The soft start waveform is shown in Figure 4.

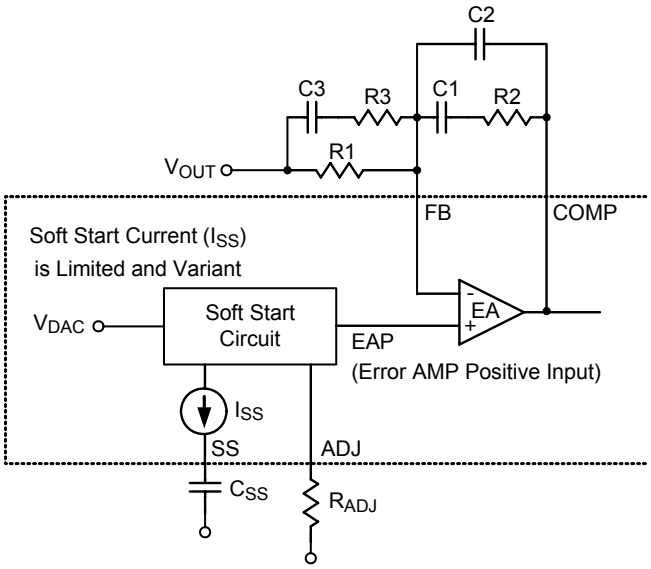


Figure 3. Circuit for Soft-Start and Dynamic VID

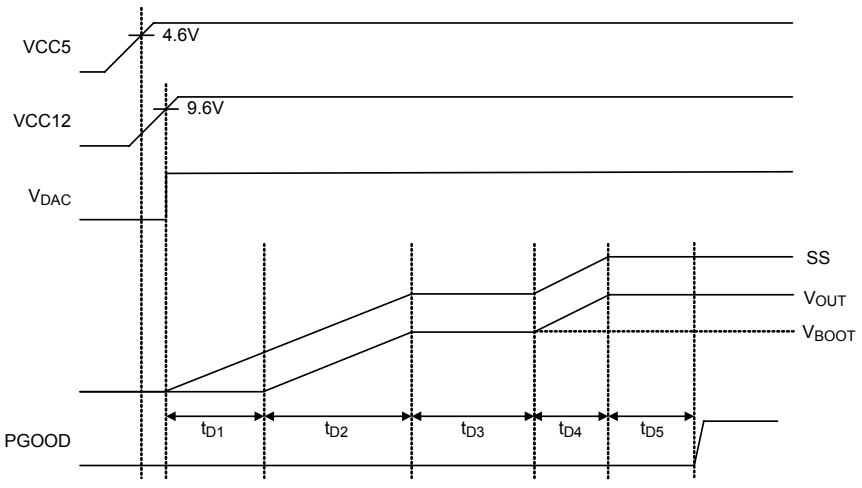


Figure 4. Soft-Start Wave forms

t_{D1} is the delay time from power on reset state to the beginning of V_{OUT} rising.

$$t_{D1} = 1600\mu s + \frac{0.7V \times C_{SS}}{16\mu A}$$

t_{D2} is the soft-start time from V_{OUT} = 0 to V_{OUT} = V_{BOOT}.

$$t_{D2} = \frac{V_{BOOT} \times C_{SS}}{16\mu A}$$

t_{D3} is the dwelling time for V_{OUT} = V_{BOOT}.

$t_{D3} \cong 800\mu s$.

t_{D4} is the soft-start time from V_{OUT} = V_{BOOT} to V_{OUT} = V_{DAC}.

$$t_{D4} \cong \frac{|V_{DAC} - V_{BOOT}| \times Css}{16\mu A}$$

t_{D5} is the power good delay time.

$t_{D5} \cong 1600\mu s$.

Dynamic VID

The RT8113 can accept VID input changing while the controller is running. This allows the output voltage (V_{OUT}) to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The CPU changes the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative. Theoretically, V_{OUT} should follow V_{DAC}, which is a staircase waveform, but in real application, the bandwidth of the converter is finite while the staircase waveform needs infinite bandwidth to follow. Thus, undesired V_{OUT} overshoot (when V_{DAC} changes up) or undershoot (when V_{DAC} changes down) is often observed in these type of designs. However, for the RT8113, as mentioned before in the Soft-Start section, V_{DAC} slew rate is limited by I_{SS2}/C_{SS} when PGOOD = high. This slew rate limiter works as a low-pass filter of V_{DAC} and makes the bandwidth of V_{DAC} waveform finite. By smoothening V_{DAC} staircase waveform, V_{OUT} will no longer overshoot or undershoot. On the other hand, C_{SS} will increase the settling time of V_{OUT} during VID OTF. In most cases, a 1nF to 30nF ceramic capacitor will be suitable for C_{SS}.

Output Voltage Differential Sensing

The RT8113 uses a high-gain low-offset error amplifier for differential sensing. The CPU voltage is sensed between the FB and FBRTN pins. A resistor (R_{FB}) connects the FB pin with the positive remote sense pin of the CPU (V_{CCP}), while the FBRTN pin connects directly to the negative remote sense pin of the CPU (V_{CCN}). The error amplifier compares V_{EAP} (= V_{DAC} – V_{ADJ}) with the V_{FB} to regulate the output voltage.

No-Load Offset

In Figure 5, I_{OFSN} and I_{OFSP} are used to generate no-load offset. Either I_{OFSN} or I_{OFSP} is active during normal operation. Connect a resistor from OFS pin to GND to activate I_{OFSN}. I_{OFSN} flows through R_{FB} from the FB pin to V_{CCP}. In this case, a negative no-load offset voltage (V_{OFSN}) is generated.

$$V_{OFSN} = I_{OFSN} \times R_{FB} = \frac{0.8 \times R_{FB}}{R_{OFS}}$$

Connect a resistor from the OFS pin to VCC5 to activate I_{OFSP}. I_{OFSP} flows through R_{FB} from the V_{CCP} to the FB pin. In this case, a positive no-load offset voltage (V_{OFSP}) is generated.

$$V_{OFSP} = I_{OFSP} \times R_{FB} = \frac{6.4 \times R_{FB}}{R_{OFS}}$$

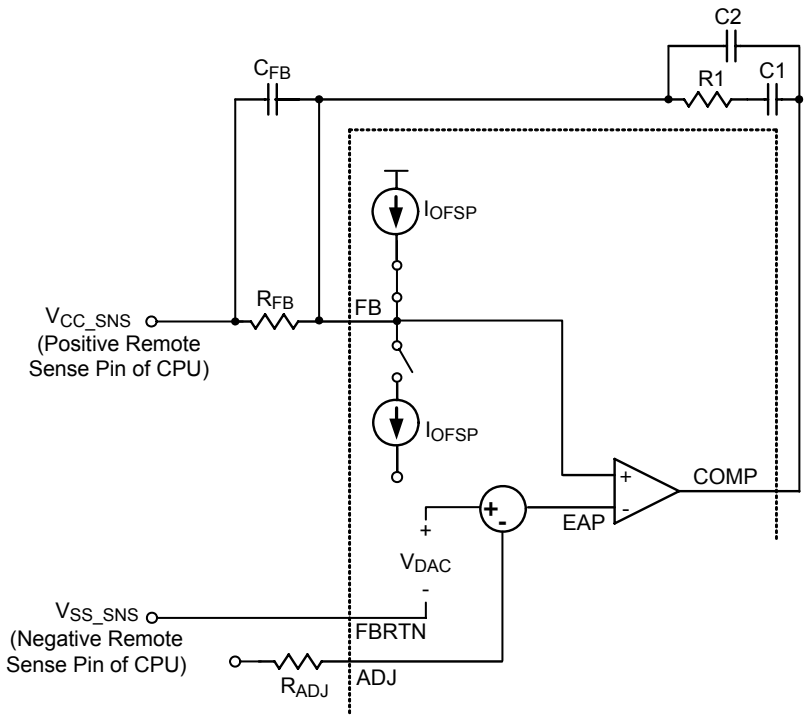


Figure 5. Circuit for V_{OUT} Differential Sensing and No Load Offset

Load Transient Quick Response

In steady state, the voltage of V_{FB} is controlled to be very close to V_{EAP}. However While a load step transient from light load to heavy load could cause V_{FB} to be lower than V_{EAP} by several tens of mV. In conventional buck converter design (without non-linear control) for CPU VR application, due to limited control bandwidth, it is hard for the VR to prevent V_{OUT} undershoot during quick load transient from light load to heavy load. Hence, the RT8113 builds in a state-of-the-art quick response function which detects load transient by comparing V_{FB} and V_{EAP}. If V_{FB} suddenly drops below "$V_{EAP} - V_{QR}$" where V_{QR} is a predetermined voltage (~40mV), the quick response indicator QR rises up. When QR = high, the RT8113 turns on all high side MOSFETs and turns off all low side MOSFETs. The sensitivity of quick response can be adjusted by varying the values of C_{FB} and R_{FB}. Smaller R_{FB} and/or larger C_{FB} will make QR easier to be triggered. Figure 6 is the circuit and typical waveforms.

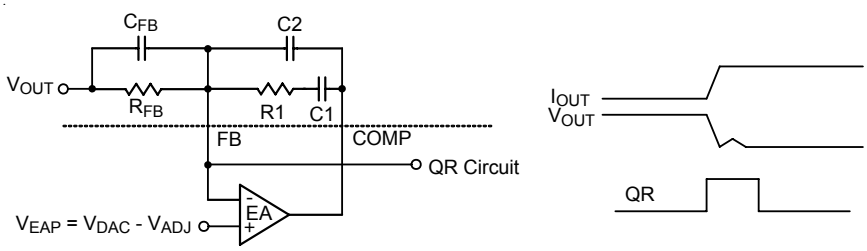


Figure 6. Load Transient Quick Response

Output Current Sensing

The RT8113 provides a low input offset current-sense amplifier (CSA) to monitor the output current. The output current of CSA (I_X) is used for load line control and over-current protection. In this inductor current sensing topology, R_S and C_S must be set according to the equation below :

$$\frac{L}{DCR} = R_S \times C_S$$

Then the output current of CSA will follow the equation below :

$$I_X = \frac{I_L \times DCR - V_{OFS\text{-}CSA} + 700n \times (R_{CSP} + R_S - R_{CSN})}{R_{CSN}}$$

700nA is a typical value of the CSA input offset current. $V_{OFS\text{-}CSA}$ is the input offset voltage of CSA. $V_{OFS\text{-}CSA}$ of the RT8113 is smaller than +/- 1.5mV. Usually, "$V_{OFS\text{-}CSA}$ + 700n x (R_{CSP} + R_S - R_{CSN})" is negligible except at very light load and the equation can be simplified as the equation below :

$$I_X = \frac{I_L \times DCR}{R_{CSN}}$$

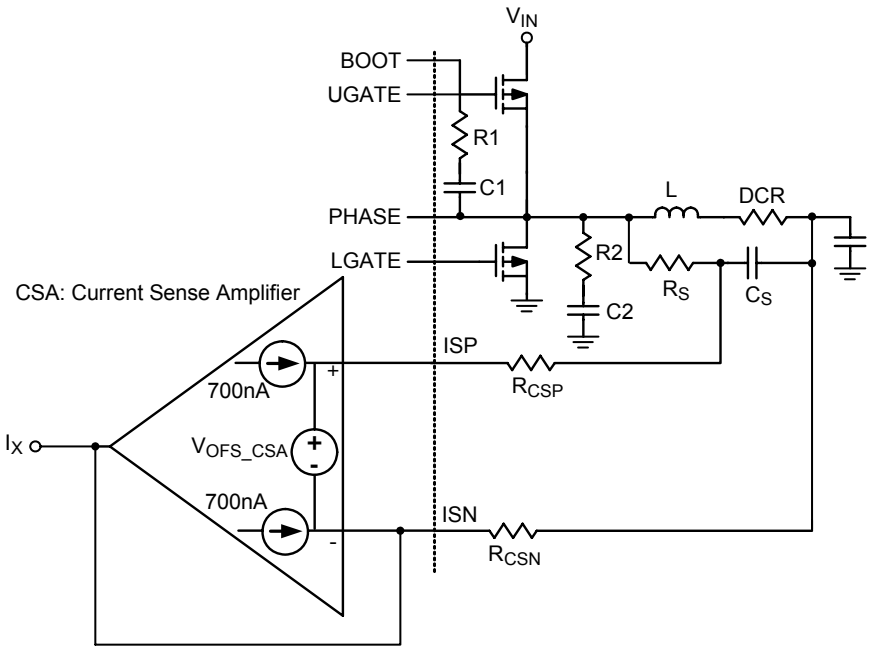


Figure 7. Circuit for Current Sensing

Load Line

The RT8113 utilizes inductor DCR current sense technique for load line control function. The sensed inductor current I_X is multiplied by 0.5 and sent to ADJ pin. After the current 0.5 x I_X injects into the ADJ resistors, the voltage of the ADJ pin is established. The V_{ADJ} is then multiplied by 0.1 and subtracted by V_{DAC} to generate V_{EAP}. Because I_X is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect ADJ pin to GND. If the NTC resistor is properly selected to compensate the temperature coefficient of I_X, the voltage on ADJ pin will be proportional to I_{OUT} without temperature effect. In the RT8113, the positive input of error amplifier is "V_{DAC} – 0.1 x V_{ADJ}" and V_{OUT} will follow "V_{DAC} – 0.1 x V_{ADJ}". Thus, the output voltage which decreases linearly with I_{OUT} is obtained. The load line is defined as :

$$\Delta V_{ADJ} = \frac{1}{2} \times I_X \times R_{ADJ}$$

$$LL(\text{Load Line}) = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{1}{10} \times \frac{\Delta V_{ADJ}}{\Delta I_{OUT}} = \frac{DCR \times R_{ADJ}}{20 \times R_{CSN}}$$

Basically, the resistance of R_{ADJ} sets the resistance of the load line. The temperature coefficient of R_{ADJ} compensates the temperature effect of the load line.

The load line function of the RT8113 can be disabled by connecting the RT/EN pin resistor to VCC5 instead of GND. When the RT/EN pin resistor is connected to VCC5, the current-sense circuit works normally while V_{EAP} no longer contains droop, and the reference voltage of the error amplifier will remain equal to V_{DAC} regardless of output current. The running frequency of the RT8113 will always be the same whether connecting RT/EN to VCC5 or GND.

Over Current Protection (OCP)

In Figure 8, V_{OCSET} is equal to VCC x R2/(R1 + R2). For the RT8113, V_{ADJ} is proportional to I_{OUT} and is thermally compensated. Once V_{ADJ} is larger than V_{OCSET}, OCP is triggered and latched. The OCP function will not be influenced by enabling or disabling load line since the voltage on the ADJ pin always contains real-time information of load current. Once OCP is triggered, the RT8113 will turn off both high-side MOSFETs and low side MOSFETs.

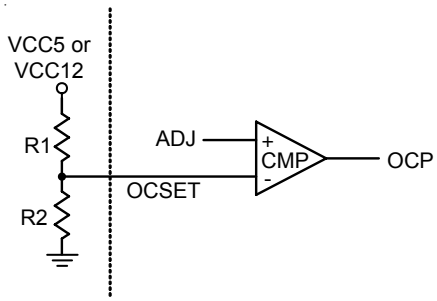


Figure 8. Over Current Protection

Over Voltage Protection (OVP)

The over-voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds "V_{EAP} + 150mV", OVP is triggered and latched. The RT8113 will turn on low-side MOSFET and turn off high side MOSFET to protect CPU. A 20μs delay is used in OVP detection circuit to prevent false trigger.

Over Temperature Protection (OTP)

The over-temperature protection function of the RT8113 is built inside the controller to prevent overheat damage. OTP occurs when the die temperature of the RT8113 exceeds 160°C, in which the RT8113 then turns off both high-side MOSFETs and low side MOSFETs.

Loop Compensation

The RT8113 is a voltage mode controller and requires external compensation. To compensate a typical voltage mode buck converter, there are two ordinary compensation schemes, commonly known as type-II compensator and type-III compensator. The choice of using type-II or type-III compensator lies with the platform designers, and the main concern deals with the position of the capacitor ESR zero and mid-frequency to high-frequency gain boost. Typically, the ESR zero of output capacitor will tend to stabilize the effect of output LC double poles. Hence, the position of the output capacitor ESR zero in frequency domain may influence the design of voltage loop compensation. Figure 9 shows a typical control loop using type-III compensator. Below is the compensator design procedure.

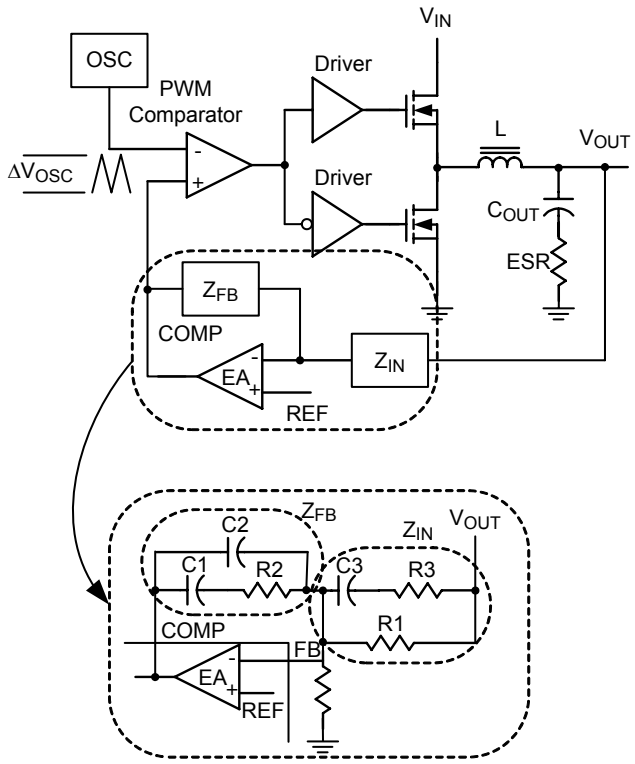


Figure 9. Compensation Circuit

1) Modulator Characteristic

The modulator consists of the PWM comparator and power stage. The PWM comparator compares error amplifier EA output (COMP) with oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) gate-driving signal. The PWM wave is smoothed out by the output filter, L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output). This transfer function is dominated by a DC gain, a double pole, and an ESR zero as shown in Figure 10.

The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage V_{OSC}. The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter is expressed as :

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires the output capacitor to have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as the following equation :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

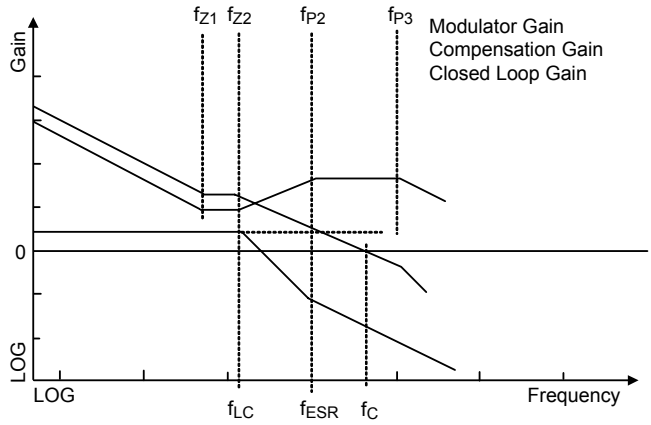


Figure 10. Bode PLot of Loop Gain

2) Design the compensator

A well-designed compensator regulates the output voltage to the reference voltage V_{REF} with fast transient response and good stability. In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (usually greater than 45°C) and the highest bandwidth (0dB crossing frequency, f_C) possible. It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

According to Figure 10, the location of poles and zeros are :

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3}$$

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times C3 \times R3}$$

$$f_{P3} = \frac{1}{2\pi \times \frac{C1 \times C2 \times R2}{C1 + C2}}$$

Generally, f_{Z1} and f_{Z2} are designed to cancel the double pole of modulation. Usually, place f_{Z1} at a fraction of the

f_{LC}, and place f_{Z2} at f_{LC}. f_{P2} is usually placed at f_{ESR} to cancel the ESR zero. And f_{P3} is placed below switching frequency to cancel high frequency noise.

For given bandwith, R2, f_{Z1}, f_{Z2}, f_{P2}, f_{P3}, then

$$C1 = \frac{1}{2\pi \times f_{Z1} \times R2}$$

$$C3 = \frac{G_{MOD@BW}}{2\pi \times f_C \times R2}$$

$$R1 = \frac{1}{2\pi \times f_{Z2} \times C3}$$

$$R3 = \frac{1}{2\pi \times f_{P2} \times C3}$$

$$C2 = \frac{C1}{2\pi \times f_{P3} \times C1 \times R2 - 1}$$

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, rate of surrounding airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following the formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT8113, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-24L 4x4 packages, the thermal resistance θ_{JA} is 52°C/W on the standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (52°C/W) = 1.923W for WQFN-24L 4x4 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance θ_{JA}. For RT8113 package, the derating curve in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

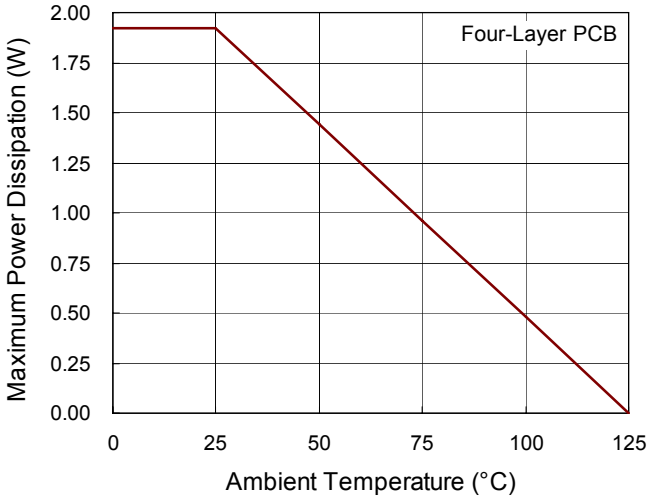


Figure 11. Derating Curves for RT8113 Package

Layout Considerations

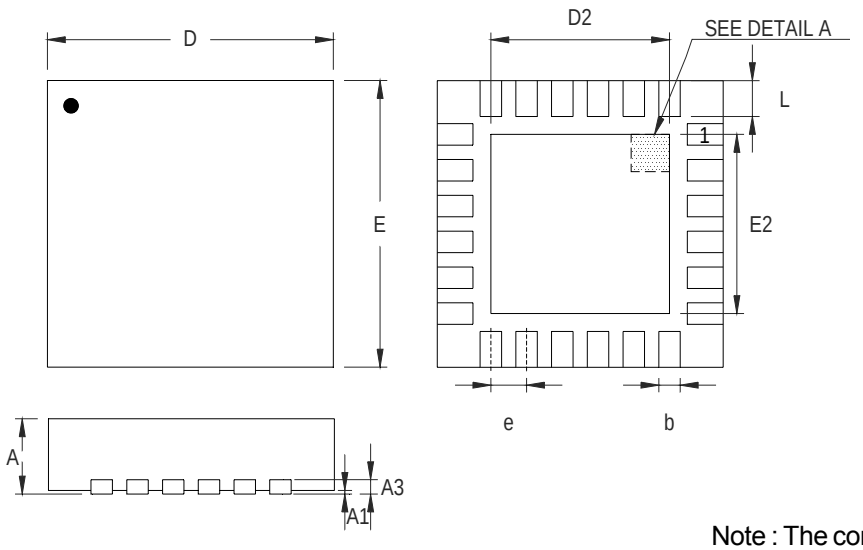
For best performance of the RT8113, the following guidelines must be strictly followed :

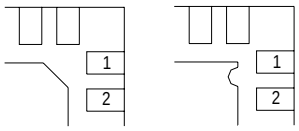
- The power components should be placed first. Keep the connection between power components as short as possible.
- The shape of the phase plane (the connection plane between high side MOSFETs, low-side MOSFETs and output inductors) has to be as square as possible. Long traces, thin bars or separated islands must be avoided in the phase plane.
- Keep snubber circuits or damping elements near its objects. Phase RC snubbers have to be close to low-side MOSFETs, UGATE damping resistor has to be close to high-side MOSFETs, and boot to phase damping resistor has to be close to high-side MOSFETs and phase plane. Also, keep the traces of these snubber circuits as short as possible.
- The area of V_{IN} plane (power stage 12V V_{IN}) and V_{OUT} plane (output bulk capacitors and inductor connection plane) has to be as wide as possible. Long traces or thin bars must be avoided in these planes. The plane trace width must be wide enough to carry large input/ output current (40mm/A).
- The following traces have to be wide and short : UGATE, LGATE, BOOT, PHASE, and VCC12. Make sure the widths of these traces are wide enough to carry large driving current (at least 40mm).

- The voltage feedback loop contains two traces, VCC and VSS, which are Kelvin sensed from CPU socket or output capacitors. These two traces should have 10mm width and be placed away from high (di/dt) switching elements such as high-side MOSFETs, low-side MOSFETs, phase plane etc. The circuit elements of voltage feedback loop, such as feedback loop short resistors and voltage loop compensation RCs, have to be kept near the RT8113 and also away from switching elements.
- The current-sense mechanism of the RT8113 is fully differential Kelvin sense. Therefore, the current-sense loop of the RT8113 contain two traces : the positive trace(ISP) comes from the positive node the of output inductor (the node connecting phase plane) and the negative trace (ISN) comes from the negative node of the output inductor (the node connecting output plane).

DO NOT connect the current-sense traces from the phase plane or output plane. Only connect these traces from both sides of the output inductor to achieve the goal of precise Kelvin sense. The current-sense feedback loops have to be routed away from switching elements, and the current-sense RC elements have to be put near their respective ISN or ISP pins of the RT8113 and also away from noise switching elements. At lease 10 mm width is suggested for current sense feedback loops.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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