Dual Single-Phase PWM Controller for CPU Core/GFX Power Supply

General Description

The RT8165A is a dual single-phase synchronous Buck PWM controller with integrated gate drivers, compliant with Intel VR12/IMVP7 specification. A serial VID (SVID) interface is built-in in the RT8165A to communicate with Intel VR12/IMVP7 compliant CPU. The integrated differential remote output voltage sensing function and built-in high accuracy DAC achieve accurate output voltage regulation.

The RT8165A supports VR12/ IMVP7 compatible power management states and VID on-the-fly function. The RT8165A operates in two power management states including DEM in PS2 and Forced-CCM in PS1/PS0. Richtek's proprietary G-NAVP™ (Green Native AVP) makes AVP (Active Voltage Positioning) design easier and more robust. By utilizing the G-NAVP™ topology, DEM and CCM efficiency can be improved.

The RT8165A integrates high accuracy ADC for platform setting functions, such as no-load offset or over current level. Individual VR ready output signals are provided for both CORE VR and GFX VR. The IC also features complete fault protection functions, including over voltage, under voltage, negative voltage, over current and under voltage lockout. The RT8165A is available in a WQFN-48L 6x6 small foot print package.

Marking Information

RT8165AGQW

RT8165AGQW : Product Number
YMDNN : Date Code

RT8165AZQW

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Features

- **G-NAVP™ (Green Native Active Voltage Positioning) Topology**
- **Dual Output Controller with Two Built-in Gate Drivers**
- **Serial VID Interface**
- **0.5% DAC Accuracy**
- **Differential Remote Output Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Diode Emulation Mode (DEM) at Light Load Condition**
- **Droop Enable/Disable**
- **Fast Transient Response**
- **VR12/IMVP7 Compatible Power Management States**
- **VR Ready Indicator**
- **Thermal Throttling Indicator**
- **Current Monitor Output**
- **Switching Frequency up to 1MHz per Phase**
- **Protection : OVP, UVP, NVP, OCP, UVLO**
- **Small 48-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- VR12 / IMVP7 Intel CPU Core Supply
- AVP Step-down Converter
- Notebook/ Netbook/ Desktop Computer CPU Core Supply

Ordering Information

RT8165A□□

Package Type
QW : WQFN-48L 6x6 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)
Z : ECO (Ecological Element, Halogen Free)

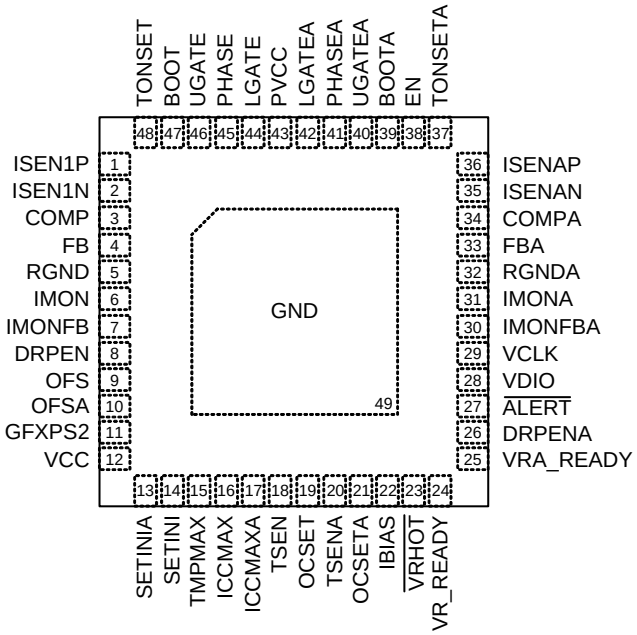
Note :

Richtek Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



WQFN-48L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	ISEN1P	Positive Current Sense Input of CORE VR
2	ISEN1N	Negative Current Sense Input of CORE VR
3	COMP	CORE VR Compensation. This pin is the output node of the error amplifier.
4	FB	CORE VR Feedback. This is the negative input node of the error amplifier.
5	RGND	Return Ground for CORE VR. This pin is the negative input for differential remote voltage sensing.
6	IMON	Current Monitor Output of CORE VR. The output voltage V_{IMON} of this pin is proportional to the output current. For digital output current reporting, detailed V_{IMON} is generated by built-in ADC.
7	IMONFB	This pin is used to externally set the current monitor output gain of CORE VR. Connect this pin with one resistor R_{IMONFB} to CORE VCC_SENSE while IMON pin is connected to ground with another resistor, R_{IMON}. The current monitor output gain can be set by the ratio of these two resistors.
8	DRPEN	Droop Enable Mode Setting of CORE VR. An internal 80μA current source is connected to the DRPEN pin and flows out of this pin for 10μs. Connect this pin to V_{CC} to enable droop function. Connect this pin to GND to disable droop function.
9	OFS	Output Voltage No-Load Offset Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{OFS} for offset setting. Connect this pin to GND for no offset setting.
10	OFSA	Output Voltage No-Load Offset Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{OFSA} for offset setting. Connect this pin to GND for no offset setting.

To be continued

Pin No.	Pin Name	Pin Function
11	GFXPS2	Forced DEM Enable Setting of GFX VR. Connect to V_{CC} for forced-DEM setting and connect to GND for following SVID power state command.
12	VCC	5V Power Supply Input of Controller. Bypass this pin to GND with a 1μF or greater ceramic capacitor.
13	SETINIA	Initial Startup Voltage V_{INI_GFX} Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage $V_{SETINIA}$ for GFX VR initial startup voltage V_{INI_GFX} setting. Connect this pin to GND for 0V V_{INI_GFX} setting.
14	SETINI	Initial Startup Voltage V_{INI_CORE} Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{SETINI} for CORE VR initial startup voltage V_{INI_CORE} setting. Connect this pin to GND for 0V V_{INI_CORE} setting.
15	TMPMAX	Maximum Temperature Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{TMPMAX} for TMPMAX setting.
16	ICCMAX	Maximum Current Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{ICCMAX} for ICCMAX setting.
17	ICCMAXA	Maximum Current Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage $V_{ICCMAXA}$ for ICCMAXA setting.
18	TSEN	Thermal Monitor Sense Pin of CORE VR.
19	OCSET	Over Current Protection Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{OCSET} from 0 to 3.3V for CORE VR over current protection threshold.
20	TSENA	Thermal Monitor Sense Pin of GFX VR.
21	OCSETA	Over Current Protection Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to adjust the pin voltage V_{OCSETA} from 0 to 3.3V for GFX VR over current protection threshold.
22	IBIAS	Internal bias current setting. Connect a 53.6kΩ resistor from IBIAS pin to GND.
23	$\overline{\text{VRHOT}}$	Thermal Monitor Output (Active Low). Connect a pull high resistor from $\overline{\text{VRHOT}}$ pin to 1.05V.
24	VR_READY	Voltage Ready Indicator of CORE VR. Connect a pull high resistor from VR_READY pin to 1.05V.
25	VRA_READY	Voltage Ready Indicator GFX VR. Connect a pull high resistor from VRA_READY pin to 1.05V.
26	DRPENA	Droop Enable Mode Setting of GFX VR. An internal 80μA current source is connected to DRPENA pin and flows out of this pin for 10μs. Connect this pin to V_{CC} to enable droop function. Connect this pin to GND to disable droop function.
27	$\overline{\text{ALERT}}$	SVID Alert Pin (Active Low). Connect a 75Ω resistor from $\overline{\text{ALERT}}$ pin to 1.05V.
28	VDIO	Controller and CPU Data Transmission Interface. Connecting a 64.9Ω resistor between VDIO pin to 1.05V.
29	VCLK	Synchronous Clock from the CPU. Connect a 64.9Ω resistor from VCLK pin to 1.05V.
30	IMONFBA	This pin is used to externally set the current monitor output gain of GFX VR. Connect this pin with one resistor $R_{IMONFBA}$ to GFX VCC_SENSE while IMON pin is connected to ground with another resistor R_{IMONA}. The current monitor output gain can be set by the ratio of these two resistors.
31	IMONA	Current Monitor Output of GFX VR. The output voltage VIMONA of this pin is proportional to the output current. For digital output current reporting, detailed VIMONA is generated by built-in ADC.

To be continued

Pin No.	Pin Name	Pin Function
32	RGNDA	Return Ground for GFX VR. This pin is the negative input for differential remote voltage sensing.
33	FBA	GFX VR Feedback. This is the negative input node of the error amplifier.
34	COMPA	GFX VR Compensation. This pin is the output node of the error amplifier.
35	ISENAN	Negative Current Sense Input of GFX VR.
36	ISENAP	Positive Current Sense Input of GFX VR.
37	TONSETA	On-Time Setting of GFX VR. Connect this pin to VIN with one resistor.
38	EN	Chip Enable (Active High).
39	BOOTA	Bootstrap Flying Capacitor Connection for GFX VR. This pin powers the high side MOSFET drivers. Connect this pin to PHASEA with an external ceramic capacitor.
40	UGATEA	High Side MOSFET Floating Gate Driver Output for GFX VR. Connect this pin to the gate of high side MOSFET.
41	PHASEA	Switching Node Connection for GFX VR. PHASEA is also the zero cross detect input for GFX VR. Connect this pin to the high side MOSFET sources together with the low side MOSFET drains and the inductor.
42	LGATEA	Synchronous-Rectifier Gate Driver Output of GFX VR. Connect this pin to the gate of low side MOSFET.
43	PVCC	5V Power Supply of Driver. Bypass this pin to GND with a 1μF or greater ceramic capacitor.
44	LGATE	Synchronous-Rectifier Gate Driver Output of CORE VR. Connect this pin to the gate of low side MOSFET.
45	PHASE	Switching Node Connection for CORE VR. PHASE is the internal lower supply rail for the UGATE. PHASE is also the zero cross detect input for CORE VR. Connect this pin to the high side MOSFET sources together with the low side MOSFET drains and the inductor.
46	UGATE	High Side MOSFET Floating Gate Driver Output for CORE VR. Connect this pin to the gate of high side MOSFET.
47	BOOT	Bootstrap Flying Capacitor Connection for CORE VR. This pin powers the high side MOSFET drivers. Connect this pin to PHASE with an external ceramic capacitor.
48	TONSET	On-Time Setting of CORE VR. Connect this pin to VIN with one resistor.
49 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Typical Application Circuit

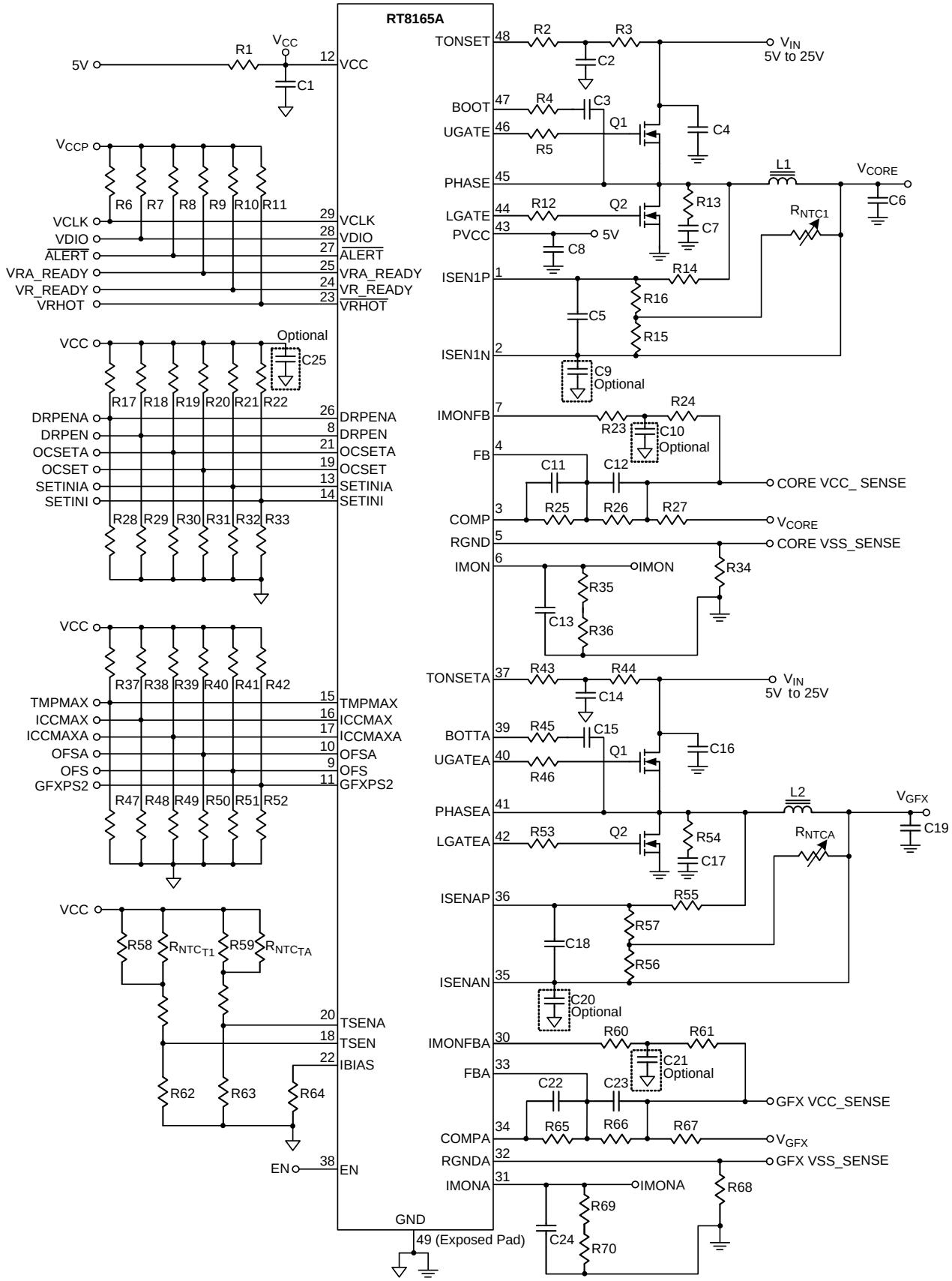


Figure 1. Dual Output Application Circuit

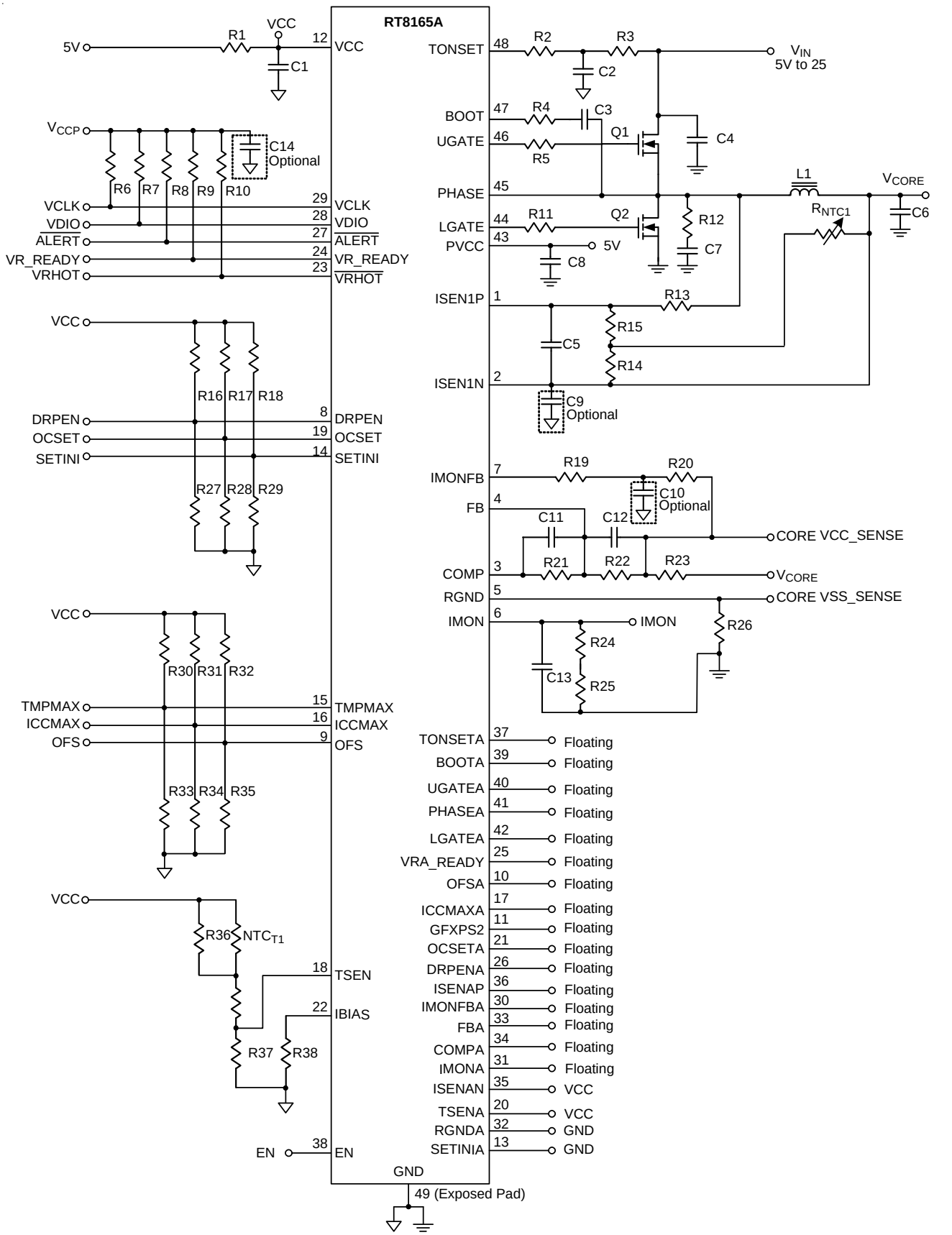


Figure 2. Single Output Application Circuit

Function Block Diagram

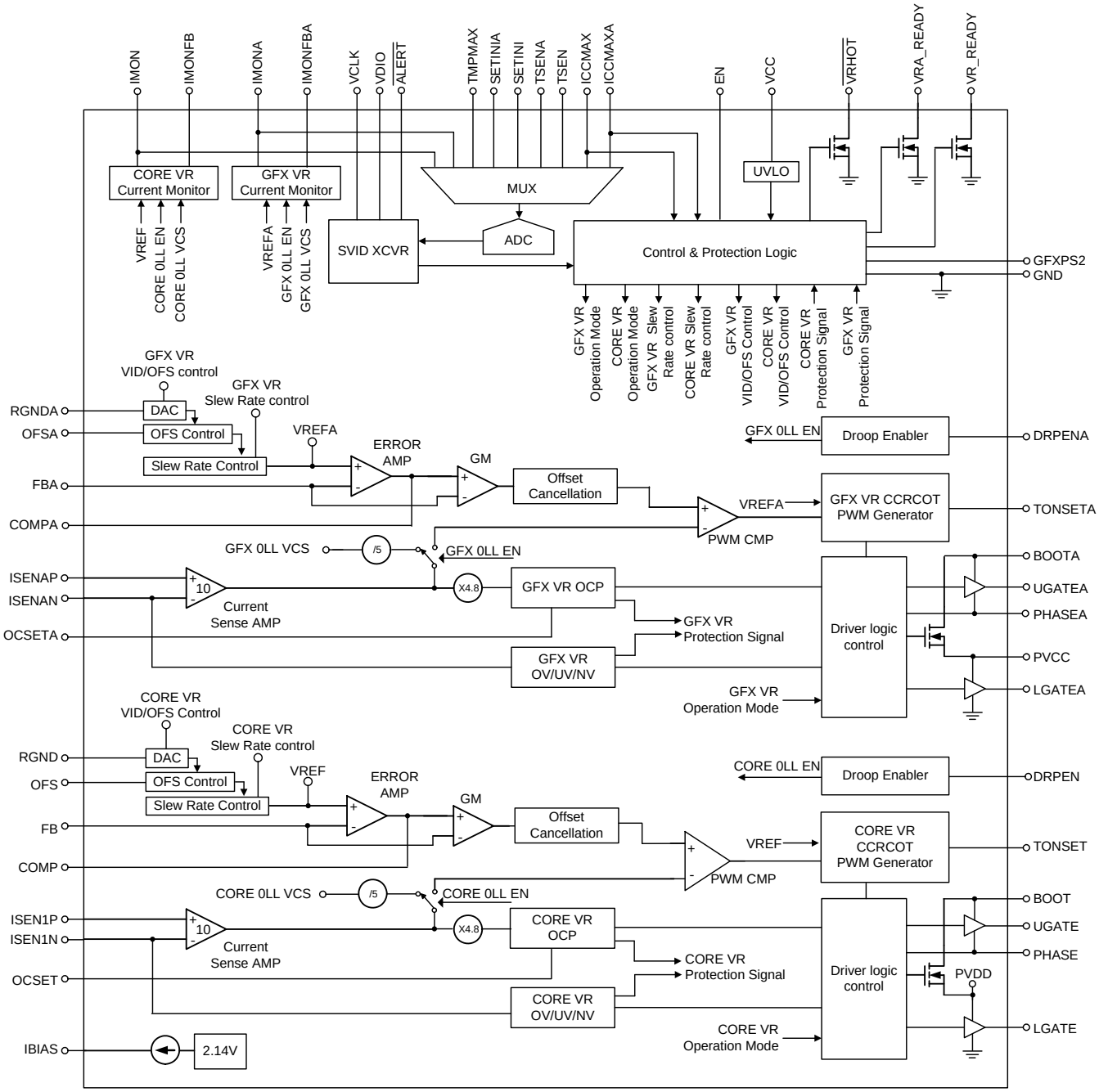


Table 1. IMVP7/VR12 Compliant VID Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	VDAC Voltage
0	0	0	0	0	0	0	0	0	0	0.000
0	0	0	0	0	0	0	1	0	1	0.250
0	0	0	0	0	0	1	0	0	2	0.255
0	0	0	0	0	0	1	1	0	3	0.260
0	0	0	0	0	1	0	0	0	4	0.265
0	0	0	0	0	1	0	1	0	5	0.270
0	0	0	0	0	1	1	0	0	6	0.275
0	0	0	0	0	1	1	1	0	7	0.280
0	0	0	0	1	0	0	0	0	8	0.285
0	0	0	0	1	0	0	1	0	9	0.290
0	0	0	0	1	0	1	0	0	A	0.295
0	0	0	0	1	0	1	1	0	B	0.300
0	0	0	0	1	1	0	0	0	C	0.305
0	0	0	0	1	1	0	1	0	D	0.310
0	0	0	0	1	1	1	0	0	E	0.315
0	0	0	0	1	1	1	1	0	F	0.320
0	0	0	1	0	0	0	0	1	0	0.325
0	0	0	1	0	0	0	1	1	1	0.330
0	0	0	1	0	0	1	0	1	2	0.335
0	0	0	1	0	0	1	1	1	3	0.340
0	0	0	1	0	1	0	0	1	4	0.345
0	0	0	1	0	1	0	1	1	5	0.350
0	0	0	1	0	1	1	0	1	6	0.355
0	0	0	1	0	1	1	1	1	7	0.360
0	0	0	1	1	0	0	0	1	8	0.365
0	0	0	1	1	0	0	1	1	9	0.370
0	0	0	1	1	0	1	0	1	A	0.375
0	0	0	1	1	0	1	1	1	B	0.380
0	0	0	1	1	1	0	0	1	C	0.385
0	0	0	1	1	1	0	1	1	D	0.390
0	0	0	1	1	1	1	0	1	E	0.395
0	0	0	1	1	1	1	1	1	F	0.400
0	0	1	0	0	0	0	0	2	0	0.405
0	0	1	0	0	0	0	1	2	1	0.410
0	0	1	0	0	0	1	0	2	2	0.415

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	0	1	0	0	0	1	1	2	3	0.420
0	0	1	0	0	1	0	0	2	4	0.425
0	0	1	0	0	1	0	1	2	5	0.430
0	0	1	0	0	1	1	0	2	6	0.435
0	0	1	0	0	1	1	1	2	7	0.440
0	0	1	0	1	0	0	0	2	8	0.445
0	0	1	0	1	0	0	1	2	9	0.450
0	0	1	0	1	0	1	0	2	A	0.455
0	0	1	0	1	0	1	1	2	B	0.460
0	0	1	0	1	1	0	0	2	C	0.465
0	0	1	0	1	1	0	1	2	D	0.470
0	0	1	0	1	1	1	0	2	E	0.475
0	0	1	0	1	1	1	1	2	F	0.480
0	0	1	1	0	0	0	0	3	0	0.485
0	0	1	1	0	0	0	1	3	1	0.490
0	0	1	1	0	0	1	0	3	2	0.495
0	0	1	1	0	0	1	1	3	3	0.500
0	0	1	1	0	1	0	0	3	4	0.505
0	0	1	1	0	1	0	1	3	5	0.510
0	0	1	1	0	1	1	0	3	6	0.515
0	0	1	1	0	1	1	1	3	7	0.520
0	0	1	1	1	0	0	0	3	8	0.525
0	0	1	1	1	0	0	1	3	9	0.530
0	0	1	1	1	0	1	0	3	A	0.535
0	0	1	1	1	0	1	1	3	B	0.540
0	0	1	1	1	1	0	0	3	C	0.545
0	0	1	1	1	1	0	1	3	D	0.550
0	0	1	1	1	1	1	0	3	E	0.555
0	0	1	1	1	1	1	1	3	F	0.560
0	1	0	0	0	0	0	0	4	0	0.565
0	1	0	0	0	0	0	1	4	1	0.570
0	1	0	0	0	0	1	0	4	2	0.575
0	1	0	0	0	0	1	1	4	3	0.580
0	1	0	0	0	1	0	0	4	4	0.585
0	1	0	0	0	1	0	1	4	5	0.590

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	1	0	0	0	1	1	0	4	6	0.595
0	1	0	0	0	1	1	1	4	7	0.600
0	1	0	0	1	0	0	0	4	8	0.605
0	1	0	0	1	0	0	1	4	9	0.610
0	1	0	0	1	0	1	0	4	A	0.615
0	1	0	0	1	0	1	1	4	B	0.620
0	1	0	0	1	1	0	0	4	C	0.625
0	1	0	0	1	1	0	1	4	D	0.630
0	1	0	0	1	1	1	0	4	E	0.635
0	1	0	0	1	1	1	1	4	F	0.640
0	1	0	1	0	0	0	0	5	0	0.645
0	1	0	1	0	0	0	1	5	1	0.650
0	1	0	1	0	0	1	0	5	2	0.655
0	1	0	1	0	0	1	1	5	3	0.660
0	1	0	1	0	1	0	0	5	4	0.665
0	1	0	1	0	1	0	1	5	5	0.670
0	1	0	1	0	1	1	0	5	6	0.675
0	1	0	1	0	1	1	1	5	7	0.680
0	1	0	1	1	0	0	0	5	8	0.685
0	1	0	1	1	0	0	1	5	9	0.690
0	1	0	1	1	0	1	0	5	A	0.695
0	1	0	1	1	0	1	1	5	B	0.700
0	1	0	1	1	1	0	0	5	C	0.705
0	1	0	1	1	1	0	1	5	D	0.710
0	1	0	1	1	1	1	0	5	E	0.715
0	1	0	1	1	1	1	1	5	F	0.720
0	1	1	0	0	0	0	0	6	0	0.725
0	1	1	0	0	0	0	1	6	1	0.730
0	1	1	0	0	0	1	0	6	2	0.735
0	1	1	0	0	0	1	1	6	3	0.740
0	1	1	0	0	1	0	0	6	4	0.745
0	1	1	0	0	1	0	1	6	5	0.750
0	1	1	0	0	1	1	0	6	6	0.755
0	1	1	0	0	1	1	1	6	7	0.760
0	1	1	0	1	0	0	0	6	8	0.765
0	1	1	0	1	0	0	1	6	9	0.770

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	1	1	0	1	0	1	0	6	A	0.775
0	1	1	0	1	0	1	1	6	B	0.780
0	1	1	0	1	1	0	0	6	C	0.785
0	1	1	0	1	1	0	1	6	D	0.790
0	1	1	0	1	1	1	0	6	E	0.795
0	1	1	0	1	1	1	1	6	F	0.800
0	1	1	1	0	0	0	0	7	0	0.805
0	1	1	1	0	0	0	1	7	1	0.810
0	1	1	1	0	0	1	0	7	2	0.815
0	1	1	1	0	0	1	1	7	3	0.820
0	1	1	1	0	1	0	0	7	4	0.825
0	1	1	1	0	1	0	1	7	5	0.830
0	1	1	1	0	1	1	0	7	6	0.835
0	1	1	1	0	1	1	1	7	7	0.840
0	1	1	1	1	0	0	0	7	8	0.845
0	1	1	1	1	0	0	1	7	9	0.850
0	1	1	1	1	0	1	0	7	A	0.855
0	1	1	1	1	0	1	1	7	B	0.860
0	1	1	1	1	1	0	0	7	C	0.865
0	1	1	1	1	1	0	1	7	D	0.870
0	1	1	1	1	1	1	0	7	E	0.875
0	1	1	1	1	1	1	1	7	F	0.880
1	0	0	0	0	0	0	0	8	0	0.885
1	0	0	0	0	0	0	1	8	1	0.890
1	0	0	0	0	0	1	0	8	2	0.895
1	0	0	0	0	0	1	1	8	3	0.900
1	0	0	0	0	1	0	0	8	4	0.905
1	0	0	0	0	1	0	1	8	5	0.910
1	0	0	0	0	1	1	0	8	6	0.915
1	0	0	0	0	1	1	1	8	7	0.920
1	0	0	0	1	0	0	0	8	8	0.925
1	0	0	0	1	0	0	1	8	9	0.930
1	0	0	0	1	0	1	0	8	A	0.935
1	0	0	0	1	0	1	1	8	B	0.940
1	0	0	0	1	1	0	0	8	C	0.945
1	0	0	0	1	1	0	1	8	D	0.950

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	0	0	0	1	1	1	0	8	E	0.955
1	0	0	0	1	1	1	1	8	F	0.960
1	0	0	1	0	0	0	0	9	0	0.965
1	0	0	1	0	0	0	1	9	1	0.970
1	0	0	1	0	0	1	0	9	2	0.975
1	0	0	1	0	0	1	1	9	3	0.980
1	0	0	1	0	1	0	0	9	4	0.985
1	0	0	1	0	1	0	1	9	5	0.990
1	0	0	1	0	1	1	0	9	6	0.995
1	0	0	1	0	1	1	1	9	7	1.000
1	0	0	1	1	0	0	0	9	8	1.005
1	0	0	1	1	0	0	1	9	9	1.010
1	0	0	1	1	0	1	0	9	A	1.015
1	0	0	1	1	0	1	1	9	B	1.020
1	0	0	1	1	1	0	0	9	C	1.025
1	0	0	1	1	1	0	1	9	D	1.030
1	0	0	1	1	1	1	0	9	E	1.035
1	0	0	1	1	1	1	1	9	F	1.040
1	0	1	0	0	0	0	0	A	0	1.045
1	0	1	0	0	0	0	1	A	1	1.050
1	0	1	0	0	0	1	0	A	2	1.055
1	0	1	0	0	0	1	1	A	3	1.060
1	0	1	0	0	1	0	0	A	4	1.065
1	0	1	0	0	1	0	1	A	5	1.070
1	0	1	0	0	1	1	0	A	6	1.075
1	0	1	0	0	1	1	1	A	7	1.080
1	0	1	0	1	0	0	0	A	8	1.085
1	0	1	0	1	0	0	1	A	9	1.090
1	0	1	0	1	0	1	0	A	A	1.095
1	0	1	0	1	0	1	1	A	B	1.100
1	0	1	0	1	1	0	0	A	C	1.105
1	0	1	0	1	1	0	1	A	D	1.110
1	0	1	0	1	1	1	0	A	E	1.115
1	0	1	0	1	1	1	1	A	F	1.120
1	0	1	1	0	0	0	0	B	0	1.125
1	0	1	1	0	0	0	1	B	1	1.130

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	0	1	1	0	0	1	0	B	2	1.135
1	0	1	1	0	0	1	1	B	3	1.140
1	0	1	1	0	1	0	0	B	4	1.145
1	0	1	1	0	1	0	1	B	5	1.150
1	0	1	1	0	1	1	0	B	6	1.155
1	0	1	1	0	1	1	1	B	7	1.160
1	0	1	1	1	0	0	0	B	8	1.165
1	0	1	1	1	0	0	1	B	9	1.170
1	0	1	1	1	0	1	0	B	A	1.175
1	0	1	1	1	0	1	1	B	B	1.180
1	0	1	1	1	1	0	0	B	C	1.185
1	0	1	1	1	1	0	1	B	D	1.190
1	0	1	1	1	1	1	0	B	E	1.195
1	0	1	1	1	1	1	1	B	F	1.200
1	1	0	0	0	0	0	0	C	0	1.205
1	1	0	0	0	0	0	1	C	1	1.210
1	1	0	0	0	0	1	0	C	2	1.215
1	1	0	0	0	0	1	1	C	3	1.220
1	1	0	0	0	1	0	0	C	4	1.225
1	1	0	0	0	1	0	1	C	5	1.230
1	1	0	0	0	1	1	0	C	6	1.235
1	1	0	0	0	1	1	1	C	7	1.240
1	1	0	0	1	0	0	0	C	8	1.245
1	1	0	0	1	0	0	1	C	9	1.250
1	1	0	0	1	0	1	0	C	A	1.255
1	1	0	0	1	0	1	1	C	B	1.260
1	1	0	0	1	1	0	0	C	C	1.265
1	1	0	0	1	1	0	1	C	D	1.270
1	1	0	0	1	1	1	0	C	E	1.275
1	1	0	0	1	1	1	1	C	F	1.280
1	1	0	1	0	0	0	0	D	0	1.285
1	1	0	1	0	0	0	1	D	1	1.290
1	1	0	1	0	0	1	0	D	2	1.295
1	1	0	1	0	0	1	1	D	3	1.300
1	1	0	1	0	1	0	0	D	4	1.305
1	1	0	1	0	1	0	1	D	5	1.310

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	1	0	1	0	1	1	0	D	6	1.315
1	1	0	1	0	1	1	1	D	7	1.320
1	1	0	1	1	0	0	0	D	8	1.325
1	1	0	1	1	0	0	1	D	9	1.330
1	1	0	1	1	0	1	0	D	A	1.335
1	1	0	1	1	0	1	1	D	B	1.340
1	1	0	1	1	1	0	0	D	C	1.345
1	1	0	1	1	1	0	1	D	D	1.350
1	1	0	1	1	1	1	0	D	E	1.355
1	1	0	1	1	1	1	1	D	F	1.360
1	1	1	0	0	0	0	0	E	0	1.365
1	1	1	0	0	0	0	1	E	1	1.370
1	1	1	0	0	0	1	0	E	2	1.375
1	1	1	0	0	0	1	1	E	3	1.380
1	1	1	0	0	1	0	0	E	4	1.385
1	1	1	0	0	1	0	1	E	5	1.390
1	1	1	0	0	1	1	0	E	6	1.395
1	1	1	0	0	1	1	1	E	7	1.400
1	1	1	0	1	0	0	0	E	8	1.405
1	1	1	0	1	0	0	1	E	9	1.410
1	1	1	0	1	0	1	0	E	A	1.415
1	1	1	0	1	0	1	1	E	B	1.420
1	1	1	0	1	1	0	0	E	C	1.425
1	1	1	0	1	1	0	1	E	D	1.430
1	1	1	0	1	1	1	0	E	E	1.435
1	1	1	0	1	1	1	1	E	F	1.440
1	1	1	1	0	0	0	0	F	0	1.445
1	1	1	1	0	0	0	1	F	1	1.450
1	1	1	1	0	0	1	0	F	2	1.455
1	1	1	1	0	0	1	1	F	3	1.460
1	1	1	1	0	1	0	0	F	4	1.465
1	1	1	1	0	1	0	1	F	5	1.470
1	1	1	1	0	1	1	0	F	6	1.475
1	1	1	1	0	1	1	1	F	7	1.480
1	1	1	1	1	0	0	0	F	8	1.485

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	1	1	1	1	0	0	1	F	9	1.490
1	1	1	1	1	0	1	0	F	A	1.495
1	1	1	1	1	0	1	1	F	B	1.500
1	1	1	1	1	1	0	0	F	C	1.505
1	1	1	1	1	1	0	1	F	D	1.510
1	1	1	1	1	1	1	0	F	E	1.515
1	1	1	1	1	1	1	1	F	F	1.520

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- PVCC to GND ---------- –0.3V to 6.5V
- RGNDx to GND ---------- –0.3V to 0.3V
- TONSETx to GND ---------- –0.3V to 28V
- Others ---------- –0.3V to (VCC + 0.3V)
- BOOTx to PHASEx ---------- –0.3V to 6.5V
- PHASEx to GND
  - DC ---------- –0.3V to 28V
  - <20ns ---------- –8V to 32V
- UGATEx to PHASEx
  - DC ---------- –0.3V to (BOOTx – PHASEx)
  - <20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to (PVCC – 0.3V)
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–48L 6x6 ---------- 2.857W
- Package Thermal Resistance (Note 2)
  - WQFN–48L 6x6, θ_{JA} ---------- 35°C/W
  - WQFN–48L 6x6, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage of Controller, V_{CC} ---------- 4.5V to 5.5V
- Supply Voltage of Gate Driver, V_{PVCC} ---------- 4.5V to 5.5V
- Battery Input Voltage, V_{IN} ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Input Voltage Range	V_{CC}/V_{PVCC}	V_{EN} = 1.05V, Not Switching	4.5	5	5.5	V
	V_{IN}	Battery Input Voltage	5	--	25	V
Supply Current (V_{CC} + PVCC)	I_{VCC} + I_{PVCC}	V_{EN} = 1.05V, Not Switching	--	12	20	mA
Supply Current (TONSETx)	$I_{TONSETx}$	V_{FB} =1V, V_{IN} = 12V, R_{TON} = 100kΩ	--	110	--	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current (PVCC + V_{CC})	I_{VCC_SHDN} + I_{PVCC_SHDN}	V_{EN} = 0V	--	--	5	μA
Shutdown Current (TONSETx)	$I_{TONSETx_SHDN}$	V_{EN} = 0V	--	--	5	μA
TON Setting						
TONSETx Voltage	$V_{TONSETx}$	I_{RTON} = 80μA, V_{FBx} = 1V	0.95	1.075	1.2	0V
On-Time	t_{ON}	I_{RTON} = 80μA, V_{FBx} = 1V	315	350	385	ns
TONSETx Input Current Range	I_{RTON}	V_{FBx} = 1.1V	25	--	280	μA
Minimum Off-Time	T_{OFF_MIN}		--	350	--	ns
Droop Enable / Disable						
DRPENx Internal Current Source	I_{DRPENx}	EN goes high within 10μs	--	80	--	μA
Droop Enable Threshold	V_{DRPENx}	Detect V_{DRPENx}, EN goes high within 10μs	4.5	--	--	V
Droop Disable Threshold	V_{DRPENx}	Detect V_{DRPENx}, EN goes high within 10μs	--	--	2	V
GFX VR Forced DEM						
GFXPS2x Enable Threshold	V_{GFXPS}		4.3	--	--	V
GFXPS2x Disable Threshold	V_{GFXPS}		--	--	0.7	V
References and System Output Voltage						
DAC Accuracy (PS0/PS1)	V_{FBx}	VID_{SVID} Setting = 1.000V~1.520V OFS_{SVID} Setting = 0V	–0.5	0	0.5	%VID
		VID_{SVID} Setting = 0.800V~1.000V OFS_{SVID} Setting = 0V	–5	0	5	mV
		VID_{SVID} Setting = 0.500V~0.800V OFS_{SVID} Setting = 0V	–8	0	8	
		VID_{SVID} Setting = 0.250V~0.500V OFS_{SVID} Setting = 0V	–8	0	8	
		VID_{SVID} Setting = 1.100V OFS_{SVID} Setting = –0.640V~0.635V	–10	0	10	
SETINIx Voltage	$V_{SETINIx}$	V_{INI_CORE} = 0V, V_{INI_GFX} = 0V	0	0.3125	0.5125	V
		V_{INI_CORE} = 0.9V, V_{INI_GFX} = 0.9V	0.7375	0.9375	1.1375	
		V_{INI_CORE} = 1V, V_{INI_GFX} = 1V	1.3625	1.5625	1.7625	
		V_{INI_CORE} = 1.1V, V_{INI_GFX} = 1.1V	2.6125	--	5	
External OFSx Voltage	V_{OFSx}	Offset = 100mV	68	72	--	$\%V_{CC}$
		Offset = 50mV	52	56	60	
		Offset = –50mV	36	40	44	
		Offset = –100mV	20	24	28	
		No Offset Voltage	0	8	12	
Impedance of OFSx Pin	R_{OFSx}		1	--	--	MΩ

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 53.6kΩ	2.09	2.14	2.19	V
Dynamic VID Slew Rate	SR_{DVID}	SetVID Slow	2.5	3.125	3.75	mV/μs
		SetVID Fast	10	12.5	15	
Error Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ (Note5)	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF (Note5)	--	10	--	MHz
Slew Rate	SR_{COMP}	C_{LOAD} = 10pF (Gain = –4, R_{LOAD_COMP} = 47kΩ, V_{COMPx} = 0.5V to 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
MAX Source/Sink Current	I_{COMP}	V_{COMP} = 2V	--	250	--	μA
Impedance of FBx	R_{FBx}		1	--	--	MΩ
Current Sense Amplifier						
Input Offset Voltage	V_{OFS_CSA}		–1	--	1	mV
Impedance of Neg. Input	R_{ISENxN}		1	--	--	MΩ
Impedance of Pos. Input	R_{ISENxP}		1	--	--	MΩ
Current Sense Differential Input Range	V_{CSDIx}	V_{FBx} = 1.1V, $V_{CSDIx} = V_{ISENxP} - V_{ISENxN}$	–50	--	100	mV
Current Sense DC Gain (Loop)	A_I	V_{FBx} = 1.1V, –30mV < V_{CSDIx} < 50mV	--	10	--	V/V
V_{ISEN} Linearity	V_{ISEN_ACC}	V_{DAC} = 1.1V –30mV < V_{ISEN_IN} < 50mV	–1	--	1	%
Digital Current Monitor						
Current Monitor Output Voltage (Droop Enabled)	V_{IMONx_ENLL}	V_{FBx} = 1V, V_{ISENxN} = 0.9V, $V_{RIMONFBx}$ = 10k, R_{IMONx} = 160k	--	1.6	--	V
Current Monitor Output Voltage (Droop Disabled)	V_{IMONx_DISLL}	$V_{CSDIx} = V_{ISENxP} - V_{ISENxN}$ = 100mV V_{FBx} = 1V, $V_{RIMONFBx}$ = 10k, R_{IMONx} = 80k	--	1.6	--	V
IMON Voltage Range	V_{IMON}		0	--	3.3	V
Digital IMON LSB		3.3V / 255 = 12.94mV	--	12.94	--	mV
Digital Code of IMON	C_{DIMON}	V_{IMONx} = 388.3mV, DIOUT [7 : 0] = 30	27	30	33	Decimal
		V_{IMONx} = 776.5mV, DIOUT [7 : 0] = 60	57	60	63	Decimal
		V_{IMONx} = 1164.7mV, DIOUT [7 : 0] = 90	87	90	93	Decimal
Update Period of Digital Current Monitor	t_{IMON}		--	1600	--	μs
Gate Driver						
Upper Driver Source	R_{UGATEx_sr}	$V_{BOOTx} - V_{PHASEx}$ = 5V $V_{BOOTx} - V_{UGATEx}$ = 0.1V	--	1	--	Ω
Upper Driver Sink	R_{UGATEx_sk}	V_{UGATEx} = 0.1V	--	1	--	Ω
Lower Driver Source	R_{LGATEx_sr}	PVCC = 5V, PVCC – V_{LGATEx} = 0.1V	--	1	--	Ω
Lower Driver Sink	R_{LGATEx_sk}	V_{LGATEx} = 0.1V	--	0.5	--	Ω
Internal Boot Charging Switch On-Resistance	R_{BOOTx}	PVCC to BOOTx	--	30	--	Ω

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Zero Current Detection Threshold		V_{ZCD_TH}	V_{ZCD_TH} = GND − V_{PHASEx}	--	10	--	mV
Protection							
Under Voltage Lock-out Threshold		V_{UVLO}	VCC Falling edge	4.04	4.24	--	V
Under Voltage Lock-out Hysteresis		ΔV_{UVLO}		--	100	--	mV
Over Voltage Protection Threshold		V_{OVP}	Respect to $VOUT_MAX_{SVID}$, with 1µs filter time	100	150	200	mV
Under Voltage Protection Threshold		V_{UVP}	V_{UVP} = V_{ISENxN} − V_{REFx}, 0.8V < V_{REFx} <1.52V, with 3µs filter time	−350	−300	−250	mV
Negative Voltage Protection Threshold		V_{NVP}	V_{NVP} = V_{ISENxN} − GND	−100	−50	--	mV
Current Sense Gain for Over Current Protection		A_{OC}	V_{OCSET} = 2.4V V_{ISENxP} − V_{ISENxN} = 50mV	--	48	--	V/V
Logic Inputs							
EN Input Threshold Voltage	Logic-High	V_{IH}	With respect to 1V, 70%	0.7	--	--	V
	Logic-Low	V_{IL}	With respect to 1V, 30%	--	--	0.3	V
Leakage Current of EN				−1	--	1	µA
VCLK,VDIO Input Threshold Voltage		V_{IH}	With respect to Intel Spec.	0.65	--	--	V
		V_{IL}	With respect to Intel Spec.	--	--	0.45	V
Leakage Current of VCLK, VDIO		I_{LEAK_IN}		−1	--	1	µA
$\overline{ALERT}$							
$\overline{ALERT}$ Low Voltage		$V_{\overline{ALERT}}$	$I_{\overline{ALERT}_SINK}$ = 4mA	--	--	0.4	V
VR Ready							
VRx_READY Low Voltage		V_{VRx_READY}	$I_{VRx_READY_SINK}$ = 4mA	--	--	0.4	V
VRx_READY Delay		t_{VRx_READY}	V_{ISENxN} = V_{BOOT} to V_{VRx_READY} high	70	100	160	µs
Thermal Throttling							
$\overline{VRHOT}$ Output Voltage		$V_{\overline{VRHOT}}$	$I_{\overline{VRHOT}_SINK}$ = 40mA	--	0.4	--	V
High Impedance Output							
$\overline{ALERT}$, VRx_READY, $\overline{VRHOT}$		I_{LEAK_OUT}		−1	--	1	µA
Temperature Zone							
TSEN Threshold for Tmp_Zone [7] transition		V_{TSENx}	100°C	--	1.8725	--	V
TSEN Threshold for Tmp_Zone [6] transition			97°C	--	1.8175	--	V
TSEN Threshold for Tmp_Zone [5] transition			94°C	--	1.7625	--	V
TSEN Threshold for Tmp_Zone [4] transition			91°C	--	1.7075	--	V
TSEN Threshold for Tmp_Zone [3] transition			88°C	--	1.6525	--	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TSEN Threshold for Tmp_Zone [2] transition	V_{TSENx}	85°C	--	1.5975	--	V
TSEN Threshold for Tmp_Zone [1] transition		82°C	--	1.5425	--	V
TSEN Threshold for Tmp_Zone [0] transition		75°C	--	1.4875	--	V
Update Period	t_{TSEN}		--	1600	--	μs
ADC						
Latency	t_{LAT}		--	--	400	μs
Digital Code of ICCMAX	$C_{ICCMAX1}$	V_{ICCMAX} = 0.637V	29	32	35	decimal
	$C_{ICCMAX2}$	V_{ICCMAX} = 1.2642V	61	64	67	decimal
	$C_{ICCMAX3}$	V_{ICCMAX} = 2.5186V	125	128	131	decimal
Digital Code of ICCMAXA	$C_{ICCMAXA1}$	$V_{ICCMAXA}$ = 0.1666V	5	8	11	decimal
	$C_{ICCMAXA2}$	$V_{ICCMAXA}$ = 0.3234V	13	16	19	decimal
	$C_{ICCMAXA3}$	$V_{ICCMAXA}$ = 0.637V	29	32	35	decimal
Digital Code of TMPMAX	$C_{TMPMAX1}$	V_{TMPMAX} = 1.6758V	82	85	88	decimal
	$C_{TMPMAX2}$	V_{TMPMAX} = 1.9698V	97	100	103	decimal
	$C_{TMPMAX3}$	V_{TMPMAX} = 2.4598V	122	125	128	decimal

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

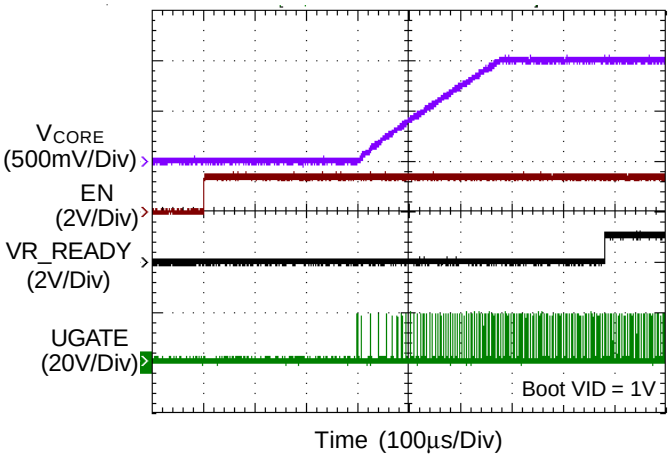
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

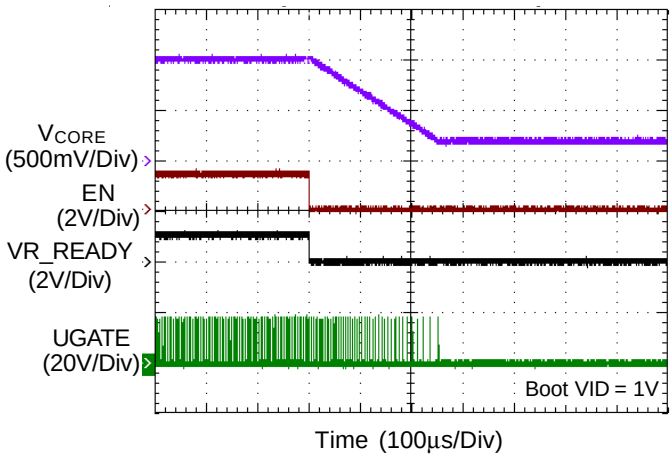
Note 5. Guaranteed by design.

Typical Operating Characteristics

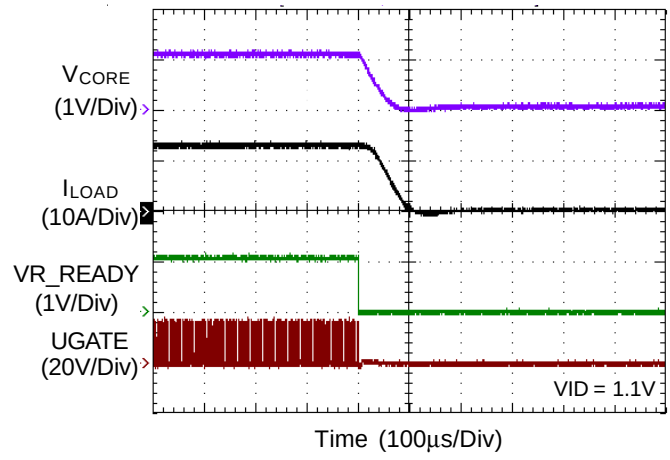
CORE VR Power On from EN



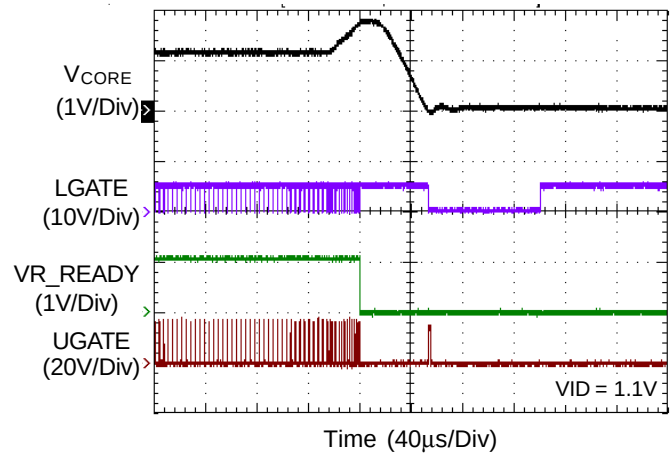
CORE VR Power Off from EN



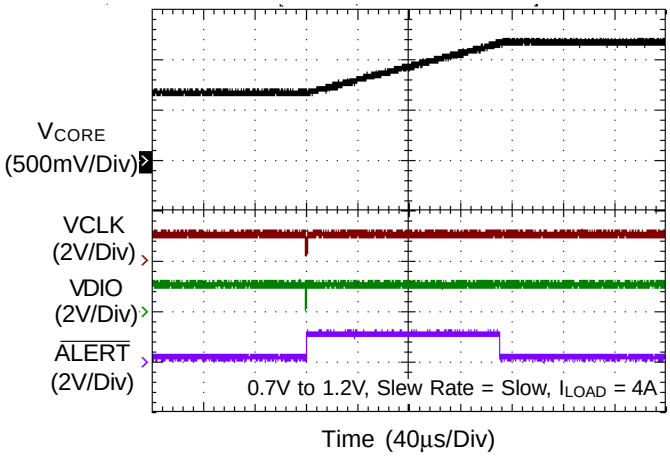
CORE VR OCP



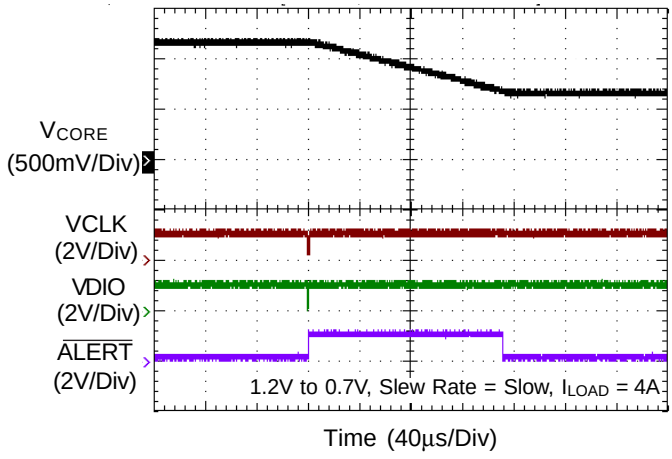
CORE VR OVP and NVP



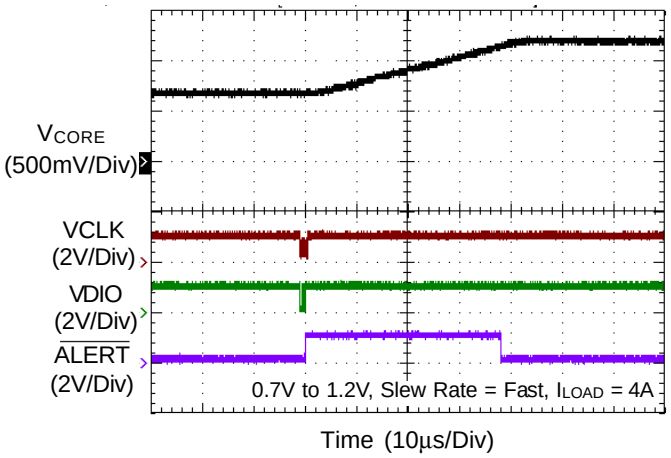
CORE VR Dynamic VID Up



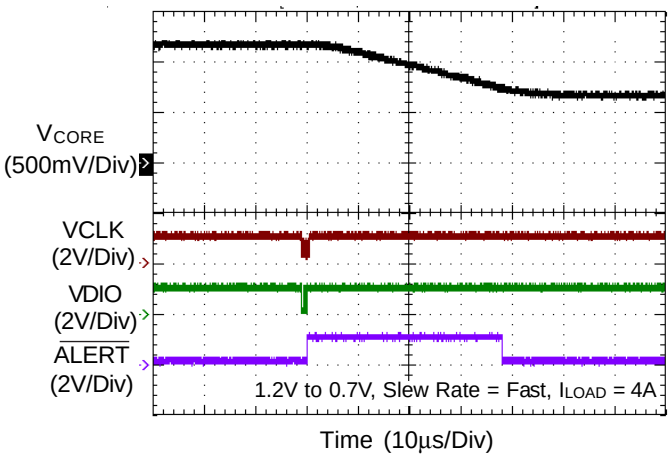
CORE VR Dynamic VID Down



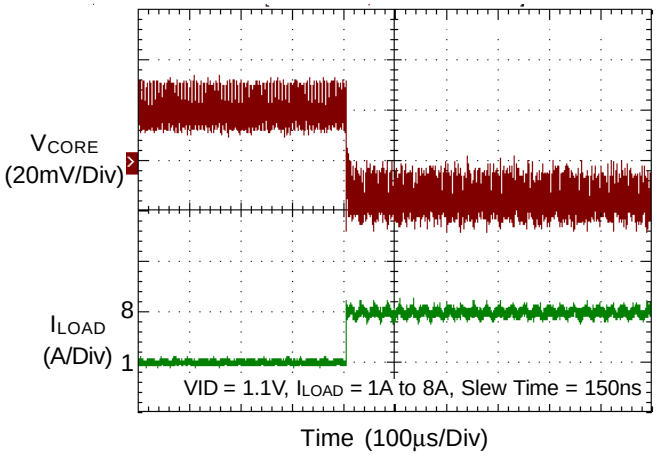
CORE VR Dynamic VID Up



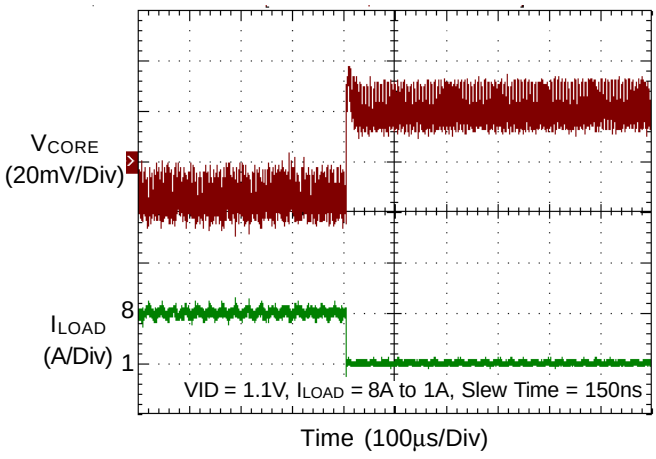
CORE VR Dynamic VID Down



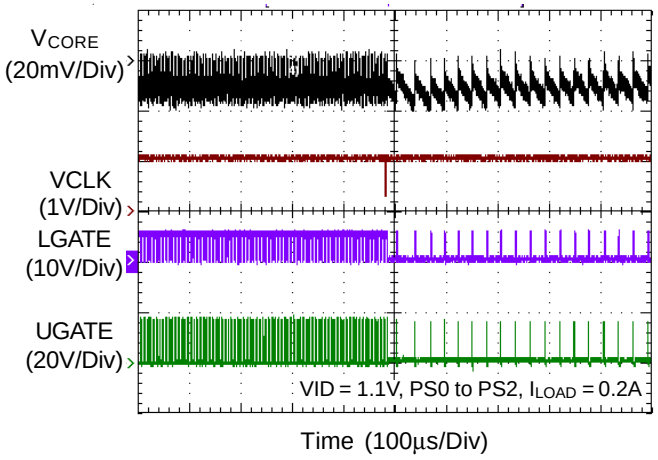
CORE VR Load Transient



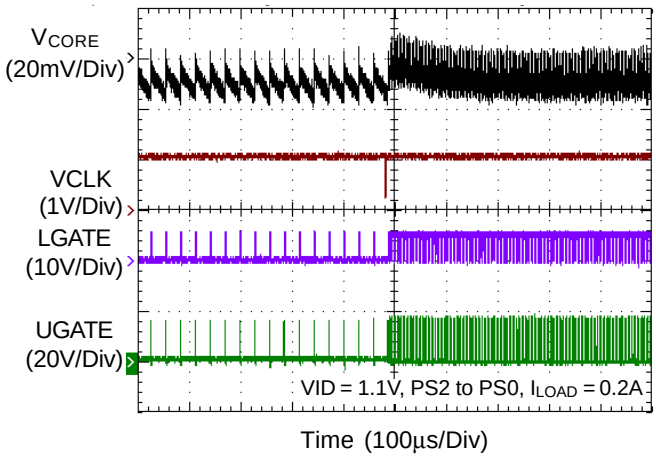
CORE VR Load Transient



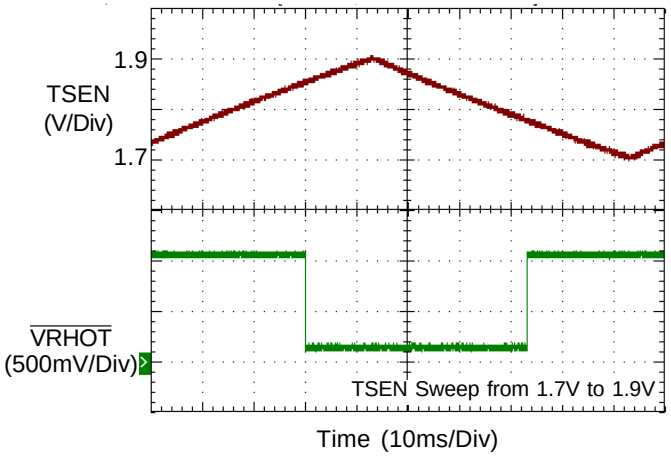
CORE VR Mode Transition



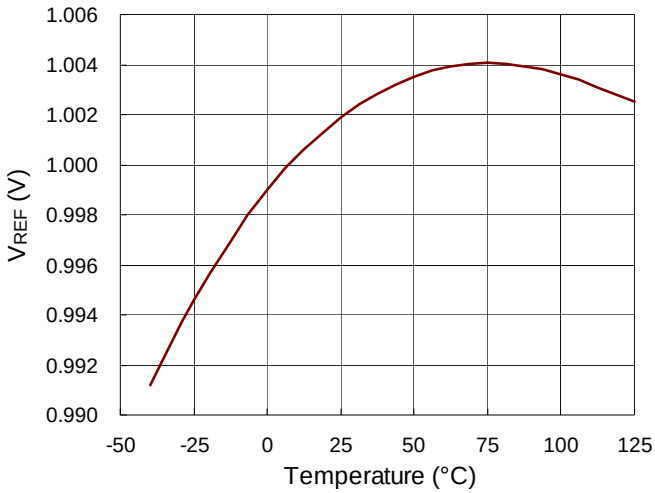
CORE VR Mode Transition



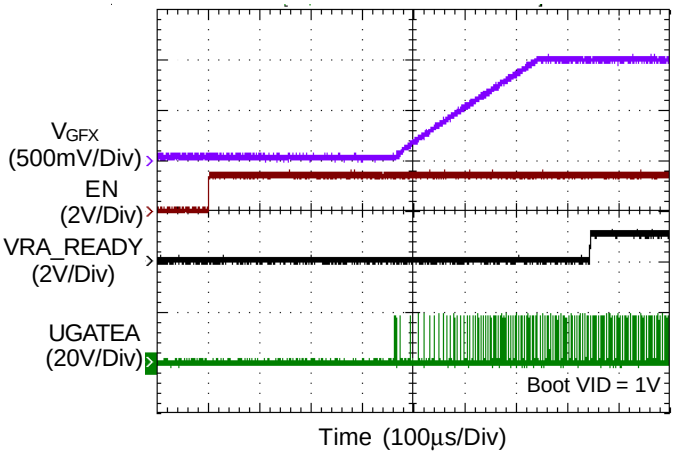
CORE VR Thermal Monitoring



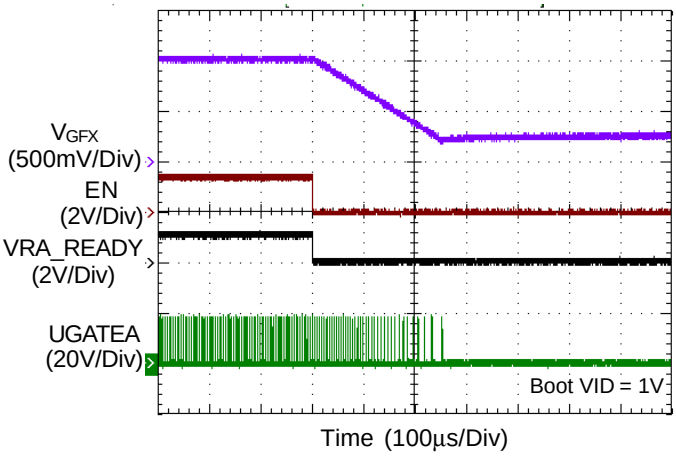
CORE VR V_{REF} vs. Temperature



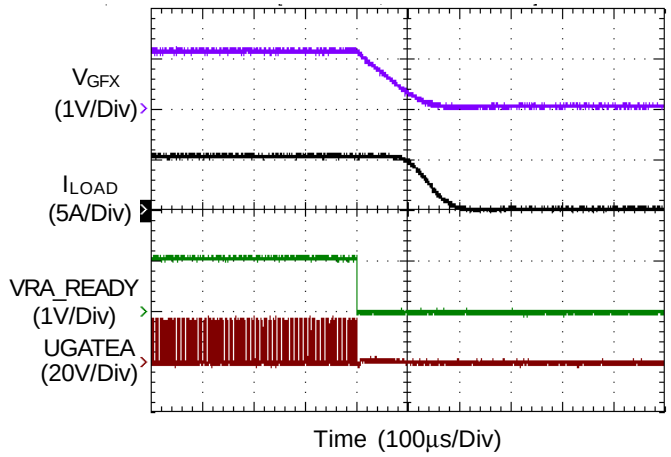
GFX VR Power On from EN



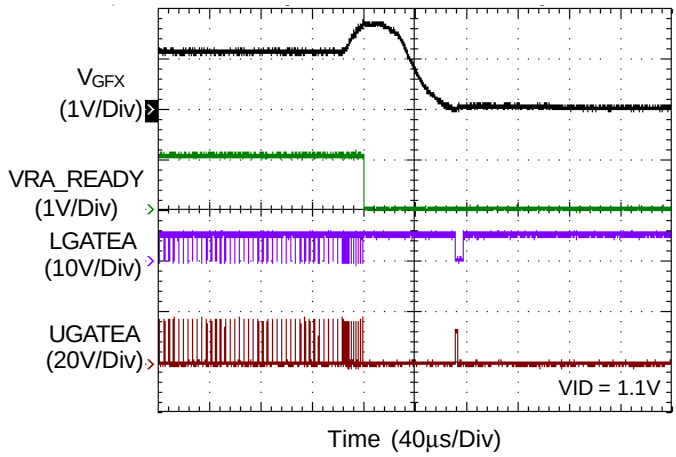
GFX VR Power Off from EN



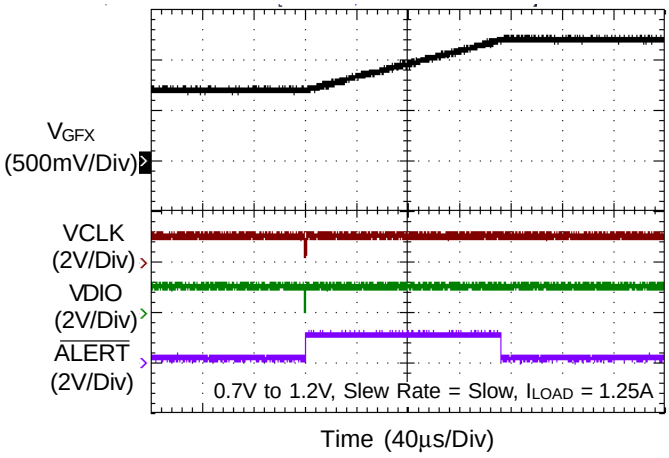
GFX VR OCP



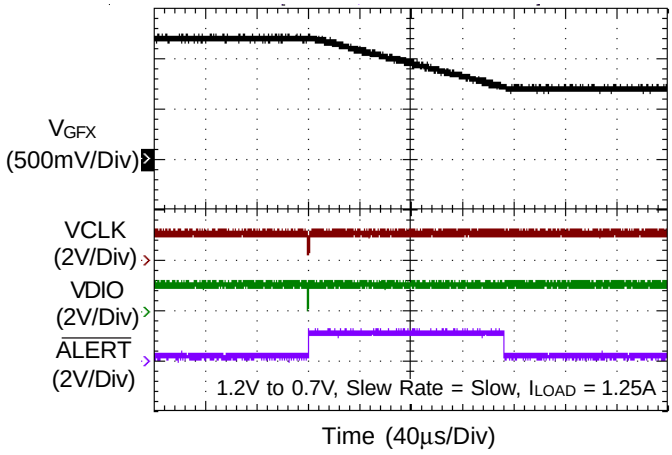
GFX VR OVP and NVP



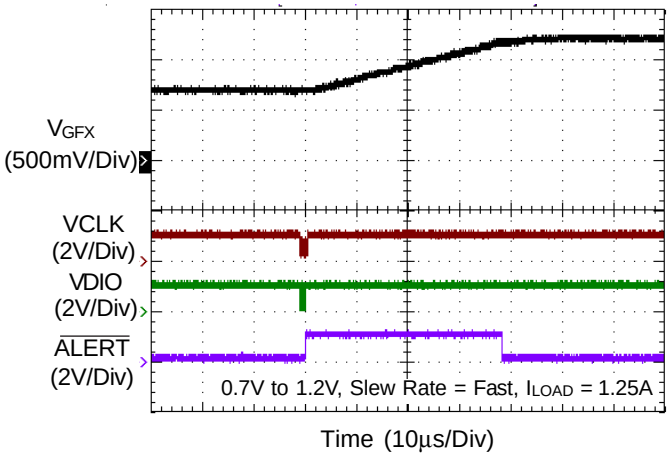
GFX VR Dynamic VID



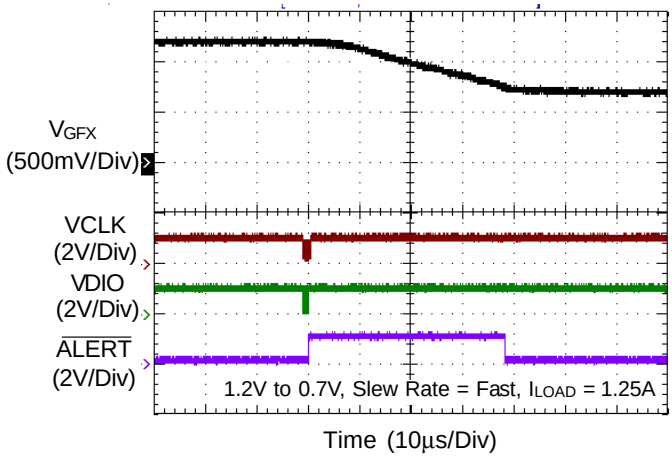
GFX VR Dynamic VID



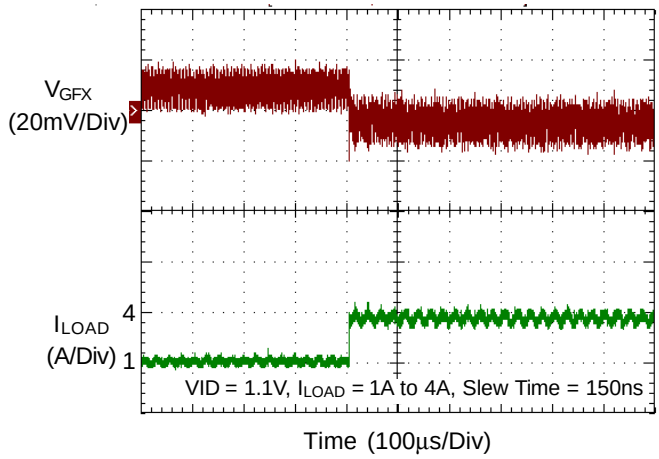
GFX VR Dynamic VID



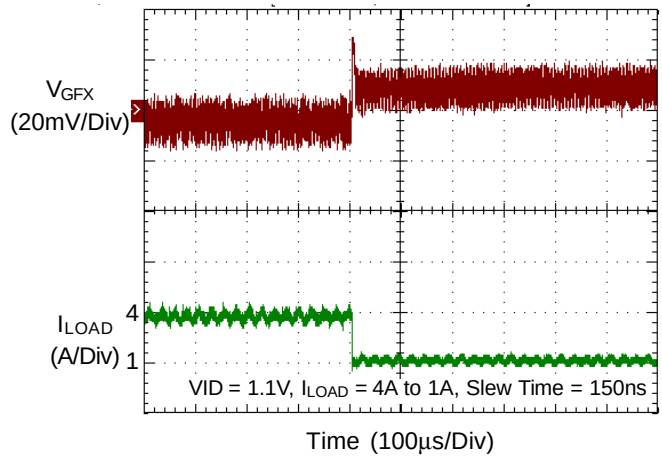
GFX VR Dynamic VID



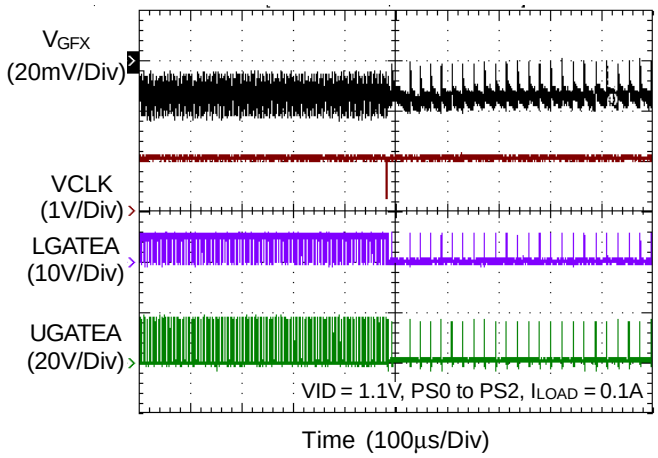
GFX VR Load Transient



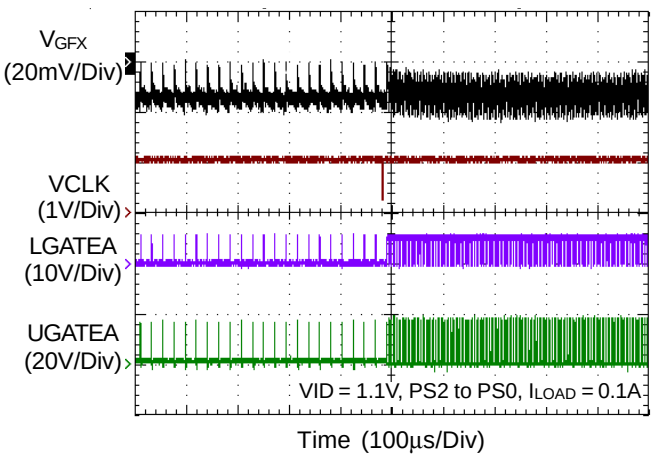
GFX VR Load Transient



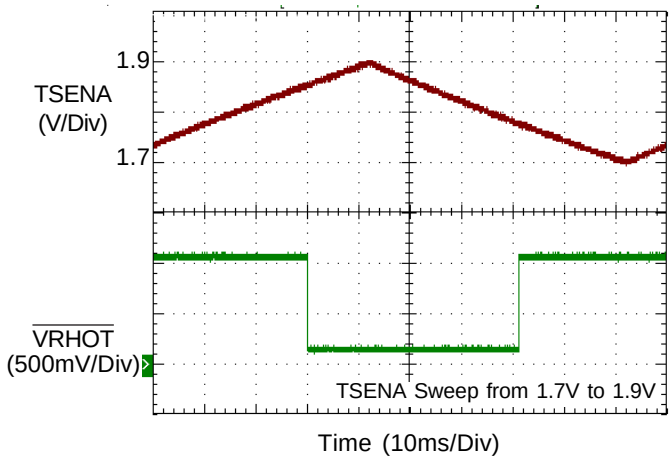
GFX VR Mode Transition



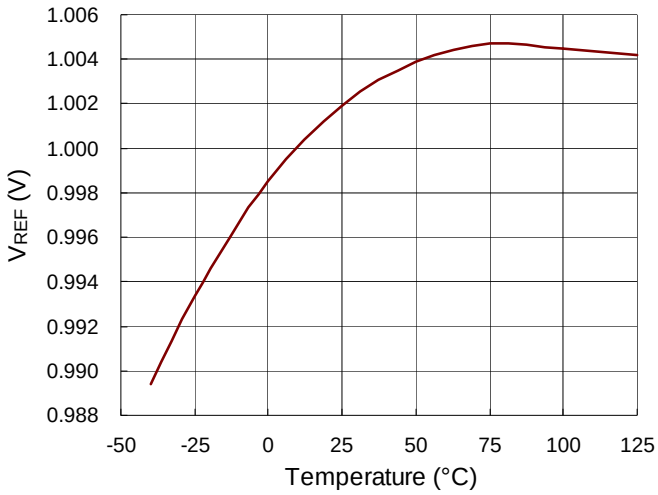
GFX VR Mode Transition



GFX VR Thermal Monitoring



GFX VR V_{REF} vs. Temperature



Application Information

The RT8165A is a VR12/IMVP7 compliant, dual single-phase synchronous Buck PWM controller for the CPU CORE VR and GFX VR. The gate drivers are embedded to facilitate PCB design and reduce the total BOM cost. A serial VID (SVID) interface is built-in in the RT8165A to communicate with Intel VR12/IMVP7 compliant CPU.

The RT8165A adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain compensator, making it an easy setting PWM controller to meet AVP requirements. The load line can be easily programmed by setting the DC gain of the error amplifier. The RT8165A has fast transient response due to the G-NAVP™ commanding variable switching frequency.

G-NAVP™ topology also represents a high efficiency system with green power concept. With G-NAVP™ topology, the RT8165A becomes a green power controller with high efficiency under heavy load, light load, and very light load conditions. The RT8165A supports mode transition function between CCM and DEM. These different operating states allow the overall power system to have low power loss. By utilizing the G-NAVP™ topology, the operating frequency of RT8165A varies with output voltage, load and VIN to further enhance the efficiency even in CCM.

The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The differential remote output voltage sense and high accuracy DAC allow the system to have high output voltage accuracy. The RT8165A supports VR12/IMVP7 compatible power management states and VID on-the-fly function. The power management states include DEM in PS2/PS3 and Forced-CCM in PS1/PS0. The VID on-the-fly function has three different slew rates : Fast, Slow and Decay. The RT8165A integrates a high accuracy ADC for platform setting functions, such as no-load offset and over current level. The controller supports both DCR and sense-resistor current sensing. The RT8165A provides VR ready output signals of both CORE VR and GFX VR. It also features complete fault protection functions including over voltage, under voltage, negative voltage, over current and under voltage lockout. The RT8165A is available in a WQFN-48L 6x6 small foot print package.

Design Tool

To help users reduce efforts and errors caused by manual calculations, a user-friendly design tool is now available on request. This design tool calculates all necessary design parameters by entering user's requirements. Please contact Richtek's representatives for details.

Serial VID (SVID) Interface

SVID is a three-wire serial synchronous interface defined by Intel. The three wire bus includes VDIO, VCLK and ALERT signals. The master (Intel's VR12/IMVP7 CPU) initiates and terminates SVID transactions and drives the VDIO, VCLK, and ALERT during a transaction. The slave (RT8165A) receives the SVID transactions and acts accordingly.

Standard Serial VID Command

Code	Commands	Master Payload Contents	Slave Payload Contents	Description
00h	not supported	N/A	N/A	N/A
01h	SetVID_Fast	VID code	N/A	Set new target VID code, VR jumps to new VID target with controlled default “fast” slew rate 12.5mV/μs.
02h	SetVID_Slow	VID code	N/A	Set new target VID code, VR jumps to new VID target with controlled default “slow” slew rate 3.125mV/μs.
03h	SetVID_Decay	VID code	N/A	Set new target VID code, VR jumps to new VID target, but does not control the slew rate. The output voltage decays at a rate proportional to the load current
04h	SetPS	Byte indicating power states	N/A	Set power state
05h	SetRegADR	Pointer of registers in data table	N/A	Set the pointer of the data register
06h	SetReg DAT	New data register content	N/A	Write the contents to the data register
07h	GetReg	Pointer of registers in data table	Specified Register Contents	Slave returns the contents of the specified register as the payload
08h - 1Fh	not supported	N/A	N/A	N/A

Data and Configuration Register

Index	Register Name	Description	Access	Default
00h	Vendor ID	Vendor ID, default 1Eh.	RO, Vendor	1Eh
01h	Product ID	Product ID.	RO, Vendor	65h
02h	Product Revision	Product Revision.	RO, Vendor	01h
05h	Protocol ID	SVID Protocol ID.	RO, Vendor	01h
06h	VR_Capability	Bit mapped register, identifies the SVID VR capabilities and which of the optional telemetry register are supported.	RO, Vendor	11h
10h	Status_1	Data register containing the status of VR.	R-M, W-PWM	00h
11h	Status-2	Data register containing the status of transmission.	R-M, W-PWM	00h
12h	Temperature Zone	Data register showing temperature zone that have been entered.	R-M, W-PWM	00h
15h	Output_Current	Data register showing direct ADC conversion of averaged output current.	R-M, W-PWM	00h
1Ch	Status_2_lastread	The register contains a copy of the status_2.	R-M, W-PWM	00h
21h	ICC_Max	Data register containing the maximum ICC of platform supports. Binary format in Amp, IE 64h = 100A.	RO, Platform	--
22h	Temp_Max	Data register containing the temperature max the platform supports. Binary format in °C, IE 64h = 100°C Only for CORE VR	RO, Platform	--
24h	SR-Fast	Data register containing the capability of fast slew rate the platform can sustains. Binary format in mV/μs, IE 0Ah = 10 mV/μs.	RO	0Ah
25h	SR-Slow	Data register containing the capability of slow slew rate. Binary format in mV/μs IE 03h = 3 mV/μs.	RO	03h
26h	VINI_x	Data register containing VINI_CORE/VINI_GFX voltage in VID steps.	Platform	00h
30h	VOUT_Max	The register is programmed by the master and sets the maximum VID.	RW, Master	BFh
31h	VID Setting	Data register containing currently programmed VID.	RW, Master	00h
32h	Power State	Register containing the current programmed power state.	RW, Master	00h
33h	Offset	Set offset in VID steps.	RW, Master	00h
34h	Multi VR Config	Bit mapped data register which configures multiple VRs behavior on the same bus.	RW, Master	00h
35h	Pointer	Scratch pad register for temporary storage of the SetRegADR pointer register.	RW, Master	30h

Notes :

RO = Read Only

RW = Read/Write

R-M = Read by Master

W-PWM = Write by PWM only

Vendor = hard coded by VR vendor

Platform = programmed by platform

Master = programmed by the master

PWM = programmed by the VR control IC

Power Ready Detection and Power On Reset (POR)

During start-up, the RT8165A detects the voltage on the voltage input pins : VCC and EN. When VCC > V_{UVLO}, the RT8165A will recognize the power state of system to be ready (POR = high) and wait for enable command at EN pin. After POR = high and EN > V_{ENTH}, the RT8165A will enter start-up sequence for both CORE VR and GFX VR. If the voltage on any voltage pin drops below POR threshold (POR = low), the RT8165A will enter power down sequence and all the functions will be disabled. SVID will be invalid within 300μs after chip becomes enabled. All the protection latches (OVP, OCP, UVP, OTP) will be cleared only after POR = low. EN = low will not clear these latches.

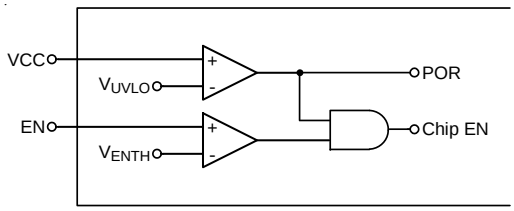


Figure 3. Power Ready Detection and Power On Reset (POR)

Precise Reference Current Generation

The RT8165A includes extensive analog circuits inside the controller. These analog circuits need very precise reference voltage/current to drive these analog devices. The RT8165A will auto-generate a 2.14V voltage source at IBIAS pin, and a 53.6kΩ resistor is required to be connected between IBIAS and analog ground. Through this connection, the RT8165A generates a 40μA current from IBIAS pin to analog ground and this 40μA current will be mirrored inside the RT8165A for internal use. Other types of connection or other values of resistance applied at the IBIAS pin may cause failure of the RT8165A's analog circuits. Thus a 53.6kΩ resistor is the only recommended component to be connected to the IBIAS pin. The resistance accuracy of this resistor is recommended to be at least 1%.

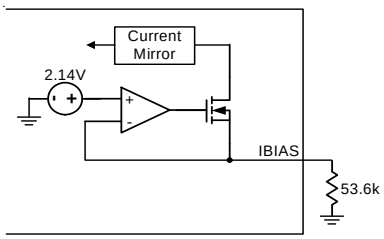


Figure 4. IBIAS Setting

ICCMAX, ICCMAXA and TMPMAX

The RT8165A provides ICCMAX, ICCMAXA and TMPMAX pins for platform users to set the maximum level of output current or VR temperature: ICCMAX for CORE VR maximum current, ICCMAXA for GFX VR maximum current, and TMPMAX for CORE VR maximum temperature.

To set ICCMAX, ICCMAXA and TMPMAX, platform designers should use resistive voltage dividers on these three pins. The current of the divider should be several milli-Amps to avoid noise effect. The three items share the same algorithms : the ADC divides 5V into 255 levels. Therefore, LSB = 5/255 = 19.6mV, which means 19.6mV applied to ICCMAX pin equals to 1A setting. For example, if a platform designer wants to set TMPMAX to 120°C, the voltage applied to TMPMAX should be 120 x 19.6mV = 2.352V. The ADC circuit inside these three pins will decode the voltage applied and store the maximum current/ temperature setting into ICC_MAX and Temp_Max registers. The ADC monitors and decodes the voltage at these three pins only after EN = high. If EN = low, the RT8165A will not take any action even when the VR output current or temperature exceeds its maximum setting at these ADC pins. The maximum level settings at these ADC pins are different from over current protection or over temperature protection. That means, these maximum level setting pins are only for platform users to define their system operating conditions and these messages will only be utilized by the CPU.

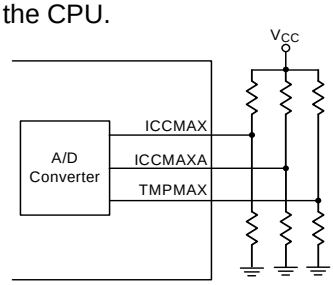
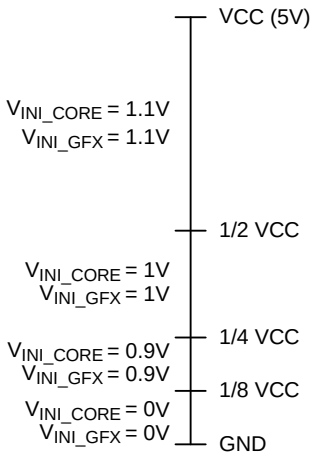


Figure 5. ADC Pins Setting

V_{INI_CORE} and V_{INI_GFX} Setting

The initial start up voltage (V_{INI_CORE}, V_{INI_GFX}) of the RT8165A can be set by platform users through SETINI and SETINIA pins. Voltage divider circuit is recommended to be applied to SETINI and SETINIA pins. The V_{INI_CORE}/ V_{INI_GFX} relate to SETINI/SETINIA pin voltage setting as shown in Figure 6. Recommended voltage setting at SETINI and SETINIA pins are also shown in Figure 6.



V_{INI_CORE} V_{INI_GFX}	Recommended SETINI/SETINIA Pin Voltage
1.1V	$\frac{5}{8}$ x VCC≒3.125V or VCC
1V	$\frac{3}{8}$ x VCC≒1.875V
0.9V	$\frac{3}{16}$ x VCC≒0.9375V
0V	$\frac{1}{16}$ x VCC≒0.3125V or GND

Figure 6. SETINI and SETINIA Pin Voltage Setting

Start Up Sequence

The RT8165A utilizes internal soft-start sequence which strictly follows Intel VR12/IMVP7 start up sequence specifications. After POR = high and EN = high, a 300µs delay is needed for the controller to determine whether all the power inputs are ready for entering start up sequence. If pin voltage of SETINI/SETINIA is zero, the output voltage of CORE/GFX VR is programmed to stay at 0V. If pin voltage of SETINI/SETINIA is not zero, VR output voltage will ramp up to initial boot voltage (V_{INI_CORE}, V_{INI_GFX}) after both POR = high and EN = high. After the output voltage of CORE/GFX VR reaches target initial boot voltage, the controller will keep the output voltage at the initial boot voltage and wait for the next SVID commands. After the RT8165A receives valid VID code (typically SetVID_Slow command), the output voltage will ramp up/down to the target voltage with specified slew rate. After the output voltage reaches the target voltage, the RT8165A will send out VR_READY signal to indicate the power state of the RT8165A is ready. The VR_READY circuit is an open-drain structure so a pull-up resistor is recommended for connecting to a voltage source.

Power Down Sequence

Similar to the start up sequence, the RT8165A also utilizes a soft shutdown mechanism during turn-off. After POR = low, the internal reference voltage (positive terminal of compensation EA) starts ramping down with 3.125mV/µs slew rate, and output voltage will follow the reference voltage to 0V. After output voltage drops below 0.2V, the RT8165A shuts down and all functions are disabled. The VR_READY will be pulled down immediately after POR = low.

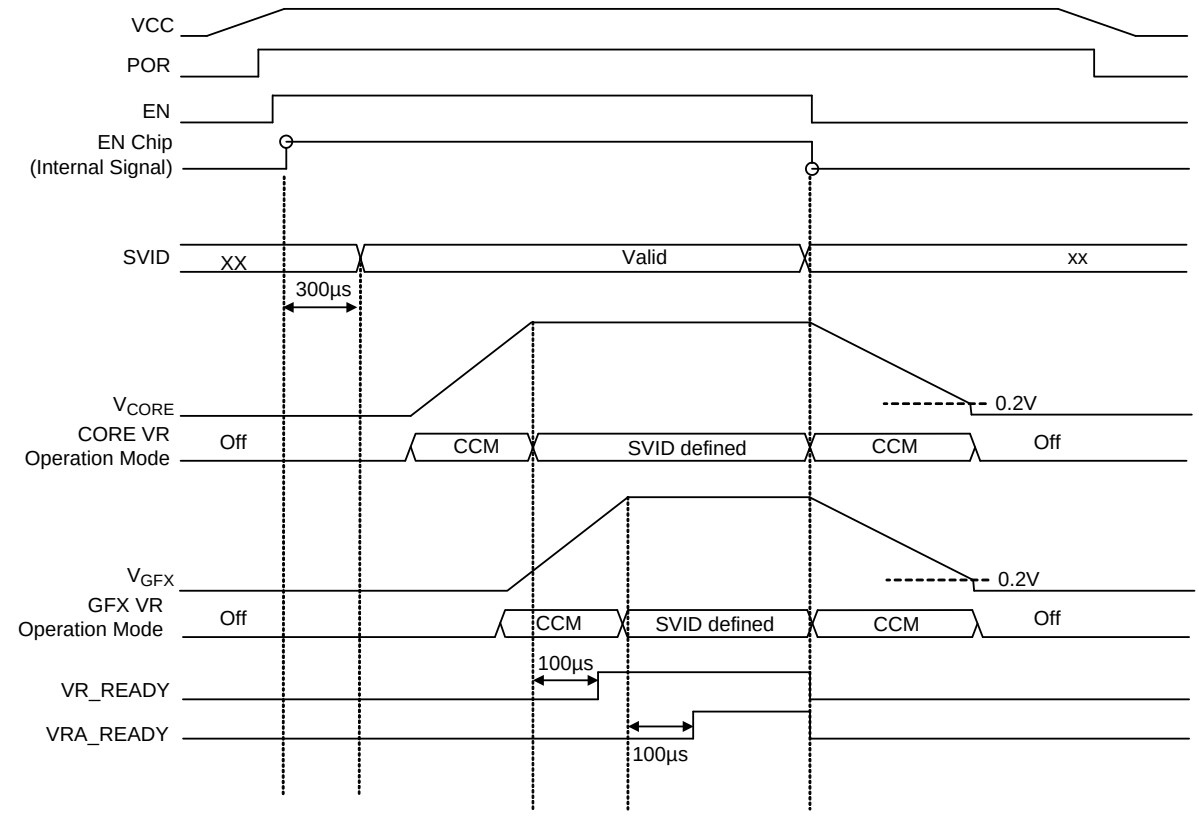


Figure 7 (a). Power sequence for RT8165A (V_{INI_CORE} = V_{INI_GFX} = 0V)

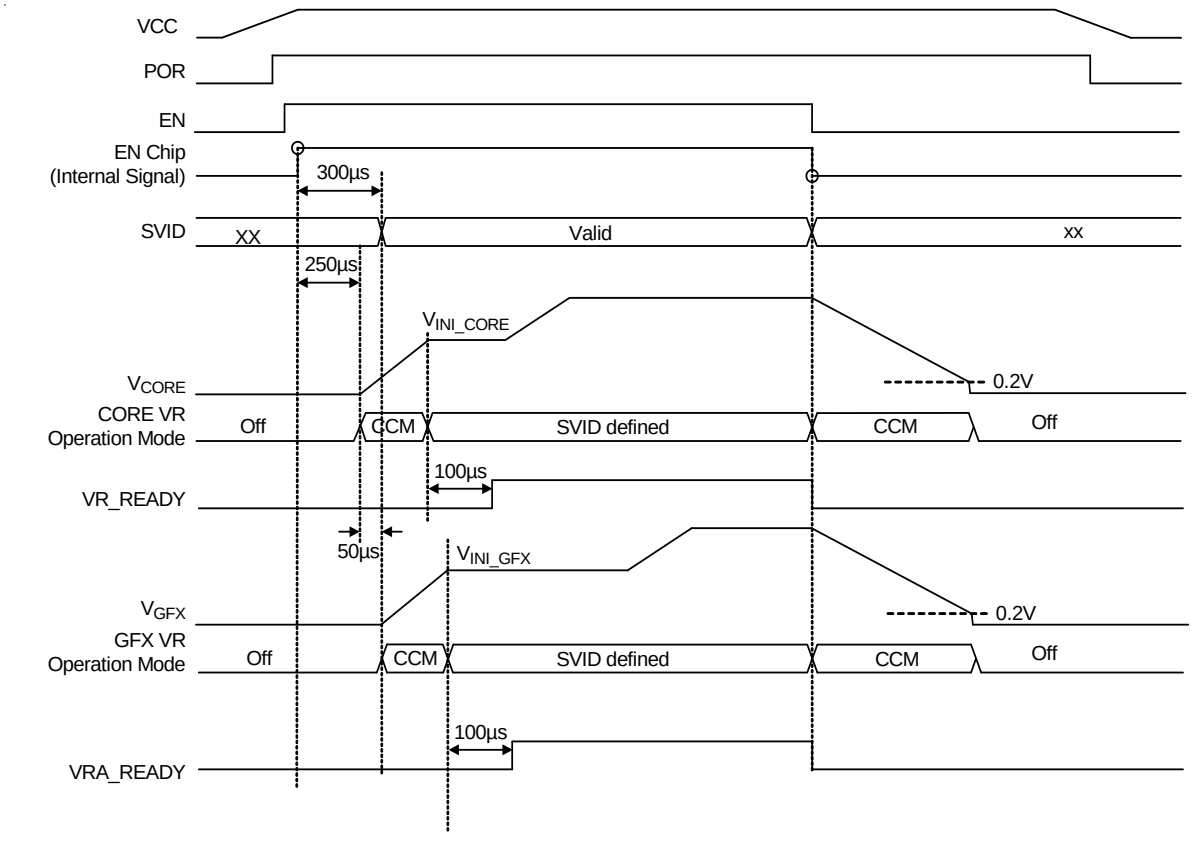


Figure 7 (b). Power sequence for RT8165A (V_{INI_CORE} ≠0, V_{INI_GFX} ≠0V)

Disable GFX VR : Before EN = High

GFX VR enable or disable is determined by the internal circuitry that monitors the ISENAN voltage during start up. Before EN = high, GFX VR detects whether the voltage of ISENAN is higher than "VCC – 1V" to disable GFX VR. The unused driver pins can be connected to GND or left floating.

GFX VR Forced-DEM Function Enable : After VRA_Ready = High

The GFX VR's forced-DEM function can be enabled or disabled with GFXPS2 pin. The RT8165A detects the voltage of GFXPS2 for forced-DEM function. If the voltage at GFXPS2 pin is higher than 4.3V, the GFX VR operates in forced-DEM. If this voltage is lower than 0.7V, the GFX VR follows SVID power state command.

Loop Control

Both CORE and GFX VR adopt Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite-gain valley current mode with CCRCOT (Constant Current Ripple Constant On Time) topology. The output voltage, V_{CORE} or V_{GFX}, will decrease with increasing output load current. The control loop consists of PWM modulator with power stage, current sense amplifier and error amplifier as shown in Figure 8.

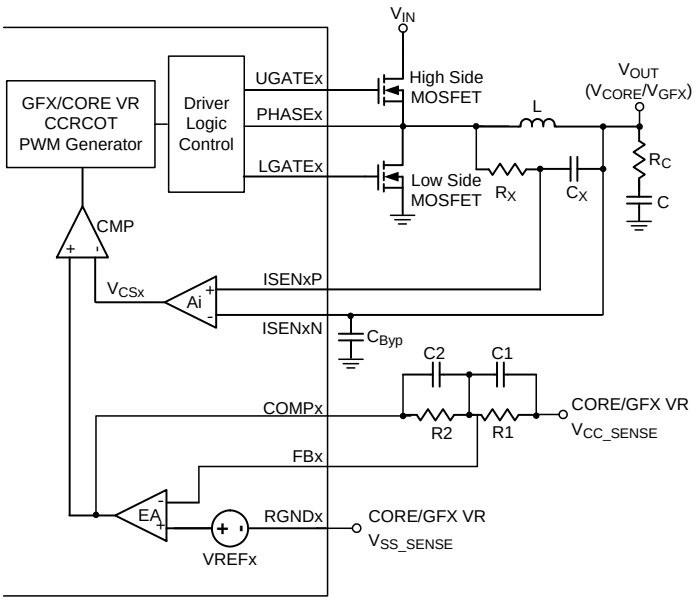


Figure 8. Simplified Schematic for Droop and Remote Sense in CCM

Similar to the valley current mode control with finite compensator gain, the high side MOSFET on-time is determined by the CCRCOT PWM generator. When load current increases, V_{CS} increases, the steady state COMP voltage also increases which makes the output voltage decrease, thus achieving AVP.

Droop Function Enable

The CORE/GFX VR's droop function can be enabled or disabled with DRPEN/DRPENA pin. After EN = high within 10μs, the RT8165A will source 80μA current from DRPEN/DRPENA pin to the external resistor to determine the voltage level. If the voltage at DRPEN/DRPENA pin is lower than 3.5V, then the VR will operate in droop-disabled mode. If the voltage is higher than 4V, then the VR will operate in droop-enabled mode.

Droop Setting (with Temperature Compensation)

It's very easy to achieve the Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. The target is to have

$$V_{OUT} = V_{REFx} - I_{LOAD} \times R_{DROOP} \quad (1)$$

Then solving the switching condition $V_{COMPx} = V_{CSx}$ in Figure 8 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{A_I \times R_{SENSE}}{R_{DROOP}} \quad (2)$$

where A_I is the internal current sense amplifier gain and R_{SENSE} is the current sense resistance. If no external sense resistor is present, the DCR of the inductor will act as R_{SENSE}. R_{DROOP} is the resistive slope value of the converter output and is the desired static output impedance.

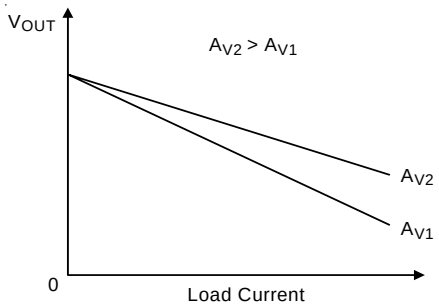


Figure 9. Error Amplifier Gain (A_V) Influence on V_{OUT} Accuracy

Since the DCR of inductor is temperature dependent, it affects the output accuracy in high temperature conditions. Temperature compensation is recommended for the lossless inductor DCR current sense method. Figure 10 shows a simple but effective way of compensating the temperature variations of the sense resistor using an NTC thermistor placed in the feedback path.

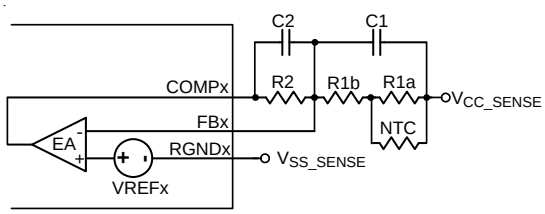


Figure 10. Loop Setting with Temperature Compensation

Usually, R1a is set to equal R_{NTC} (25°C), while R1b is selected to linearize the NTC's temperature characteristic. For a given NTC, the design would be to obtain R1b and R2 and then C1 and C2. According to (2), to compensate the temperature variations of the sense resistor, the error amplifier gain (A_V) should have the same temperature coefficient with R_{SENSE}. Hence

$$\frac{A_{V,\,HOT}}{A_{V,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (3)$$

From (2), we can have Av at any temperature (T) as

$$A_{V,\,T} = \frac{R2}{R1a\,//\,R_{NTC,\,T} + R1b} \quad (4)$$

The standard formula for the resistance of NTC thermistor as a function of temperature is given by :

$$R_{NTC,\,T} = R_{NTC,\,25}\; e^{\left\{\beta\left[\left(\frac{1}{T+273}\right)-\left(\frac{1}{298}\right)\right]\right\}} \quad (5)$$

where $R_{NTC,\,25}$ is the thermistor's nominal resistance at room temperature, β (beta) is the thermistor's material constant in Kelvins, and T is the thermistor's actual temperature in Celsius.

The DCR value at different temperatures can be calculated using the equation below :

$$DCR_T = DCR_{25} \times [1+0.00393 \times (T-25)] \quad (6)$$

where 0.00393 is the temperature coefficient of copper. For a given NTC thermistor, solving (4) at room temperature (25°C) yields

$$R2 = A_{V,\,25} \times (R1b + R1a\,//\,R_{NTC,\,25}) \quad (7)$$

where $A_{V,\,25°C}$ is the error amplifier gain at room temperature obtained from (2). R1b can be obtained by substituting (7) to (3),

$$R1b = \frac{\frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \times (R1a\,//\,R_{NTC,\,HOT}) - (R1a\,//\,R_{NTC,\,COLD})}{\left(1 - \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}}\right)} \quad (8)$$

Loop Compensation

Optimized compensation of the CORE VR allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for a proper compensation. Figure 10 shows the compensation circuit. It was previously mentioned that to determine the resistive feedback components of error amplifier gain, C1 and C2 must be calculated for the compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2 \times \pi \times C \times R_C} \quad (9)$$

where C is the capacitance of the output capacitor and R_C is the ESR of the output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (10)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching-related noise. Such that,

$$C1 = \frac{1}{(R1b + R1a\,//\,R_{NTC,\,25°C}) \times \pi \times f_{SW}} \quad (11)$$

TON Setting

High frequency operation optimizes the application by trading off efficiency due to higher switching losses with smaller component size. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure

11 shows the on-time setting circuit. Connect a resistor ($R_{TONSETx}$) between V_{IN} and TONSETx to set the on-time of UGATEx :

$$t_{ONx}\ (V_{REFx} < 1.2V) = \frac{28 \times 10^{-12} \times R_{TONSETx}}{V_{IN} - V_{REFx}} \quad (12)$$

where t_{ONx} is the UGATEx turn on period, VIN is the input voltage of converter, and V_{REFx} is the internal reference voltage.

When V_{REFx} is larger than 1.2V, the equivalent switching frequency may be over the maximum design range, making it unacceptable. Therefore, the VR implements a pseudo-constant-frequency technology to avoid this disadvantage of CCRCOT topology. When V_{REFx} is larger than 1.2V, the on-time equation will be modified to :

$$t_{ONx}\ (V_{REFx} \geq 1.2V) = \frac{23.33 \times 10^{-12} \times R_{TONSETx} \times V_{REFx}}{V_{IN} - V_{REFx}} \quad (13)$$

On-time translates roughly to switching frequencies. The on-times guaranteed in the Electrical Characteristics are influenced by switching delays in external high side MOSFET. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in CCM during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, PHASEx goes high earlier than normal, extending the on-time by a period equal to the high side MOSFET rising dead time.

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{S(MAX)}(kHz) = \frac{1}{t_{ON} - t_{HS-Delay}} \times \frac{V_{REFx(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON_LS-FET} + DCR - R_{DROOP}\right]}{V_{IN(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON_LS-FET} - R_{ON_HS-FET}\right]} \quad (14)$$

where $f_{S(MAX)}$ is the maximum switching frequency, $t_{HS-Delay}$ is the turn on delay of high side MOSFET, $V_{REFx(MAX)}$ is the maximum application DAC voltage of application, $V_{IN(MAX)}$ is the maximum application input voltage, $I_{LOAD(MAX)}$ is the maximum load of application, R_{ON_LS-FET} is the low side MOSFET $R_{DS(ON)}$, R_{ON_HS-FET} is the high side MOSFET $R_{DS(ON)}$, DCR_L is the inductor DCR, and R_{DROOP} is the load line setting.

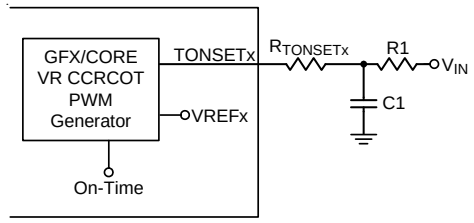


Figure 11. On-Time Setting with RC Filter

Differential Remote Sense Setting

The CORE/GFX VR includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins CORE/GFX V_{CC_SENSE} and V_{SS_SENSE}. Connect RGNDx to CORE/GFX V_{SS_SENSE}. Connect FBx to CORE/GFX V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier. The precision voltage reference V_{REFx} is referred to RGND for accurate remote sensing.

Current Sense Setting

The current sense topology of the CORE/GFX VR is continuous inductor current sensing. Therefore, the controller can be less noise sensitive. Low offset amplifiers are used for loop control and over current detection. The internal current sense amplifier gain (A_I) is fixed to be 10. The ISENxP and ISENxN denote the positive and negative input of the current sense amplifier.

Users can either use a current sense resistor or the inductor's DCR for current sensing. Using inductor's DCR allows higher efficiency as shown in Figure 12. To let

$$\frac{L}{DCR} = R_X \times C_X \quad (15)$$

then the transient performance will be optimum. For example, choose L = 0.36μH with 1mΩ DCR and C_X = 100nF, to yields for R_X :

$$R_X = \frac{0.36\mu H}{1m\Omega \times 100nF} = 3.6k\Omega \quad (16)$$

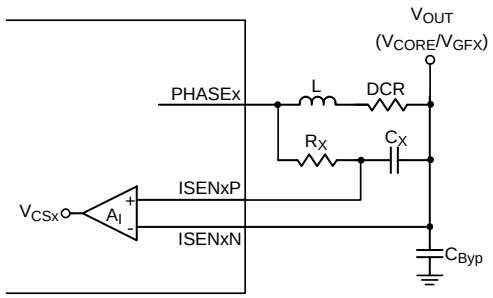


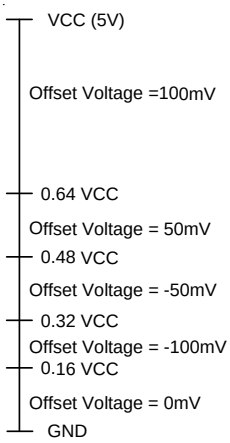
Figure 12. Lossless Inductor Sensing

Considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load line requirement with a slow recovery, R_X is too small. Vice versa, if the resistance is too large the output voltage transient will only have a small initial dip and the recovery will be too fast, causing a ring-back.

Using current-sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, a RC filter is recommended. The RC filter calculation method is similar to the above-mentioned inductor DCR sensing method.

No-Load Offset

The RT8165A provides a no-load offset function which has four-level offsets of output voltage for the CORE/GFX VR. The no-load offset function is implemented through the OFSx pin. A voltage divider circuit is recommended to be applied to OFSx pins. The output offset voltage relation to the OFSx pin voltage setting is shown in Figure 13. Recommended voltage setting at OFS and OFSA pins are also shown in Figure 13.



Offset Voltage	Recommended OFS/OFSA Pin Voltage
100mV	0.8 x VCC≒4V or VCC
50mV	0.56 x VCC≒2.8V
–50mV	0.4 x VCC≒2V
–100mV	0.24 x VCC≒1.2V
0mV	GND

Figure 13. OFS and OFSA Pins Voltage Setting

Operation Mode Transition

The RT8165A supports operation mode transition function in CORE/GFX VR for the SetPS command of Intel's VR12/IMVP7 CPU. The default operation mode of the RT8165A's CORE/GFX VR is PS0, which is CCM operation. The other operation mode is PS2 (DEM operation).

After receiving SetPS command, the CORE/GFX VR will immediately change to the new operation state. When VR receives SetPS command of PS2 operation mode, the VR operates as a DEM controller.

If VR receives dynamic VID change command (SetVID), VR will automatically enter PS0 operation mode. After output voltage reaches target voltage, VR will stay at PS0 state and ignore former SetPS command. Only by re-sending SetPS command after SetVID command will VR be forced into PS2 operation state again.

Thermal Monitoring and Temperature Reporting

CORE/GFX VR provides thermal monitoring function via sensing TSEN pin voltage. Through the voltage divider resistors R1, R2, R3 and R_{NTC}, the voltage of TSEN will be proportional to VR temperature. When VR temperature rises, the TSENx voltage also rises. The ADC circuit of VR monitors the voltage variation at TSENx pin from 1.47V to 1.89V with 55mV resolution, and this voltage is decoded into digital format and stored into the Temperature Zone register.

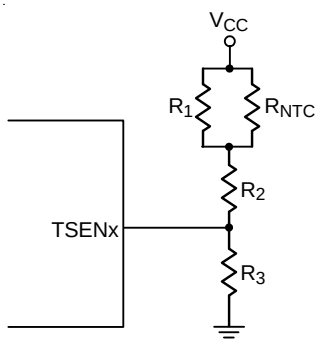


Figure 14. Thermal Monitoring Circuit

To meet Intel's VR12/IMVP7 specification, platform users have to set the TSEN voltage to meet the temperature variation of VR from 75% to 100% VR max temperature. For example, if the VR max temperature is 100°C, platform users have to set the TSEN voltage to be 1.4875V when VR temperature reaches 75°C and 1.8725V when VR temperature reaches 100°C. Detailed voltage setting versus temperature variation is shown in Table 2. Thermometer code is implemented in the Temperature Zone register.

Table 2. Temperature Zone Register

$\overline{VRHOT}$	SVID Thermal Alert	Comparator Trip Points Temperatures Scaled to maximum = 100% Voltage Represents Assert bit Minimum Level					
b7	b6	b5	b4	b3	b2	b1	b0
100%	97%	94%	91%	88%	85%	82%	75%
1.855V	1.8V	1.745 V	1.69 V	1.635 V	1.58 V	1.52 5V	1.47 V

TSEN Pin Voltage	Temperature_Zone Register Content
$1.855 \le V_{TSEN}$	1111_1111
$1.800 \le V_{TSEN} \le 1.835$	0111_1111
$1.745 \le V_{TSEN} \le 1.780$	0011_1111
$1.690 \le V_{TSEN} \le 1.725$	0001_1111
$1.635 \le V_{TSEN} \le 1.670$	0000_1111
$1.580 \le V_{TSEN} \le 1.615$	0000_0111
$1.525 \le V_{TSEN} \le 1.560$	0000_0011
$1.470 \le V_{TSEN} \le 1.505$	0000_0001
$V_{TSEN} < 1.470$	0000_0000

The RT8165A supports two temperature reporting, $\overline{VRHOT}$(hardware reporting) and $\overline{ALERT}$(software reporting), to fulfill VR12/IMVP7 specification. $\overline{VRHOT}$ is an open-drain structure which sends out active-low $\overline{VRHOT}$ signals. When TSEN voltage rises above 1.855V (100% of VR temperature), the $\overline{VRHOT}$ signal will be set to low. When TSEN voltage drops below 1.8V (97% of VR temperature), the $\overline{VRHOT}$ signal will be reset to high. When TSEN voltage rises above 1.8V (97% of VR temperature), The RT8165A will update the bit1 data from 0 to 1 in the Status_1 register and assert $\overline{ALERT}$. When TSEN voltage drops below 1.745V (94% of VR temperature), VR will update the bit1 data from 1 to 0 in the Status_1 register and assert $\overline{ALERT}$.

The temperature reporting function for the GFX VR can be disabled by pulling TSENA pin to VCC in case the temperature reporting function for the GFX VR is not used or the GFX VR is disabled. When the GFX VR's temperature reporting function is disabled, the RT8165A will reject the SVID command of getting the Temperature_Zone register content of the GFX VR. However, note that the temperature reporting function for the CORE VR is always active. CORE VR's temperature reporting function can not be disabled by pulling TSEN pin to VCC.

Current Monitoring and Current Reporting

The CORE/GFX VR provides current monitoring function via sensing the voltage difference of IMONFBx pin and output voltage. Figure 15 shows the current monitoring setting principle. The equivalent output current will be sensed from IMONFBx pin and mirrored to IMONx pin. The resistor connected to IMONx pin determines voltage gain of the IMON output.

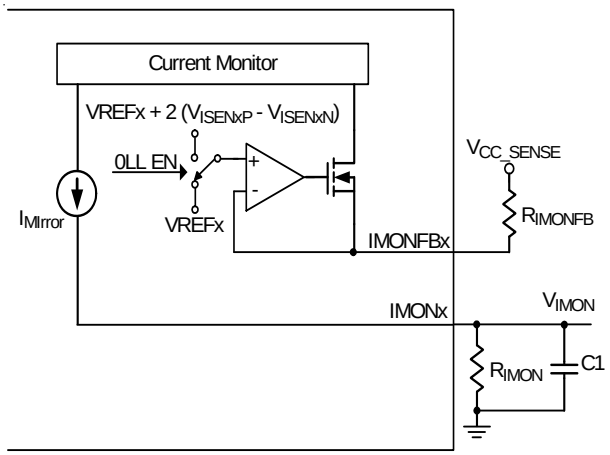


Figure 15. Current Monitor Setting Principle

The voltage of IMONFBx is different when VR operates in droop enable mode and droop disable mode :

Droop enable mode : $V_{IMONFBx} = V_{REFx}$ (17)

Droop disable mode :

$$V_{IMONFBx} = V_{REFx} + 2\,(V_{ISENxP} - V_{ISENxN}) \quad (18)$$

The current monitor indicator V_{IMON} equation is shown as:

$$V_{IMON} = \frac{(I_{IMONFBx} - V_{CC_SENSE}) \times R_{IMON}}{R_{IMONFB}} \quad (19)$$

where $V_{IMONFBx}$ is the pin voltage of IMONFBx, V_{CC_SENSE} is the output voltage of CORE/GFX VR, and R_{IMON} and R_{IMONFB} are the current monitor current setting resistors.

The maximum voltage of current monitoring will be limited at 3.3V. Platform designers have to design the R_{IMON} to meet the maximum voltage of IMON at full load.

When VR operates in droop enable mode, find R_{IMON} and R_{IMONFB} based on :

$$\frac{R_{IMON}}{R_{IMONFB}} = \frac{V_{IMON(MAX)}}{I_{(MAX)} \times R_{DROOP}} \quad (20)$$

where $V_{IMON(MAX)}$ is the maximum voltage at full load, R_{DROOP} is the load line setting of VR, and I_{MAX} is the full load current of VR.

When VR operate in droop disable mode, R_{IMON} and R_{IMONFB} can be obtained according to equation below :

$$\frac{R_{IMON}}{R_{IMONFB}} = \frac{V_{IMON(MAX)}}{I_{(MAX)} \times R_{SENSE} \times 2} \quad (21)$$

where $V_{IMON(MAX)}$ is the maximum voltage at full load, R_{SENSE} is the equivalent resistance of current sense circuit, and I_{MAX} is the full load current of VR.

The ADC circuit of the CORE/GFX VR monitors the voltage variation at the IMON pin from 0V to 3.3V, and this voltage is decoded into digital format and stored into the Output_Current register. The ADC divides 3.3V into 255 levels, so LSB = 3.3V/255 = 12.941mV. Platform designers should design V_{IMONx} to be 3.3V at ICCMAX. For example, when load current = 0.5 x ICCMAX, V_{IMON} = 1.65V and Output_Current register = 7Fh.

The IMON pin is the output of internal operational amplifier and sends out IMON signal. When IMON voltage rises above 3.3V (100% of VR output current), the VR will update the bit2 data from 0 to 1 in the Status_1 register. The 1 in bit2 of Status_1 register will be cleared to 0 only after the master (usually Intel's VR12/IMVP7 CPU) executes GetReg command to Status_1 register.

Over Current Protection

The CORE/GFX VR compares a programmable current limit set point to the voltage from the current sense amplifier output for Over Current Protection (OCP). The voltage applied to OCSETx pin defines the desired peak current limit threshold I_{LIMIT} :

$$V_{OCSET} = 48 \times I_{LIMIT} \times R_{SENSE} \quad (22)$$

Connect a resistive voltage divider from VCC to GND, with the joint of the resistive divider connected to OCSET pin as shown in Figure 16. For a given R_{OC2}, then

$$R_{OC1} = R_{OC2} \times \left(\frac{V_{CC}}{V_{OCSET}} - 1 \right) \quad (23)$$

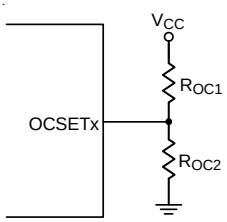


Figure 16. OCP Setting without Temperature Compensation

The current limit is triggered when inductor current exceeds the current limit threshold I_{LIMIT}, defined by V_{OCSET}. The driver will be forced to turn off UGATE until the over current condition is cleared. If the over current condition remains valid for 15 PWM cycles, VR will trigger OCP latch. Latched OCP forces both UGATE and LGATE to go low. When OCP is triggered in one of VRs, the other VR will enter into soft shutdown sequence. The OCP latch mechanism will be masked when VRx_READY = low, which means that only the current limit will be active when V_{OUT} is ramping up to initial voltage (or V_{REFx}).

If inductor DCR is used as the current sense component, then temperature compensation is recommended for protection under all conditions. Figure 17 shows a typical OCP setting with temperature compensation.

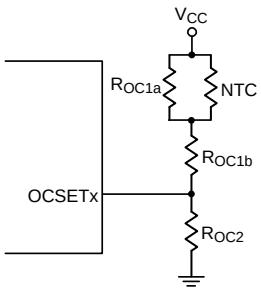


Figure 17. OCP Setting with Temperature Compensation

Usually, R_{OC1a} is selected to be equal to the thermistor's nominal resistance at room temperature. Ideally, V_{OCSET} is assumed to have the same temperature coefficient as R_{SENSE} (Inductor DCR) :

$$\frac{V_{OCSET,\,HOT}}{V_{OCSET,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (24)$$

According to the basic circuit calculation, V_{OCSET} can be obtained at any temperature :

$$V_{OCSET,\,T} = V_{CC} \times \frac{R_{OC2}}{R_{OC1a} \,//\, R_{NTC,\,T} + R_{OC1b} + R_{OC2}} \quad (25)$$

Re-write (24) from (25), to get V_{OCSET} at room temperature

$$\frac{R_{OC1a} \,//\, R_{NTC,\,COLD} + R_{OC1b} + R_{OC2}}{R_{OC1a} \,//\, R_{NTC,\,HOT} + R_{OC1b} + R_{OC2}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (26)$$

$$V_{OCSET,\,25} = V_{CC} \times \frac{R_{OC2}}{R_{OC1a} \,//\, R_{NTC,\,25} + R_{OC1b} + R_{OC2}} \quad (27)$$

Solving (26) and (27) yields R_{OC1b} and R_{OC2}

$$R_{OC2} = \frac{\alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD} + (1-\alpha) \times R_{EQU,\,25}}{\frac{V_{CC}}{V_{OCSET,\,25}} \times (1-\alpha)} \quad (28)$$

$$R_{OC1b} = \frac{(\alpha - 1) \times R2 + \alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD}}{(1-\alpha)} \quad (29)$$

where

$$\alpha = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} = \frac{DCR_{25} \times [1 + 0.00393 \times (T_{HOT} - 25)]}{DCR_{25} \times [1 + 0.00393 \times (T_{COLD} - 25)]} \quad (30)$$

$$R_{EQU,\,T} = R_{OC1a} \,//\, R_{NTC,\,T} \quad (31)$$

Over Voltage Protection (OVP)

The over voltage protection circuit of CORE/GFX VR monitors the output voltage via the ISENxN pin. The supported maximum operating VID of VR ($V_{(MAX)}$) is stored in the Vout_Max register. Once V_{ISENxN} exceeds "$V_{(MAX)}$ + 200mV", OVP is triggered and latched. VR will try to turn on low side MOSFETs and turn off high side MOSFETs to protect CPU. When OVP is triggered by the one of the VRs, the other VR will enter soft shutdown sequence. A 10µs delay is used in OVP detection circuit to prevent false trigger.

Negative Voltage Protection (NVP)

During OVP latch state, both CORE/GFX VRs also monitor ISENxN pin for negative voltage protection. Since the OVP latch will continuously turn on low side MOSFET of VR, VR may suffer negative output voltage. Therefore, when the voltage of ISENxN drops below –0.05V after triggering OVP, VR will turn off low side MOSFETs while high side MOSFETs remain off. The NVP function will be active only after OVP is triggered.

Under Voltage Protection (UVP)

Both CORE/GFX VR implement Under Voltage Protection (UVP). If ISENxN is less than V_{REFx} by 300mV + V_{OFFSET}, VR will trigger UVP latch. The UVP latch will turn off both high side and low side MOSFETs. When UVP is triggered by one of the VRs, the other VR will enter into soft shutdown sequence. The UVP mechanism is masked when VRx_READY = low.

Under Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below UVLO falling edge threshold, both VR will trigger UVLO. The UVLO protection forces all high side MOSFETs and low side MOSFETs off to turn off.

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{I_{Ripple(MAX)}} \times t_{ON} \quad (32)$$

where t_{ON} is the UGATE turn on period.

Higher inductance induces less ripple current and hence higher efficiency. However, the tradeoff is a slower transient response of the power stage to load transients. This might increase the need for more output capacitors, thus driving up the cost. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to be saturated at the peak inductor current.

Output Capacitor Selection

Output capacitors are used to obtain high bandwidth for the output voltage beyond the bandwidth of the converter itself. Usually, the CPU manufacturer recommends a capacitor configuration. Two different kinds of output capacitors can be found, bulk capacitors closely located to the inductors and ceramic output capacitors in close proximity to the load. Latter ones are for mid-frequency decoupling with very small ESR and ESL values while the bulk capacitors have to provide enough stored energy to overcome the low-frequency bandwidth gap between the regulator and the CPU.

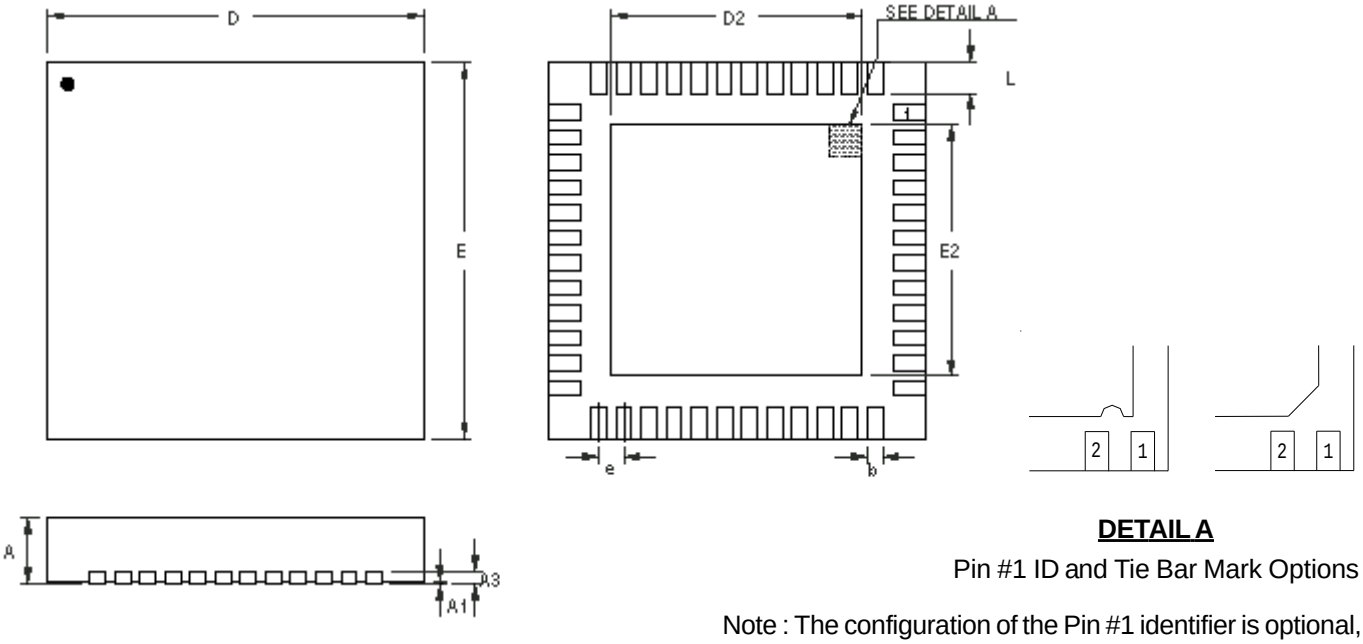
PCB Layout Guideline

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for optimum PC board layout :

- Keep the high current paths short, especially at the ground terminals.

- Keep the power traces and load connections short. This is essential for high efficiency.
- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharging path.
- Place the current sense component close to the controller. ISENxP and ISENxN connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee the current sense accuracy. The PCB trace from the sense nodes should be parallel to the controller.
- Route high-speed switching nodes away from sensitive analog areas (COMPx, FBx, ISENxP, ISENxN, etc...)
- Special attention should be paid in placing the DCR current sensing components. The DCR current sensing capacitor and resistors must be placed close to the controller.
- The capacitor connected to the ISEN1N/ISENAN for noise decoupling is optional and it should also be placed close to the ISEN1N/ISENAN pin.
- The NTC thermistor should be placed physically close to the inductor for better DCR thermal compensation.

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.250	4.350	0.167	0.171
E	5.950	6.050	0.234	0.238
E2	4.250	4.350	0.167	0.171
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 48L QFN 6x6 Package

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