High Power Synchronous Boost Converter

General Description

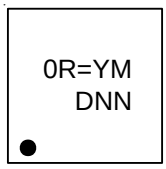
The RT8540A is a high-efficiency, high-current Boost converter in all single-cell Lithium-ion / polymer battery operated products. The RT8540A maintains output current regulation by switching the internal high side and low side switch transistors. The transistor switches are pulse-width modulated at a fixed frequency of 2MHz. The high switching frequency allows the use of a small inductor and output capacitor, making the RT8540A ideally suited for small battery-powered applications. Output voltage can be set by an external resistor on the FB pin or by I^2C interface.

The RT8540A contains over voltage protection, over current protection and over temperature protection to prevent the device from output open circuit or short circuit condition. Built-in soft-start circuitry prevents excessive inrush current during start-up. The shutdown feature reduces quiescent current to less than 5μA.

Features

- **Input Voltage Range : 2.8V to 5.5V**
- **True Load Disconnect**
- **Internal Synchronous Rectifier**
- **Up to 90% Efficiency with Small Magnetics**
- **Current Mode PWM Operation with Internal Compensation**
- **Internal Soft-Start Control**
- **Flexible on/off Control by I^2C or EN.**
- **Short Circuit Protection**
- **Input Current Limit up to 4A**
- **Over Voltage, Over Temperature Protection**
- **Shutdown Current : 2μA**
- **–40°C to 85°C Temperature Range**
- **20-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Marking Information



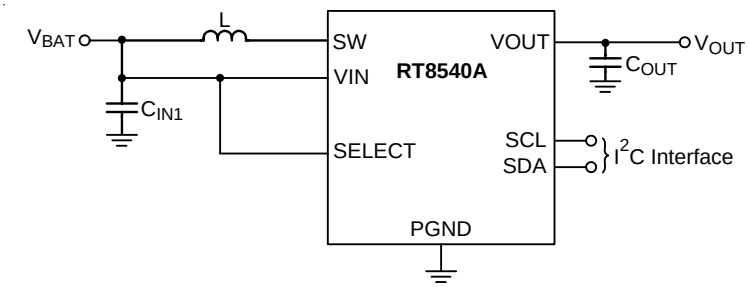
0R= : Product Code

YMDNN : Date Code

Applications

- Cellular Phones
- Digital Cameras
- Probable Instruments

Simplified Application Circuit



Ordering Information

RT8540A□□

- Package Type
  QW : WQFN-20L 4x4 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

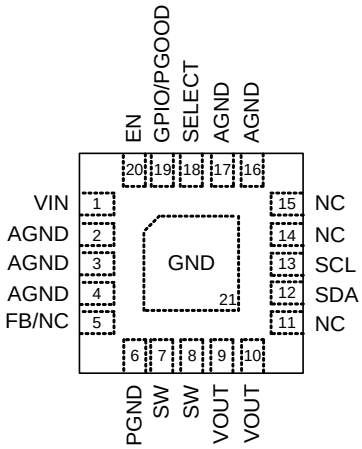
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

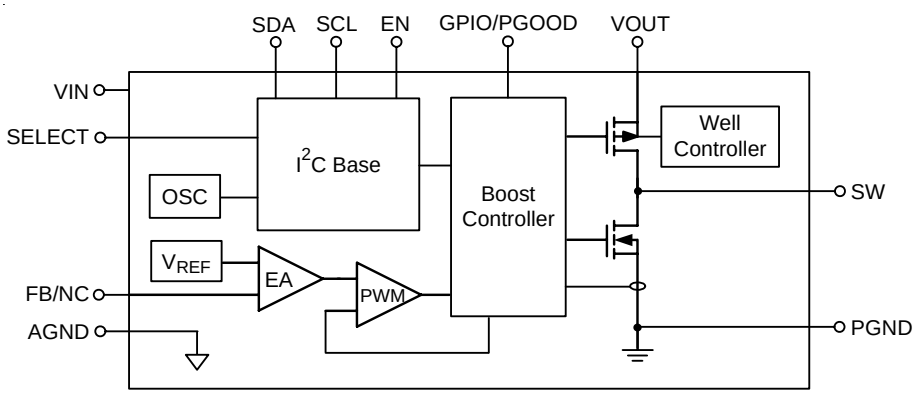


WQFN-20L 4x4

Functional Pin Description

Pin No.	Pin Name.	Pin Function
1	VIN	Power Input. Connect VIN to the power supply. Connect a 4.7μF or larger ceramic capacitor from VIN to ground as close as possible to the IC.
2, 3, 4, 16, 17	AGND	Analog Ground. Connect AGND to GND at single point as close to the IC as possible.
5	FB/NC	Feedback Voltage Input. When the pin is floating, the output voltage is controlled by I^2C interface.
6	PGND	Power Ground. Connect PGND to GND at a single point as close to the IC as possible.
7, 8	SW	Switch Node. Connect an inductor between SW and VIN.
9, 10	VOUT	Output of the Boost Conductor. Connect a 10μF or larger ceramic capacitor from VOUT to ground as close as possible to the IC.
11, 14, 15	NC	No Internal Connection.
12	SDA	Data Signal Input for I^2C. Open drain output, connect a 10kΩ pull-up resistor.
13	SCL	Clock Signal Input for I^2C. Open drain output, connect a 10kΩ pull-up resistor.
18	SELECT	Select IC I^2C/EN Control. SELECT = HIGH. I^2C control. SELECT = LOW. EN control.
19	GPIO/PGOOD	General Purpose Input Output Input or Power Good Indicator Output.
20	EN	Enable Control Input for non I^2C control Version (Active High).
21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

Boost Controller

The core of the Boost regulator with normal operations and provides protection functions like UVLO, OCP, OVP, OTP.

OSC

Generates 2MHz clock.

VREF

Generates the reference voltage for Error-amp and other bias circuit.

EA

Error amplifier generates COMP signal by the difference between FB and VREF.

PWM

PWM comparator compares COMP signal and current feedback signal to initial PWM signal.

I²C BASE

Digital logic and registers part.

Well Controller

It compares VIN and VOUT, the higher one will be the big P-MOSFET well potential.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 6V
- Boost Output Voltage, VOUT ---------- –0.3V to 6.5V
- Switching Voltage, SW ---------- –0.3V to 6.5V
- SCL, SDA, EN, GPIO/PGOOD, FB/NC, SELECT ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20L 4x4 ---------- 3.57W
- Package Thermal Resistance (Note 2)
  WQFN-20L 4x4, θ_{JA} ---------- 28°C/W
  WQFN-20L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V
  CDM (Charge Device Model) ---------- 500V

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ---------- 2.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, C_{IN} = 4.7µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage Range	V_{IN}		2.8	--	5.5	V
UVLO	UV	VIN Falling	--	2.4	--	V
VIN Supply Current	I_Q	I_{OUT} = 0A	--	590	700	µA
VIN Shutdown Current	I_{SHDN}	V_{IN} = 5V	--	1	5	µA
Output						
Output Voltage Range	V_{OUT}	I^2C Control, OV[3:0] = 0000 to 1111	3.825	--	5.45	V
Feedback Voltage	V_{FB}	EN Control	0.9702	0.99	1.0098	V
Oscillator and Timer						
Operating Frequency	f_{OSC}		1.6	2	2.4	MHz
Maximum Duty Cycle	D_{MAX}		70	--	--	%
Power Switch						
N-MOSFET Ron	$R_{DS(ON)\_N}$	V_{OUT} = 3.6V	--	90	--	mΩ
P-MOSFET Ron	$R_{DS(ON)\_P}$	V_{OUT} = 3.6V	--	110	--	mΩ
Leakage into SW	I_{LKG_SW}	V_{OUT} = 0V, EN = LOW	--	0.3	4	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection Function						
N-MOSFET Current Limit	I_{OCP}	V_{OUT} = 5V	3.6	4	4.4	A
Over Voltage Protection	V_{OVP}	VOUT Rising, 0000 ≤ OV[3:0] ≤ 0100	4.464	4.65	4.836	V
		VOUT Rising, 0101 ≤ OV[3:0] ≤ 1111, SELECT = LOW	5.568	5.8	6.032	V
OVP Hysteresis	V_{OVP_HYS}	VOUT Falling	--	150	--	mV
Thermal Shutdown	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	T_{SD_HYS}		--	20	--	°C
Logic Control						
SELECT Logic High	V_{SELH}		1.4	--	--	V
SELECT Logic Low	V_{SELL}		--	--	0.4	V
EN Logic High	V_{ENLH}		1.4	--	--	V
EN Logic Low	V_{ENLL}		--	--	0.4	V
SCL Logic High	V_{SCLH}		1.4	--	--	V
SCL Logic Low	V_{SCLL}		--	--	0.4	V
SDA Logic High	V_{SDAH}		1.4	--	--	V
SDA Logic Low	V_{SDAL}		--	--	0.4	V
GPIO Output Voltage High	V_{OH_GPIO}	DIR = 1, GPIOTYPE = 0, I_{OH} = 8mA	VIN – 0.4	--	--	V
GPIO Output Voltage Low	V_{OL_GPIO}	DIR = 1, I_{OL} = 5mA	--	--	0.3	V
EN Pull Low Resistance	R_{EN}		--	400	--	kΩ
SELECT Pull Low Resistance	R_{SEL}		--	400	--	kΩ
Clock Frequency of SCL	f_{SCL}		--	--	400	kHz

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

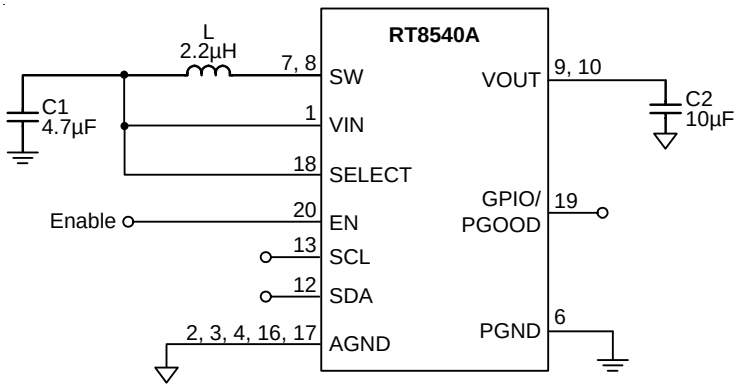


Figure 1. For I^{2}C Control

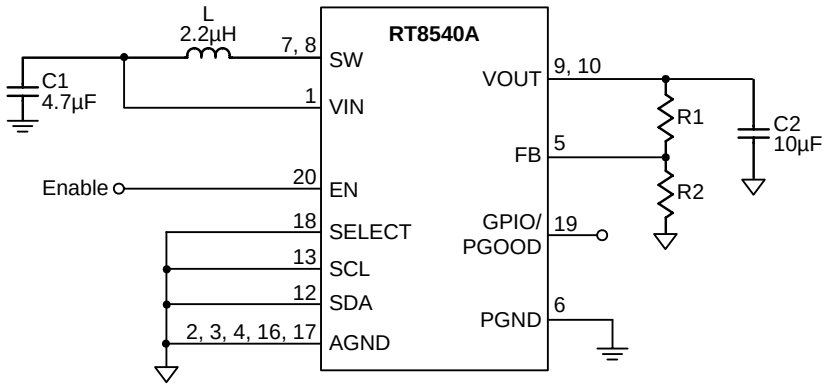
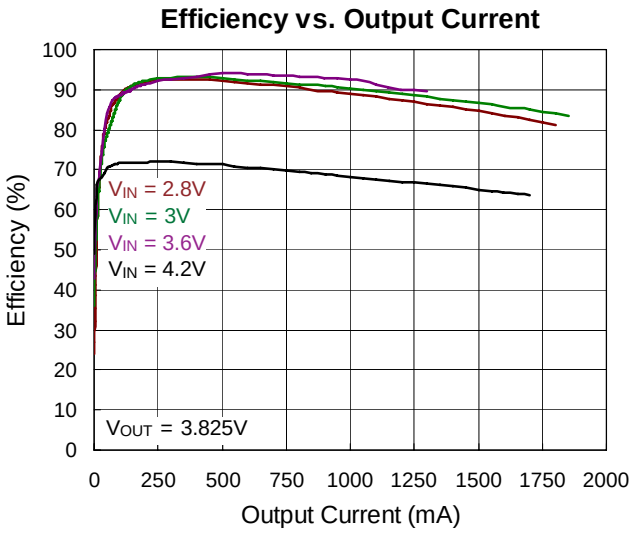
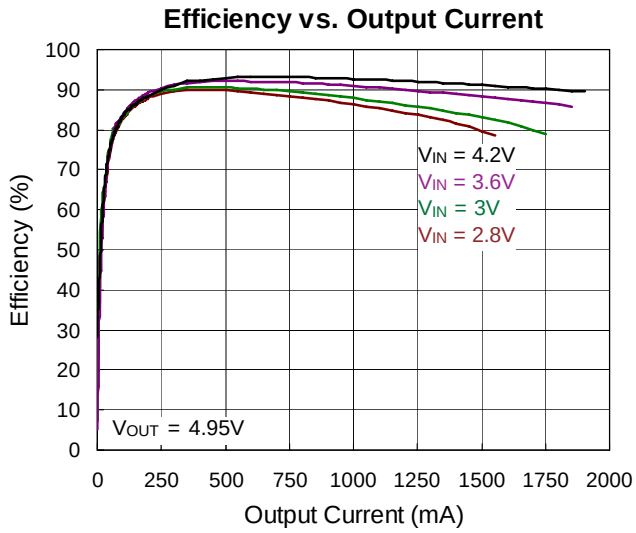
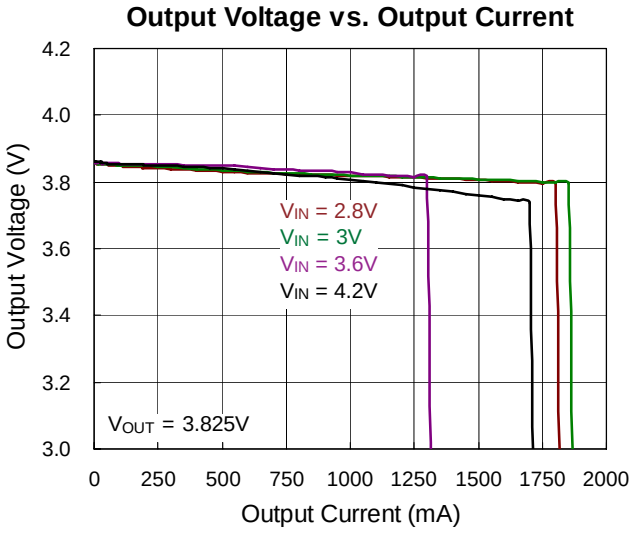


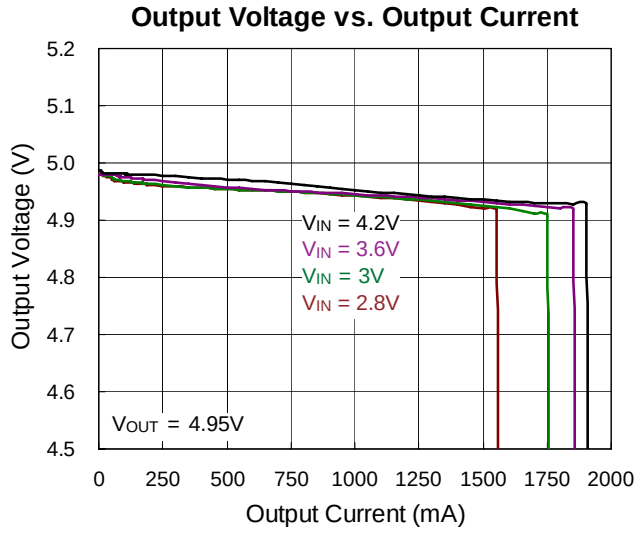
Figure 2. For EN Control

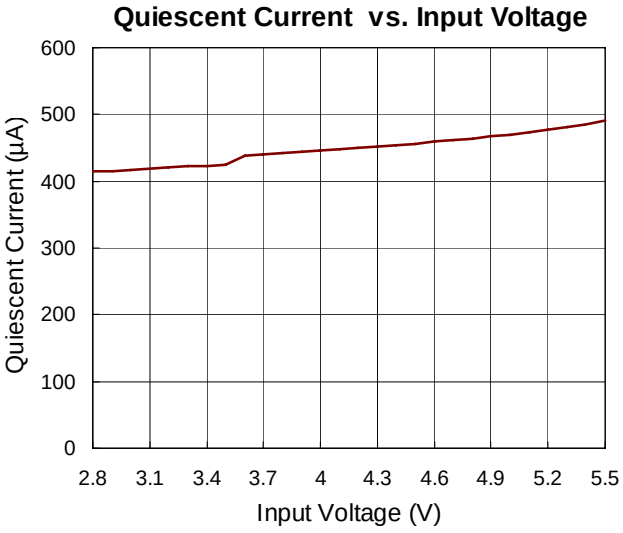
Typical Operating Characteristics

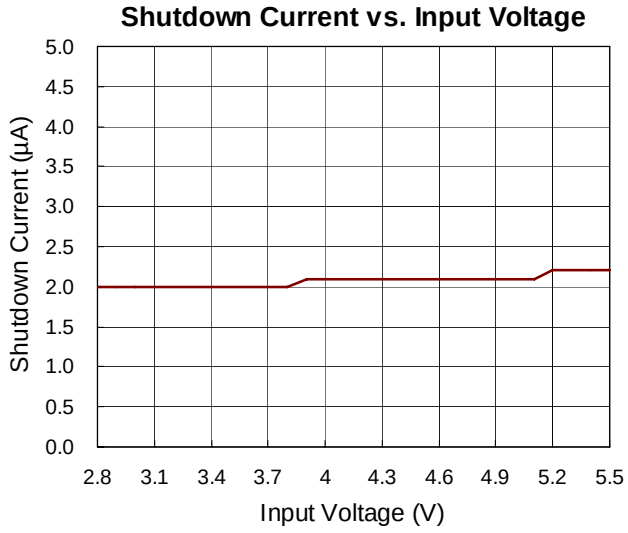




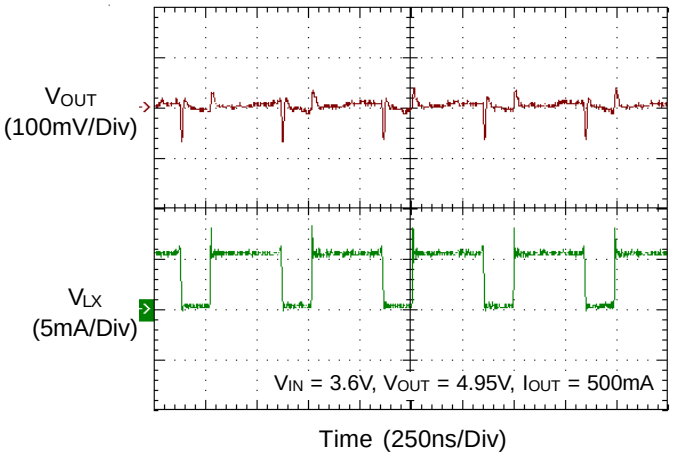




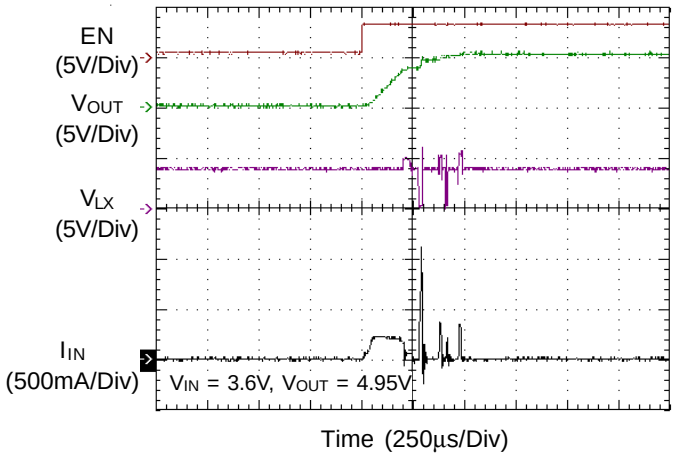




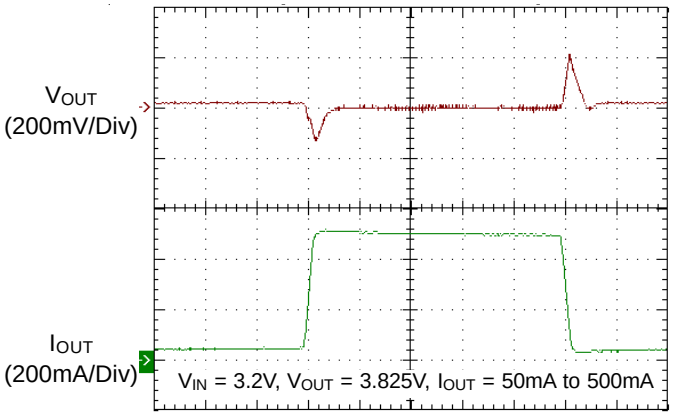
Output Voltage Ripple



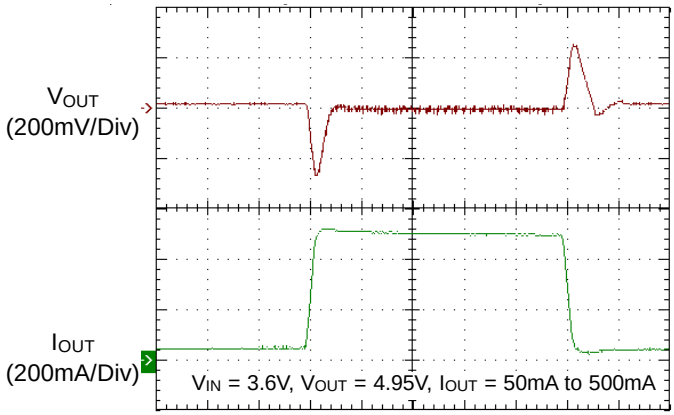
Power On



Voltage Mode Load Transient Response



Voltage Mode Load Transient Response



Application Information

The RT8540A is a high-efficiency, high-current Boost converter in all single-cell Lithium-ion/polymer battery operated products. The RT8450A provides the ability to regulate the input voltage that is higher than the designed output voltage with its down-conversion mode. The RT8450A turns off its down-conversion mode automatically once the input voltage falls to approximately 200mV below the output voltage.

Soft-Start

The RT8540A employs a soft-start feature to limit the inrush current. The soft-start circuit prevents the excessive inrush current and input voltage droop. The soft-start clamps the input inrush current for a typical period of 400μs.

Input UVLO

The input operating voltage range is from 2.8V to 5.5V. The RT8540A provides an Under Voltage Lockout (UVLO) function to prevent it from unstable issue when startup. The UVLO threshold of input rising voltage is set at 2.3V typically with a hysteresis of 200mV.

Over Voltage Protection (Open Circuit)

The RT8540A provides an internal over voltage protection to limit its output voltage. The OVP function prevents the RT8540A from damaging while open circuit condition is occurred.

Over Current Protection

The RT8540A provides an internal over current protection to limit its output current. The typical value of the maximum current is 4A.

Over Temperature Protection

The RT8540A provides an over temperature protection to prevent the IC from overheating. When the junction temperature of the RT8540A rises above 160°C, the OTP function will be triggered and then the regulator will be shutdown. The OTP comes with a hysteresis of 20°C. Once the temperature is reduced below the over temperature protection threshold by 20°C, the output will soft-start again.

Inductor Selection

The RT8540A adopts fixed frequency PWM control architecture. For stable operation and the 2MHz high switching frequency, it is recommended to use a 2.2μH inductor. Small size and high efficiency are the major concerns for portable device, so the inductor should have low core loss at 2MHz and low DCR for better efficiency.

Capacitor Selection

Input and output ceramic capacitors of 10μF are recommended for RT8540A applications. For better voltage filtering, ceramic capacitors with low ESR are recommended. The best performance of the RT8540A can be achieved by using the capacitor of large capacitance. X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Enable Selection Function

There is a SELECT pin on the RT8450A which provides the selection of I^2C enable or non-I^2C enable. By setting the SELECT pin "Low", the IC enters non-I^2C control operation. The IC will be enable when the EN pin is set "High", and the output is regulated by connecting the FB pin to VOUT with the dividing resistors. The VOUT is set between 3.825V and 5.45V. Setting the SELECT pin "High", the IC enters I^2C control operation. The RT8450A provides an integrated software control bit ENVM bit to force the converter to enter normal operation. Under this condition, the output will be regulated by integrated software control bits OV[3:0].

SELECT	EN	ENVM	Operation description
0	0	0	Shutdown
0	1	0	Enable
1	x	0	Shutdown
1	x	1	Enable

Register Map

Table 1. 0x04 Error Flag

Description	PG	FREE	OTP	FREE	FREE	Vout Short	FREE	
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory	R/W	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0
PG	Power Good bit. In write mode, this bit selects the functionality of the GPIO/PG output. 0 : PG signal is routed to the GPIO port. 1 : GPIO PORT VALUE bit is routed to the GPIO port. In read mode, this bit indicates the output voltage conditions. 0 : The converter is not operating within the voltage regulation limits. 1 : The output voltage is within it nominal value.							
OTP	Thermal shutdown tripped Indicator flag reset after readout.							
VOUT Short	VOUT Short error flag reset after readout.							

Table 2. 0x05

Description	RESET	ENPSM	DIR	GPIO	GPIOTYPE	FREE		
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory	R/W	R/W	R/W	R/W	R/W	R	R	R
Default	0	1	1	0	1	0	0	0
RESET	Register Reset bit. 0 : Normal operation. 1 : Default values are set to all internal registers.							
ENPSM	Enable/Disable Power-Save Mode bit. 0 : Power-save mode disabled. 1 : Power-save mode enabled.							
DIR	GPIO Direction bit. 0 : GPIO configured as input. 1 : GPIO configured as output.							
GPIO	GPIO Port Value. This bit contains the GPIO port Value.							
GPIOTYPE	GPIO Port Type. 0 : GPIO is configured as push-pull output. 1 : GPIO is configured as open-drain output.							

Table 3. 0x06 Output Voltage

Description	ENVM	FREE			OV [3:0]			
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory	R/W	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	0	0	1
OV[3:0]	Output Voltage Selection bits for I^2C Control : 0000 : 3.825V 0001 : 3.95V 0010 : 4.075V 0011 : 4.2V 0100 : 4.325V 0101 : 4.45V 0110 : 4.575V 0111 : 4.7V 1000 : 4.825V 1001 : 4.95V 1010 : 5.075V 1011 : 5.2V 1100 : 5.325V 1101 to 1111 : 5.45V							
ENVM	Enable Voltage Mode bit. 0 : Shutdown mode. 1 : Normal operation.							

Register Summary

Address : 0110011x

Register	Description	PG	FREE	OTP	FREE	FREE	Vout Short	FREE	
0x04	Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	Memory	R/W	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0
0x05	Description	RESET	ENPSM	DIR	GPIO	GPIOTYPE	FREE		
	Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	Memory	0	1	1	0	1	0	0	0
	Default	R/W	R/W	R/W	R/W	R/W	R	R	R
0x06	Description	ENVM	FREE			OV [3:0]			
	Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	Memory	R/W	R	R	R	R/W	R/W	R/W	R/W
	Default	0	0	0	0	1	0	0	1

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-20L 4x4 package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 3.57W for WQFN-20L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

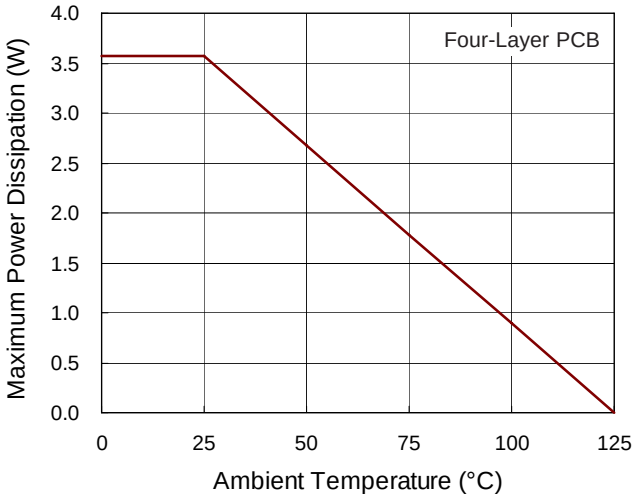


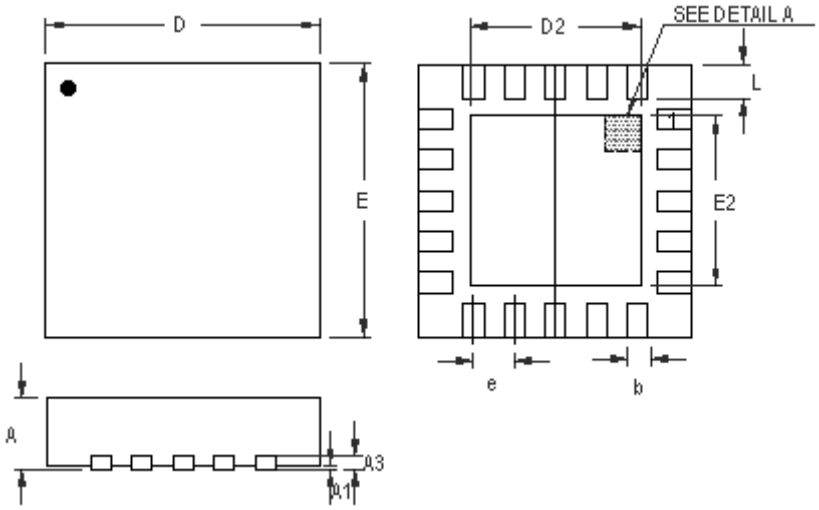
Figure 3. Derating Curve of Maximum Power Dissipation

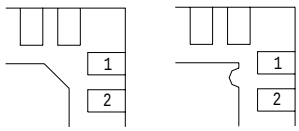
Layout Consideration

For the best performance of the RT8540A, following PCB layout guidelines should be strictly followed.

- The PGND of the IC should be connected to the ground plane of the PCB
- The output bypass capacitor should be placed as close to the IC as possible
- The trace lengths from the IC to the inductor, input capacitor and the output capacitor must be kept as short, direct and wide as possible.
- C_{IN} and C_{OUT} of the RT8540A should be placed as close as possible and connected to PGND of the IC.
- It is recommended to add additional PCB exposed pad area for the flash LEDs for maximized heat-sinking ability. This is necessary for high current application and long flash duration application.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.300	0.006	0.012
D		3.900	4.100	0.154	0.161
D2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.100	2.200	0.083	0.087
E		3.900	4.100	0.154	0.161
E2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.100	2.200	0.083	0.087
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 20L QFN 4x4 Package

Richtek Technology Corporation

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789