76V Boost DC/DC Converter with APD Current Monitor

General Description

The RT8550 is a high performance, low noise Boost DC/DC converter with an integrated internal switch and an avalanche photodiodes (APD) current monitor. The RT8550's input voltage ranges from 2.8V to 5.5V, and it can support the output voltage up to 76V. When used in optical receiver application to drive the high voltage APD diode, the output voltage of the RT8550 can be further doubled up by a typical voltage doubler circuit. The RT8550 adapts fixed frequency, current mode PWM control loop to regulate the output voltage with fast transient response and cycle-by-cycle current limit. With 400kHz switching frequency, the RT8550 system board can be made compact to achieve low system BOM cost. The soft-start function and PWM loop compensation is also built-in internally to save external soft-start capacitor and PWM loop compensation components. The RT8550 features accurate APD current monitoring output with 5:1 ratio at the MON pin. A Resistor-adjustable APD current limit function protects the APD diode from Boost output transients. The protection features of the RT8550 include input under-voltage lockout and over temperature protection. The RT8550 is available in the small and WQFN-16L 3x3 package.

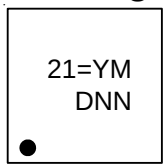
Features

- **Input Voltage Range : 2.8V to 5.5V**
- **Up to 76V Output Voltage**
- **400kHz Fixed Switching Frequency**
- **Internal Compensation and Soft-Start**
- **APD Current Monitor within ±5% Tolerance**
- **5:1 Ratio outputs for APD Current Monitoring**
- **Low Shutdown Current : <1μA**
- **Programmable APD Current Limit**
- **RoHS Compliant and Halogen Free**

Applications

- APD Bias Supply
- PIN Diode Bias Supply
- Optical Receivers and Modules
- Fiber Optic Network Equipment
- GPON Modules

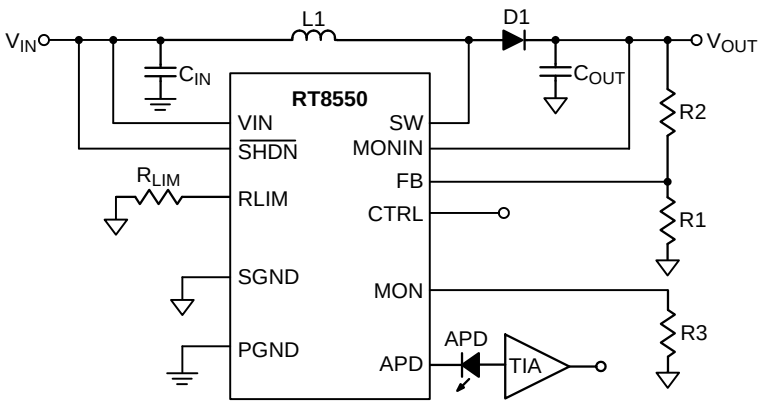
Marking Information



21= : Product Code

YMDNN : Date Code

Simplified Application Circuit



Ordering Information

RT8550□□

- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

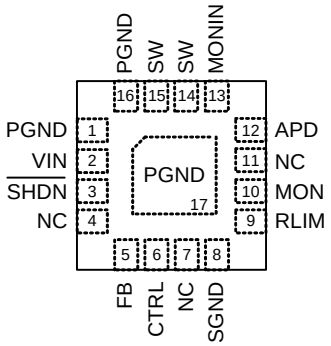
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

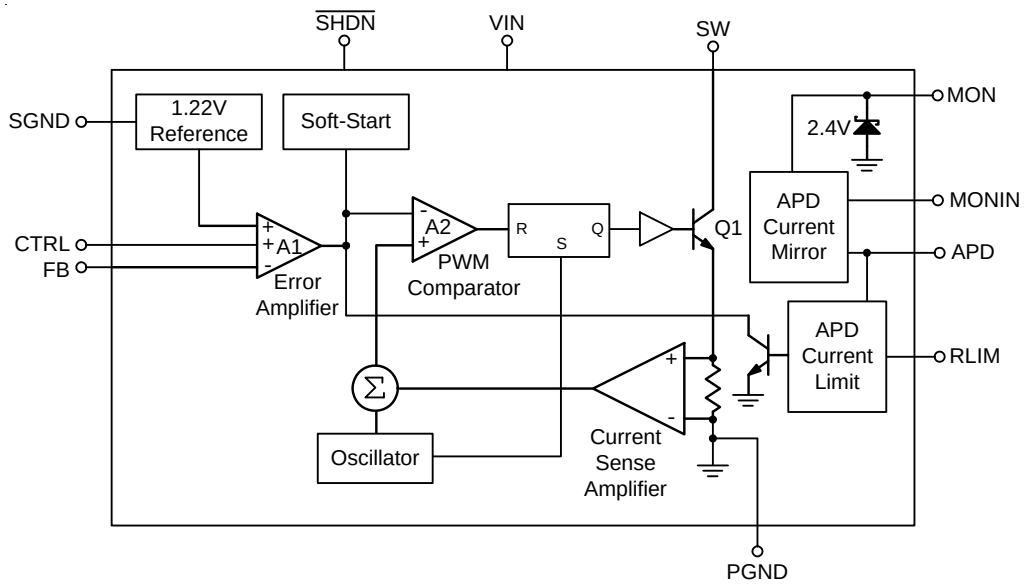


WQFN-16L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 16, 17 (Exposed Pad)	PGND	Power Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation
2	VIN	Supply Voltage Input. Connect a 1μF capacitor from this pin to GND.
3	$\overline{SHDN}$	Shutdown Control Input. Apply a logic-low voltage to $\overline{SHDN}$ to shut down the device. Connect $\overline{SHDN}$ to VIN for normal operation. Ensure that $\overline{SHDN}$ is not greater than the input voltage, VIN.
4, 7, 11	NC	No Internal Connection.
5	FB	Feedback Voltage Input. Connect the pin to the output resistor divider for output voltage setting.
6	CTRL	External Reference Control Input. This allows the FB voltage to follow the external reference between 0V and 1.2V. Tie this pin higher than 1.5V to use the internal reference of 1.22V.
8	SGND	Signal Ground.
9	RLIM	Current Limit Resistor Connection. Connect a resistor from RLIM to SGND to program the APD current limit threshold. When RLIM is connected to SGND, the current limit is set to 4mA.
10	MON	Output for Current Monitor. It sources a current equal to 20% of the APD current and converts to a reference voltage through an external resistor. An internal clamp circuit for MON pin with clamp level around 2.4V is included inside.
12	APD	Output for APD. Connect this Pin to the APD Cathode.
13	MONIN	Current Monitor Input. An optional resistor between the VOUT and MONIN pins can be used for current limit setting.
14, 15	SW	Switch Node of Boost Converter. Minimize the trace area on this pin to reduce EMI.

Function Block Diagram



Operation

The RT8550 Boost converter uses a constant frequency current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Functional Diagram. At the start of each oscillator cycle, the SR latch is set, which turns on the power switch, Q1. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator, A2. When this voltage exceeds the level at the negative input of A2, the SR latch is reset to turn off the power switch. The level at the negative input of A2 is set by the error amplifier A1, and is simply an amplified version of the difference between the feedback voltage and the reference voltage of 1.22V, or externally provided CTRL voltage. In this manner, the error amplifier sets the correct peak current level to keep the output in regulation.

If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered.

The RT8550 has an integrated high-side APD current monitor with a 5:1 ratio. The MONIN pin can accept a supply voltage up to 76V, which is suitable for APD photodiode applications. The MON pin has an open circuit protection feature and is internally clamped to 2.4V. If an APD is tied to the APD pin, the current will be mirrored to the MON pin and converted to a voltage signal by the resistor R3. This voltage signal can be used to drive an external control block to adjust the APD voltage by adjusting the feedback threshold of EAMP A1 through the CTRL input. The RT8550 also integrates an internal clamp circuit for the MON pin with clamp level around 2.4V.

Absolute Maximum Ratings (Note 1)

- VIN, $\overline{SHDN}$, FB, RLIM, CTRL to SGND ---------- –0.3V to 6V
- SW to PGND ---------- –0.3V to 80V
- MONIN, APD to SGND ---------- –0.3V to 80V
- MON to SGND ---------- –0.3V to 3V
- PGND to SGND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = $V_{\overline{SHDN}}$ = V_{CTRL} = 3.3V, C_{IN} = 1µF, V_{PGND} = V_{SGND} = 0V, V_{MONIN} = 40V, SW = APD = unconnected, V_{MOUT} = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
Supply Current	I_{SUPPLY}	V_{FB} = 1.4V, Not Switching	--	2	2.5	mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	--	2.3	2.75	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}		--	130	200	mV
Shutdown Current	$I_{CC\_\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V	--	0.1	1	µA
Shutdown Input Current	$I_{\overline{SHDN}}$	V_{IN} = 3.3V, $V_{\overline{SHDN}}$ = 3V	--	--	2	µA
Boost Converter						
Output Voltage Adjustment Range			V_{IN} + 5	--	76	V
Switching Frequency	f_{SW}	V_{IN} = 5V	--	400	--	kHz
Maximum Duty Cycle	D_{MAX}	V_{IN} = 2.8V	90	92	--	%
FB Voltage	V_{FB}		1.2	1.23	1.26	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.2V	--	100	500	nA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Switch On-Resistance		I_{SW} = 100mA, V_{IN} = 3.3V	--	1	2	Ω
Peak Switch Current Limit			0.58	0.7	0.88	A
SW Leakage Current		V_{SW} = 76V	--	--	1	μA
Line Regulation		V_{IN} = 2.8V to 5.5V	--	0.5	1	%
Soft-Start Duration		(Note 5)	--	10	--	ms
Control Input (CTRL)						
CTRL Transition Threshold		V_{FB} = V_{REF} above this voltage	--	1.37	--	V
CTRL Input Bias Current		V_{CTRL} = V_{FB_SET}	--	--	500	nA
Current Monitor						
MONIN Voltage Range	V_{MONIN}		4.5	10	76	V
MONIN Supply Current	I_{MONIN}	I_{APD} = 1μA, V_{MONIN} = 76V	--	1.3	--	μA
		I_{APD} = 2.5mA, V_{MONIN} = 76V	--	3	5	mA
Voltage Drop	V_{DROP}	I_{APD} = 2mA, V_{MONIN} = 76V, V_{DROP} = V_{MONIN} − V_{APD}	--	3.5	5	V
MON Leakage Current		APD is Unconnected	--	1	300	nA
MON Clamp Voltage	V_{MOUT}	Forward Diode Current = 1mA	--	2.3	--	V
Current Gain	$\frac{I_{MON}}{I_{APD}}$	I_{APD} = 1μA, 10V ≤ MONIN ≤ 76V Boost Switch Off	0.18	0.2	0.22	mA/mA
		I_{APD} = 2.5mA, 10V ≤ MONIN ≤ 76V Boost Switch Off	0.18	0.2	0.22	
Current Limit Adjustment Range		R_{LIM} = 4.7kΩ	--	2	--	mA
Logic I/O						
$\overline{SHDN}$ Input Voltage	High	V_{IH}	2	--	--	V
	Low	V_{IL}	--	--	0.5	
Thermal Protection						
Thermal Shutdown Threshold	T_{SD}	Temperature Rising	--	150	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

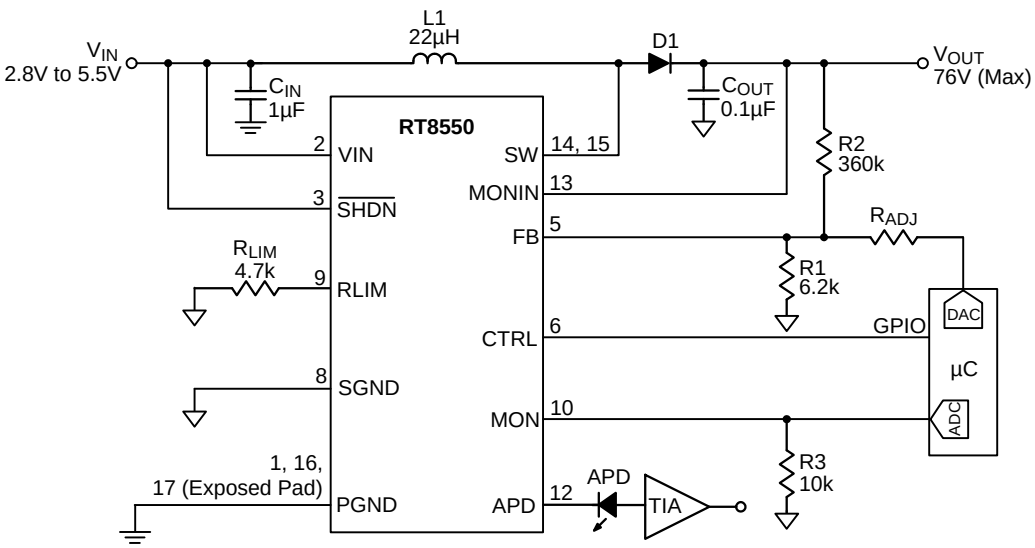
Note 2. θ_{JA} is measured at T_A = 25 °C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

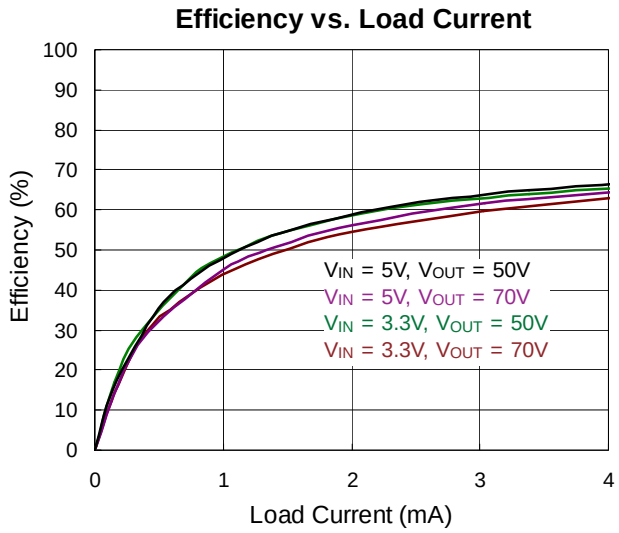
Note 4. The device is not guaranteed to function outside its operating conditions.

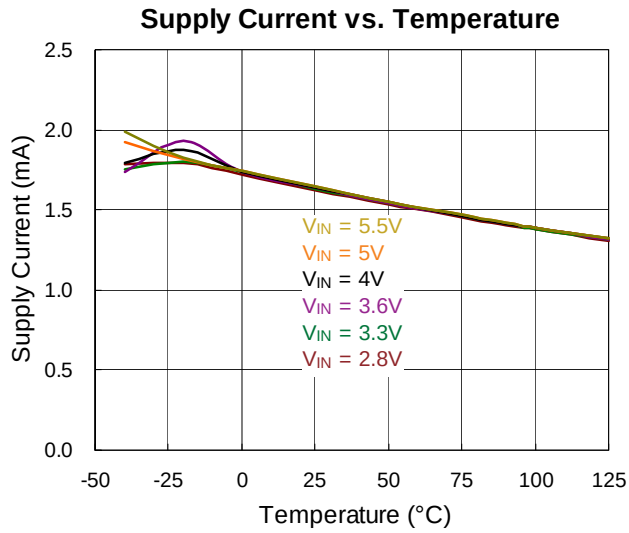
Note 5. Guarantee by design.

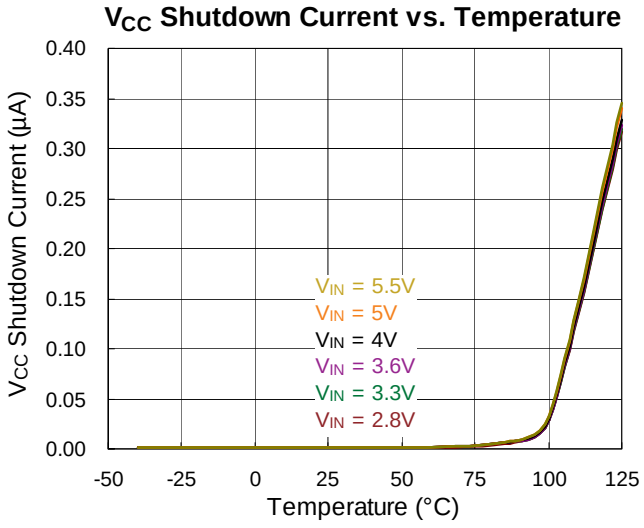
Typical Application Circuit

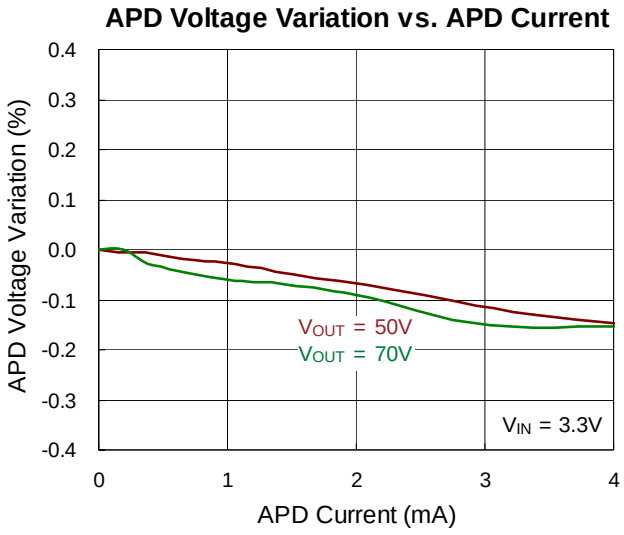


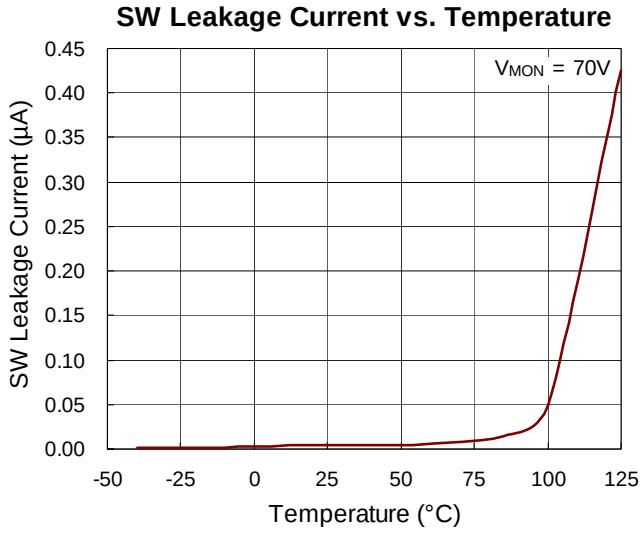
Typical Operating Characteristics

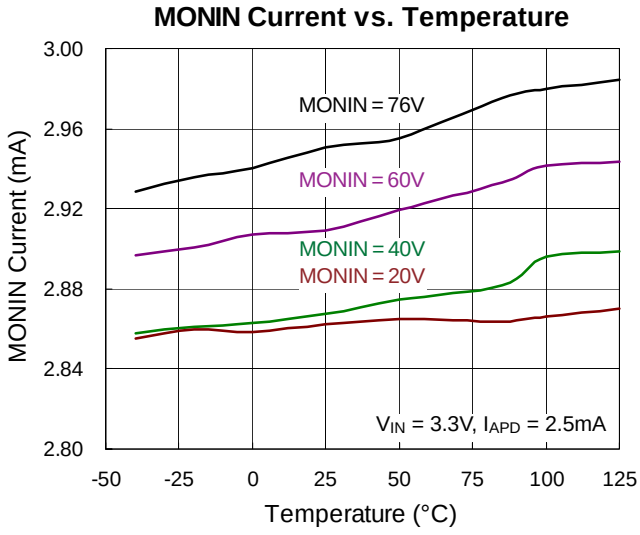




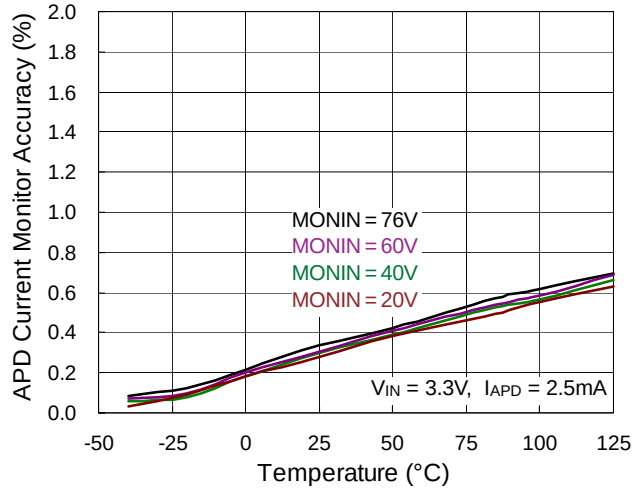




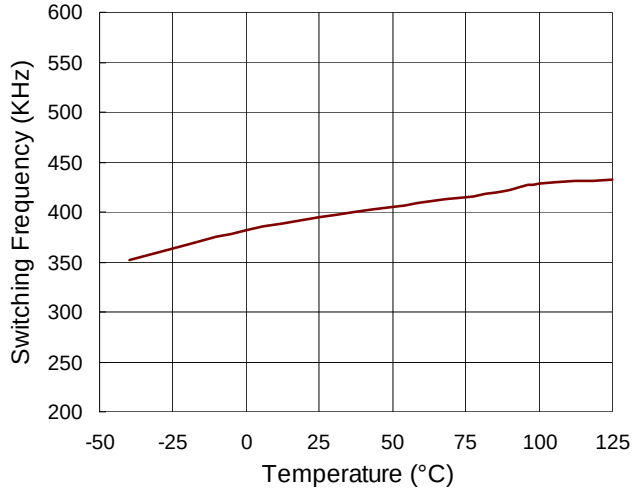




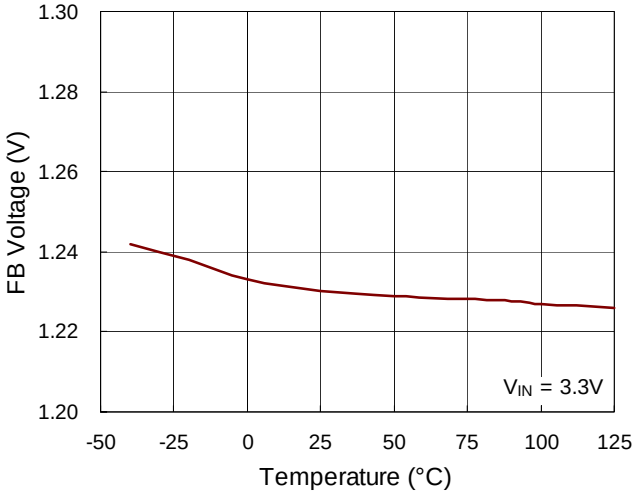
APD Current Monitor Accuracy vs. Temperature



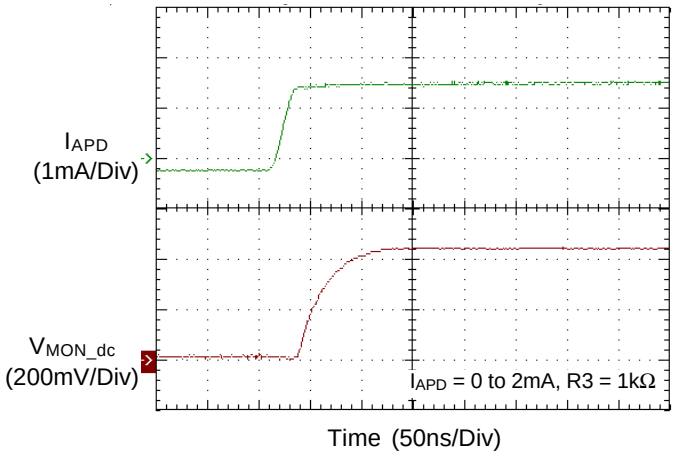
Switching Frequency vs. Temperature



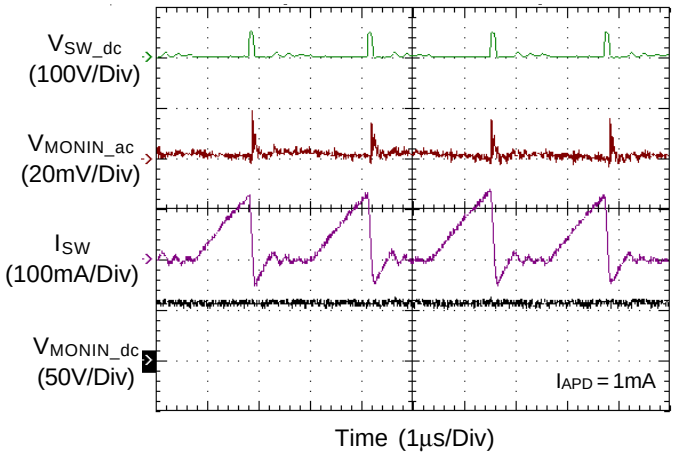
FB Voltage vs. Temperature



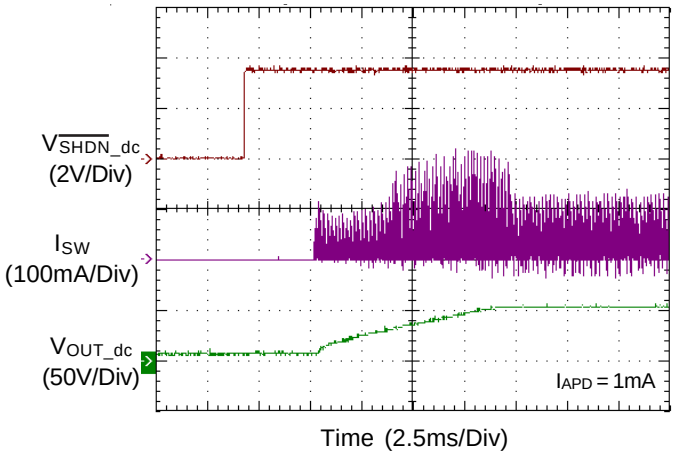
APD Transient Response



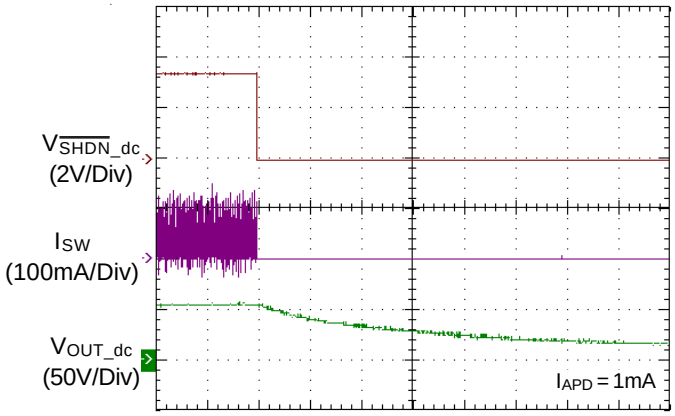
Switching Waveform Response



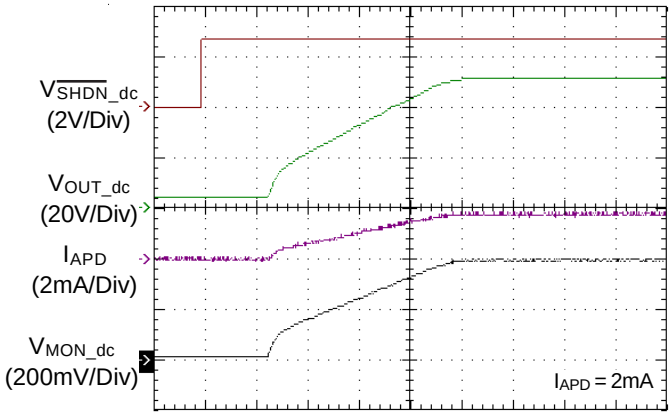
SHDN ON Response



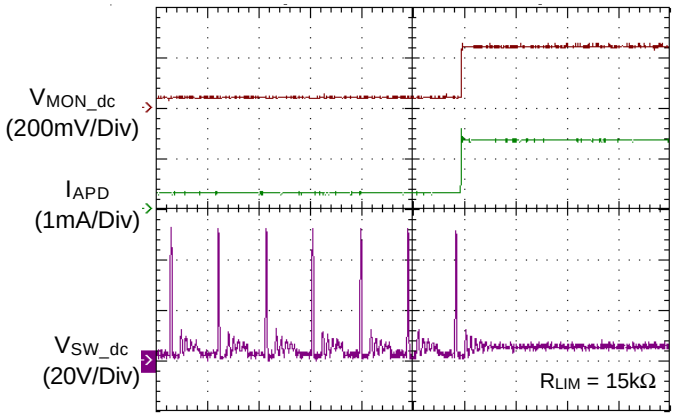
SHDN OFF Response



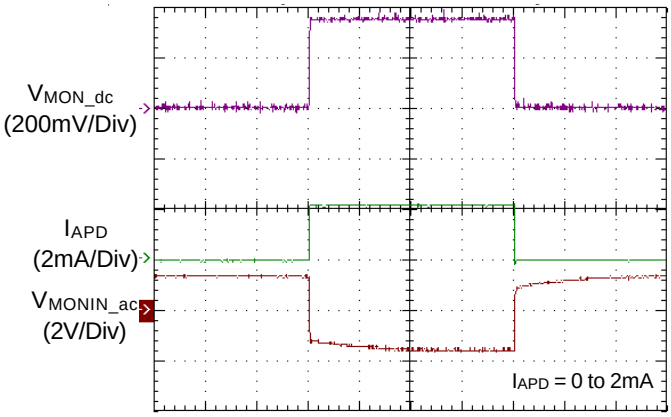
Start Up Delay Response



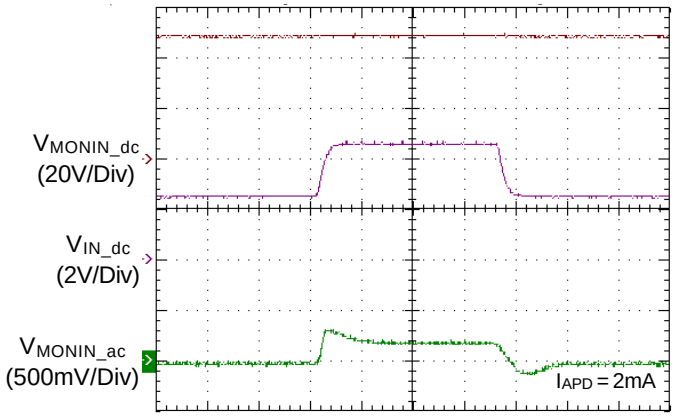
APD Short Response



Load Transient Response



Line Transient Response



Applications Information

Boost Regulator

The RT8550 is a current mode Boost converter integrated with a 76V/700mA power switch over a wide VIN range from 2.8V to 5.5V. It performs fast transient responses to support the avalanche photodiodes (APDs) in optical receivers. The high operation frequency allows the use of small components to minimize the thickness of the optical transceiver. The output voltage can be adjusted by an external resistive voltage divider connected to the FB pin. The error amplifier compensates the output voltage by comparing the FB voltage and internal reference voltage. For better stability, the slope compensation signal summed with the current sense signal will be compared with internal compensation to determine the current trip point and duty cycle.

Output Voltage Setting

The RT8550 regulated output voltage is shown as the following equation :

$$V_{OUT} = V_{REF} \times \left(1+\frac{R1}{R2}\right), \text{ where } V_{REF} = 1.22V \quad (typ.)$$

The recommended value for R2 should be at least 10kΩ without some sacrifices. Place the resistive voltage divider as close as possible to the chip to reduce noise sensitivity.

Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{APD}}{\eta \times V_{IN}}$$

where η is the efficiency of the converter, $I_{IN(MAX)}$ is the maximum input current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

I_{PEAK} = 1.2 x $I_{IN(MAX}$

Note that the saturated current of the inductor must be greater than I_{PEAK}. The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{APD} \times f_{SET}}$$

where f_{SET} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems. Place a higher 22μH inductor to achieve the lower output voltage ripple.

Output Capacitor Selection

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of the inductor current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. ΔV_{OUT} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{APD}\right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{APD}\right)\right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{SET}} = C_{OUT} \times \Delta V_{OUT}$$

where f_{SET} is the switching frequency, and ΔI_L is the inductor ripple current. Bring C_{OUT} to the left side to estimate the value of ΔV_{OUT} according to the following equation :

$$\Delta V_{OUT} = \frac{D \times I_{APD}}{\eta \times C_{OUT} \times f_{SET}}$$

where D is the duty cycle and η is the Boost converter efficiency. Finally, taking ESR into account, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

For applications with output voltage less than 45V, intermediate output V_{OUT} can directly serve as the output. Typically use a 0.47μF capacitor for output voltage less than 25V and 1μF capacitor for output voltage between 25V and 45V. Either ceramic or solid tantalum capacitors may be used for the input decoupling capacitor, which should be placed as close as possible to the RT8550. A 1μF capacitor is sufficient for most applications.

Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input voltage ripple caused by switching operation. A 10μF capacitor is sufficient for most applications. Nevertheless, this value can be decreased for lower output current requirement. Another consideration is the voltage rating of the input capacitor which must be greater than the maximum input voltage.

APD Current Monitor

The power supply switching noise associated with a switching power supply can interfere with the photodiode DC measurement. To suppress this noise, a 0.1μF capacitor is recommended at the MONIN pin. An additional output low-pass filter, a 10k resistor and a 10nF capacitor in parallel at the MON pin might limit the measurement accuracy of low level signals. For applications requiring fast current monitor response time, a RC low-pass filter at the MONIN pin is used to replace the 0.1μF capacitor at the APD pin to reduce the power supply noise and other wide band noise.

APD Short Current Protection

The current limit of the current monitor is adjustable from 1mA to 4mA (typ). Connect RLIM to SGND to get a default current-limit threshold of 4mA or connect a resistor from RLIM to SGND to program the current-limit threshold below the default setting. Calculate the value of the external resistor, R_{LIM}, for a given current limit using the following Table 1 :

Table 1. APD Current Limit vs. R_{LIM} Value (1% Resistors)

R_{LIM} (kΩ)	APD Current Limit (mA)
8.2	1
4.7	2
3	3
1	4

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

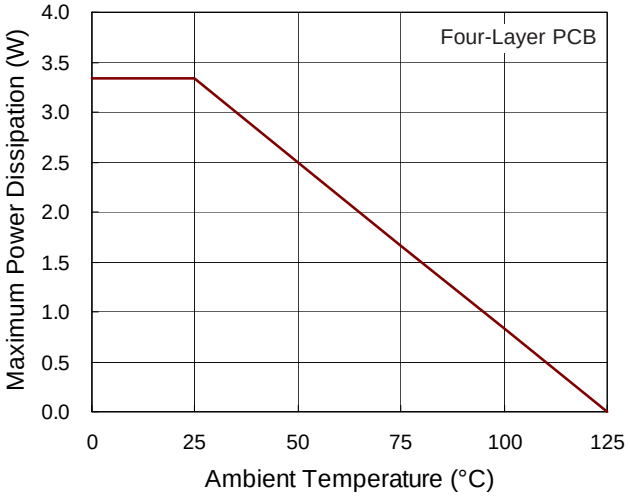


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

PCB layout is very important for designing switching power converter circuits. The following layout guides should be strictly followed for best performance of the RT8550.

The power components, L1, D1, C_{IN}, C_{OUT} must be placed as close as possible to reduce current loop. The PCB trace between power components must be as short and wide as possible.

- Place L1 and C_{IN} as close as possible to VIN pin. The trace of SW connection should be as short and wide as possible.
- The Feedback loop should be kept away from the power path and should be shielded with a ground trace to prevent any noise coupling. Place the feedback components as close as possible to FB pin.
- The exposed pad of the chip should be connected to ground plane for thermal consideration.

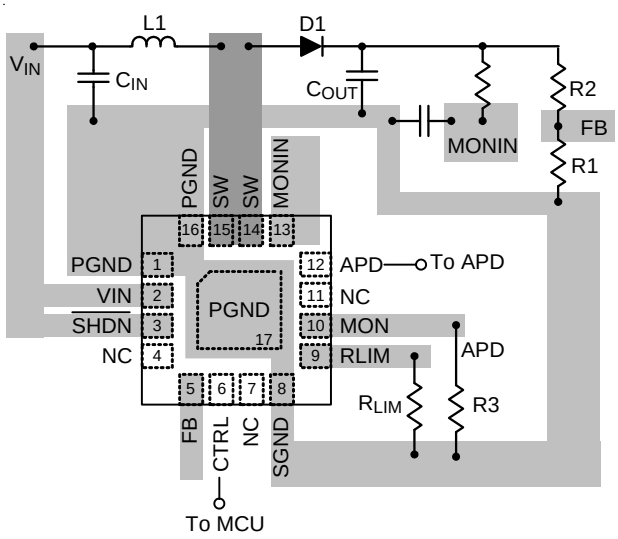
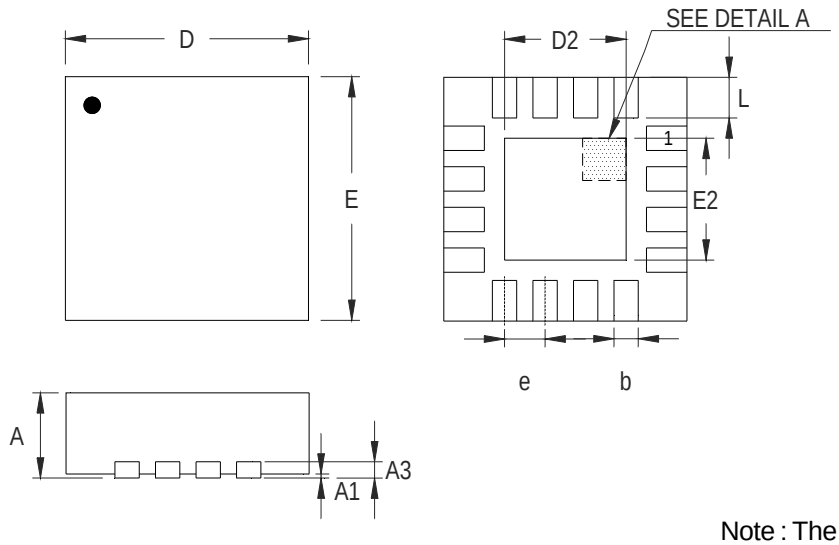
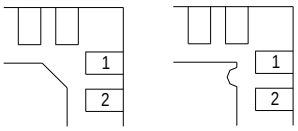


Figure 2. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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