4/3/2-Phase PWM Controller for AMD AM2/AM2+/AM3/FM1 CPUs

General Description

The RT8871A/B is a 4/3/2-phase synchronous buck controller with two integrated MOSFET drivers for CPU power application and a single-phase buck with integrated MOSFET driver for North-Bridge (NB) chipset. The RT8871A/B uses differential inductor DCR current sense to achieve phase current balance and active voltage positioning. Other features include adjustable operating frequency, power good indication, external error-amp compensation, over voltage protection, over current protection and enable/shutdown for various applications. The RT8871A/B comes in a small footprint with WQFN-48L 7x7 and WQFN-48L 6x6 packages.

Applications

- Desktop CPU Core Power
- Low Voltage, High Current DC/DC Converter

Ordering Information

RT8871A/B □□

- Package Type
  - QW : WQFN-48L 7x7 (W-Type)
  - QW : WQFN-48L 6x6 (W-Type) (Exposed Pad-Option 1)
- Lead Plating System
  - Z : ECO (Ecological Element with Halogen Free and Pb free)
- A : WQFN-48L 7x7
  - B : WQFN-48L 6x6

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **12V Power Supply Voltage**
- **4/3/2-Phase Power Conversion for V_{CORE} Power**
- **3 Embedded MOSFET Drivers (2 for CPU and 1 for NB)**
- **Internal Regulated 5V Output**
- **Support AMD AM2 6-bit Parallel and AM2+ 7-bit Serial VID with Dual OCP**
- **Support 3.4MHz High Speed I^2C**
- **Support Programmable Load Line for CORE and NB Sections**
- **Continuous Differential Inductor DCR Current Sense**
- **Adjustable Frequency (Typically at 300kHz)**
- **Selectable 1 or 2 Phase in Power-Saving (PS) Mode**
- **Phase-Interleaving for V_{CORE} Controller**
- **Power Good Indication**
- **Adjustable Over Current Protection**
- **Over Voltage Protection**
- **Small 48-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Marking Information

RT8871AZQW

RT8871AZQW : Product Code

YMDNN : Date Code

RT8871BZQW

RT8871BZQW : Product Code

YMDNN : Date Code

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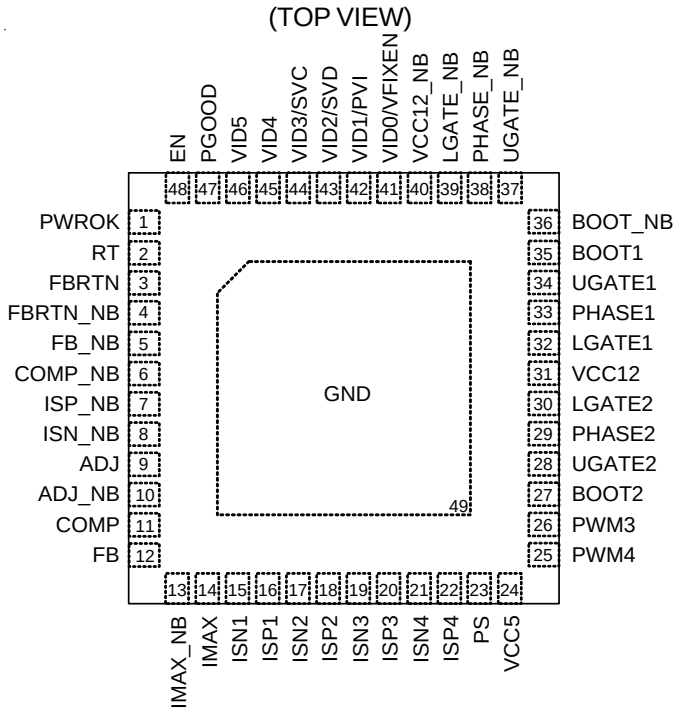
Pin Configurations



WQFN-48L 7x7/WQFN-48L 6x6

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Typical Application Circuit

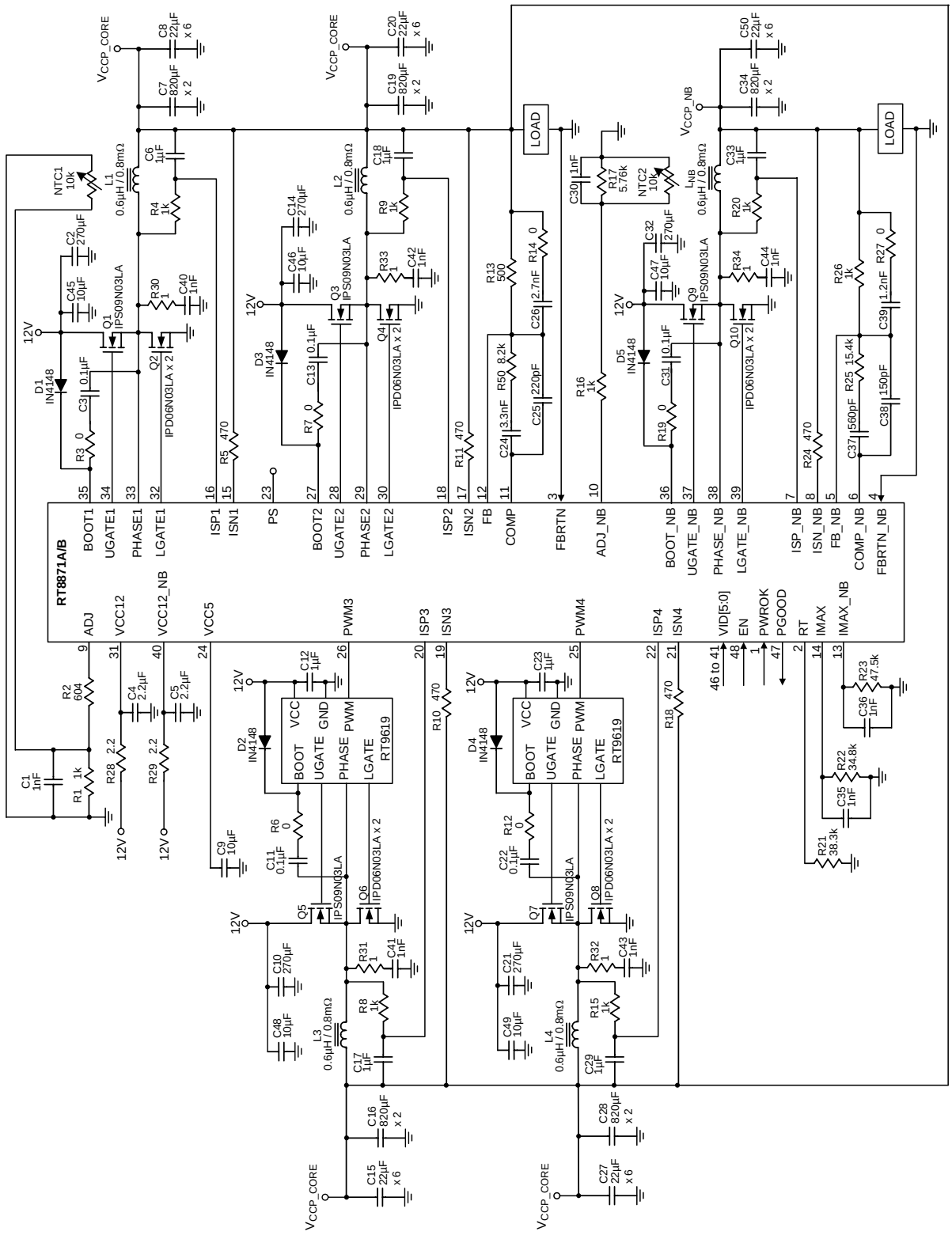

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Table 1. 7-bit VID Code Table for AM2+/AM3/FM1 CPU (Serial)

SVID[6:0]	Voltage	SVID[6:0]	Voltage	SVID[6:0]	Voltage	SVID[6:0]	Voltage
0000000	1.5500	0100000	1.1500	1000000	0.7500	1100000	0.3500
0000001	1.5375	0100001	1.1375	1000001	0.7375	1100001	0.3375
0000010	1.5250	0100010	1.1250	1000010	0.7250	1100010	0.3250
0000011	1.5125	0100011	1.1125	1000011	0.7125	1100011	0.3125
0000100	1.5000	0100100	1.1000	1000100	0.7000	1100100	0.3000
0000101	1.4875	0100101	1.0875	1000101	0.6875	1100101	0.2875
0000110	1.4750	0100110	1.0750	1000110	0.6750	1100110	0.2750
0000111	1.4625	0100111	1.0625	1000111	0.6625	1100111	0.2625
0001000	1.4500	0101000	1.0500	1001000	0.6500	1101000	0.2500
0001001	1.4375	0101001	1.0375	1001001	0.6375	1101001	0.2375
0001010	1.4250	0101010	1.0250	1001010	0.6250	1101010	0.2250
0001011	1.4125	0101011	1.0125	1001011	0.6125	1101011	0.2125
0001100	1.4000	0101100	1.0000	1001100	0.6000	1101100	0.2000
0001101	1.3875	0101101	0.9875	1001101	0.5875	1101101	0.1875
0001110	1.3750	0101110	0.9750	1001110	0.5750	1101110	0.1750
0001111	1.3625	0101111	0.9625	1001111	0.5625	1101111	0.1625
0010000	1.3500	0110000	0.9500	1010000	0.5500	1110000	0.1500
0010001	1.3375	0110001	0.9375	1010001	0.5375	1110001	0.1375
0010010	1.3250	0110010	0.9250	1010010	0.5250	1110010	0.1250
0010011	1.3125	0110011	0.9125	1010011	0.5125	1110011	0.1125
0010100	1.3000	0110100	0.9000	1010100	0.5000	1110100	0.1000
0010101	1.2875	0110101	0.8875	1010101	0.4875	1110101	0.0875
0010110	1.2750	0110110	0.8750	1010110	0.4750	1110110	0.0750
0010111	1.2625	0110111	0.8625	1010111	0.4625	1110111	0.0675
0011000	1.2500	0111000	0.8500	1011000	0.4500	1111000	0.0500
0011001	1.2375	0111001	0.8375	1011001	0.4375	1111001	0.0375
0011010	1.2250	0111010	0.8250	1011010	0.4250	1111010	0.0250
0011011	1.2125	0111011	0.8125	1011011	0.4125	1111011	0.0125
0011100	1.2000	0111100	0.8000	1011100	0.4000	1111100	OFF
0011101	1.1875	0111101	0.7875	1011101	0.3875	1111101	OFF
0011110	1.1750	0111110	0.7750	1011110	0.3750	1111110	OFF
0011111	1.1625	0111111	0.7625	1011111	0.3625	1111111	OFF

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Table 2. 6-bit VID Code Table for AM2 CPU (Parallel)

VID[5:0]	Voltage	VID[5:0]	Voltage	VID[5:0]	Voltage	VID[5:0]	Voltage
000000	1.5500	010000	1.1500	100000	0.7625	110000	0.5625
000001	1.5250	010001	1.1250	100001	0.7500	110001	0.5500
000010	1.5000	010010	1.1000	100010	0.7375	110010	0.5375
000011	1.4750	010011	1.0750	100011	0.7250	110011	0.5250
000100	1.4500	010100	1.0500	100100	0.7125	110100	0.5125
000101	1.4250	010101	1.0250	100101	0.7000	110101	0.5000
000110	1.4000	010110	1.0000	100110	0.6875	110110	0.4875
000111	1.3750	010111	0.9750	100111	0.6750	110111	0.4750
001000	1.3500	011000	0.9500	101000	0.6625	111000	0.4625
001001	1.3250	011001	0.9250	101001	0.6500	111001	0.4500
001010	1.3000	011010	0.9000	101010	0.6375	111010	0.4375
001011	1.2750	011011	0.8750	101011	0.6250	111011	0.4250
001100	1.2500	011100	0.8500	101100	0.6125	111100	0.4125
001101	1.2250	011101	0.8250	101101	0.6000	111101	0.4000
001110	1.2000	011110	0.8000	101110	0.5875	111110	0.3875
001111	1.1750	011111	0.7750	101111	0.5750	111111	0.3750

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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PWROK	PWROK Input Signal.
2	RT	Frequency Adjust Pin. Connect this pin to GND via a resistor to adjust frequency.
3	FBRTN	Remote Sense Ground for CORE.
4	FBRTN_NB	Remote Sense Ground for NB.
5	FB_NB	Inverting Input of Error-Amp for NB.
6	COMP_NB	Output of Error-Amp and Input of PWM Comparator for NB.
7	ISP_NB	Positive Current Sense Pin of NB.
8	ISN_NB	Negative Current Sense Pin of NB.
9	ADJ	Load Line Set Pin for VCORE. Connect this pin to GND via a resistor to set load line of VCORE.
10	ADJ_NB	Load Line Set Pin for NB. Connect this pin to GND by a resistor to set load line of NB.
11	COMP	Output of Error-Amp and Input of PWM Comparator of V_{CORE}.
12	FB	Inverting Input of Error-Amp of V_{CORE}.
13	IMAX_NB	OCP Set Pin for NB. Connect this pin to GND via a resistor to set OCP of NB.
14	IMAX	OCP Set Pin for VCORE. Connect this pin to GND via a resistor to set OCP of VCORE.
15, 17, 19, 21	ISN1, ISN2, ISN3, ISN4	Negative Current Sense Pin of Channel 1, 2, 3 and 4.
16, 18, 20, 22	ISP1, ISP2, ISP3, ISP4	Positive Current Sense Pin of Channel 1, 2, 3 and 4.
23	PS	Power Saving Mode Selection Pin.
24	VCC5	Output of Internal 5V Regulator for Control Circuits Power Supply. Connect this pin to GND by a ceramic capacitor larger than 1μF.
25,26	PWM4, PWM3	PWM Output for Channel 4 and Channel 3.
27, 35, 36	BOOT2, BOOT1, BOOT_NB	Bootstrap Supply for Channel 2 and Channel 1 and NB.
28, 34, 37	UGATE2, UGATE1, UGATE_NB	Upper Gate Driver for Channel 2 and Channel 1 and NB.
29, 33, 38	PHASE2, PHASE1, PHASE_NB	Switching Node of Channel 2 and Channel 1 and NB.
30, 32, 39	LGATE2, LGATE1, LGATE_NB	Lower Gate Driver for Channel 2 and Channel 1 and NB.
31, 40	VCC12, VCC12_NB	IC Power Supply. Connect this pin to 12V.
41	VID0/VFIXEN	PVI Mode : Voltage Identification Input for DAC. SVI Mode : VFIXEN Selection Input.
42	VID1/PVI	This Pin Selects PVI/SVI Mode Based on the State of this Pin Prior to EN Signal. PVI Mode : Voltage Identification Input for DAC.
43	VID2/SVD	PVI Mode : Voltage Identification Input for DAC. SVI Mode : Serial Data Input.
44	VID3/SVC	PVI Mode : Voltage Identification Input for DAC. SVI Mode : Serial Clock Input.
45, 46	VID4, VID5	PVI Mode : Voltage Identification Input for DAC.
47	PGOOD	Power Good Indicator (open drain).
48	EN	Enable Input Signal.
49 (Exposed pad)	GND	Reference Ground for IC. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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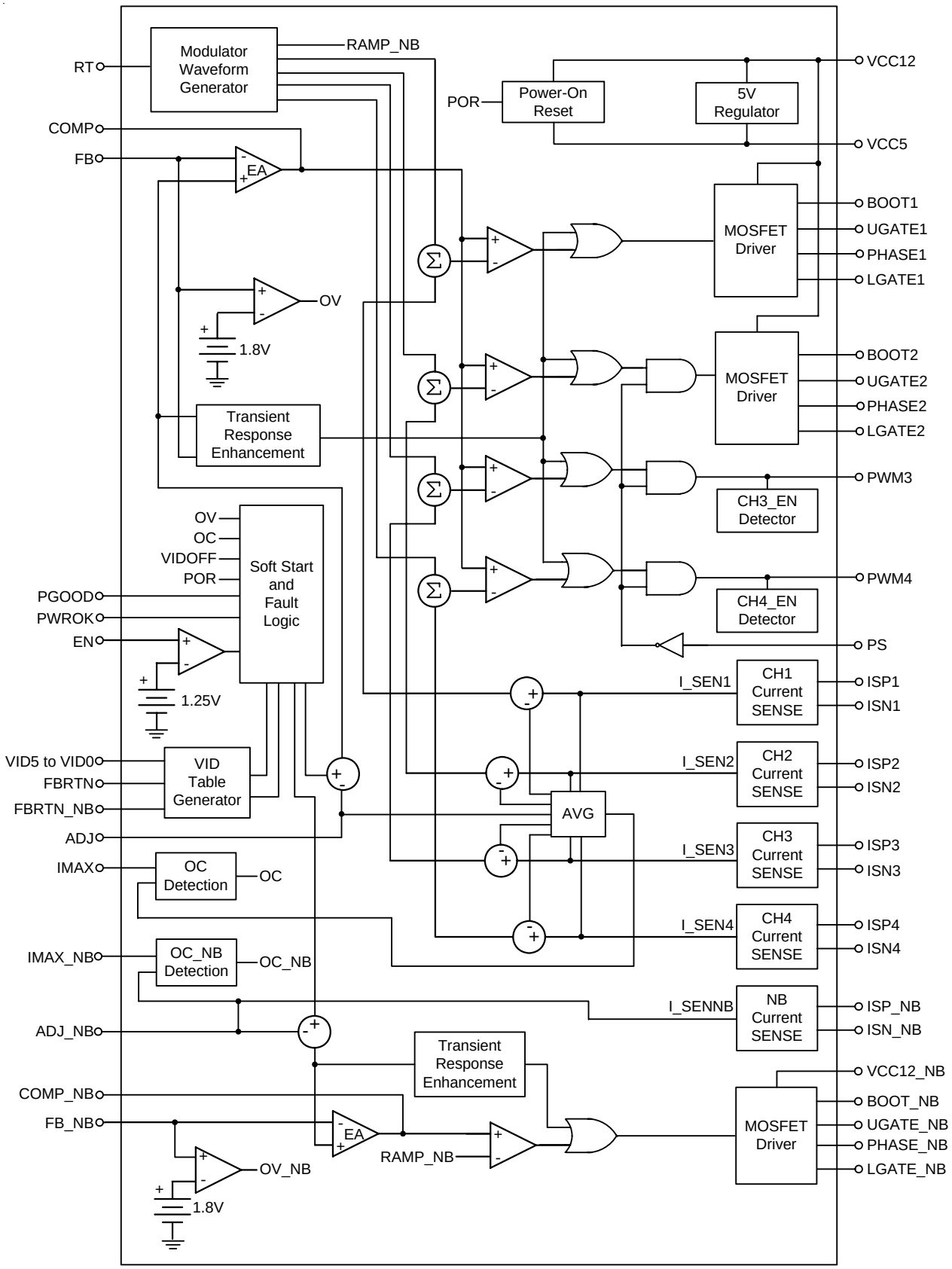
Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 15V
- BOOTx to PHASEx ---------- –0.3V to 15V
- PHASEx to GND
  - DC ---------- –2V to 15V
  - < 20ns ---------- –5V to 30V
- UGATEx to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 20ns ---------- (V_{PHASE} – 5V) to (V_{BOOT} + 5V)
- LGATEx to GND
  - DC ---------- (GND – 0.3V) to (V_{CC} + 0.3V)
  - < 20ns ---------- (GND – 5V) to (V_{CC} + 5V)
- Input/Output Voltage or I/O Voltage ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–48L 7x7 ---------- 3.226W
  - WQFN–48L 6x6 ---------- 2.857W
- Package Thermal Resistance (Note 2)
  - WQFN-48L 7x7, θ_{JA} ---------- 31°C/W
  - WQFN-48L 7x7, θ_{JC} ---------- 6°C/W
  - WQFN-48L 6x6, θ_{JA} ---------- 35°C/W
  - WQFN-48L 6x6, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC12 ---------- 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

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Electrical Characteristics

(V_{VCC12} = 12V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Input							
VCC12 Supply Voltage		V_{VCC12}		10.8	12	13.2	V
VCC12 Supply Current		I_{VCC12}		--	10	--	mA
VCC12_NB Supply Voltage		V_{VCC12_NB}		10.8	12	13.2	V
VCC12_NB Supply Current		I_{VCC12_NB}		--	5	--	mA
VCC5 Power							
VCC5 Supply Voltage		V_{VCC5}	I_{LOAD} = 10mA	4.9	5	5.1	V
VCC5 Output Sourcing		I_{VCC5}		10	--	--	mA
Power On Reset							
VCC12 Rising Threshold		$V_{VCC12TH}$	VCC12 Rising	9.2	9.8	10.2	V
VCC12 Hysteresis		$V_{VCC12HY}$	VCC12 Falling	--	0.9	--	V
Input Threshold							
Enable Input Threshold Voltage	Logic-High	V_{ENHI}	EN Rising	2	--	--	V
	Logic-Low	V_{ENLO}	EN Falling	--	--	0.8	
PWROK Input Threshold Voltage	Logic-High	V_{POKHI}	PWROK Rising	0.7	--	--	V
	Logic-Low	V_{POKLO}	PWROK Falling	0.65	0.7	0.3	
VID5 to VID0 Rising Threshold		$V_{VID5\ to\ 0}$	VID5 to VID0 Rising	--	--	0.75	V
VID5 to VID0 Hysteresis		$V_{VID5\ to\ 0\ HYS}$	VID5 to VID0 Falling	--	50	--	mV
VID5 to VID0 Pull-Down Current		$I_{VID5\ to\ 0}$	$V_{VID5\ to\ 0}$ = 1.5V	--	16	30	µA
Reference Voltage Accuracy							
DAC Accuracy			1V to 1.55V	–0.5	--	0.5	%
			0.8V to 1V	–8	--	8	mV
			0.5V to 0.8V	–10	--	10	
Error Amplifier							
DC Gain		A_{DC}	No Load	--	80	--	dB
Gain-Bandwidth		GBW	C_{LOAD} = 10pF	--	10	--	MHz
Slew Rate		SR	C_{LOAD} = 10pF	10	--	--	V/µs
Output Voltage Range		V_{COMP}	R_{LOAD} = 47kΩ	0.5	--	3.6	V
Power Good							
Over Voltage Threshold		$V_{PGOOD-OV}$	FB Rising	V_{DAC} +210mV	V_{DAC} +240mV	V_{DAC} +270mV	V
Under Voltage Threshold		$V_{PGOOD-UV}$	FB Falling	V_{DAC} –330mV	V_{DAC} –300mV	V_{DAC} –270mV	V
Over Voltage Threshold_NB		$V_{PGOOD-OV\_NB}$	FB_NB Rising	V_{DAC} +210mV	V_{DAC} +240mV	V_{DAC} +270mV	V
Under Voltage Threshold_NB		$V_{PGOOD-UV\_NB}$	FB_NB Falling	V_{DAC} –330mV	V_{DAC} –300mV	V_{DAC} –270mV	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Range	V_{COMP}	R_{LOAD} = 47kΩ	0.5	--	3.6	V
Power Good						
Over Voltage Threshold	$V_{PGOOD-OV}$	FB Rising	V_{DAC} +210mV	V_{DAC} +240mV	V_{DAC} +270mV	V
Under Voltage Threshold	$V_{PGOOD-UV}$	FB Falling	V_{DAC} –330mV	V_{DAC} –300mV	V_{DAC} –270mV	V
Over Voltage Threshold_NB	$V_{PGOOD-OV\_NB}$	FB_NB Rising	V_{DAC} +210mV	V_{DAC} +240mV	V_{DAC} +270mV	V
Under Voltage Threshold_NB	$V_{PGOOD-UV\_NB}$	FB_NB Falling	V_{DAC} –330mV	V_{DAC} –300mV	V_{DAC} –270mV	V
Power Good Low Voltage	V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
Current Sense Amplifier						
Max Current	I_{GMMAX}	V_{CSP} = 1.3V Sink Current from CSN	100	--	--	μA
Input Offset Voltage	V_{OSCS}		–2	0	2	mV
Oscillator						
Running Frequency	f_{OSC}	R_{RT} = 40kΩ	270	300	330	kHz
Ramp Amplitude	V_{RAMP}		--	1.6	--	V
Soft-Start						
Soft-Start Slew Rate	SR_{SS}	Slew Rate	2.5	3.25	4	mV/μs
VID change Slew Rate	SR_{VID}	Slew Rate	2.5	3.25	4	mV/μs
Protection						
Over Voltage Threshold	V_{OVP}	Sweep FB Voltage	1.7	1.8	1.9	V
	V_{OVP_NB}	Sweep FB_NB Voltage	1.7	1.8	1.9	
Over Current Threshold	I_{OCP}	R_{IMAX} = 40kΩ	64.5	83	101.5	μA
	V_{IMAX}	R_{IMAX} = 40kΩ	1.44	1.6	1.76	V
	I_{OCP_NB}	R_{IMAX_NB} = 40kΩ	64.5	83	101.5	μA
	V_{IMAX_NB}	R_{IMAX_NB} = 40kΩ	1.44	1.6	1.76	V
Gate Driver						
UGATE Drive Source	$R_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 8V 250mA Source Current	--	1	--	Ω
UGATE Drive Sink	$R_{UGATEsk}$	$V_{BOOT} - V_{PHASE}$ = 8V 250mA Sink Current	--	1	--	Ω
LGATE Drive Source	$R_{LGATEsr}$	V_{LGATE} = 8V	--	1	--	Ω
LGATE Drive Sink	$R_{LGATEsk}$	250mA Sink Current	--	0.9	--	Ω

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Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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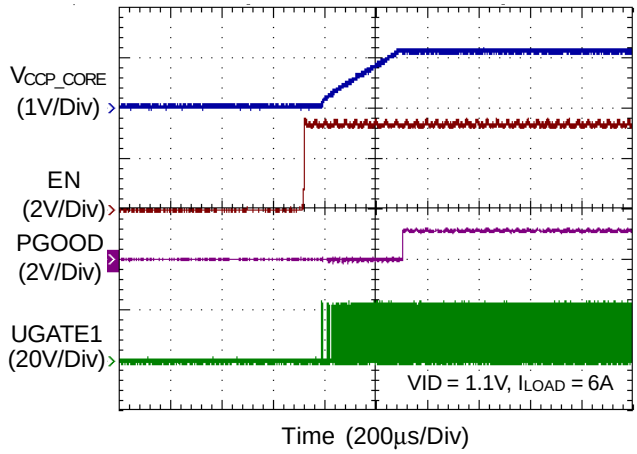
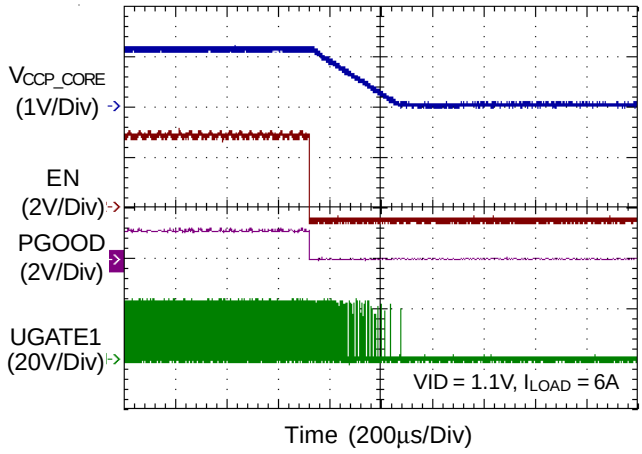
Typical Operating Characteristics

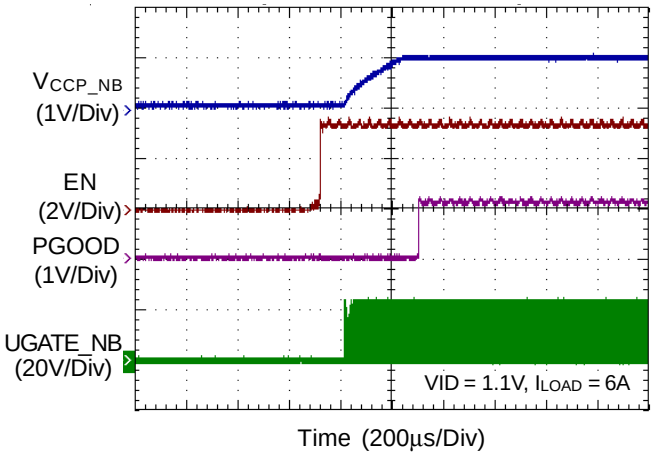
Power On from EN_CORE



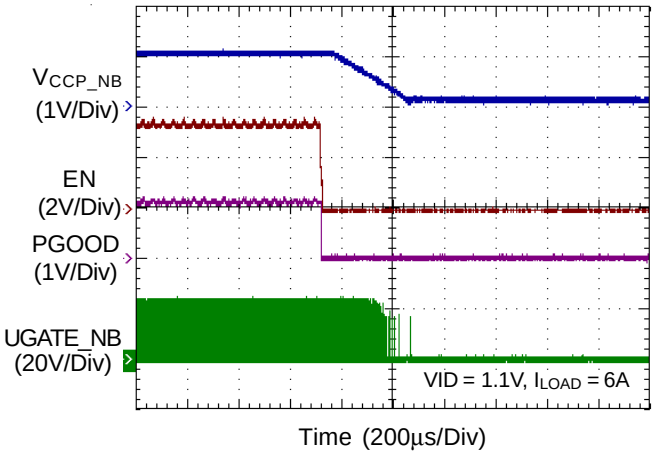
Power Off from EN_CORE



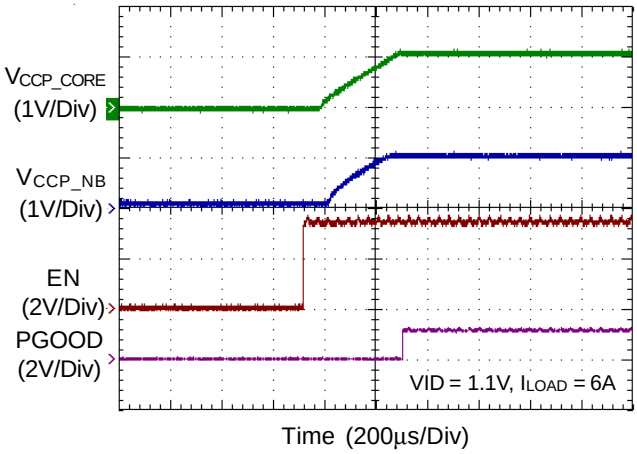
Power On from EN_NB



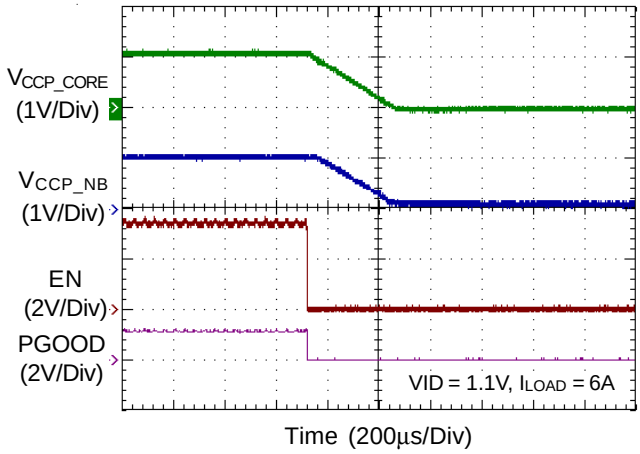
Power Off from EN_NB



Power On from EN_SVI Mode



Power Off from EN_SVI Mode



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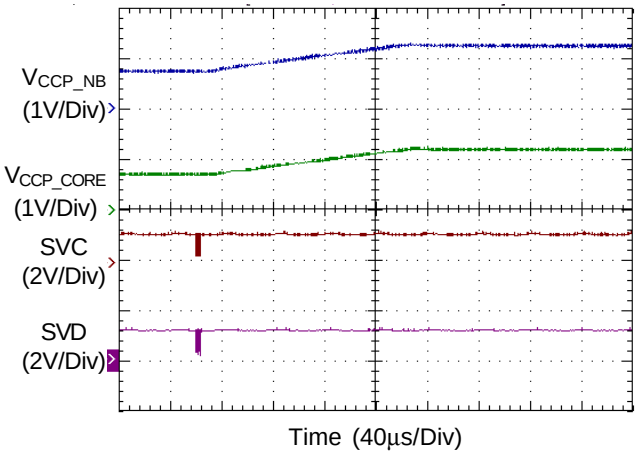
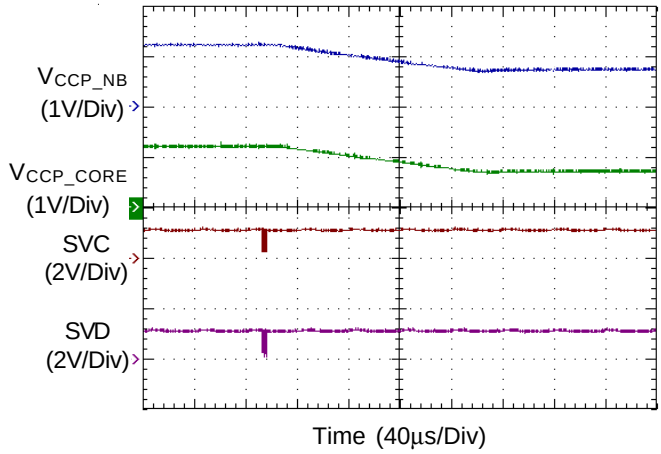
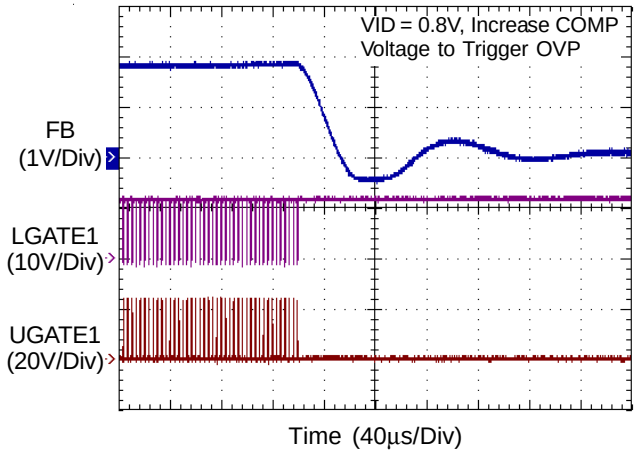
Dynamic VID Up



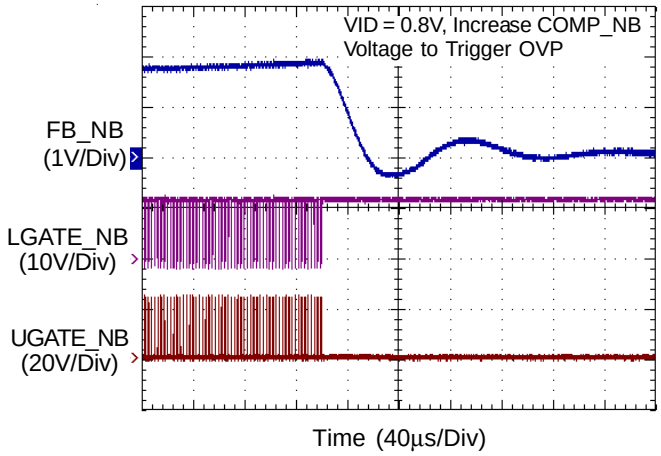
Dynamic VID Down



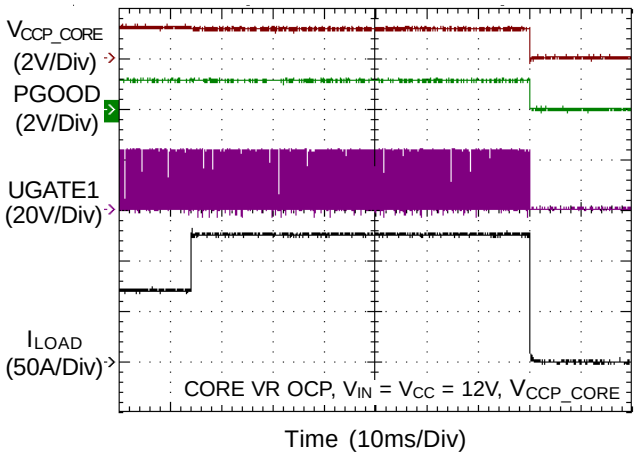
Over Voltage Protection_CORE



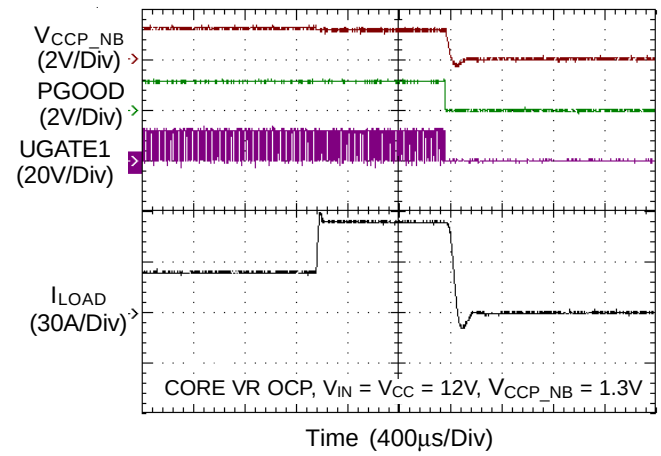
Over Voltage Protection_NB



Over Current Protection_CORE



Over Current Protection_NB



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Application Information

The RT8871A/B is a dual output PWM controller that supports hybrid power control of AMD processors which operate from either a 6-bit Parallel VID Interface (PVI) or a Serial VID Interface (SVI). One of the outputs is a 4/3/2-phase PWM controller with two integrated MOSFET drivers to support CPU core voltage (VDD) and another is a single-phase buck controller with an integrated MOSFET driver to power North-Bridge (NB) chipset (VDDNB) in SVI mode. In PVI mode, only multiphase PWM controller is active for single plane VDD only processor.

Richtek's proprietary Burst Transient Response(BTR™) provides fast initial response to high di/dt load transients and requires less bulk and ceramic output capacitance to meet transient regulation specifications. The RT8871A/B incorporates differential voltage sensing, continuous inductor DCR phase current sensing, programmable load-line voltage positioning and offset voltage to provide high accuracy regulated power for both VDD and VDDNB. While VDDNB is enabled in SVI mode, it will be automatically phase-shifted with respect to the CPU Core phases in order to reduce the total input RMS current amount.

CPU_TYPE Detection and System Start-Up

At system start-up, on the rising-edge of EN signal, the RT8871A/B monitors the status of VID1 and latches the PVI mode (VID1 = 1) or SVI mode (VID1 = 0).

PVI Mode

PVI is a 6-bit-wide parallel interface used to address the CPU Core section reference. According to the selected code, the device sets the Core section reference and regulates its output voltage according to Table 2. In this mode, NB section is kept in high impedance. Furthermore, PWROK information is ignored as well since the signal only applies to the SVI protocol.

SVI Mode

SVI is a two wire, Clock and Data, bus that connects a single master (CPU) to one slave (RT8871A/B). The master initiates and terminates SVI transactions and drives the clock, SVC, and the data, SVD, during a transaction. The slave receives the SVI transactions and acts accordingly. SVI wire protocol is based on fast-mode I^2C as shown in Figure 1. SVI interface also considers two additional signals needed to manage the system start-up. These signals are EN and PWROK. The device asserts a PGOOD signal if the output voltages are in regulation.

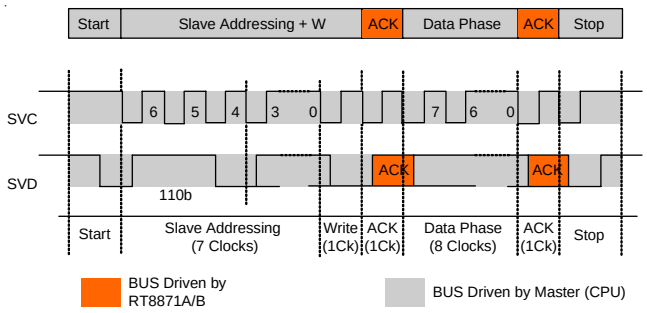

Figure 1. SVI Communication-Send Byte

Set VID Command

The Set VID Command is defined as the command sequence that the CPU issues on the SVI bus to modify the voltage level of the Core section and NB section, as shown is Figure 1. During a Set VID Command, the processor sends the start (Start) sequence followed by the address of the Section which the Set VID Command applies. The processor then sends the write (WRITE) bit. After the write bit, the Voltage Regulator (VR) sends the acknowledge (ACK) bit. The processor then sends the VID bits code during the data phase. The VR sends the acknowledge (ACK) bit after the data phase. Finally, the processor sends the stop (Stop) sequence. After the VR has detected the stop, it performs an On-the-Fly VID transition for the addressed section(s). Refer to Table 3 for the details of SVI send byte.

The RT8871A/B is able to manage individual power off for both VCORE and NB sections. The CPU may issue a serial VID command to power off or power on one section while the other one remains powered. In this case, the PGOOD signal remains asserted.

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Table 3. SVI Send Byte-Address and Data Phase Description / Example

bits	Description
Address Phase	
6 : 4	Always 110b
3	Not Applicable, ignored.
2	Not Applicable, ignored.
1	CORE Section. (Note) If set then the following data byte contains the VID code for CORE Section.
0	NB Section. (Note) If set then the following data byte contains the VID code for NB Section.
Data Phase	
7	PSI_L Flag (Active Low). When asserted, the VR is allowed to enter Power-Saving Mode.
6 : 0	VID Code.

Note : Assertion in both bit 1 and 0 will address the VID code to both CORE and NB simultaneously.

Example :

SVI Address Bits [6 : 0]	Description
1100_000	Should be ignored.
1100_001	Set VID on VDDNB.
1100_110	Set VID on VDD0 and VDD1.
1100_100	Set VID on VDD1.
1100_010	Set VID on VDD0 or VDD (Uniplane).
1100_111	Set VID on VDDNB, VDD0 and VDD1.

PWROK De-assertion

PWROK stays low after EN signal is asserted, and the controller regulates all the planes according to the Pre-PWROK Metal VID.

PGOOD is de-asserted as long as Pre-PWROK Metal VID voltage is out of the initial voltage specifications.

V_FIX Mode Function

Anytime the pin VID0/VFIXEN is pulled high, the controller enters V-FIX mode. When in V_FIX mode, both VCORE and NB section voltages are governed by the information shown in Table 4. Regardless of the state of PWROK, the device will work in SVI mode. SVC and SVD are considered as static VID and the output voltage will be changed according to their status. Dynamic SVC/SVD-change management is provided in this condition. V_FIX mode is intended for system debug only.

Table 4. V_FIX Mode and Pre-PWROK Metal VID

SVC	SVD	Output Voltage (V)	
		Pre-PWROK Metal VID	V_FIX Mode
0	0	1.1V	1.4V
0	1	1.0V	1.2V
1	0	0.9V	1.0V
1	1	0.8V	0.8V

Power Ready Detection

During start-up, the RT8871A/B will detect VCC12, VCC5 and EN signal. Figure 2 shows the power ready detection circuit. When VCC12 > 9.6V and VCC5 > 4.6V, POR (Power On Reset) will go high. POR is the internal signal to indicate all input powers are ready to allow the RT8871A/B and the companioned MOSFET drivers to work properly. When POR = L, the RT8871A/B will turn off both high side and low side MOSFETs.

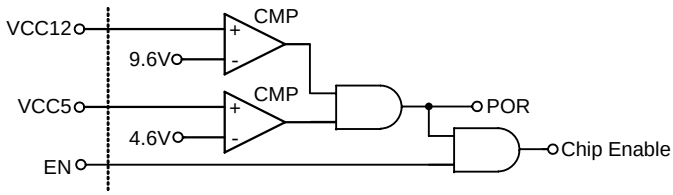

Figure 2. Circuit for Power Ready Detection

Power Up Sequencing

Figure 3 and 4 are the power-up sequencing diagram of the RT8871A/B. Once power_on_reset is valid (POR = H), on the rising edge of the EN signal, the RT8871A/B detects the VID1 pin and determines whether to operate in SVI or PVI mode. Figure3 shows the PVI-mode power sequence, the controller stays in T1 state waiting for valid parallel VID code sent by CPU. After receiving valid parallel VID code, VCORE continues ramping up to the specified voltage according to the VID code in T2 state. Figure 4 shows the SVI-mode power sequence, the controller samples the two serial VID pins, SVC and SVD. Then, the controller stores this value as the boot VID that is the so-called "Pre-PWROK Metal VID" in T1 state. After the processor starts with boot VID voltages, PWROK is asserted and the processor initializes the serial VID interface in T2 state. The processor uses the serial VID interface to issue VID commands to move the power planes from the boot VID values to the dual power planes in T3 state.

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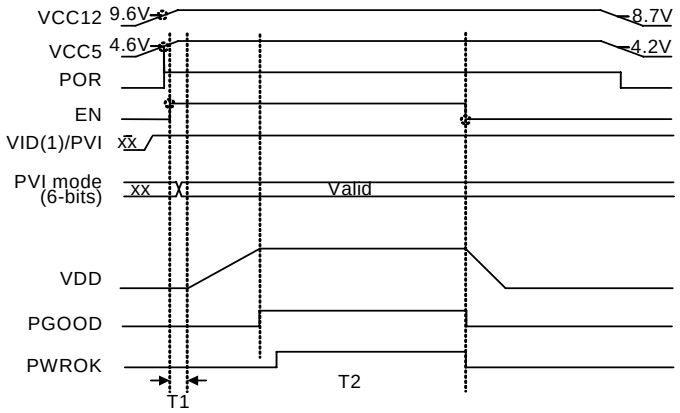

Figure 3. PVI-Mode Power Sequencing Diagram

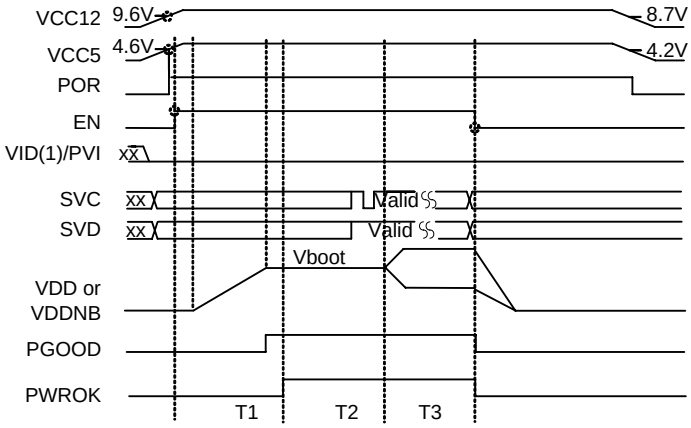

Figure 4. SVI-Mode Power Sequencing Diagram

CORE Section Output Current Sensing

The RT8871A/B provides a low input offset Current Sense Amplifier (CSA) to monitor the continuous output current of each phase for V_{CORE}. Output current of CSA (I_X[n]) is used for current balance and active voltage position as shown in Figure 5. In this inductor current sensing topology, R_S and C_S must be set according to the equation below :

$$\frac{L}{DCR} = R_S \times C_S$$

Then the output current of CSA will follow the equation below :

$$I_X = \frac{[I_L \times DCR - V_{OFS\text{-}CSA} + 235nA \times (R_{CSP} - R_{CSN})]}{R_{CSN}}$$

235nA is the typical value of the CSA input offset current. $V_{OFS\text{-}CSA}$ is the input offset. Usually, "$V_{OFS\text{-}CSA}$ + 235nA x ($R_{CSP} - R_{CSN}$)" is negligible except at very light load and the equation can be simplified as the equation below :

$$I_X = \frac{I_L \times DCR}{R_{CSN}}$$

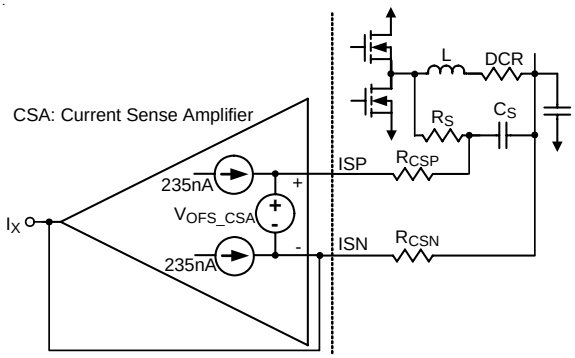

Figure 5. Current Sensing Circuit

CORE Section Phase Detection

The number of the operational phases is determined by the internal circuitry that monitors the ISNx voltages during start up. Normally, the RT8871A/B operates as a 4-phase PWM controller. Pull ISN4 and ISP4 to 5VCC programs 3-phase operation, pull ISN3 and ISP3 to 5VCC programs 2-phase operation. The RT8871A/B detects the voltage of ISN4 and ISN3 at rising edge of POR. At the rising edge, the RT8871A/B detects whether the voltage of ISN4 and ISN3 are higher than "VCC5-1V" respectively to decide how many phases should be active. Phase detection is only active during start up. Once POR = high, the number of operational phases is determined and latched.

CORE Section Switching Frequency

Connecting a resistor (R_{RT}) from the RT pin to GND programs the switching frequency of each phase. Figure 6 shows the relationship between the resistance and switching frequency.

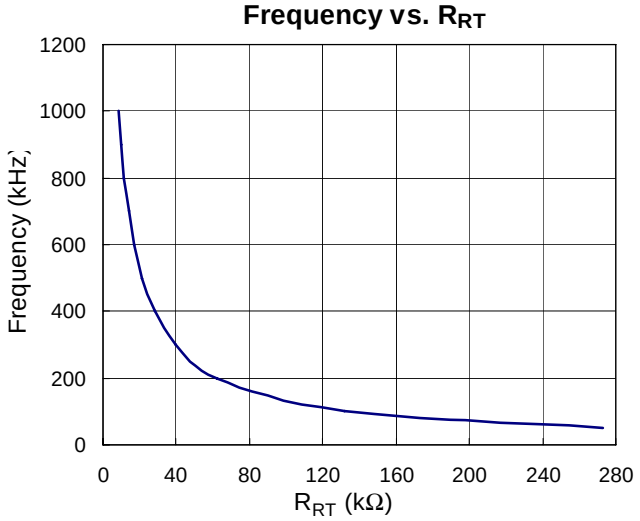

Figure 6. R_{RT} vs. Phase Switching Frequency

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CORE Section Differential Output Voltage Sensing

The RT8871A/B uses differential voltage sensing by a high gain low offset error-amp as shown in Figure 7. Connect the negative on-die CPU remote sense pin to FBRTN. Connect the positive on-die remote sense pin to FB with a resistor (R_{FB}) The error-amp compares EAP (= V_{DAC} – V_{ADJ}) with V_{FB} to regulate the output voltage.

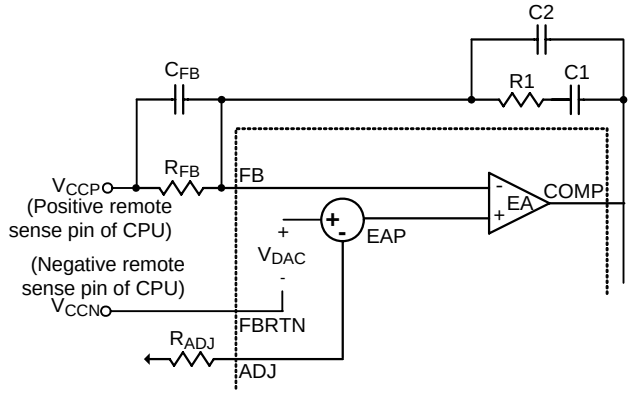

Figure 7. Circuit for VCORE Differential Sensing and No Load Offset

CORE Section Programmable Load-line

Output current of CSA is summed and averaged in the RT8871A/B. Then 0.5Σ (I_X[n]) is sent to ADJ pin. Because Σ I_X[n] is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect ADJ pin to GND. If the NTC resistor is properly selected to compensate the temperature coefficient of I_X[n], the voltage on ADJ pin will be proportional to I_{OUT} without temperature effect. In the RT8871A/B, the positive input of error-amp is "V_{DAC} – V_{ADJ}". V_{OUT} will follow "V_{DAC} – V_{ADJ}", too. Thus, the output voltage which decreases linearly with I_{OUT} is obtained. The loadline is defined as :

$$LL(loadline) = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{\Delta V_{ADJ}}{\Delta I_{OUT}} = \frac{1}{2} \times DCR \times \frac{R_{ADJ}}{R_{CSN}}$$

Briefly, the resistance of R_{ADJ} sets the resistance of loadline. The temperature coefficient of R_{ADJ} compensates the temperature effect of loadline.

CORE Section Load Transient Quick Response

In steady state, the value of V_{FB} is controlled to be very close to V_{EAP}. However, a load step transient from light load to heavy load can still cause V_{FB} to become lower than V_{EAP} by several tens of mV. In prior design, owing to limited control bandwidth, it is difficult for the controller to prevent V_{OUT} undershoot during quick load transient from light load to heavy load. The RT8871A/B has a built-in proprietary Burst Transient Response (BTR™) technology that detects load transient by comparing V_{FB} and V_{EAP}. If V_{FB} suddenly drops below "V_{EAP} – V_{QR}" (V_{QR} is a predetermined voltage), the quick response indicator QR rises up. When QR = high, the RT8871A/B turns on all high side MOSFETs and turns off all low side MOSFETs. The sensitivity of quick response can be adjusted by the values of C_{FB} and R_{FB}. Smaller R_{FB} and/or larger C_{FB} will make QR easier to be triggered. Figure 8 illustrates the circuit and typical waveforms.

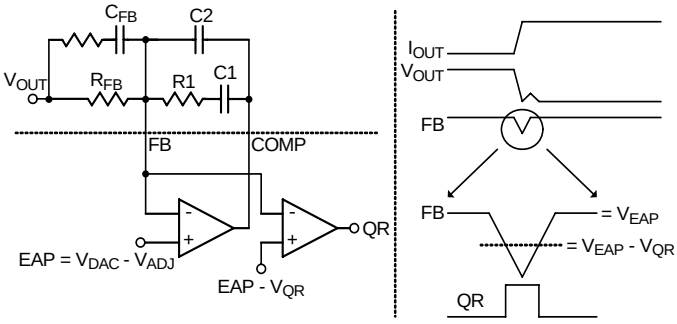

Figure 8. Load Transient Quick Response

CORE Section Current Balance

In Figure 9, I_X[n] is the current signal which is proportional to the current flowing through channel n. The current error signals I_{ERR}[n] (= I_X[n] – AVG(I_X[n])) are used to raise or lower the valley of internal sawtooth waveforms (EAMP[1] to RAMP[n]) which is compared with error-amp output (COMP) to generate PWM signal. Raising the valley of sawtooth waveform will decrease the PWM duty of the corresponding channel, while lowering the sawtooth waveform valley will increase the PWM duty. Eventually, the current flowing through each channel will be balanced.

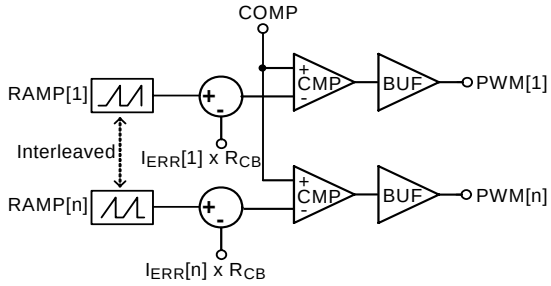

Figure 9. Circuit Channel Current Balance

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CORE Section Phase Current Adjustment

If phase current is not balanced due to asymmetric PCB layout of power stage, external resistors can be adjusted to correct current imbalance. Figure10 shows two types of current imbalance, constant ratio type and constant difference type. If the initial current distribution is constant ratio type, according to Equation (3), reducing $R_{CSN}[1]$ can reduce $I_L[1]$ and improve current balance. If the initial current distribution is constant difference type, according to Equation (2), increasing $R_{CSP}[1]$ can reduce $I_L[1]$ and improve current balance.

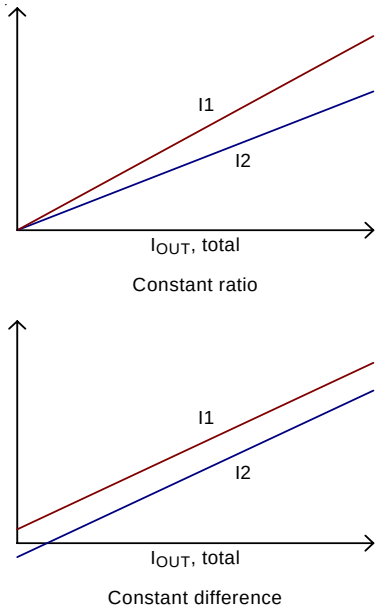

Figure 10. Category of Phase Current Imbalance

CORE Section Over Current Protection (OCP)

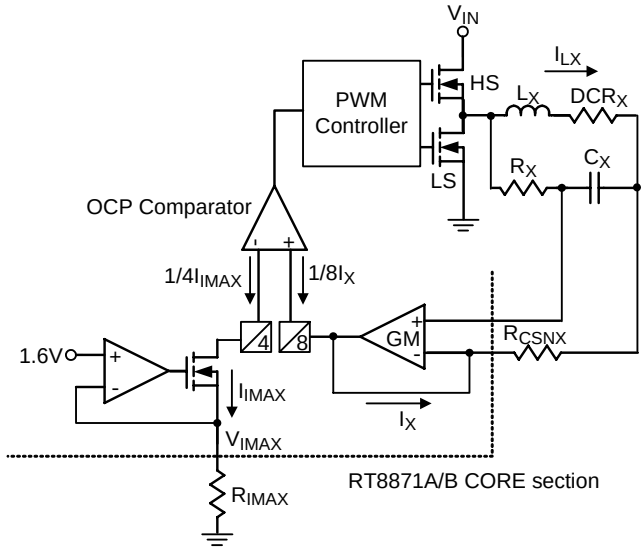

Figure 11. Over Current Protection for CORE Section

CORE Section Over Current Protection (OCP)

The RT8871A/B has dual OCP mechanism. The dual OCP mechanism has two types of thresholds. The first type, referred to as OCP-TDC, is a time and current based threshold. OCP-TDC should trip when the average output current exceeds TDC by some percentage for a period of time. This period of time is referred to as the trigger delay.

The RT8871A/B uses an external resistor R_{IMAX} connected to IMAX pin to generate a reference current I_{MAX} for over current protection as depicted in Figure 11.

$$I_{MAX} = \frac{V_{IMAX}}{R_{IMAX}}$$

where V_{IMAX} is typically 1.6V. The RT8871A/B senses each phase current I_X, and the OCP comparator compares sensed average current with the reference current. Equivalently, the maximum phase average current $I_{LX(MAX)}$ is calculated as below :

$$\frac{1}{4} \times I_{IMAX} = \frac{1}{8} \times I_{X(MAX)}$$

$$I_{X(MAX)} = 2 \times I_{IMAX} = 2 \times \frac{V_{IMAX}}{R_{IMAX}}$$

$$I_{LX(MAX)} = I_{X(MAX)} \times \frac{R_{CSNX}}{DCR_X} = 2 \times \frac{V_{IMAX}}{R_{IMAX}} \times \frac{R_{CSNX}}{DCR_X}$$

Once I_X is larger than 2 x I_{IMAX} and about 50ms trigger delay exceeds, the OCP of CORE section is triggered and latched. Accordingly the RT8871A/B will turn off both high side MOSFET and low side MOSFET of all channels.

The second type, referred to as OCP-Spike, is a current based threshold. OCP-Spike should trip when the cycle-by-cycle output current exceeds IDD-Spike by some percentage. The trigger level of the OCP-Spike is designed 1.5 times of OCP-TDC threshold level. Hence, the equation of short circuit OCP threshold is :

$$I_{LX(MAX),\ spike} = 1.5 \text{ x } I_{LX(MAX)} = 3 \times \frac{V_{IMAX}}{R_{IMAX}} \times \frac{R_{CSNX}}{DCR_X}$$

To prevent false trigger as well, the OCP-Spike still has 20µs trigger delay time. When OCP-Spike is triggered, the RT8871A/B will turn off both high side MOSFET and low side MOSFET of all channels.

CORE Section Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds 1.8V, OVP is triggered and latched for VCORE section. RT8871A/B will try to turn on each low side MOSFET and turn off each high side MOSFET to protect CPU.

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NB Section Output Current Sensing

The RT8871A/B provides low input offset Current Sense Amplifier (CSA) to monitor the continuous output current of NB section. Output current of CSA (I_{X_NB}) is used for over current detection as shown in Figure 12. In this inductor current sensing topology, R_{S_NB} and C_{S_NB} must be set according to the equation below :

$$\frac{L_{NB}}{DCR_{NB}} = R_{S\_NB} \times C_{S\_NB}$$

Then the output current of CSA will follow the equation below :

$$I_{X\_NB} = \frac{I_{L\_NB} \times DCR_{NB}}{R_{CSN\_NB}}$$

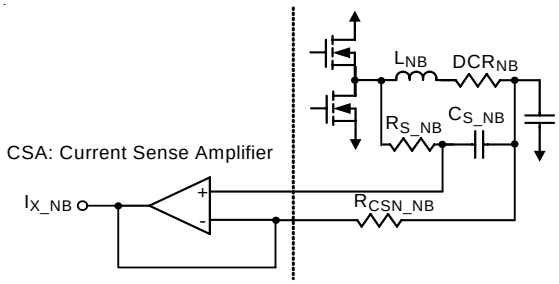

Figure 12. Current Sensing Circuit for NB Section

NB Section Programmable Load Line

Output current of CSA is summed and averaged in the RT8871A/B. Then, 0.5Σ (I x [n]) is sent to ADJ_NB pin. BecauseΣI x [n] is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect ADJ_NB pin to GND. If the NTC resistor is properly selected to compensate the temperature coefficient of IX[n], the voltage on ADJ_NB pin will be proportional to IOUT without temperature effect. In the RT8871A/B, the positive input of error-amp is "VDAC – V_{ADJ_NB}". VOUT will follow "$V_{DAC} - V_{ADJ\_NB}$" too. Thus, the output voltage which decreases linearly with I_{OUT} is obtained. The load line is defined as :

LL (Loadline)

$$= \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{\Delta V_{ADJ\_NB}}{\Delta I_{OUT}} = \frac{1}{2} \text{ x DCR x } \frac{R_{ADJ\_NB}}{R_{CSN\_NB}}$$

The resistor, R_{ADJ_NB}, sets the resistance of the load line. The temperature coefficient of R_{ADJ_NB} compensates the temperature effect of the load line.

NB Section Over Current Protection (OCP)

For NB section, the RT8871A/B has dual OCP mechanism as well. The RT8877A/B uses an external resistor R_{IMAX_NB} connected to IMAX_NB pin to generate a reference current I_{MAX_NB} for over current protection as depicted in Figure 13.

$$I_{MAX\_NB} = \frac{V_{IMAX\_NB}}{R_{IMAX\_NB}}$$

where V_{IMAX_NB} is typically 1.6V. The RT8871A/B senses each phase current I_{X_NB}, and the OCP comparator compares sensed average current with the reference current. Equivalently, the maximum phase average current $I_{LX\_NB(MAX)}$ is calculated as below :

$$\frac{1}{4} \times I_{IMAX\_NB} = \frac{1}{8} \times I_{X\_NB}$$

$$I_{X\_NB} = 2 \times I_{IMAX\_NB} = 2 \times \frac{V_{IMAX\_NB}}{R_{IMAX\_NB}}$$

$$I_{LX\_NB(MAX)} = I_{X\_NB} \times \frac{R_{CSN\_NB}}{DCR_{NB}}$$

$$= 2 \times \frac{V_{IMAX\_NB}}{R_{IMAX\_NB}} \times \frac{R_{CSN\_NB}}{DCR_{NB}}$$

Once I_{X_NB} is larger than 2 x I_{IMAX_NB} and about 1ms trigger delay exceeds, the OCP of NB sections is triggered and latched. Accordingly the RT8871A/B will turn off both high side MOSFET and low side MOSFET of all channels.

The second type, referred to as OCP-Spike, is a current based threshold. OCP-Spike should trip when the cycle-by-cycle output current exceeds IDD-Spike by some percentage. The trigger level of the OCP-Spike is designed 1.5 times of OCP-TDC threshold level. Hence, the equation of short circuit OCP threshold is :

$$I_{LX\_NB(MAX),\ spike} = 1.5 \text{ x } I_{LX\_NB(MAX)}$$

$$= 3 \times \frac{V_{IMAX\_NB}}{R_{IMAX\_NB}} \times \frac{R_{CSN\_NB}}{DCR_{NB}}$$

To prevent false trigger as well, the OCP-Spike of NB section still has 20μs trigger delay time. When OCP-Spike is triggered, the RT8871A/B will turn off both high side MOSFET and low side MOSFET of all channels.

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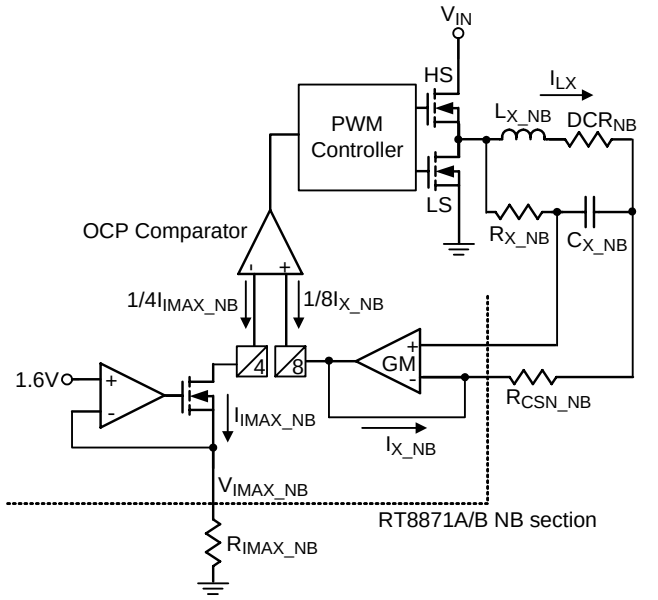

Figure 13. Over Current Protection for NB Section

NB Section Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB_NB pin. Once V_{FB_NB} exceeds 1.8V, OVP is triggered and latched for NB section. The RT8871A/B will try to turn on low side MOSFET and turn off high side MOSFET to protect NB.

Power Saving Indicator (PSI)

This is an active low flag that can be set by the CPU to allow the regulator to enter Power-Saving mode to maximize the system efficiency when in light-load conditions. The status of the flag is communicated to the controller through either the SVI bus or PS pin. The RT8871A/B monitors the PS pin to define the action performed by the controller when PSI is asserted.

According to Figure 14, by programming different voltage on PS pin, this configures the controller to operate in one or two-phase condition when PSI is asserted. By pulling up PS pin to 3.3V through a resistor, the controller operates in only one-phase configuration. If the 3.3V is changed to 5V, the RT8871A/B operates in two-phase configuration. When PSI is de-asserted, the controller will return to the original configuration. The PSI strategy is summarized as shown in Table 5.

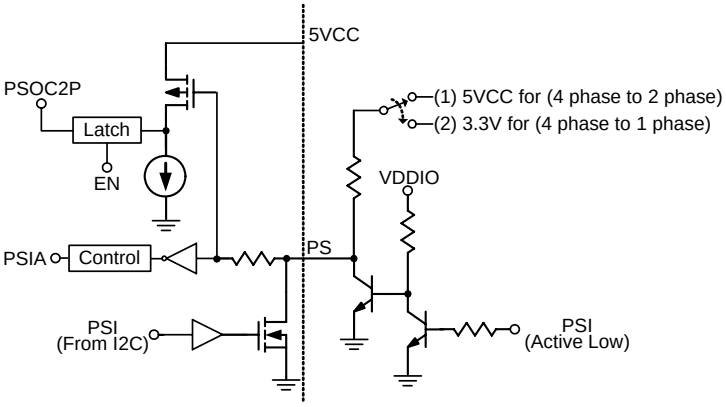

Figure 14. Power-Saving-Mode Circuit

Table 5. PSI Strategy

PS pin	PSI Strategy
Pull-Up to 3.3V	Phase number is set to 1 while PSI is asserted.
Pull-Up to 5V	Phase number is set to 2 while PSI is asserted.

Non-overlap Control of MOSFET Driver

To prevent the overlap of the gate drives during the UGATE pull low and the LGATE pull high, the non-overlap circuit monitors the voltages at the PHASE node and high side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low (after propagation delay). Before LGATE can pull high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.1V. Once the monitored voltages fall below 1.1V, LGATE begins to turn high. By waiting for the voltages of the PHASE pin and high side gate drive to fall below 1.1V, the non-overlap protection circuit ensures that UGATE is low before LGATE pulls high.

Also to prevent the overlap of the gate drives during LGATE pull low and UGATE pull high, the non-overlap circuit monitors the LGATE voltage. When LGATE go below 1.1V, UGATE goes high after propagation delay.

Layout Considerations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The high power switching power stage requires particular attention. Follow these guidelines for optimum PCB layout.

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Place the power components first, including power MOSFETs, input and output capacitors, and inductors. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each. Symmetrical layout allows heat to be dissipated equally across all power trains. Great attention should be paid for routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs with short, high current pulses. It is important to size them as large and short as possible to reduce their overall impedance and inductance. Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot through.

When placing the MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close to each other as possible. Input bulk capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs.

Locate the output inductors and output capacitors between the MOSFETs and the load. Route high-speed switching nodes away from sensitive analog areas (ISP, ISN, FB, FBRTN, COMP, ADJ, OFS, IMAX.....)

Keep the routing of the bootstrap capacitor short between BOOT and PHASE.

Place the snubber R&C as close as possible to the lower MOSFETs of each phase.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-48L 7x7 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WQFN-48L 6x6 package, the thermal resistance, θ_{JA}, is 35°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.226W for WQFN-48L 7x7 package

$P_{D(MAX)}$ = (125°C – 25°C) / (35°C/W) = 2.857W for WQFN-48L 6x6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 15 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

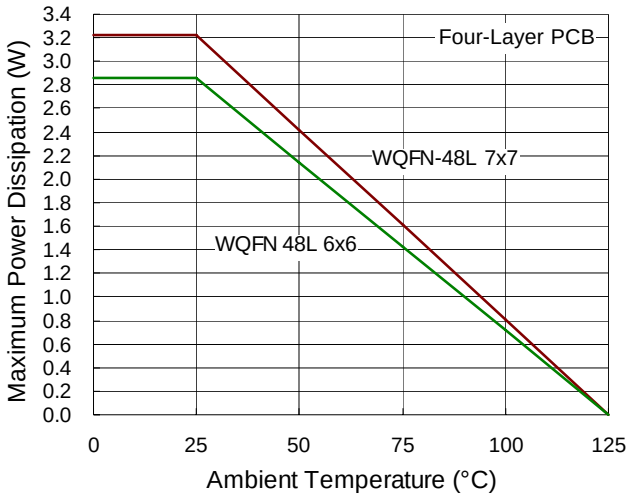

Figure 15.Derating Curve of Maximum Power Dissipation

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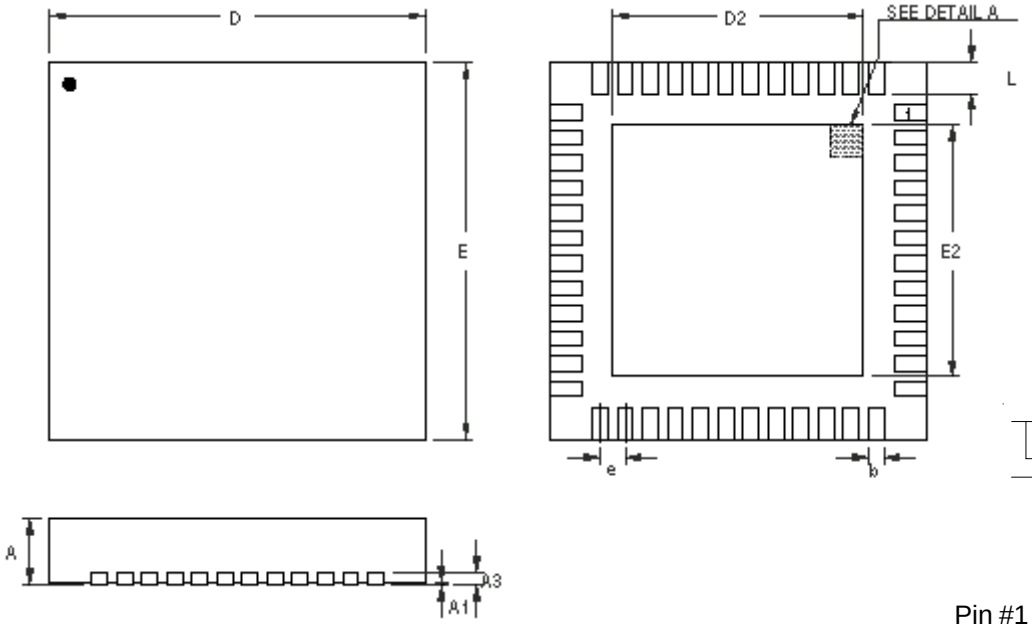
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	6.950	7.050	0.274	0.278
D2	5.050	5.250	0.199	0.207
E	6.950	7.050	0.274	0.278
E2	5.050	5.250	0.199	0.207
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 48L QFN 7x7 Package

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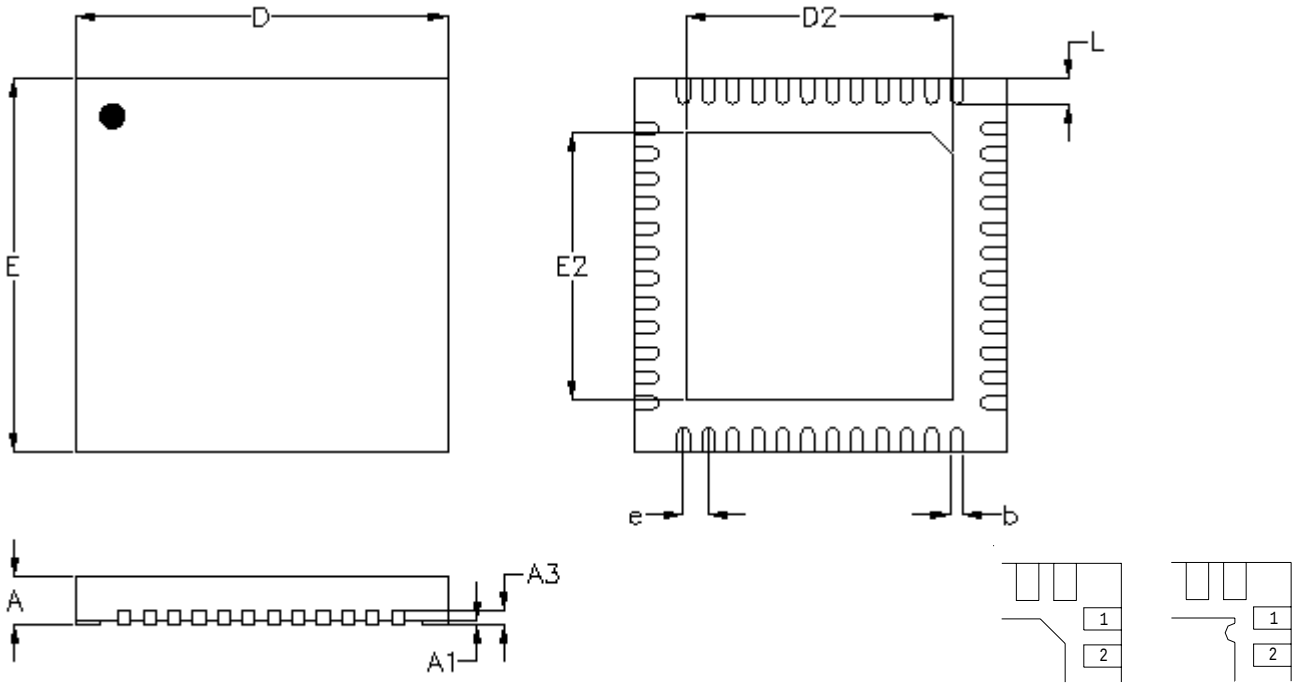

DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		5.950	6.050	0.234	0.238
D2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
E		5.950	6.050	0.234	0.238
E2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
e		0.400		0.016	
L		0.350	0.450	0.014	0.018

W-Type 48L QFN 6x6 Package

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Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

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