Dual Output 3-Phase + 2-Phase PWM Controller For CPU and GPU Core Power Supply

General Description

The RT8885A is a dual output 3-phase + 2-phase PWM controller with 3 integrated MOSFET gate drivers and a single SVID interface for CPU and GPU core power supply. This part complies with Intel VR12/IMVP7 Pulse Width Modulation Specification. The RT8885A adopts G-NAVP™ (Green-Native AVP), which is a Richtek proprietary topology derived from finite DC gain compensator in constant on-time control mode. G-NAVP™ makes this part an easy-setting PWM controller to meet all Intel mobile CPU/GPU AVP (Active Voltage Positioning) requirements. The RT8885A uses SVID interface to control an internal 8-bit DAC for output voltage programming. The built-in high accuracy DAC converts the VID code to a reference voltage ranging from 0V to 1.52V with 5mV step voltage. The system accuracy of the controller reaches 0.8%. Each output channel of the RT8885A can operate in multi-phase continuous conduction mode or in single-phase diode emulation mode to reach a maximum of 90% efficiency in different load conditions. The droop function (load line) is selectable and the load line is easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient response can achieve optimized AVP performance. The output voltage transition slew rate is programmed via the SVID interface. The RT8885A supports inductor DCR and sense-resistor current sensing. This device provides power good indication, current monitor, thermal monitor and thermal throttling output signals for IMVP7 CPU and GPU core. This part also provides complete fault protection functions including over voltage, under voltage, negative voltage, over current, thermal shutdown and under voltage lockout.

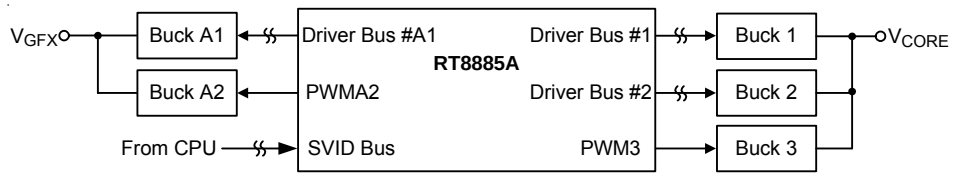
Features

- **Dual Output : 3-Phase (CORE) + 2-Phase (GFX)**
- **Integrated MOSFET Drivers : 2 (CORE) + 1 (GFX)**
- **VR12/IMVP7 PWM Specification Compliant**
- **Serial VID Interface**
- **G-NAVP™ Topology**
- **Fast Line/Load Transient Response**
- **Quick Response for Load Transient**
- **0.5% DAC Accuracy**
- **0.8% System Accuracy**
- **Accurate Current Balance**
- **Selectable Droop Function**
- **Selectable Forced DEM Operation**
- **Built-in ADC for Platform Programming**
- **Power Good Indicator**
- **Current Monitor Output**
- **Thermal Monitor**
- **Thermal Throttling Indicator $\overline{\text{VRHOT}}$**
- **Phase Shedding in PS1**
- **Phase Shedding and Diode Emulation in PS2**
- **Differential Remote Output Voltage Sense**
- **Lossless Inductor DCR Current Sense**
- **Switching Frequency up to 1MHz per Phase**
- **OVP, UVP, NVP, OCP, OTP, UVLO**
- **56-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- IMVP7 Intel CPU/CPU Core Power Supply
- Laptop Computer
- AVP Step-Down Converter

Simplified Application Circuit



Ordering Information

RT8885A □□

- Package Type
  QW : WQFN-56L 7x7 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

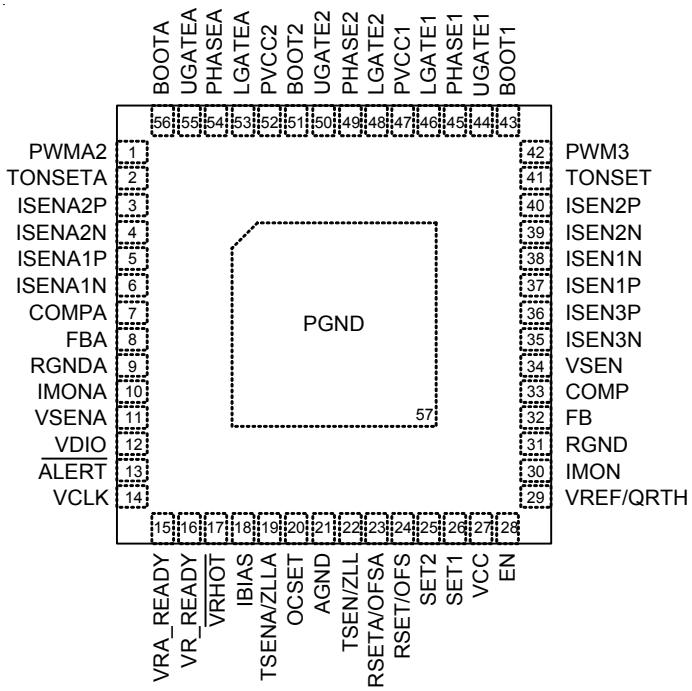
Marking Information

RT8885AZQW : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-56L 7x7

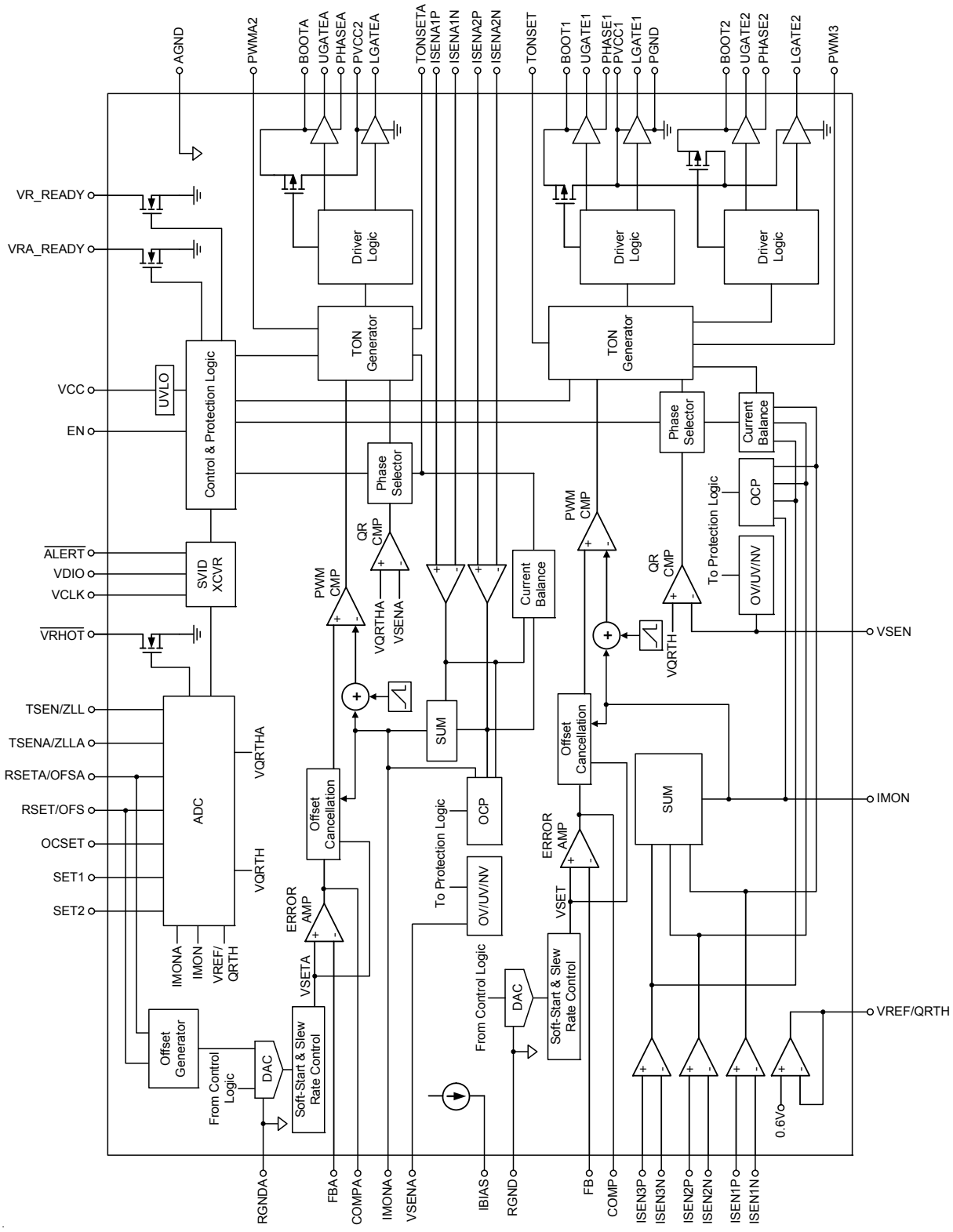
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PWMA2	GFX VR Channel 2 PWM Signal Output. Connect this pin to the PWM input of external MOSFET driver for channel 2 of GFX VR.
2	TONSETA	GFX VR PWM On-Time Setting Pin. Connect this pin to input voltage VIN via a resistor to set the ripple size of GFX VR output in CCM.
3, 5	ISENA[2:1]P	Positive Current Sense Input for Channel 2 and Channel 1 of GFX VR.
4, 6	ISENA[2:1]N	Negative Current Sense Input Pin for Channel 2 and Channel 1 of GFX VR. ISENA2N can be pulled high to VCC to disable GFX VR channel 2. Connect to this pin with a sense resistor of 680Ω.
7	COMPA	GFX VR Compensation Pin. This pin is the output of the error amplifier.
8	FBA	GFX VR Output Voltage Feedback Pin. Connect this pin to the CPU voltage remote sense pin with a resistor. This pin is the inverting input node of the error amplifier.
9	RGNDA	Return Ground for GFX VR. This pin is the inverting input node for differential remote voltage sensing.
10	IMONA	GFX VR Current Monitor Output. Connect a thermally compensated resistor network from this pin to VREF/QRTH pin. IMONA pin output voltage V_{IMONA} is proportional to the total output current of GFX VR.
11	VSENA	GFX VR Output Voltage Sensing Pin. Voltage on this pin is monitored for voltage-related protections.
12	VDIO	Data Transmission Line of SVID Interface. This pin has an open drain structure. Pull high this pin to platform VCCIO rail with a resistor placed close to controller.
13	$\overline{\text{ALERT}}$	Alert Line of the SVID Interface (Active Low). This pin has an open drain structure. Pull high this pin to platform VCCIO rail with a resistor placed close to controller.
14	VCLK	Clock Signal Line of SVID Interface. This pin has an open drain structure. Pull high VCLK to platform VCCIO rail with a resistor placed close to controller.
15	VRA_READY	GFX VR Power Good Indicator Output. This pin has an open drain structure. Pull high this pin to platform VCCIO rail with a resistor.
16	VR_READY	CORE VR Power Good Indicator Output. This pin has an open drain structure. Pull high this pin to platform VCCIO rail with a resistor.
17	$\overline{\text{VRHOT}}$	Thermal Throttling Output (Active Low). This pin has an open drain structure. Pull high this pin to platform VCCIO rail with a resistor.
18	IBIAS	Internal Bias Current Setting Pin. Connect this pin to GND only with a 53.6kΩ resistor placed close to the controller.
19	TSENA/ZLLA	This Pin Provides Two Functions for GFX VR : Thermal Monitor Input, and Droop Enable/Disable Setting. Connect a thermally compensated resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin.
20	OCSET	CORE VR and GFX VR Over Current Protection Threshold Setting Pin. Connect a resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin to set summed total over current protection threshold and per phase over current protection threshold for CORE VR and GFX VR individually.
21	AGND	Analog Ground Pin.
22	TSEN/ZLL	This Pin Provides Two Functions for CORE VR : Thermal Monitor Input, and Droop Enable/Disable Setting. Connect a thermally compensated resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin.

Pin No.	Pin Name	Pin Function
23	RSETA/OFSA	This pin provides three settings for GFX VR : internal compensation ramp factor for control loop, output voltage offset and forced-DEM operation. Connect a resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin.
24	RSET/OFS	This pin provides three settings for CORE VR : internal compensation ramp factor for control loop, output voltage offset and forced-DEM operation. Connect a resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin.
25	SET2	This pin provides three settings for GFX VR : initial startup voltage V_{INI_GFX}, maximum output current ICCMAXA and PWM on-time of quick response for load transient response boost. Connect a resistive voltage divider from VCC to GND, and connect the joint of the voltage divider to this pin.
26	SET1	This pin provides three settings for CORE VR : Initial startup voltage V_{INI_CORE}, maximum output current ICCMAX and PWM on-time of quick response for load transient response boost. Connect a resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin.
27	VCC	Controller Power Supply Pin. Connect this pin to GND with a ceramic capacitor larger than 1μF.
28	EN	Voltage Regulator Enable Signal Input.
29	VREF/QRTH	This Pin Provides Two Functions : Fixed 0.6V Reference Voltage Output, and Quick Response Trigger Threshold Setting. Connect a resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin. Bypass this pin to GND with ceramic capacitor for noise decoupling.
30	IMON	CORE VR Current Monitor Output. Connect a thermally compensated resistor network from this pin to VREF/QRTH pin. IMON pin output voltage V_{IMON} is proportional to the total output current of CORE VR.
31	RGND	Return Ground for CORE VR. This pin is the inverting input node for differential remote voltage sensing.
32	FB	CORE VR Feedback Pin. This pin is the inverting input node of the error amplifier.
33	COMP	CORE VR Compensation Pin. This pin is the output of the error amplifier.
34	VSEN	CORE VR output voltage sensing pin. Voltage on this pin is monitored for voltage related protections.
35, 39, 38	ISEN[3:1]N	Negative Current Sense Input Pin for Channel 3, 2 and 1 of CORE VR. ISENA2N and ISENA3N can be pulled high to VCC to disable CORE VR channel 2 and channel 3, respectively. Connect to this pin with a sense resistor of 680Ω.
36, 40, 37	ISEN[3:1]P	Positive current sense input for channel 3, 2 and 1 of CORE VR.
41	TONSET	CORE VR PWM On-Time Setting Pin. Connect this pin to input voltage VIN via a resistor to set the ripple size of CORE VR output in CCM.
42	PWM3	CORE VR Channel 3 PWM Signal Output. Connect this pin to the PWM input of external MOSFET driver for channel 3 of CORE VR.
43	BOOT1	CORE VR Channel 1 Bootstrap Flying Capacitor Connection Pin. This pin powers channel 1 high side MOSFET drivers. Connect this pin to PHASE1 pin with a ceramic capacitor.
44	UGATE1	CORE VR Channel 1 High Side MOSFET Floating Gate Driver Output. Connect this pin to the gate of high side MOSFET of channel 1.

Pin No.	Pin Name	Pin Function
45	PHASE1	CORE VR Channel 1 Switching Node Connection Pin. Connect this pin to the joint of high side MOSFET sources, the low side MOSFET drains and the inductor of channel 1.
46	LGATE1	CORE VR Channel 1 Low Side MOSFET Gate Driver Output. Connect this pin to the gate of low side MOSFET of channel 1.
47	PVCC1	CORE VR Embedded MOSFET Driver Power Supply Pin. This pin powers channel 1 and channel 2 MOSFET gate drivers. Connect this pin to GND with a ceramic capacitor larger than 1μF.
48	LGATE2	CORE VR Channel 2 Low Side MOSFET Gate Driver Output. Connect this pin to the gate of low side MOSFET of channel 2.
49	PHASE2	CORE VR Channel 2 Switching Node Connection Pin. Connect this pin to the joint of high side MOSFET sources, the low side MOSFET drains and the inductor of channel 2.
50	UGATE2	CORE VR Channel 2 High Side MOSFET Floating Gate Driver Output. Connect this pin to the gate of high side MOSFET of channel 2.
51	BOOT2	CORE VR Channel 2 Bootstrap Flying Capacitor Connection Pin. This pin powers channel 2 high side MOSFET drivers. Connect this pin to PHASE2 pin with a ceramic capacitor.
52	PVCC2	GFX VR Embedded MOSFET Driver Power Supply Pin. Connect this pin to GND with a ceramic capacitor larger than 1μF.
53	LGATEA	GFX VR Channel 1 Low Side MOSFET Gate Driver Output. Connect this pin to the gate of low side MOSFET of channel 1.
54	PHASEA	GFX VR Channel 1 Switching Node Connection Pin. Connect this pin to the joint of high side MOSFET sources, the low side MOSFET drains and the inductor of channel 1.
55	UGATEA	GFX VR Channel 1 High Side MOSFET Floating Gate Driver Output. Connect this pin to the gate of high side MOSFET of channel 1.
56	BOOTA	GFX VR Channel 1 Bootstrap Flying Capacitor Connection Pin. This pin powers channel 1 high side MOSFET drivers. Connect this pin to PHASEA pin with a ceramic capacitor.
57 (Exposed Pad)	PGND	Power Ground. The exposed pad is the return ground of all low side MOSFET gate drivers. This exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

The RT8885A adopts G-NAVPTM (Green-Native AVP), which is a Richtek proprietary topology derived from finite DC gain compensator in constant on-time control mode. G-NAVPTM is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in functional block diagram. The HS_FET on-time is determined by CCRCOT on-time generator. Low offset current sense amplifiers are used for current balance, loop control and over current detection.

By increasing the loading current, the current signal is rose to increase the steady state COMP voltage, and then the output voltage is decreased to achieving AVP.

A near-DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller. After EN go high, the internal ADC sense pin setting for VINITAL, ICCMAX, over current protection and internal compensation ramp setting. The internal ADC also sense IMON and TSEN pin voltage for INTEL reporting.

Table 1. VR12/IMVP7 Compliant VID Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage (V)
0	0	0	0	0	0	0	0	0	0	0.000
0	0	0	0	0	0	0	1	0	1	0.250
0	0	0	0	0	0	1	0	0	2	0.255
0	0	0	0	0	0	1	1	0	3	0.260
0	0	0	0	0	1	0	0	0	4	0.265
0	0	0	0	0	1	0	1	0	5	0.270
0	0	0	0	0	1	1	0	0	6	0.275
0	0	0	0	0	1	1	1	0	7	0.280
0	0	0	0	1	0	0	0	0	8	0.285
0	0	0	0	1	0	0	1	0	9	0.290
0	0	0	0	1	0	1	0	0	A	0.295
0	0	0	0	1	0	1	1	0	B	0.300
0	0	0	0	1	1	0	0	0	C	0.305
0	0	0	0	1	1	0	1	0	D	0.310
0	0	0	0	1	1	1	0	0	E	0.315
0	0	0	0	1	1	1	1	0	F	0.320
0	0	0	1	0	0	0	0	1	0	0.325
0	0	0	1	0	0	0	1	1	1	0.330
0	0	0	1	0	0	1	0	1	2	0.335
0	0	0	1	0	0	1	1	1	3	0.340
0	0	0	1	0	1	0	0	1	4	0.345
0	0	0	1	0	1	0	1	1	5	0.350
0	0	0	1	0	1	1	0	1	6	0.355
0	0	0	1	0	1	1	1	1	7	0.360
0	0	0	1	1	0	0	0	1	8	0.365
0	0	0	1	1	0	0	1	1	9	0.370
0	0	0	1	1	0	1	0	1	A	0.375
0	0	0	1	1	0	1	1	1	B	0.380
0	0	0	1	1	1	0	0	1	C	0.385
0	0	0	1	1	1	0	1	1	D	0.390
0	0	0	1	1	1	1	0	1	E	0.395
0	0	0	1	1	1	1	1	1	F	0.400
0	0	1	0	0	0	0	0	2	0	0.405
0	0	1	0	0	0	0	1	2	1	0.410
0	0	1	0	0	0	1	0	2	2	0.415
0	0	1	0	0	0	1	1	2	3	0.420
0	0	1	0	0	1	0	0	2	4	0.425
0	0	1	0	0	1	0	1	2	5	0.430
0	0	1	0	0	1	1	0	2	6	0.435
0	0	1	0	0	1	1	1	2	7	0.440
0	0	1	0	1	0	0	0	2	8	0.445
0	0	1	0	1	0	0	1	2	9	0.450
0	0	1	0	1	0	1	0	2	A	0.455
0	0	1	0	1	0	1	1	2	B	0.460
0	0	1	0	1	1	0	0	2	C	0.465

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage (V)
0	0	1	0	1	1	0	1	2	D	0.470
0	0	1	0	1	1	1	0	2	E	0.475
0	0	1	0	1	1	1	1	2	F	0.480
0	0	1	1	0	0	0	0	3	0	0.485
0	0	1	1	0	0	0	1	3	1	0.490
0	0	1	1	0	0	1	0	3	2	0.495
0	0	1	1	0	0	1	1	3	3	0.500
0	0	1	1	0	1	0	0	3	4	0.505
0	0	1	1	0	1	0	1	3	5	0.510
0	0	1	1	0	1	1	0	3	6	0.515
0	0	1	1	0	1	1	1	3	7	0.520
0	0	1	1	1	0	0	0	3	8	0.525
0	0	1	1	1	0	0	1	3	9	0.530
0	0	1	1	1	0	1	0	3	A	0.535
0	0	1	1	1	0	1	1	3	B	0.540
0	0	1	1	1	1	0	0	3	C	0.545
0	0	1	1	1	1	0	1	3	D	0.550
0	0	1	1	1	1	1	0	3	E	0.555
0	0	1	1	1	1	1	1	3	F	0.560
0	1	0	0	0	0	0	0	4	0	0.565
0	1	0	0	0	0	0	1	4	1	0.570
0	1	0	0	0	0	1	0	4	2	0.575
0	1	0	0	0	0	1	1	4	3	0.580
0	1	0	0	0	1	0	0	4	4	0.585
0	1	0	0	0	1	0	1	4	5	0.590
0	1	0	0	0	1	1	0	4	6	0.595
0	1	0	0	0	1	1	1	4	7	0.600
0	1	0	0	1	0	0	0	4	8	0.605
0	1	0	0	1	0	0	1	4	9	0.610
0	1	0	0	1	0	1	0	4	A	0.615
0	1	0	0	1	0	1	1	4	B	0.620
0	1	0	0	1	1	0	0	4	C	0.625
0	1	0	0	1	1	0	1	4	D	0.630
0	1	0	0	1	1	1	0	4	E	0.635
0	1	0	0	1	1	1	1	4	F	0.640
0	1	0	1	0	0	0	0	5	0	0.645
0	1	0	1	0	0	0	1	5	1	0.650
0	1	0	1	0	0	1	0	5	2	0.655
0	1	0	1	0	0	1	1	5	3	0.660
0	1	0	1	0	1	0	0	5	4	0.665
0	1	0	1	0	1	0	1	5	5	0.670
0	1	0	1	0	1	1	0	5	6	0.675
0	1	0	1	0	1	1	1	5	7	0.680
0	1	0	1	1	0	0	0	5	8	0.685
0	1	0	1	1	0	0	1	5	9	0.690
0	1	0	1	1	0	1	0	5	A	0.695

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage (V)
0	1	0	1	1	0	1	1	5	B	0.700
0	1	0	1	1	1	0	0	5	C	0.705
0	1	0	1	1	1	0	1	5	D	0.710
0	1	0	1	1	1	1	0	5	E	0.715
0	1	0	1	1	1	1	1	5	F	0.720
0	1	1	0	0	0	0	0	6	0	0.725
0	1	1	0	0	0	0	1	6	1	0.730
0	1	1	0	0	0	1	0	6	2	0.735
0	1	1	0	0	0	1	1	6	3	0.740
0	1	1	0	0	1	0	0	6	4	0.745
0	1	1	0	0	1	0	1	6	5	0.750
0	1	1	0	0	1	1	0	6	6	0.755
0	1	1	0	0	1	1	1	6	7	0.760
0	1	1	0	1	0	0	0	6	8	0.765
0	1	1	0	1	0	0	1	6	9	0.770
0	1	1	0	1	0	1	0	6	A	0.775
0	1	1	0	1	0	1	1	6	B	0.780
0	1	1	0	1	1	0	0	6	C	0.785
0	1	1	0	1	1	0	1	6	D	0.790
0	1	1	0	1	1	1	0	6	E	0.795
0	1	1	0	1	1	1	1	6	F	0.800
0	1	1	1	0	0	0	0	7	0	0.805
0	1	1	1	0	0	0	1	7	1	0.810
0	1	1	1	0	0	1	0	7	2	0.815
0	1	1	1	0	0	1	1	7	3	0.820
0	1	1	1	0	1	0	0	7	4	0.825
0	1	1	1	0	1	0	1	7	5	0.830
0	1	1	1	0	1	1	0	7	6	0.835
0	1	1	1	0	1	1	1	7	7	0.840
0	1	1	1	1	0	0	0	7	8	0.845
0	1	1	1	1	0	0	1	7	9	0.850
0	1	1	1	1	0	1	0	7	A	0.855
0	1	1	1	1	0	1	1	7	B	0.860
0	1	1	1	1	1	0	0	7	C	0.865
0	1	1	1	1	1	0	1	7	D	0.870
0	1	1	1	1	1	1	0	7	E	0.875
0	1	1	1	1	1	1	1	7	F	0.880
1	0	0	0	0	0	0	0	8	0	0.885
1	0	0	0	0	0	0	1	8	1	0.890
1	0	0	0	0	0	1	0	8	2	0.895
1	0	0	0	0	0	1	1	8	3	0.900
1	0	0	0	0	1	0	0	8	4	0.905
1	0	0	0	0	1	0	1	8	5	0.910
1	0	0	0	0	1	1	0	8	6	0.915
1	0	0	0	0	1	1	1	8	7	0.920
1	0	0	0	1	0	0	0	8	8	0.925

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage (V)
1	0	0	0	1	0	0	1	8	9	0.930
1	0	0	0	1	0	1	0	8	A	0.935
1	0	0	0	1	0	1	1	8	B	0.940
1	0	0	0	1	1	0	0	8	C	0.945
1	0	0	0	1	1	0	1	8	D	0.950
1	0	0	0	1	1	1	0	8	E	0.955
1	0	0	0	1	1	1	1	8	F	0.960
1	0	0	1	0	0	0	0	9	0	0.965
1	0	0	1	0	0	0	1	9	1	0.970
1	0	0	1	0	0	1	0	9	2	0.975
1	0	0	1	0	0	1	1	9	3	0.980
1	0	0	1	0	1	0	0	9	4	0.985
1	0	0	1	0	1	0	1	9	5	0.990
1	0	0	1	0	1	1	0	9	6	0.995
1	0	0	1	0	1	1	1	9	7	1.000
1	0	0	1	1	0	0	0	9	8	1.005
1	0	0	1	1	0	0	1	9	9	1.010
1	0	0	1	1	0	1	0	9	A	1.015
1	0	0	1	1	0	1	1	9	B	1.020
1	0	0	1	1	1	0	0	9	C	1.025
1	0	0	1	1	1	0	1	9	D	1.030
1	0	0	1	1	1	1	0	9	E	1.035
1	0	0	1	1	1	1	1	9	F	1.040
1	0	1	0	0	0	0	0	A	0	1.045
1	0	1	0	0	0	0	1	A	1	1.050
1	0	1	0	0	0	1	0	A	2	1.055
1	0	1	0	0	0	1	1	A	3	1.060
1	0	1	0	0	1	0	0	A	4	1.065
1	0	1	0	0	1	0	1	A	5	1.070
1	0	1	0	0	1	1	0	A	6	1.075
1	0	1	0	0	1	1	1	A	7	1.080
1	0	1	0	1	0	0	0	A	8	1.085
1	0	1	0	1	0	0	1	A	9	1.090
1	0	1	0	1	0	1	0	A	A	1.095
1	0	1	0	1	0	1	1	A	B	1.100
1	0	1	0	1	1	0	0	A	C	1.105
1	0	1	0	1	1	0	1	A	D	1.110
1	0	1	0	1	1	1	0	A	E	1.115
1	0	1	0	1	1	1	1	A	F	1.120
1	0	1	1	0	0	0	0	B	0	1.125
1	0	1	1	0	0	0	1	B	1	1.130
1	0	1	1	0	0	1	0	B	2	1.135
1	0	1	1	0	0	1	1	B	3	1.140
1	0	1	1	0	1	0	0	B	4	1.145
1	0	1	1	0	1	0	1	B	5	1.150
1	0	1	1	0	1	1	0	B	6	1.155

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage (V)
1	0	1	1	0	1	1	1	B	7	1.160
1	0	1	1	1	0	0	0	B	8	1.165
1	0	1	1	1	0	0	1	B	9	1.170
1	0	1	1	1	0	1	0	B	A	1.175
1	0	1	1	1	0	1	1	B	B	1.180
1	0	1	1	1	1	0	0	B	C	1.185
1	0	1	1	1	1	0	1	B	D	1.190
1	0	1	1	1	1	1	0	B	E	1.195
1	0	1	1	1	1	1	1	B	F	1.200
1	1	0	0	0	0	0	0	C	0	1.205
1	1	0	0	0	0	0	1	C	1	1.210
1	1	0	0	0	0	1	0	C	2	1.215
1	1	0	0	0	0	1	1	C	3	1.220
1	1	0	0	0	1	0	0	C	4	1.225
1	1	0	0	0	1	0	1	C	5	1.230
1	1	0	0	0	1	1	0	C	6	1.235
1	1	0	0	0	1	1	1	C	7	1.240
1	1	0	0	1	0	0	0	C	8	1.245
1	1	0	0	1	0	0	1	C	9	1.250
1	1	0	0	1	0	1	0	C	A	1.255
1	1	0	0	1	0	1	1	C	B	1.260
1	1	0	0	1	1	0	0	C	C	1.265
1	1	0	0	1	1	0	1	C	D	1.270
1	1	0	0	1	1	1	0	C	E	1.275
1	1	0	0	1	1	1	1	C	F	1.280
1	1	0	1	0	0	0	0	D	0	1.285
1	1	0	1	0	0	0	1	D	1	1.290
1	1	0	1	0	0	1	0	D	2	1.295
1	1	0	1	0	0	1	1	D	3	1.300
1	1	0	1	0	1	0	0	D	4	1.305
1	1	0	1	0	1	0	1	D	5	1.310
1	1	0	1	0	1	1	0	D	6	1.315
1	1	0	1	0	1	1	1	D	7	1.320
1	1	0	1	1	0	0	0	D	8	1.325
1	1	0	1	1	0	0	1	D	9	1.330
1	1	0	1	1	0	1	0	D	A	1.335
1	1	0	1	1	0	1	1	D	B	1.340
1	1	0	1	1	1	0	0	D	C	1.345
1	1	0	1	1	1	0	1	D	D	1.350
1	1	0	1	1	1	1	0	D	E	1.355
1	1	0	1	1	1	1	1	D	F	1.360
1	1	1	0	0	0	0	0	E	0	1.365
1	1	1	0	0	0	0	1	E	1	1.370
1	1	1	0	0	0	1	0	E	2	1.375
1	1	1	0	0	0	1	1	E	3	1.380
1	1	1	0	0	1	0	0	E	4	1.385

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage (V)
1	1	1	0	0	1	0	1	E	5	1.390
1	1	1	0	0	1	1	0	E	6	1.395
1	1	1	0	0	1	1	1	E	7	1.400
1	1	1	0	1	0	0	0	E	8	1.405
1	1	1	0	1	0	0	1	E	9	1.410
1	1	1	0	1	0	1	0	E	A	1.415
1	1	1	0	1	0	1	1	E	B	1.420
1	1	1	0	1	1	0	0	E	C	1.425
1	1	1	0	1	1	0	1	E	D	1.430
1	1	1	0	1	1	1	0	E	E	1.435
1	1	1	0	1	1	1	1	E	F	1.440
1	1	1	1	0	0	0	0	F	0	1.445
1	1	1	1	0	0	0	1	F	1	1.450
1	1	1	1	0	0	1	0	F	2	1.455
1	1	1	1	0	0	1	1	F	3	1.460
1	1	1	1	0	1	0	0	F	4	1.465
1	1	1	1	0	1	0	1	F	5	1.470
1	1	1	1	0	1	1	0	F	6	1.475
1	1	1	1	0	1	1	1	F	7	1.480
1	1	1	1	1	0	0	0	F	8	1.485
1	1	1	1	1	0	0	1	F	9	1.490
1	1	1	1	1	0	1	0	F	A	1.495
1	1	1	1	1	0	1	1	F	B	1.500
1	1	1	1	1	1	0	0	F	C	1.505
1	1	1	1	1	1	0	1	F	D	1.510
1	1	1	1	1	1	1	0	F	E	1.515
1	1	1	1	1	1	1	1	F	F	1.520

Table 2. OCSET Pin Setting (Summed/Per Phase OCP) for CORE VR

CORE VR Per Phase Over Current Protection (OCP) Threshold I_{PHOCP} (μA)	CORE VR Total Summed Current OCP (% of I_{CCMAX})	ADC Code PHOC_CTRL [2:0]	OCSET Pin Voltage Before Current Injection V_{OCSET}
10	120	000	52.5
	128		87.5
	136		122.5
	144		157.5
	152		192.5
	160		227.5
	Disable		262.5
15	120	001	332.5
	128		367.5
	136		402.5
	144		437.5
	152		472.5
	160		507.5
	Disable		542.5

CORE VR Per Phase Over Current Protection (OCP) Threshold I_{PHOCP} (μA)	CORE VR Total Summed Current OCP (% of I_{CCMAX})	ADC Code PHOC_CTRL [2:0]	OCSET Pin Voltage Before Current Injection V_{OCSET}
22.5	120	010	612.5
	128		647.5
	136		682.5
	144		717.5
	152		572.5
	160		787.5
	Disable		822.5
33.8	120	011	892.5
	128		927.5
	136		962.5
	144		997.5
	152		1032.5
	160		1067.5
	Disable		1102.5
50.6	120	100	1172.5
	128		1207.5
	136		1242.5
	144		1277.5
	152		1312.5
	160		1347.5
	Disable		1382.5
75.9	120	101	1452.5
	128		1487.5
	136		1522.5
	144		1557.5
	152		1592.5
	160		1627.5
	Disable		1662.5
113.9	120	110	1732.5
	128		1767.5
	136		1802.5
	144		1837.5
	152		1872.5
	160		1907.5
	Disable		1942.5
170.9	120	111	2012.5
	128		2047.5
	136		2082.5
	144		2117.5
	152		2152.5
	160		2187.5
	Disable		2222.5

Table 2. OCSET Pin Setting (Summed/Per Phase OCP) for GFX VR

GFX VR Per Phase Over Current Protection (OCP) Threshold I_{PHOCPA} (μA)	GFX VR Total Summed Current OCP (% of I_{CCMAXA})	ADC Code PHOC_CTRL [2:0]	OCSET Pin Voltage Difference ΔV_{OCSET} (Before and After Current Injection) (mV)
170.9	120	111	52.5
	128		87.5
	136		122.5
	144		157.5
	152		192.5
	160		227.5
	Disable		262.5
113.9	120	110	332.5
	128		367.5
	136		402.5
	144		437.5
	152		472.5
	160		507.5
	Disable		542.5
75.9	120	101	612.5
	128		647.5
	136		682.5
	144		717.5
	152		572.5
	160		787.5
	Disable		822.5
50.6	120	100	892.5
	128		927.5
	136		962.5
	144		997.5
	152		1032.5
	160		1067.5
	Disable		1102.5
33.8	120	011	1172.5
	128		1207.5
	136		1242.5
	144		1277.5
	152		1312.5
	160		1347.5
	Disable		1382.5
22.5	120	010	1452.5
	128		1487.5
	136		1522.5
	144		1557.5
	152		1592.5
	160		1627.5
	Disable		1662.5

GFX VR Per Phase Over Current Protection (OCP) Threshold I_{PHOCPA} (μA)	GFX VR Total Summed Current OCP (% of I_{CCMAXA})	ADC Code PHOC_CTRL [2:0]	OCSET Pin Voltage Difference ΔV_{OCSET} (Before and After Current Injection) (mV)
15	120	001	1732.5
	128		1767.5
	136		1802.5
	144		1837.5
	152		1872.5
	160		1907.5
	Disable		1942.5
10	120	000	2012.5
	128		2047.5
	136		2082.5
	144		2117.5
	152		2152.5
	160		2187.5
	Disable		2222.5

Table 3. SET1 Pin Setting (V_{INI_CORE} and I_{CCMAX})

CORE VR Initial Startup Voltage V_{INI_CORE} (V)	Maximum Output Current I_{CCMAX} for 3 Phase Operation (A)	Maximum Output Current I_{CCMAX} for 2/1 Phase Operation* (A)	SET1 Pin Voltage Difference ΔV_{SET1} (Before and After Current Injection) (mV)
0	40	40	52.5
	50	45	87.5
	60	50	122.5
	70	55	157.5
	75	60	192.5
	80	65	227.5
	85	70	262.5
	90	75	297.5
	95	80	332.5
	100	85	367.5
	105	90	402.5
	110	100	437.5
	115	110	472.5
	120	120	507.5
0.9	40	40	612.5
	50	45	647.5
	60	50	682.5
	70	55	717.5
	75	60	752.5
	80	65	787.5
	85	70	822.5
	90	75	857.5
	95	80	892.5
	100	85	927.5
	105	90	962.5
	110	100	997.5
	115	110	1032.5
	120	120	1067.5

CORE VR Initial Startup Voltage V_{INI_CORE} (V)	Maximum Output Current I_{CCMAX} for 3 Phase Operation (A)	Maximum Output Current I_{CCMAX} for 2/1 Phase Operation* (A)	SET1 Pin Voltage Difference ΔV_{SET1} (Before and After Current Injection) (mV)
1	40	40	1172.5
	50	45	1207.5
	60	50	1242.5
	70	55	1277.5
	75	60	1312.5
	80	65	1347.5
	85	70	1382.5
	90	75	1417.5
	95	80	1452.5
	100	85	1487.5
	105	90	1522.5
	110	100	1557.5
	115	110	1592.5
	120	120	1627.5
1.1	40	40	1732.5
	50	45	1767.5
	60	50	1802.5
	70	55	1837.5
	75	60	1872.5
	80	65	1907.5
	85	70	1942.5
	90	75	1977.5
	95	80	2012.5
	100	85	2047.5
	105	90	2082.5
	110	100	2117.5
	115	110	2152.5
	120	120	2187.5
* Pull high ISEN2N or ISEN3N to VCC to disable channel 2 or channel 3.			

Table 4. SET2 Pin Setting (V_{INI_GFX} and I_{CCMAXA})

GFX VR Initial Startup Voltage V_{INI_GFX} (V)	Maximum Output Current I_{CCMAXA} (A)	SET2 Pin Voltage Difference ΔV_{SET2} (Before and After Current Injection) (mV)
0	15	52.5
	20	87.5
	25	122.5
	30	157.5
	35	192.5
	40	227.5
	45	262.5
	50	297.5
	55	332.5
	60	367.5
	65	402.5
	70	437.5
	75	472.5
	80	507.5
0.9	15	612.5
	20	647.5
	25	682.5
	30	717.5
	35	752.5
	40	787.5
	45	822.5
	50	857.5
	55	892.5
	60	927.5
	65	962.5
	70	997.5
	75	1032.5
	80	1067.5
1	15	1172.5
	20	1207.5
	25	1242.5
	30	1277.5
	35	1312.5
	40	1347.5
	45	1382.5
	50	1417.5
	55	1452.5
	60	1487.5
	65	1522.5
	70	1557.5
	75	1592.5
	80	1627.5
1.1	15	1732.5
	20	1767.5
	25	1802.5
	30	1837.5
	35	1872.5
	40	1907.5
	45	1942.5
	50	1977.5
	55	2012.5
	60	2047.5
	65	2082.5
	70	2117.5
	75	2152.5
	80	2187.5

Table 5. RSET/OFS Pin Setting (Forced-DEM Enable and Ramp Factor)

CORE VR Forced-DEM	CORE VR Compensation Ramp Factor	RSET/OFS Pin Voltage Difference ΔV_{RSET} (Before and After Current Injection) (mV)
Disable	1	52.5
	2	87.5
	3	122.5
	4	157.5
	5	192.5
	6	227.5
	7	262.5
	8	297.5
	9	332.5
	10	367.5
	11	402.5
	12	437.5
	13	472.5
	14	507.5
	15	542.5
	16	577.5
	17	612.5
	18	647.5
	19	682.5
	20	717.5
	21	752.5
	22	787.5
	23	822.5
	24	857.5
	25	892.5
	26	927.5
	27	962.5
	28	997.5
	29	1032.5
	30	1067.5

CORE VR Forced-DEM	CORE VR Compensation Ramp Factor	RSET/OFS Pin Voltage Difference ΔV_{RSET} (Before and After Current Injection) (mV)
Enable	1	1172.5
	2	1207.5
	3	1242.5
	4	1277.5
	5	1312.5
	6	1347.5
	7	1382.5
	8	1417.5
	9	1452.5
	10	1487.5
	11	1522.5
	12	1557.5
	13	1592.5
	14	1627.5
	15	1662.5
	16	1697.5
	17	1732.5
	18	1767.5
	19	1802.5
	20	1837.5
	21	1872.5
	22	1907.5
	23	1942.5
	24	1977.5
	25	2012.5
	26	2047.5
	27	2082.5
	28	2117.5
	29	2152.5
	30	2187.5

Table 6. RSETA/OFSA Pin Setting (Forced-DEM Enable and Ramp Factor)

GFX VR Forced-DEM	GFX VR Compensation Ramp Factor	RSETA/OFSA Pin Voltage Difference ΔV_{RSETA} (Before and After Current Injection) (mV)
Disable	1	52.5
	2	87.5
	3	122.5
	4	157.5
	5	192.5
	6	227.5
	7	262.5
	8	297.5
	9	332.5
	10	367.5
	11	402.5
	12	437.5
	13	472.5
	14	507.5
	15	542.5
	16	577.5
	17	612.5
	18	647.5
	19	682.5
	20	717.5
	21	752.5
	22	787.5
	23	822.5
	24	857.5
	25	892.5
	26	927.5
	27	962.5
	28	997.5
	29	1032.5
	30	1067.5

GFX VR Forced-DEM	GFX VR Compensation Ramp Factor	RSETA/OFSA Pin Voltage Difference ΔV_{RSETA} (Before and After Current Injection) (mV)
Enable	1	1172.5
	2	1207.5
	3	1242.5
	4	1277.5
	5	1312.5
	6	1347.5
	7	1382.5
	8	1417.5
	9	1452.5
	10	1487.5
	11	1522.5
	12	1557.5
	13	1592.5
	14	1627.5
	15	1662.5
	16	1697.5
	17	1732.5
	18	1767.5
	19	1802.5
	20	1837.5
	21	1872.5
	22	1907.5
	23	1942.5
	24	1977.5
	25	2012.5
	26	2047.5
	27	2082.5
	28	2117.5
	29	2152.5
	30	2187.5

Table 7. VREF/QRTH Pin Setting (CORE/GFX VR Quick Response Threshold)

VREF/QRTH Pin Voltage $V_{REF/QRTH}$ (mV)	CORE VR Quick Response Threshold (mV)	GFX VR Quick Response Threshold (mV)
17.5	Disable	Disable
52.5		32
87.5		43
122.5		54
157.5		64
192.5		75
227.5		85
262.5		95
297.5	32	Disable
332.5		32
367.5		43
402.5		54
437.5		64
472.5		75
507.5		85
542.5		95
577.5	43	Disable
612.5		32
647.5		43
682.5		54
717.5		64
752.5		75
787.5		85
822.5		95
857.5	54	Disable
892.5		32
927.5		43
962.5		54
997.5		64
1032.5		75
1067.5		85
1102.5		95
1137.5	64	Disable
1172.5		32
1207.5		43
1242.5		54
1277.5		64
1312.5		75
1347.5		85
1382.5		95
1417.5	75	Disable
1452.5		32
1487.5		43
1522.5		54
1557.5		64
1592.5		75
1627.5		85
1662.5		95
1697.5	85	Disable
1732.5		32
1767.5		43
1802.5		54
1837.5		64
1872.5		75
1907.5		85
1942.5		95
1977.5	95	Disable
2012.5		32
2047.5		43
2082.5		54
2117.5		64
2152.5		75
2187.5		85
2222.5		95

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- RGNDx to GND ---------- –0.3V to 0.3V
- TONSETx to GND ---------- –0.3V to 28V
- PVCCx to PGND ---------- –0.3V to 6.5V
- BOOTx to PHASEx ---------- –0.3V to 6.5V
- UGATEx to PHASEx
  - DC ---------- –0.3V to (BOOTx – PHASEx)
  - < 20ns ---------- –5V to 7.5V
- PHASEx to GND
  - DC ---------- –0.3V to 28V
  - < 20ns ---------- –8V to 32V
- LGATEx to GND
  - DC ---------- –0.3V to (PVCCx + 0.3V)
  - < 20ns ---------- –2.5V to 7.5V
- Others ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–56L 7x7 ---------- 3.226W
- Package Thermal Resistance (Note 2)
  - WQFN-56L 7x7, θ_{JA} ---------- 31°C/W
  - WQFN-56L 7x7, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 4.5V to 5.5V
- Battery Input Voltage, V_{IN} ---------- 6V to 24V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = PVCC1 = PVCC2 = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Input						
Supply Current	I_{CC}	V_{EN} = 1.05V, not switching, measure I_{VCC} + I_{PVCCx}	--	12	20	mA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, measure I_{VCC} + I_{PVCCx}	--	--	5	μA
Reference and DAC						
DAC Accuracy	V_{FBx}	1.000V ≤ V_{DAC} ≤ 1.520V, no load, active mode	–0.5	0	0.5	%VID
		0.800V ≤ V_{DAC} < 1.000V	–5	0	5	mV
		0.500V ≤ V_{DAC} < 0.800V	–8	0	8	mV
		0.250V ≤ V_{DAC} < 0.500V	–8	0	8	mV
RGND/RGNDA						
RGND Pin Current	I_{RGNDx}	V_{EN} = 1.05V, not switching	--	--	500	μA
Slew Rate						
Dynamic VID Slew Rate	SR	SetVID_slow	2.5	3.125	3.75	mV/μs
		SetVID_fast	10	12.5	15	
Error Amplifier						
Input Offset	V_{EAOFS}		--	--	2	mV
DC Gain	A_V	R_L = 47kΩ (Note 5)	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF (Note 5)	--	10	--	MHz
Slew Rate	SR	C_{LOAD} = 10pF (Gain = –4, R_{LOAD} = 47kΩ, V_{COMPx} = 0.5V to 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMPx}	R_{LOAD} = 47kΩ	0.3	--	3.6	V
Maximum Source Current	I_{OUTEA_MAX}	V_{COMP} = 2V	--	250	--	μA
Current Sense Amplifier						
Input Offset Voltage	V_{CSOFS}		–0.75	--	0.75	mV
Impedance at Neg. Input	R_{ISENxN}		1	--	--	MΩ
Impedance at Pos. Input	R_{ISENxP}		1	--	--	MΩ
DC Gain CORE VR	A_{I_CORE}		--	10	--	V/V
DC Gain GFX VR	A_{I_GFX}		--	10	--	
Output Current Range	I_{SENxN}	Measure ISENxN/ISENAxN pin	–13	--	100	μA
Current Mirror Gain to IMON	A_{MIRROR}	I_{IMON}/ I_{ISENXN}	--	1	--	A/A
Zero Current Detection						
Zero Current Detection Threshold	V_{ZCD_TH}	V_{ZCD_TH} = GND – V_{PHASEx}	--	5	--	mV
PWM On-Time Setting						
TONSETx Pin Voltage	$V_{TONSETx}$	$I_{TONSETx}$ = 80μA, V_{DAC} = 1.1V	--	1.1	--	V
PWM On-Time	T_{ONx}	$I_{TONSETx}$ = 80μA, V_{DAC} = 1V	--	305	--	ns
TONSETx Input Current Range	$I_{TONSETx}$	V_{DAC} = 1V	25	--	280	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBIAS						
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 53.6kΩ	2.09	2.14	2.19	V
VREF/QRTH						
Reference Voltage Output	V_{REF}		--	0.6	--	V
Output Accuracy		C_{VREF} = 0.1μF, I_{VREF} = 400μA	–2	--	2	%
Sink Current Capability	I_{VREF}	C_{VREF} = 0.1μF	--	400	--	μA
External Compensation Capacitor	C_{VREF}	use MLCC	0.1	--	2.2	μF
Source Current Capability	I_{VREF_Source}	C_{VREF} = 0.1μF	--	100	--	μA
QRTH (Refer to VREF/QRTH Pin Setting table for other settings not listed below)						
CORE VR Quick Response Trigger Threshold Voltage	V_{QRTH}	297.5mV < V_{REF_INI} < 542.5mV V_{REF_INI} comes from voltage divider	--	32	--	mV
		1977.5mV < V_{REF_INI} < 2222.5mV V_{REF_INI} comes from voltage divider	--	95	--	
		V_{REF_INI} < 262.5mV, CORE QR is disabled				
QRATH (Refer to VREF/QRTH Pin Setting table for other settings not listed below)						
GFX VR Quick Response Trigger Threshold Voltage	V_{QRTHA}	V_{REF} = (52.5 + 35 x K) mV, (K = 0, 8, 16, 24, 32, 40, 48, 56).	--	32	--	mV
		V_{REF} = (262.5 + 35 x K) mV, (K = 0, 8, 16, 24, 32, 40, 48, 56).	--	95	--	
		V_{REF} = (17.5 + 35 x K) mV, (K = 0, 8, 16, 24, 32, 40, 48, 56), GFX QR is disabled				
RSET/RSETA (Refer to RSET/RSETA Pin Setting table for other settings not listed below)						
Ramp Factor		V_{RSETx0} = (52.5 + 35 x K) mV, (K = 0, 32) V_{RSETx0} comes from voltage divider	--	1	--	
		V_{RSETx1} = (577.5 + 35 x K) mV, (K = 0, 32) V_{RSETx1} comes from voltage divider	--	16	--	
		V_{RSETx2} = (1067.5 + 35 x K) mV, (K = 0, 32) V_{RSETx2} comes from voltage divider	--	30	--	
Forced-DEM Function						
Forced-DEM Enable Threshold	V_{RSETx_DEM}	V_{RSETx} comes from voltage divider	1172.5	--	2187.5	mV
OFS/OFSA						
Output Offset Accuracy	V_{FBx_OFFSET}	V_{OFSx} = 1.2V, V_{DAC} = 1.000V, measure FBx voltage	0.985	1	1.015	V
		V_{OFSx} = 1.6V, V_{DAC} = 1.000V, measure FBx voltage	1.375	1.4	1.425	
		V_{OFSx} = 1.0V, V_{DAC} = 1.000V, measure FBx voltage	0.775	0.8	0.825	
OFS/OFSA Pin Upper Voltage Clamping Threshold	V_{OFSx_CLAMPH}		--	1.8	--	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
OFS/OFSA Pin Lower Voltage Clamping Threshold	V_{OFSx_CLAMPL}			--	0.9	--	V
Protection							
Under Voltage Lockout Threshold	V_{UVLO}	VCC Falling Edge		4.04	4.24	4.44	V
Under Voltage Lockout Hysteresis	ΔV_{UVLO}			--	100	--	mV
UVLO Delay Time	t_{UVLO_DELAY}	VCC Rising Above UVLO Threshold		--	3	--	μs
Absolute Over Voltage Protection Threshold (without Offset)	V_{OVABS_NOOFS}	With respect to VOUT_MAX, measure VSENx		100	150	200	mV
Absolute Over Voltage Protection Threshold (with Offset)	V_{OVABS_OFS}	With respect to VOUT_MAX, measure VSENx		400	450	500	mV
OVP Delay Time	t_{OVP_DELAY}	VSENx Rising Above Threshold		--	1	--	μs
Under Voltage Protection Threshold (without Offset)	V_{UVP_NOOFS}	Measured at VSEN/VSENA with respect to unloaded output voltage (UOV) 0.8V < UOV < 1.52V		–450	–400	–350	mV
Under Voltage Protection Threshold (with Offset)	V_{UVP_OFS}	Measured at VSEN/VSENA with respect to unloaded output voltage (UOV) 0.8V< UOV <1.52V		–550	–500	–450	mV
Delay of UVP	t_{UVP}	VSENx Falling Below UVP Threshold		--	3	--	μs
Negative Voltage Protection Threshold	V_{NVP}	Measure VSENx after OVP		–100	–50	--	mV
NVP Delay	t_{NV_DELAY}	VSENx falling below threshold after OVP		--	1	--	μs
OCSET Pin							
CORE VR Per Phase Over Current Protection (OCP) Threshold Setting	V_{OCPH0}	PHOC_CTRL [2:0] = [000]	Measure OCSET Pin Voltage	52.5	157.5	262.5	mV
	V_{OCPH1}	PHOC_CTRL [2:0] = [001]		332.5	437.5	542.5	
	V_{OCPH2}	PHOC_CTRL [2:0] = [010]		612.5	717.5	822.5	
	V_{OCPH3}	PHOC_CTRL [2:0] = [011]		892.5	997.5	1102.5	
	V_{OCPH4}	PHOC_CTRL [2:0] = [100]		1172.5	1277.5	1382.5	
	V_{OCPH5}	PHOC_CTRL [2:0] = [101]		1452.5	1557.5	1662.5	
	V_{OCPH6}	PHOC_CTRL [2:0] = [110]		1732.5	1837.5	1942.5	
	V_{OCPH7}	PHOC_CTRL [2:0] = [111]		2012.5	2117.5	2222.5	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CORE VR Per Phase OCP Threshold	I_{PHOCP}	PHOC_CTRL[2:0] = [000]	Measure Current Sense Amplifier Output Current	8.2	10	11.8	µA
		PHOC_CTRL[2:0] = [001]		12.3	15	17.7	
		PHOC_CTRL[2:0] = [010]		18.5	22.5	26.6	
		PHOC_CTRL[2:0] = [011]		27.7	33.8	39.8	
		PHOC_CTRL[2:0] = [100]		41.5	50.6	59.7	
		PHOC_CTRL[2:0] = [101]		62.3	75.9	89.6	
		PHOC_CTRL[2:0] = [110]		93.4	113.9	134.4	
		PHOC_CTRL[2:0] = [111]		140.1	170.9	201.6	
CORE VR per Phase OCP Delay Time	t_{PHOCP_DELAY}			--	1	--	µs
CORE VR Summed Total OCP Threshold Setting	V_{OCAVG0}	I_{AVGOCP} = 120% of ICCMAX	Measure OCSET pin Voltage, PHOC_CTRL [2:0] = [001]	--	332.5	--	mV
	V_{OCAVG1}	I_{AVGOCP} =128% of ICCMAX		--	367.5	--	
	V_{OCAVG2}	I_{AVGOCP} = 136% of ICCMAX		--	402.5	--	
	V_{OCAVG3}	I_{AVGOCP} = 144% of ICCMAX		--	437.5	--	
	V_{OCAVG4}	I_{AVGOCP} = 152% of ICCMAX		--	472.5	--	
	V_{OCAVG5}	I_{AVGOCP} = 160% of ICCMAX		--	507.5	--	
	V_{OCAVG6}	Average total OCP is disabled		--	542.5	--	
Summed Total Over Current Protection Threshold on IMON/IMONA	V_{IMONx_OCP}	I_{AVGOCP} = 120% of ICCMAX	Measure V_{IMONx} with Respect to 0.6V V_{REF}	2.05	2.15	2.25	V
		I_{AVGOCP} = 128% of ICCMAX		2.24	2.29	2.34	
		I_{AVGOCP} = 136% of ICCMAX		2.39	2.44	2.49	
		I_{AVGOCP} = 144% of ICCMAX		2.53	2.58	2.63	
		I_{AVGOCP} = 152% of ICCMAX		2.67	2.72	2.77	
		I_{AVGOCP} = 160% of ICCMAX		2.82	2.87	2.92	
Summed Total OCP Delay Time	t_{AOCP_DELAY}	V_{IMONx} Rising Above Summed OCP Threshold		--	40	--	µs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
GFX VR per Phase Over Current Protection (OCP) Threshold Setting	ΔV_{OCAPH0}	PHOCA_CTRL [2:0] = [000]	Measure OCSET Pin Voltage Difference Before and After 40μA Current Injection	2012.5	2117.5	2222.5	mV
	ΔV_{OCAPH1}	PHOCA_CTRL [2:0] = [001]		1732.5	1837.5	1942.5	
	ΔV_{OCAPH2}	PHOCA_CTRL [2:0] = [010]		1452.5	1557.5	1662.5	
	ΔV_{OCAPH3}	PHOCA_CTRL [2:0] = [011]		1172.5	1277.5	1382.5	
	ΔV_{OCAPH4}	PHOCA_CTRL [2:0] = [100]		892.5	997.5	1102.5	
	ΔV_{OCAPH5}	PHOCA_CTRL [2:0] = [101]		612.5	717.5	822.5	
	ΔV_{OCAPH6}	PHOCA_CTRL [2:0] = [110]		332.5	437.5	542.5	
	ΔV_{OCAPH7}	PHOCA_CTRL [2:0] = [111]		52.5	157.5	262.5	
GFX VR Per Phase OCP Threshold	I_{PHOCPA}	PHOCA_CTRL[2:0] = [000]	Measure Current Sense Amplifier Output Current	8.2	10	11.8	μA
		PHOCA_CTRL[2:0] = [001]		12.3	15	17.7	
		PHOCA_CTRL[2:0] = [010]		18.5	22.5	26.6	
		PHOCA_CTRL[2:0]= [011]		27.7	33.8	39.8	
		PHOCA_CTRL[2:0] = [100]		41.5	50.6	59.7	
		PHOCA_CTRL[2:0] = [101]		62.3	75.9	89.6	
		PHOCA_CTRL[2:0] = [110]		93.4	113.9	134.4	
		PHOCA_CTRL[2:0] = [111]		140.1	170.9	201.6	
Summed Total OCP Threshold Setting for GFX VR	$\Delta V_{OCASUM0}$	$I_{AAVGOCP}$ = 120% of ICCMAXA	Measure OCSET Pin Voltage Difference Before and After 40μA Current Injection, PHOCA_CTRL [2:0] = [001]	–	1732.5	--	mV
	$\Delta V_{OCASUM1}$	$I_{AAVGOCP}$ = 128% of ICCMAXA		–	1767.5	--	
	$\Delta V_{OCASUM2}$	$I_{AAVGOCP}$ = 136% of ICCMAXA		–	1802.5	--	
	$\Delta V_{OCASUM3}$	$I_{AAVGOCP}$ = 144% of ICCMAXA		–	1837.5	--	
	$\Delta V_{OCASUM4}$	$I_{AAVGOCP}$ = 152% of ICCMAXA		–	1872.5	--	
	$\Delta V_{OCASUM5}$	$I_{AAVGOCP}$ = 160% of ICCMAXA		–	1907.5	--	
	$\Delta V_{OCASUM6}$	Average total OCP is disabled		–	1942.5	--	
OCSET Pin Output Injection Current	$I_{INJECTOCSET}$			–	40	--	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Inputs							
EN Input Threshold Voltage	Logic-High	V_{EN_H}	With respect to 1V, 70%	0.7	--	--	V
	Logic-Low	V_{EN_L}	With respect to 1V, 30%	--	--	0.3	
EN Hysteresis		V_{ENHYS}		--	30	--	mV
Leakage Current of EN		I_{LEAK_EN}		–1	--	1	μA
VCLK, VDIO Input DC Threshold Voltage	Logic-High	V_{IH}	With respect to Intel Spec.	0.65	--	--	V
	Logic-Low	V_{IL}	With respect to Intel Spec.	--	--	0.45	
Leakage Current of VCLK, VDIO		I_{LEAK_IN}		–1	--	1	μA
VDIO Low Voltage		V_{VDIO}	I_{VDIO} = 10mA	--	--	0.13	V
$\overline{\text{ALERT}}$							
$\overline{\text{ALERT}}$ Low Voltage		$V_{\overline{ALERT}}$	$I_{\overline{ALERT}}$ = 10mA	--	--	0.13	V
Power Good Indication							
VR_READY/VRA_READY Low Voltage		V_{VRx_READY}	I_{VRx_READY} = 4mA	--	--	0.4	V
VR_READY/VRA_READY Delay Time		$t_{VRx\_READY\_DELAY}$	V_{VSEN} = V_{INI_CORE} to VR_READY goes high V_{VSENA} = V_{INI_GFX} to VRA_READY goes high	70	100	130	μs
Delay Time of SVID Interface Ready		$t_{SVID\_RDY\_DELAY}$	From EN goes high to SVID is ready for receiving command	--	--	2	ms
$\overline{\text{VRHOT}}$							
$\overline{\text{VRHOT}}$ Output Voltage		$V_{\overline{VRHOT}}$	$I_{\overline{VRHOT}}$ = 10mA	--	--	0.13	V
Current Monitor IMON/IMONA							
CORE VR Unloaded Current Monitor Output Voltage		V_{IMON_0A}	With respect to 0.6V V_{REF}, voltage across inductor DCR V_{DCR} = 0V, R_{SENSE} = 680Ω, R_{IMON} = 20.4kΩ	–67.5	0	67.5	mV
GFX VR Unloaded Current Monitor Output Voltage		V_{IMONA_0A}	With respect to 0.6V V_{REF}, voltage across inductor DCR V_{DCR} = 0V, R_{SENSE} = 680Ω, R_{IMON} = 20.4kΩ	–45	0	45	mV
SET1 Pin (Refer to SET1 Pin Setting Table for Other Settings Not Listed Below)							
Initial Startup Voltage for CORE VR							
SET1 Pin Voltage for V_{INI_CORE} Setting		V_{SET1_VINI}	V_{INI_CORE} = 1.1V, V_{SET1} = R_{SET1} x $I_{INJECT1}$	1732	--	2187	mV
			V_{INI_CORE} = 1V, V_{SET1} = R_{SET1} x $I_{INJECT1}$	1172	--	1627	
			V_{INI_CORE} = 0.9V, V_{SET1} = R_{SET1} x $I_{INJECT1}$	612	--	1027	
			V_{INI_CORE} = 0V, V_{SET1} = R_{SET1} x $I_{INJECT1}$	52	--	507	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SET1 Pin Output Injection Current	$I_{INJECT1}$		--	40	--	μA
ICCMAX Setting						
SET1 Pin Voltage for ICCMAX Setting	V_{SET1_ICCMAX}	V_{INI_CORE} = 1.1V, V_{SET1} = R_{SET1} x $I_{INJECT1}$, I_{CCMAX} = 40A	--	1732.5	--	mV
		V_{INI_CORE} = 1.1V, V_{SET1} = R_{SET1} x $I_{INJECT1}$, I_{CCMAX} = 80A	--	1907.5	--	
		V_{INI_CORE} =1 .1V, V_{SET1} = R_{SET1} x $I_{INJECT1}$, I_{CCMAX} = 120A	--	2187.5	--	
Quick Response Setting						
CORE VR Quick Response On-Time	$t_{ON\_QR\_CORE}$	V_{DAC} = 0.75V, V_{SET1} = 0.4V, I_{TONSET} = 80μA	--	305	--	ns
SET2 Pin (Refer to SET2 Pin Setting Table for Other Settings Not Listed Below)						
Initial Startup Voltage for GFX VR						
SET2 Pin Voltage for V_{INI_GFX} Setting	V_{SET2_VINI}	V_{INI_GFX} = 1.1V, V_{SET2} = R_{SET2} x $I_{INJECT2}$	0.0525	--	0.5075	V
		V_{INI_GFX} = 1.0V, V_{SET2} = R_{SET2} x $I_{INJECT2}$	0.6125	--	1.0675	
		V_{INI_GFX}=0.9V, V_{SET2} = R_{SET2} x $I_{INJECT2}$	1.1725	--	1.6275	
		V_{INI_GFX} = 0V, V_{SET2} = R_{SET2} x $I_{INJECT2}$	1.7325	--	2.1875	
SET2 Pin Output Injection Current	$I_{INJECT2}$		--	40	--	μA
ICCMAXA Setting						
SET2 Pin Voltage for ICCMAXA Setting	V_{IMAXA0}	V_{INI_GFX} = 1.1V, V_{SET2} = R_{SET2} x $I_{INJECT2}$, I_{CCMAXA} = 15A	--	1732.5	--	mV
	V_{IMAXA1}	V_{INI_GFX}=1.1V, V_{SET2} = R_{SET2} x $I_{INJECT2}$, I_{CCMAXA} = 50A	--	1977.5	--	
	V_{IMAXA2}	V_{INI_GFX} = 1.1V, V_{SET2} = R_{SET2} x $I_{INJECT2}$, I_{CCMAXA} = 80A	--	2187.5	--	
GFX VR Quick Response On-Time	$t_{ON\_QR\_GFX}$	V_{DAC} = 0.75V, V_{SET2} = 0.4V, $I_{TONSETA}$ = 80μA	--	305	--	ns
Temperature Zone						
TSEN Threshold for Tmp_Zone[7] Transition		100% of TEMP_MAX	1.855	1.8725	1.89	V
TSEN Threshold for Tmp_Zone[6] Transition		97% of TEMP_MAX	1.8	1.8175	1.835	
TSEN Threshold for Tmp_Zone[5] Transition		94% of TEMP_MAX	1.745	1.7625	1.78	
TSEN Threshold for Tmp_Zone[4] Transition		91% of TEMP_MAX	1.69	1.7075	1.725	
TSEN Threshold for Tmp_Zone[3] Transition		88% of TEMP_MAX	1.635	1.6525	1.67	
TSEN Threshold for Tmp_Zone[2] Transition		85% of TEMP_MAX	1.58	1.5975	1.615	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TSEN Threshold for Tmp_Zone[1] Transition		82% of TEMP_MAX	1.525	1.5425	1.56	V
TSEN Threshold for Tmp_Zone[0] Transition		75% of TEMP_MAX	1.47	1.4875	1.505	V
Register Update Period	t_{TSEN}		--	300	--	μs
ADC						
Latency	t_{LAT}		--	--	150	μs
Droop Disable						
Droop Disable Threshold	V_{DRPDIS_L}	Measure TSENx/ZLLx voltage when current injection is on	--	--	3.1	V
	V_{DRPDIS_H}	Measure TSENx/ZLLx voltage when current injection is on	3.8	--	--	
TSEN Pin Injection Current	I_{INJECT_TSEN}		--	40	--	μA
TSEN/TSENA Disable						
TSENx Disable Threshold	$V_{TSENDIS\_L}$	Measure TSENx/ZLLx voltage when current injection is off	--	--	2.5	V
	$V_{TSENDIS\_H}$	Measure TSENx/ZLLx voltage when current injection is off	2.9	--	--	
PWM Output Driving Capability						
PWM3, PWMA2 Source/Sink Resistance	R_{PWM_SRC}		--	20	--	Ω
	R_{PWM_SNK}		--	10	--	
MOSFET Gate Driver						
Upper Driver Source	$R_{UGATEsr}$	$V_{BOOTx} - V_{PHASEx} = 5V$, $V_{BOOTx} - V_{UGATEx} = 1V$	--	1	--	Ω
Upper Driver Sink	$R_{UGATEsk}$	$V_{UGATE} = 1V$	--	1	--	
Lower Driver Source	$R_{LGATEsr}$	$V_{PVCCx} = 5V$, $V_{PVCCx} - V_{LGATEx} = 1V$	--	1	--	
Lower Driver Sink	$R_{LGATEsk}$	$V_{LGATEx} = 1V$	--	0.5	--	
Internal Boost Charging Switch On-Resistance	R_{BOOT}	PVCCx to BOOTx	--	30	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

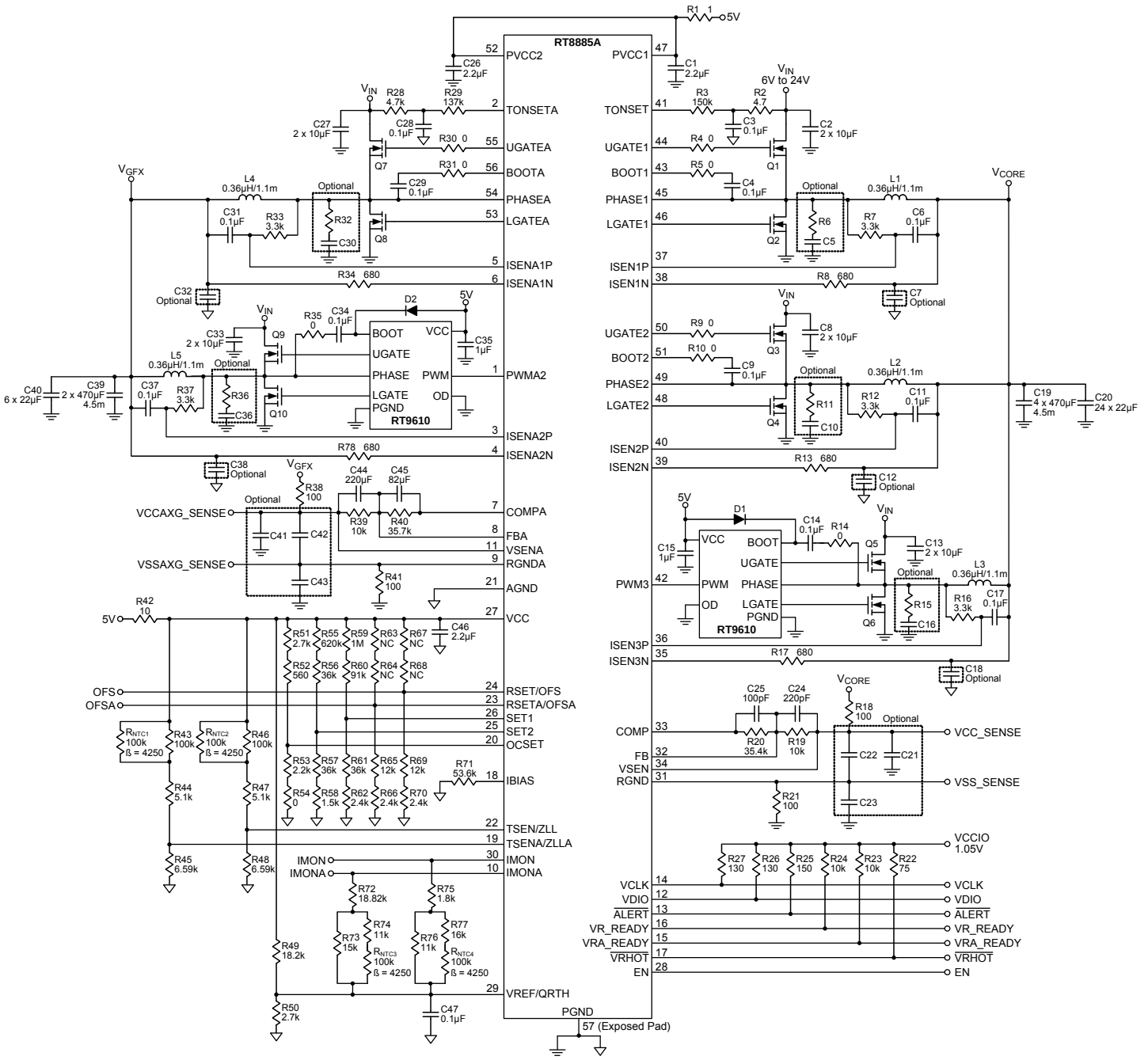
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

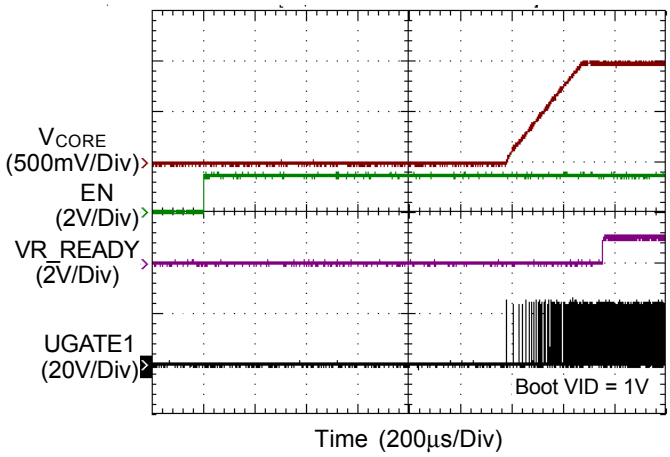
Note 5. Guaranteed by Design.

Typical Application Circuit

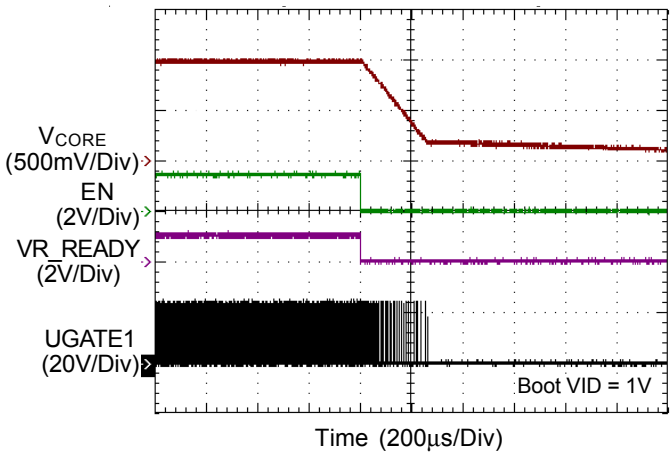


Typical Operating Characteristics

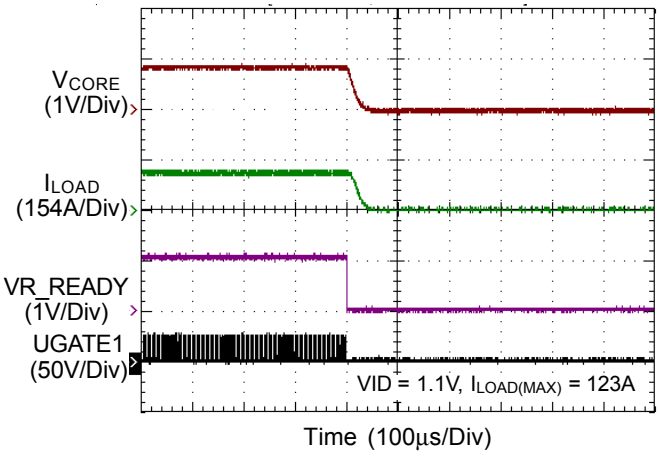
CORE VR Power On from EN



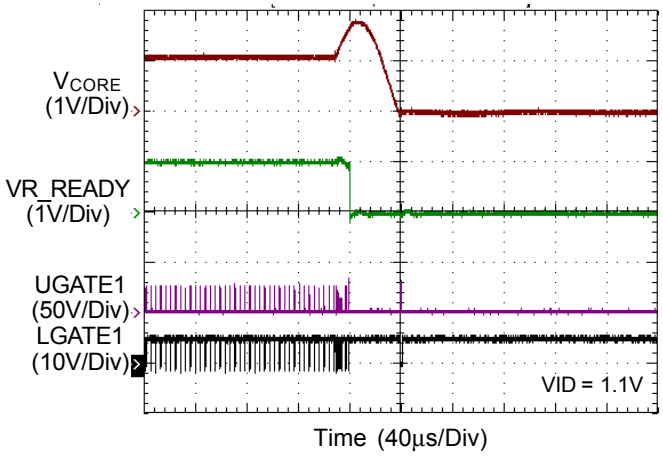
CORE VR Power Off from EN



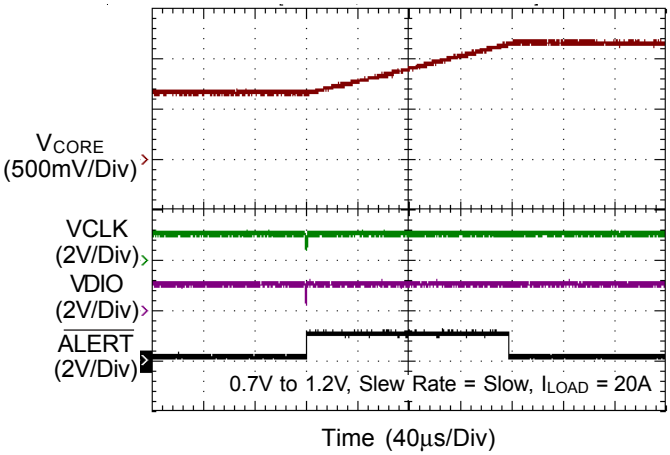
CORE VR OCP



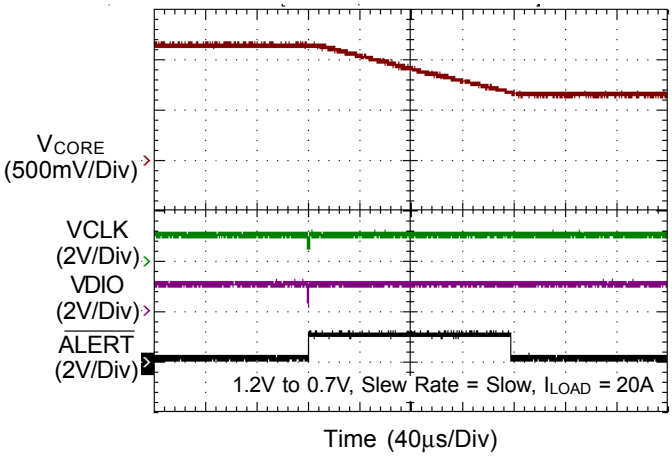
CORE VR OVP and NVP



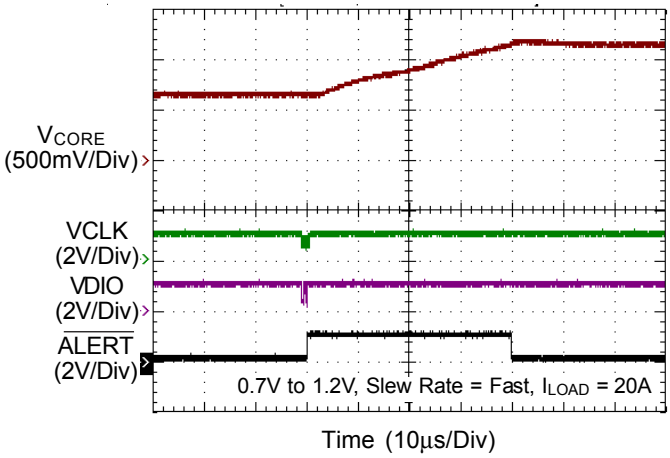
CORE VR Dynamic VID Up



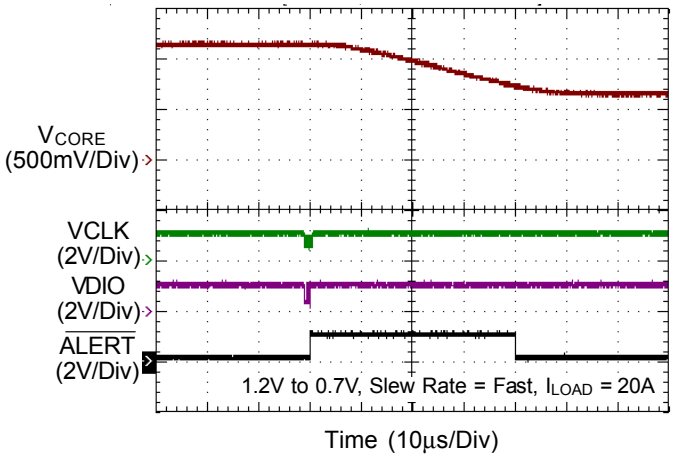
CORE VR Dynamic VID Down



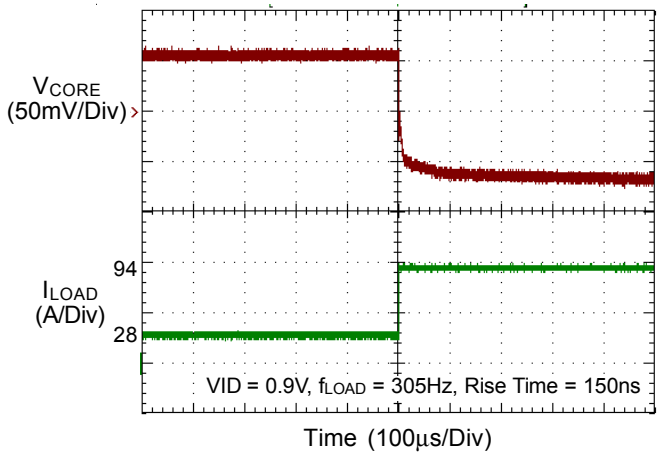
CORE VR Dynamic VID Up



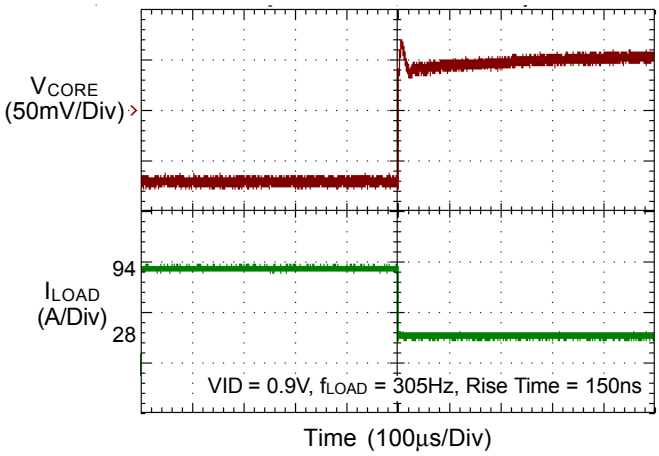
CORE VR Dynamic VID Down



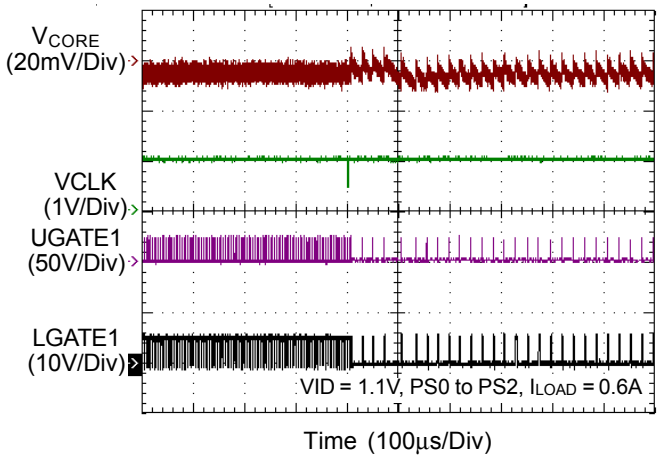
CORE VR Load Transient



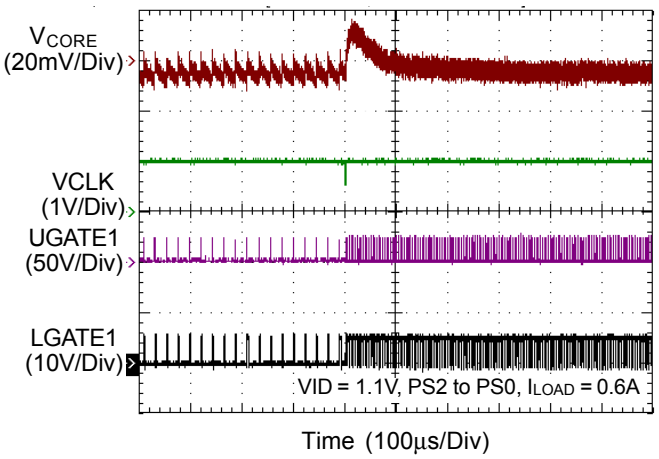
CORE VR Load Transient



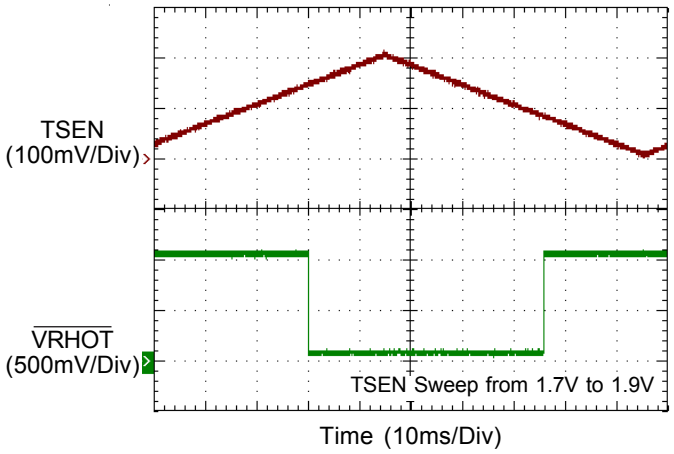
CORE VR Mode Transient



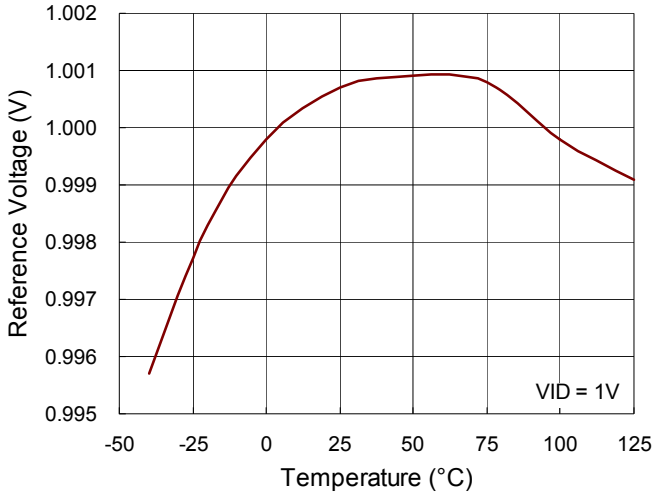
CORE VR Mode Transient



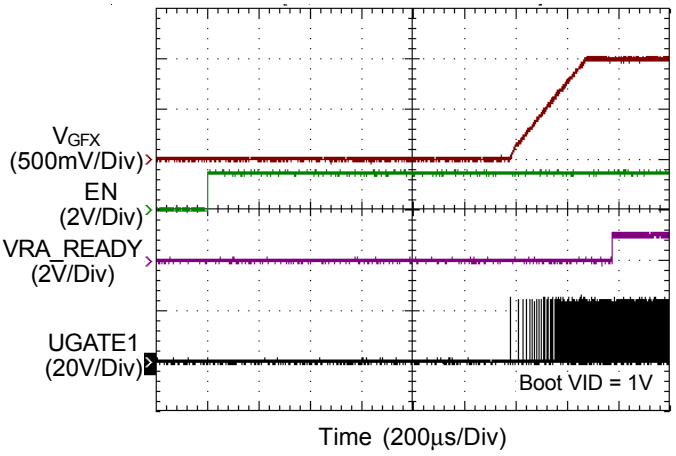
CORE VR Thermal Monitoring



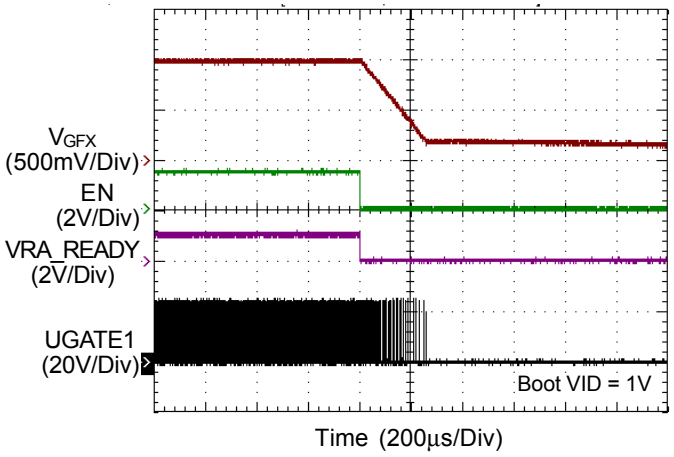
CORE VR Reference Voltage vs. Temperature



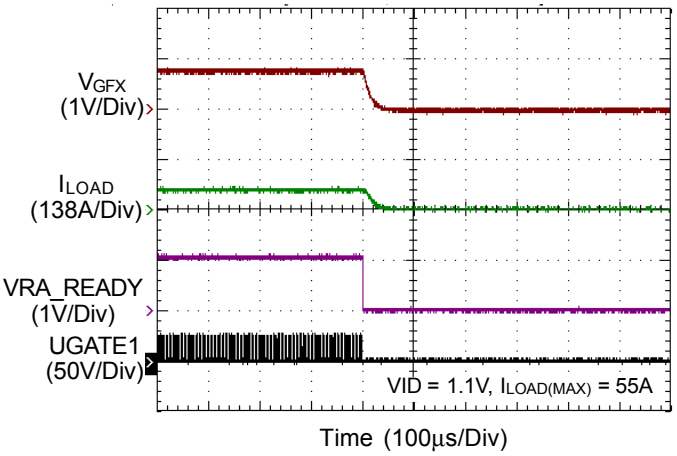
GFX VR Power On form EN



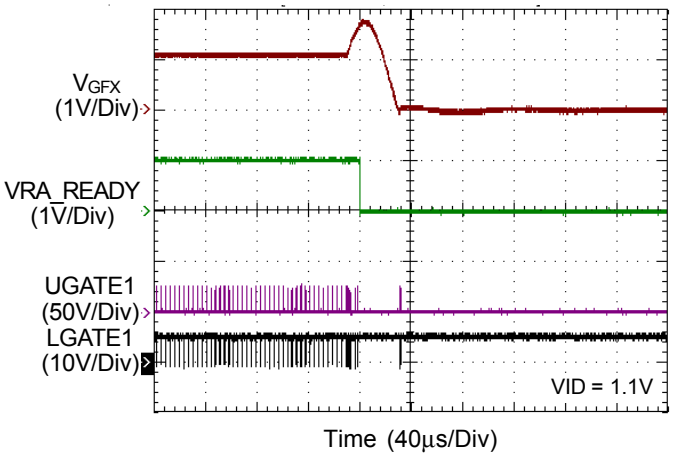
GFX VR Power Off form EN



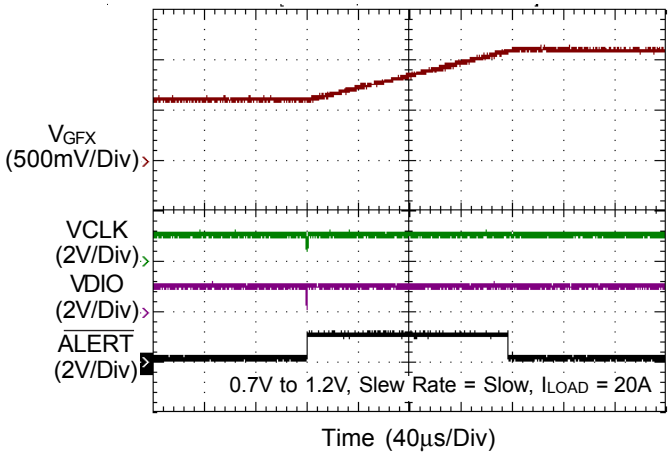
GFX VR OCP



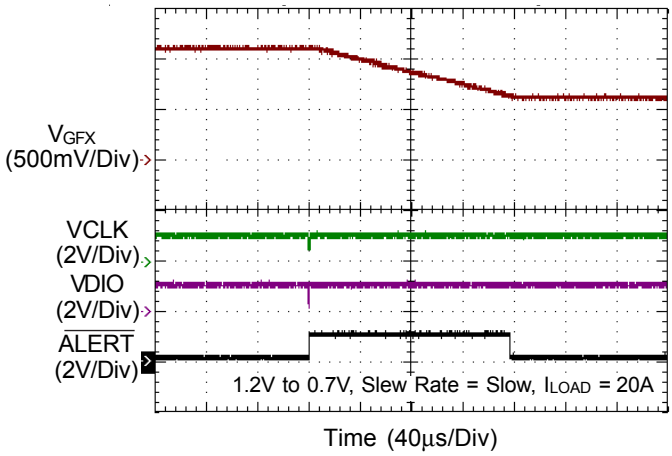
GFX VR OVP and NVP



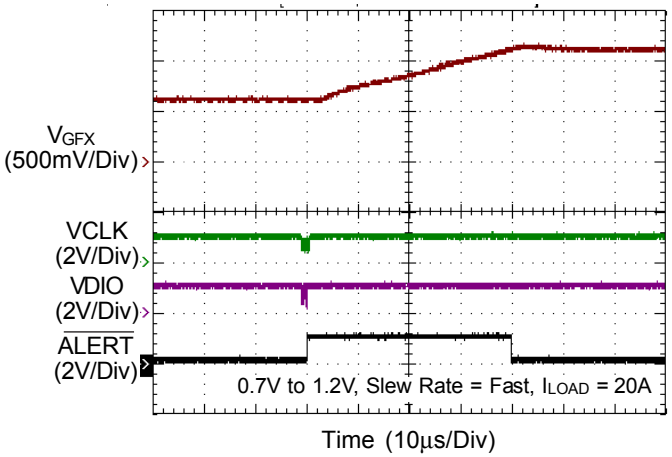
GFX VR Dynamic VID Up



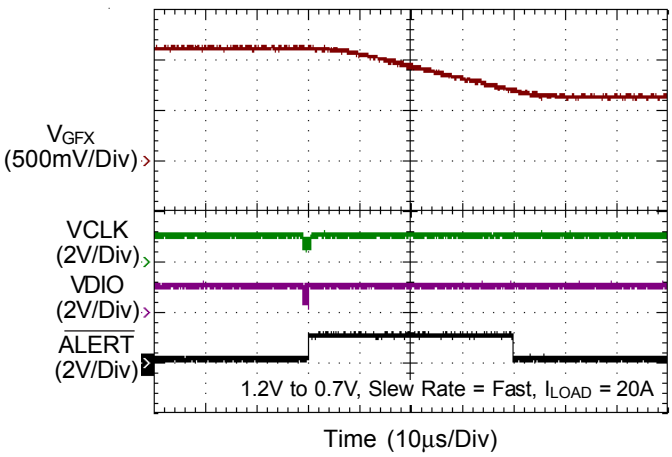
GFX VR Dynamic VID Down



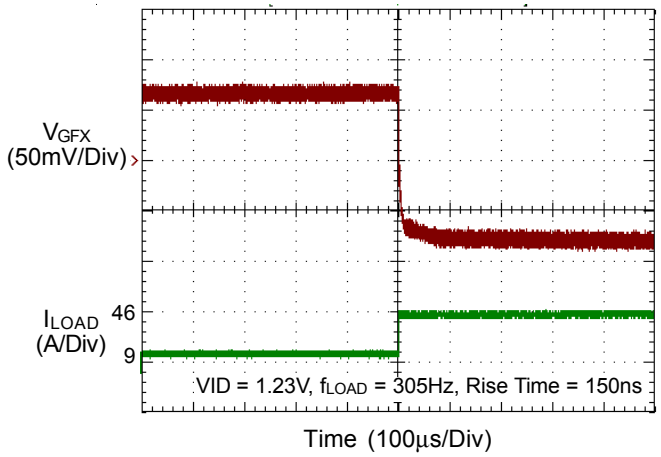
GFX VR Dynamic VID Up



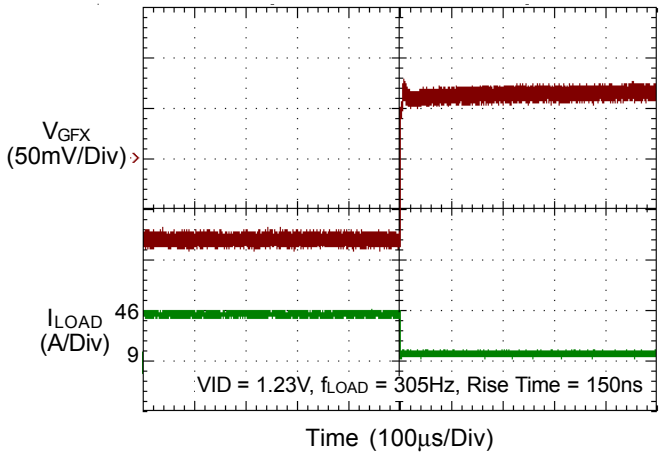
GFX VR Dynamic VID Down



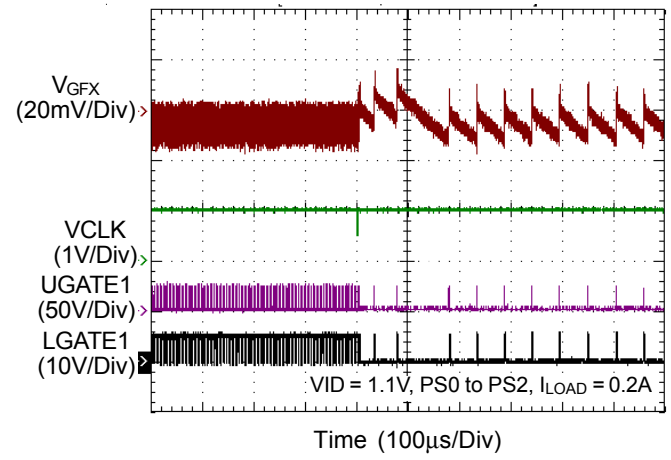
GFX VR Load Transient



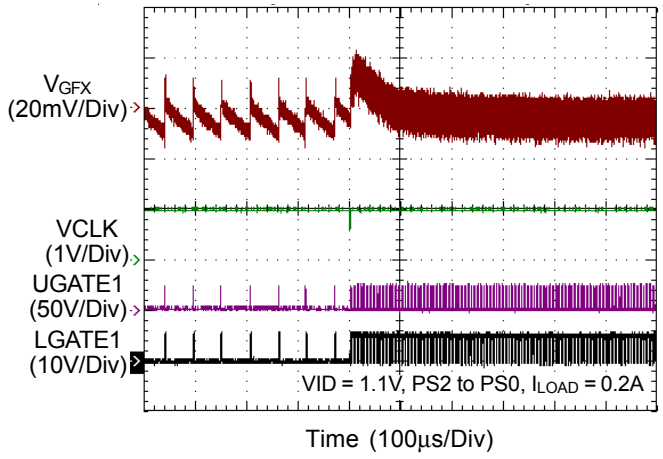
GFX VR Load Transient



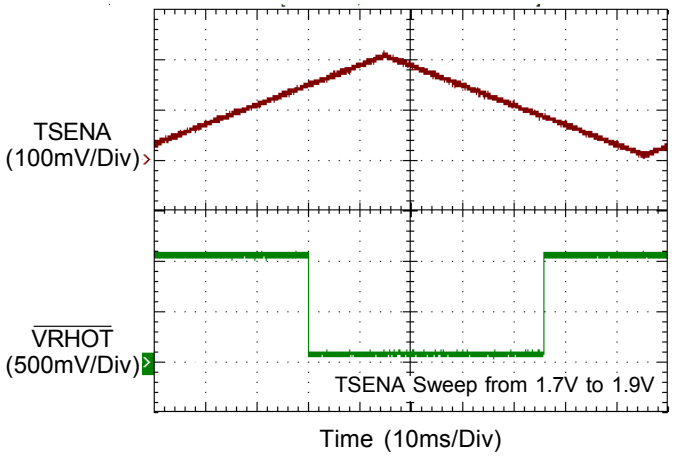
GFX VR Mode Transient



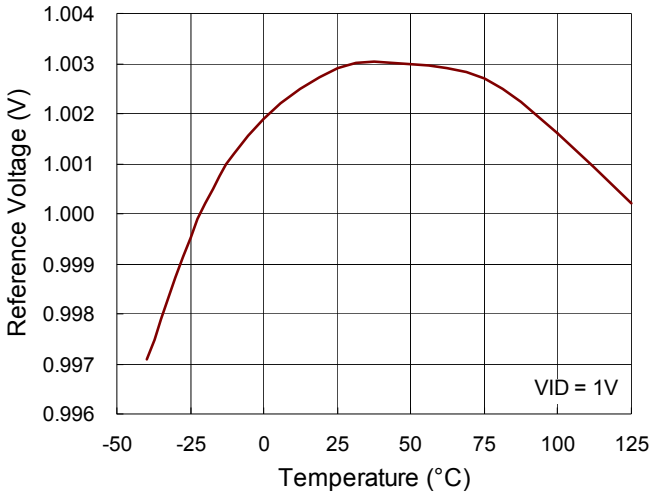
GFX VR Mode Transient



GFX VR Thermal Monitoring



GFX VR Reference Voltage vs. Temperature



Application Information

The RT8885A is a CPU power controller which includes two voltage rails : a 3/2/1 phase synchronous buck controller, the CORE VR, and a 2/1 phase synchronous buck controller, the GFX VR. The IC is compliant with Intel VR12/IMVP7 voltage regulator specification to fulfill Intel's CPU power supply requirements of both CORE and GFX voltage rails. A Serial VID (SVID) interface is built-in the RT8885A to communicate with Intel VR12/IMVP7 compliant CPU.

The RT8885A adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain compensator with current mode control, making it an easy setting PWM controller, meeting all Intel CPU requirements of AVP (Active Voltage Positioning). The load line can be easily programmed by setting the DC gain of the error amplifier. The RT8885A has fast transient response due to the G-NAVP™ commanding variable switching frequency. Based on the G-NAVP™ topology, the IC also features a quick response mechanism for optimized AVP performance during load transient.

The G-NAVP™ topology also represents a high efficiency system with green power concept. With the G-NAVP™ topology, the RT8885A becomes a green power controller with high efficiency under heavy load, light load, and very light load conditions. The IC supports mode transition function with various operating states, including multi-phase, single phase and diode emulation modes. These different operating states allow the overall power control system to have the lowest power loss. By utilizing the G-NAVP™ topology, the operating frequency of the RT8885A varies with VID, load, and input voltage to further enhance the efficiency even in CCM.

The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT8885A supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. The RT8885A also built-in in a high accuracy ADC for some platform setting functions, such as no-load offset or over current level. The controller supports both DCR and sense resistor current sensing. The RT8885A provides VR_READY and VRA_READY signals for both CORE VR and GFX VR. It also features complete fault protection function including over voltage, under voltage, negative voltage, over current and under voltage lockout. The RT8885A is available in a WQFN-56L 7x7 small footprint package.

General Loop Functions :

Precise Reference Current Generation

The RT8885A includes complicated analog circuits inside the controller. These analog circuits need very precise reference voltage/current to drive these analog devices. The RT8885A will auto generate a 2.14V voltage source at IBIAS pin, and an exact 53.6kΩ resistor is required to be connected between IBIAS and analog ground, as shown in Figure 1. Through this connection, the RT8885A will generate a 40μA current from the IBIAS pin to analog ground, and this 40μA current will be mirrored inside the RT8885A for internal use. Note that other type of connection or other values of resistance applied at the IBIAS pin may cause failure of the RT8885A's functions, such as slew rate control, OFS accuracy, etc. In other words, the IBIAS pin can only be connected with an exact 53.6kΩ resistor to GND. The resistance accuracy of this resistor is recommended to be 1% or higher.

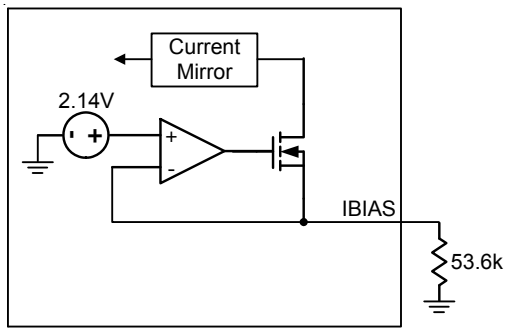


Figure 1. IBIAS Setting

SET1 Pin Setting

The RT8885A provides SET1 pin for platform users to set CORE VR's functions : initial startup voltage V_{INI_CORE}, maximum output current ICCMAX and PWM on-time of quick response for load transient boost.

Figure 2 (a) shows PWM on-time of quick response QR for CORE VR setting with the SET1 pin voltage V_{SET1_DIV}. When EN pin goes high, the SET1 pin voltage is sensed

and held to set PWM on-time of quick response for load transient boost. The SET1 pin voltage V_{SET1_DIV} is shown as :

$$V_{SET1\_DIV} = VCC \times \frac{R_{SET1\_D}}{R_{SET1\_U} + R_{SET1\_D}} \quad (1)$$

Figure 2 (b) shows V_{INI_CORE} and ICCMAX for CORE VR setting with the SET1 pin voltage difference ΔV_{SET1}. After PWM on-time of QR for CORE VR setting, a 40μA is injected into SET1 pin while the SET1 pin voltage difference ΔV_{SET1} is sensed and decoded to set initial startup voltage V_{INI_CORE} and maximum output current ICCMAX. The SET1 pin voltage difference ΔV_{SET1} is shown as :

$$\Delta V_{SET1} = 40\mu A \times \frac{R_{SET1\_U} \times R_{SET1\_D}}{R_{SET1\_U} + R_{SET1\_D}} \quad (2)$$

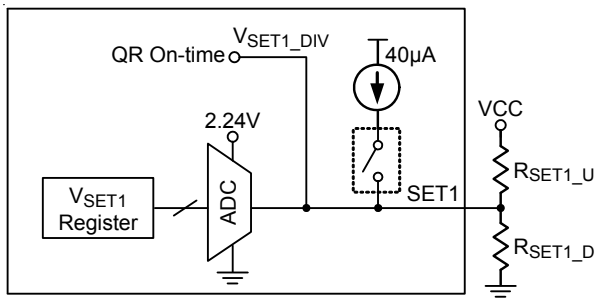


Figure 2 (a). PWM On-Time of Quick Response for CORE VR Setting

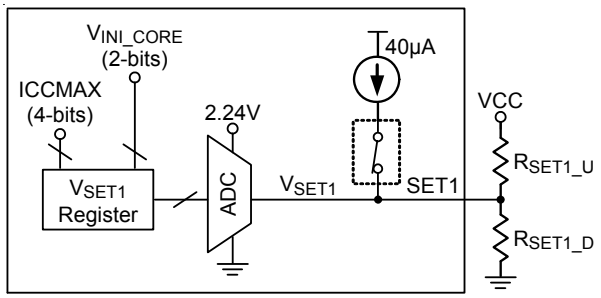


Figure 2 (b). V_{INI_CORE} and ICCMAX for CORE VR Setting

If V_{SET1_DIV} and ΔV_{SET1} are determined, R_{SET1_U} and R_{SET1_D} can be calculated as follows :

$$R_{SET1\_U} = \frac{VCC \times \Delta V_{SET1}}{40\mu A \times V_{SET1\_DIV}} \quad (3)$$

$$R_{SET1\_D} = \frac{R_{SET1\_U} \times V_{SET1\_DIV}}{VCC - V_{SET1\_DIV}} \quad (4)$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the SET1 resistor network for CORE VR.

SET2 Pin Setting

The RT8885A provides SET2 pin for platform users to set GFX VR's functions : initial startup voltage V_{INI_GFX}, maximum output current ICCMAXA and PWM on-time of quick response for load transient boost.

Figure 3 (a) shows PWM on-time of quick response QR for GFX VR setting with the SET2 pin voltage V_{SET2_DIV}. When EN pin goes high, the SET2 pin voltage is sensed and held to set PWM on-time of quick response for load transient boost. The SET2 pin voltage V_{SET2_DIV} is shown as :

$$V_{SET2\_DIV} = VCC \times \frac{R_{SET2\_D}}{R_{SET2\_U} + R_{SET2\_D}} \quad (5)$$

Figure 3 (b) shows V_{INI_GFX} and ICCMAXA for GFX VR setting with the SET2 pin voltage difference ΔV_{SET2}. After PWM on-time of QR for GFX VR setting, a 40μA is injected into SET2 pin while the SET2 pin voltage difference ΔV_{SET2} is sensed and decoded to set initial startup voltage V_{INI_GFX} and maximum output current ICCMAXA. The SET2 pin voltage difference ΔV_{SET2} is shown as :

$$\Delta V_{SET2} = 40\mu A \times \frac{R_{SET2\_U} \times R_{SET2\_D}}{R_{SET2\_U} + R_{SET2\_D}} \quad (6)$$

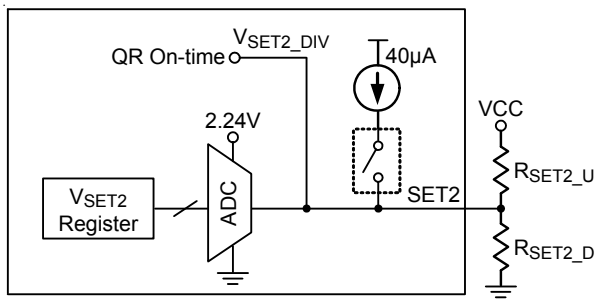


Figure 3 (a). PWM On-Time of Quick Response for GFX VR Setting

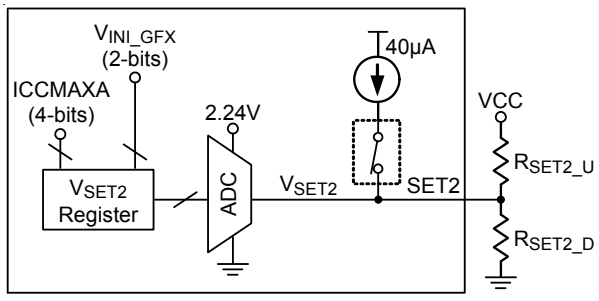


Figure 3 (b). V_{INI_GFX} and ICCMAXA for GFX VR Setting

If V_{SET2_DIV} and ΔV_{SET2} are determined, R_{SET2_U} and R_{SET2_D} can be calculated as follows :

$$R_{SET2\_U} = \frac{VCC \times \Delta V_{SET2}}{40\mu A \times V_{SET2\_DIV}} \quad (7)$$

$$R_{SET2\_D} = \frac{R_{SET2\_U} \times V_{SET2\_DIV}}{VCC - V_{SET2\_DIV}} \quad (8)$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the SET2 resistor network for GFX VR.

RSET/OFS Pin Setting

The RT8885A provides RSET/OFS pin for platform users to set CORE VR's functions : internal compensation ramp factor for control loop, output voltage offset and forced-DEM operation.

Figure 4 (a) shows output voltage offset for CORE VR setting with the RSET/OFS pin voltage V_{RSET_DIV}. When EN pin goes high, the RSET/OFS pin voltage is sensed and held to set output voltage offset for CORE VR. The RSET/OFS pin voltage V_{RSET_DIV} is shown as :

$$V_{RSET\_DIV} = VCC \times \frac{R_{RSET\_D}}{R_{RSET\_U} + R_{RSET\_D}} \quad (9)$$

Figure 4 (b) shows internal compensation ramp factor and forced-DEM operation for CORE VR setting with the RSET/OFS pin voltage difference ΔV_{RSET}. After output voltage offset for CORE VR setting, a 40μA is injected into RSET/OFS pin while the RSET/OFS pin voltage difference ΔV_{RSET} is sensed and decoded to set internal compensation ramp factor and forced-DEM operation. The RSET/OFS pin voltage difference ΔV_{RSET} is shown as :

$$\Delta V_{RSET} = 40\mu A \times \frac{R_{RSET\_U} \times R_{RSET\_D}}{R_{RSET\_U} + R_{RSET\_D}} \quad (10)$$

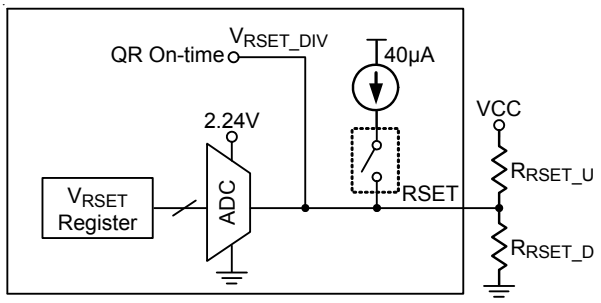


Figure 4 (a). Output Voltage Offset for CORE VR Setting

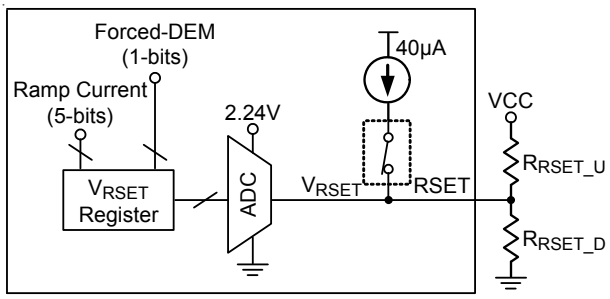


Figure 4 (b). Internal Compensation Ramp Factor and Forced-DEM Operation for CORE VR Setting

If V_{RSET_DIV} and ΔV_{RSET} are determined, R_{RSET_U} and R_{RSET_D} can be calculated as follows :

$$R_{RSET\_U} = \frac{VCC \times \Delta V_{RSET}}{40\mu A \times V_{RSET\_DIV}} \quad (11)$$

$$R_{RSET\_D} = \frac{R_{RSET\_U} \times V_{RSET\_DIV}}{VCC - V_{RSET\_DIV}} \quad (12)$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the RSET/OFS resistor network for CORE VR.

RSETA/OFSA Pin Setting

The RT8885A provides RSETA/OFSA pin for platform users to set GFX VR's functions : internal compensation ramp factor for control loop, output voltage offset and forced-DEM operation.

Figure 5 (a) shows output voltage offset for GFX VR setting with the RSETA/OFSA pin voltage V_{RSETA_DIV}. When EN pin goes high, the RSETA/OFSA pin voltage is sensed and held to set output voltage offset for GFX VR. The RSETA/OFSA pin voltage V_{RSETA_DIV} is shown as :

$$V_{RSETA\_DIV} = VCC \times \frac{R_{RSETA\_D}}{R_{RSETA\_U} + R_{RSETA\_D}} \quad (13)$$

Figure 5 (b) shows internal compensation ramp factor and forced-DEM operation for GFX VR setting with the RSETA/OFSA pin voltage difference ΔV_{RSETA}. After output voltage offset for GFX VR setting, a 40μA is injected into RSETA/OFSA pin while the RSETA/OFSA pin voltage difference ΔV_{RSETA} is sensed and decoded to set internal compensation ramp factor and forced-DEM operation. The RSETA/OFSA pin voltage difference ΔV_{RSETA} is shown as:

$$\Delta V_{RSETA} = 40\mu A \times \frac{R_{RSETA\_U} \times R_{RSETA\_D}}{R_{RSETA\_U} + R_{RSETA\_D}} \quad (14)$$

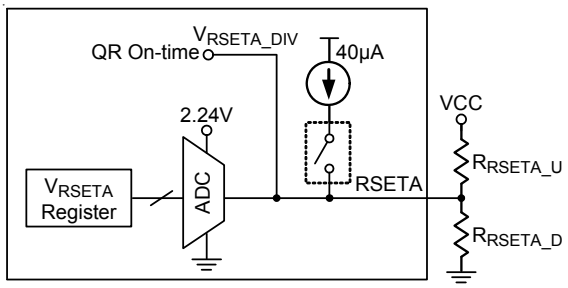


Figure 5 (a). Output Voltage Offset for GFX VR Setting

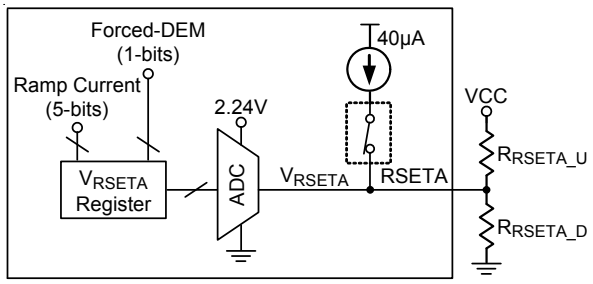


Figure 5 (b). Internal Compensation Ramp Factor and Forced-DEM Operation for GFX VR Setting

If V_{RSETA_DIV} and ΔV_{RSETA} are determined, R_{RSETA_U} and R_{RSETA_D} can be calculated as follows :

$$R_{RSETA\_U} = \frac{VCC \times \Delta V_{RSETA}}{40\mu A \times V_{RSETA\_DIV}} \quad (15)$$

$$R_{RSETA\_D} = \frac{R_{RSETA\_U} \times V_{RSETA\_DIV}}{VCC - V_{RSETA\_DIV}} \quad (16)$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the RSETA/OFSA resistor network for GFX VR.

OCSET Pin Setting

The RT8885A provides OCSET pin for platform users to set CORE VR and GFX VR over current protection thresholds.

Figure 6 (a) shows CORE VR's summed total over current protection SUM_OCP threshold and per phase over current protection PH_OCP threshold setting with the OCSET pin voltage V_{OCSET_DIV}. When EN pin goes high, the OCSET pin voltage is sensed, held and decoded to set SUM_OCP and PH_OCP thresholds for CORE VR. The OCSET pin voltage V_{OCSET_DIV} is shown as :

$$V_{OCSET\_DIV} = VCC \times \frac{R_{OCSET\_D}}{R_{OCSET\_U} + R_{OCSET\_D}} \quad (17)$$

Figure 6 (b) shows GFX VR's summed total over current protection SUM_OCP threshold and per phase over current protection PH_OCP threshold setting with the OCSET pin voltage difference ΔV_{OCSET}. After CORE VR over current protection thresholds setting, a 40μA is injected into OCSET pin while the OCSET pin voltage difference ΔV_{OCSET} is sensed and decoded to set SUM_OCP and PH_OCP thresholds for GFX VR. The OCSET pin voltage difference ΔV_{OCSET} is shown as :

$$\Delta V_{OCSET} = 40\mu A \times \frac{R_{OCSET\_U} \times R_{OCSET\_D}}{R_{OCSET\_U} + R_{OCSET\_D}} \quad (18)$$

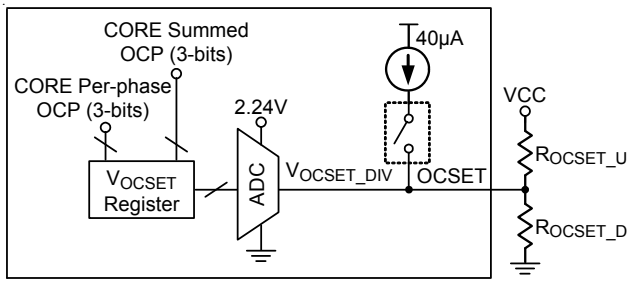


Figure 6 (a). CORE VR SUM_OCP and PH_OCP Thresholds Setting

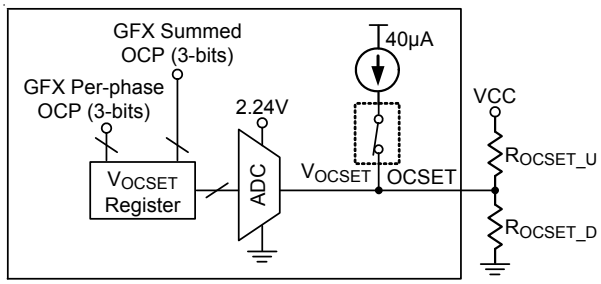


Figure 6 (b). GFX VR SUM_OCP and PH_OCP Thresholds Setting

If V_{OCSET_DIV} and ΔV_{OCSET} are determined, R_{OCSET_U} and R_{OCSET_D} can be calculated as follows :

$$R_{OCSET\_U} = \frac{VCC \times \Delta V_{OCSET}}{40\mu A \times V_{OCSET\_DIV}} \quad (19)$$

$$R_{OCSET\_D} = \frac{R_{OCSET\_U} \times V_{OCSET\_DIV}}{VCC - V_{OCSET\_DIV}} \quad (20)$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the OCSET resistor network for both VRs.

VREF/QRTH Pin Setting

The VREF/QRTH pin provides two functions: providing fixed 0.6V reference voltage output during normal operation of VR controller and programming the quick response trigger thresholds (QRTH) for CORE VR and GFX VR.

Figure 7 (a) shows CORE VR and GFX VR QRTH setting with the VREF/QRTH pin voltage V_{QRTH_DIV}. When the rising edge of EN pin goes high, the VREF/QRTH pin voltage V_{QRTH_DIV} is sensed and decoded to set QRTH for CORE VR and GFX VR. The VREF/QRTH pin voltage V_{QRTH_DIV} is shown as :

$$V_{QRTH\_DIV} = V_{CC} \times \frac{R_{QRTH\_D}}{R_{QRTH\_U} + R_{QRTH\_D}} \quad (21)$$

Figure 7 (b) shows the illustration of 0.6V regulation at the VREF/QRTH pin during the normal operation of VR controller after EN pin goes high. Due to the design margin of the internal voltage regulator, the sink current through the VREF/QRTH pin should be under 300μA and source current through the VREF/QRTH pin should be under 80μA.

$$I_{VREF} = \pm \left| \frac{V_{CC} - 0.6V}{R_{QRTH\_U}} - \frac{0.6V}{R_{QRTH\_D}} \right| \quad (22)$$

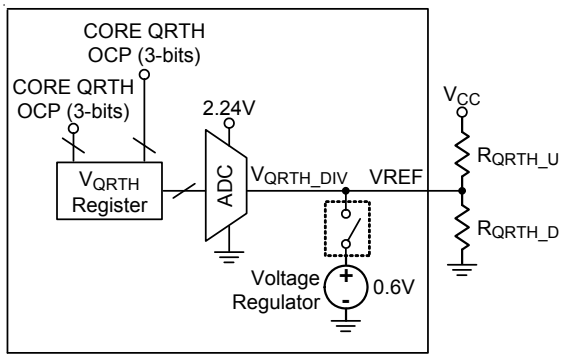


Figure 7 (a). CORE VR and GFX VR QRTH Setting

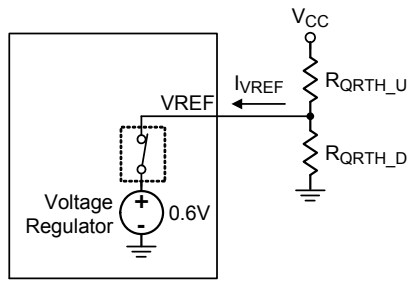


Figure 7 (b). Illustration of 0.6V Regulation at VREF Pin

If V_{QRTH_DIV} and I_{VREF} are determined, R_{QRTH_U} and R_{QRTH_D} can be calculated as follows :

$$R_{QRTH\_U} = \left| \frac{V_{CC}}{I_{VREF}} \times \left(1 - \frac{0.6V}{V_{QRTH\_DIV}} \right) \right| \quad (23)$$

$$R_{QRTH\_D} = \frac{V_{QRTH\_DIV}}{\left(V_{CC} - V_{QRTH\_DIV} \right)} \times R_{QRTH\_U} \quad (24)$$

In the application circuit, the C_{VREF} is used to stabilize the internal voltage regulator at VREF/QRTH pin, as in shown Figure 8. Therefore, the capacitance of C_{VREF} must be greater than 0.1μF and the maximum capacitance of this capacitor is 2.2μF. However, this capacitance should be chosen carefully due to the pin setting accuracy.

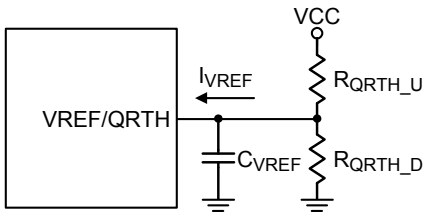


Figure 8. Illustration of Capacitor C_{VREF} at VREF/QRTH Pin

In order to ensure the voltage on VREF/QRTH pin has been settled when the rising edge of EN pin goes high for pin setting accuracy, the equivalent RC time constant at this pin should be under 2ms as shown in follows :

$$5 \times R_{QUTH\_EQU} \times C_{VREF} < 2ms \quad (25)$$

$$R_{QRTH\_EQU} = \frac{V_{QRTH\_U} \times R_{QRTH\_D}}{V_{QRTH\_U} + R_{QRTH\_D}} \quad (26)$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the VREF/QRTH resistor network for both VRs.

TSEN/ZLL Pin Setting

The TSEN/ZLL pin provides two functions for CORE VR : thermal monitor input, and droop enable/disable setting.

Figure 9 (a) shows CORE VR droop enable/disable setting with the TSEN/ZLL pin voltage difference ΔV_{TSEN}. When EN pin goes high, a 40μA is injected into TSEN/ZLL pin. If the TSEN/ZLL pin voltage difference ΔV_{TSEN} is greater than 3.8V, CORE VR droop is disabled. If not CORE VR droop

is enabled. The TSEN/ZLL pin voltage difference ΔV_{TSEN} is shown as :

$$\Delta V_{TSEN} = 40\mu A \times \frac{R_{TSEN\_3} \times R_{TSEN\_EQU}}{R_{TSEN\_3} + R_{TSEN\_EQU}} \quad (27)$$

$$\text{where } R_{TSEN\_EQU} = \frac{R_{TSEN\_1} \times R_{TSEN\_NTC}}{R_{TSEN\_1} + R_{TSEN\_NTC}} + R_{TSEN\_2}$$

Figure 9 (b) shows CORE VR thermal monitor function enable/disable setting with the TSEN/ZLL pin voltage V_{TSEN_DIV}. After CORE VR droop enable/disable setting, the TSEN/ZLL pin voltage V_{TSEN_DIV} is sensed and held. If the TSEN/ZLL pin voltage V_{TSEN_DIV} is greater than 2.9V, CORE VR thermal monitor function is disabled. If not CORE VR thermal monitor function is enabled. The TSEN/ZLL pin voltage V_{TSEN_DIV} is shown as :

$$V_{TSEN\_DIV} = VCC \times \frac{R_{TSEN\_3}}{R_{TSEN\_3} + R_{TSEN\_EQU}} \quad (28)$$

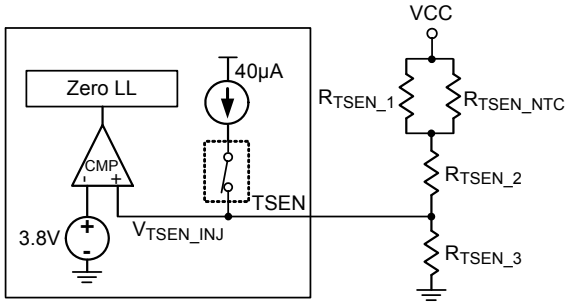


Figure 9 (a). CORE VR Droop Enable/Disable Setting

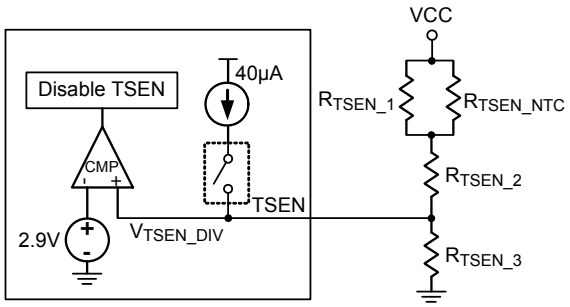


Figure 9 (b). CORE VR Thermal Monitor Function Enable/Disable Setting

If V_{TSEN_DIV} and ΔV_{TSEN} are determined, R_{TSEN_EQU} and R_{TSEN_3} can be calculated as follows :

$$R_{TSEN\_EQU} = \frac{VCC \times \Delta V_{TSEN}}{40\mu A \times V_{TSEN\_DIV}} \quad (29)$$

$$R_{TSEN\_3} = \frac{R_{TSEN\_EQU} \times V_{TSEN\_DIV}}{VCC - V_{TSEN\_DIV}} \quad (30)$$

TSENA/ZLLA Pin Setting

The TSENA/ZLLA pin provides two functions for GFX VR : thermal monitor input, and droop enable/disable setting.

Figure 10 (a) shows GFX VR droop enable/disable setting with the TSENA/ZLLA pin voltage difference ΔV_{TSENA}. When EN pin goes high, a 40μA is injected into TSENA/ZLLA pin. If the TSENA/ZLLA pin voltage difference ΔV_{TSENA} is greater than 3.8V, GFX VR droop is disabled. If not GFX VR droop is enabled. The TSENA/ZLLA pin voltage difference ΔV_{TSENA} is shown as :

$$\Delta V_{TSENA} = 40\mu A \times \frac{R_{TSENA\_3} \times R_{TSENA\_EQU}}{R_{TSENA\_3} + R_{TSENA\_EQU}} \quad (31)$$

$$\text{where } R_{TSENA\_EQU} = \frac{R_{TSENA\_1} \times R_{TSENA\_NTC}}{R_{TSENA\_1} + R_{TSENA\_NTC}} + R_{TSENA\_2}$$

Figure 10 (b) shows GFX VR thermal monitor function enable/disable setting with the TSENA/ZLLA pin voltage V_{TSENA_DIV}. After GFX VR droop enable/disable setting, the TSENA/ZLLA pin voltage V_{TSENA_DIV} is sensed and held. If the TSENA/ZLLA pin voltage V_{TSENA_DIV} is greater than 2.9V, GFX VR thermal monitor function is disabled. If not GFX VR thermal monitor function is enabled. The TSENA/ZLLA pin voltage V_{TSENA_DIV} is shown as :

$$V_{TSENA\_DIV} = VCC \times \frac{R_{TSENA\_3}}{R_{TSENA\_3} + R_{TSENA\_EQU}} \quad (32)$$

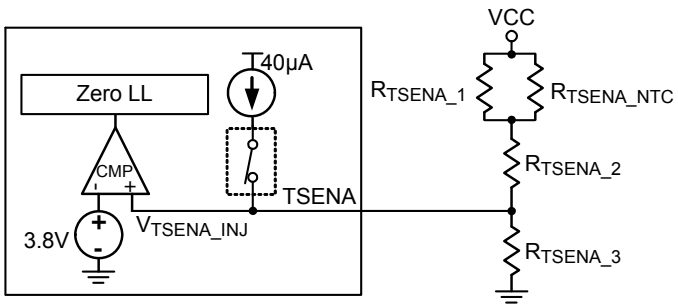


Figure 10 (a). GFX VR Droop Enable/Disable Setting

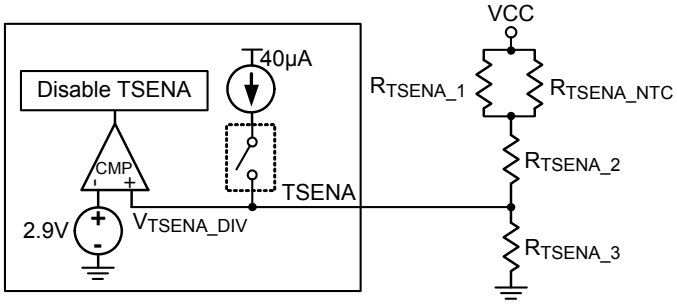


Figure 10 (b). GFX VR Thermal Monitor Function Enable/Disable Setting

If V_{TSENA_DIV} and ΔV_{TSENA} are determined, R_{TSENA_EQU} and R_{TSENA_3} can be calculated as follows :

$$R_{TSENA\_EQU} = \frac{VCC \times \Delta V_{TSENA}}{40\mu A \times V_{TSENA\_DIV}} \quad (33)$$

$$R_{TSENA\_3} = \frac{R_{TSENA\_EQU} \times V_{TSENA\_DIV}}{VCC - V_{TSENA\_DIV}} \quad (34)$$

V_{INITAL} Setting

The initial startup voltage of the RT8885A can be set by platform users through the SET1 and the SET2 pins. Refer to the SET1 and SET2 pin setting section and Table 3 and Table 4, platform users can set the V_{INI_CORE} and V_{INI_GFX}. For example, choose VCC = 5V, V_{INI_CORE} = 1V, ICCMAX = 53A and $T_{ON\_QR} = T_{ON}$, then solve for R_{SET1_U} and R_{SET1_D} :

$$R_{SET1\_U} = \frac{VCC \times \Delta V_{SET1}}{40\mu A \times V_{SET1\_DIV}} = \frac{5V \times 1207.5mV}{40\mu A \times 0.4V} = 377.34k\Omega \quad (35)$$

$$R_{SET1\_D} = \frac{V_{SET1\_U} \times V_{SET1\_DIV}}{VCC - V_{SET1\_DIV}} = \frac{377.34k\Omega \times 0.4V}{5V - 0.4V} = 32.81k\Omega \quad (36)$$

Start-Up Sequence

The RT8885A utilizes an internal soft-start sequence which strictly follows Intel VR12/IMVP7 start-up sequence specifications. After POR and EN go high, the controller considers all the power inputs ready and enters start-up sequence. If V_{INITAL} = 0V, V_{OUT} is programmed to stay at 0V for 2ms waiting for SVID command as shown in Figure 11 (a). If $V_{INITAL} \neq 0V$, V_{OUT} will ramp up to V_{INITAL} voltage (which is not zero) immediately after both POR go high and EN go high as shown in Figure 11 (b). After V_{OUT} reaches target V_{INITAL}, V_{OUT} will stay at V_{INITAL} waiting for SVID command. After the RT8885A receives a valid VID code (typically SetVID_Slow command), V_{OUT} will ramp up to the target voltage with specified slew rate (see section "Data and Configuration Register"). After V_{OUT} reaches target voltage (VID voltage for V_{INITAL} = 0 or V_{INITAL} for $V_{INITAL} \neq 0$), the RT8885A will send out VR_READY signal to indicate that the power state of the RT8885A is ready. The VR ready circuit is an open-drain structure, so a pull-up resistor connected to a voltage source is required.

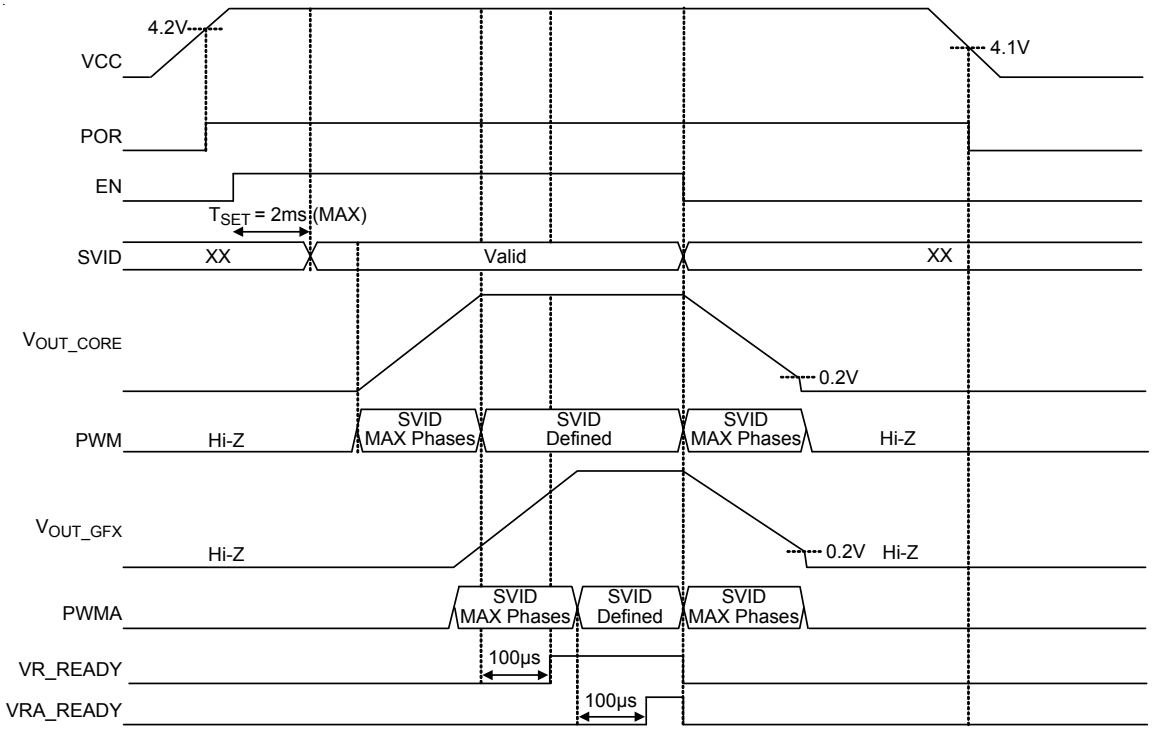


Figure 11 (a). Power Sequence for the RT8885A ($V_{INITIAL}$ = $V_{INITIALA}$ = 0V)

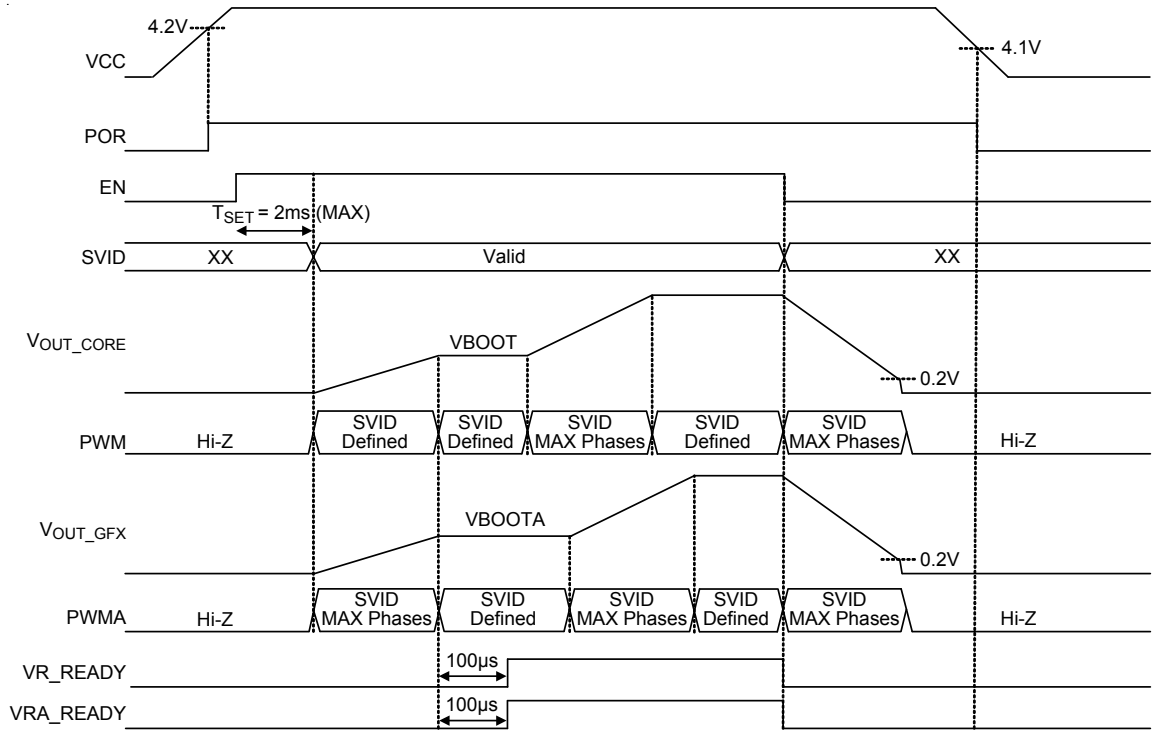


Figure 11 (b). Power Sequence for the RT8885A ($V_{INITIAL} \neq 0V$, $V_{INITIALA} \neq 0V$)

Power Down Sequence

Similar to the start-up sequence, the RT8885A also utilizes a soft shutdown mechanism during turn-off. After EN goes low, the internal reference voltage (positive terminal of compensation EA) starts ramping down with 3.125mV/µs slew rate, and V_{OUT} will follow the reference voltage to 0V. After V_{OUT} drops below 0.2V, the RT8885A will be shut down and all functions (drivers) are disabled. The VR_READY and VRA_READY will be pulled down immediately after POR goes low or EN goes low.

CORE VR

Active Phase Determination : Before EN

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during start-up. Normally, the CORE VR operates as a 3-phase PWM controller. Setting ISEN3N to VCC before power on can program a 2-phase operation, and pulling ISEN2N, and setting ISEN2N, and ISEN3N to VCC before power on can program a 1-phase operation. Before EN, CORE VR detects whether the voltages of ISEN2N and ISEN3N are higher than "VCC – 0.5V" respectively to decide how many phases should be active. Phase selection is only active during EN. When EN = high, the number of active phases is determined and latched. The unused ISENxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

Loop Control

The CORE VR adopts Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The output voltage, V_{OUT_CORE} will decrease with increasing output load current. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 12.

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases, V_{CS} increases, the steady state COMP voltage also increases and induces V_{OUT_CORE} to decrease, thus achieving AVP. A near-DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller.

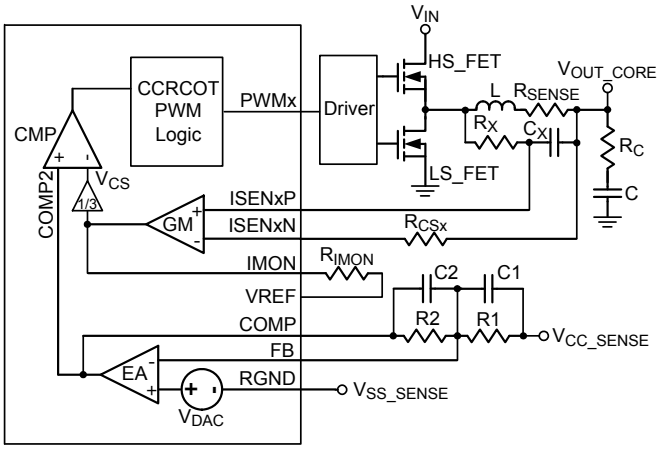


Figure 12. CORE VR : Simplified Schematic for Droop and Remote Sense in CCM

TON Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure 13 shows the On-Time setting Circuit. Connect a resistor (R_{TON}) between V_{IN_CORE} and TONSET to set the on-time of UGATE :

$$t_{ON}\ (0.5V < V_{DAC} < 1.2V) = \frac{24.4 \times 10^{-12} \times R_{TON}}{V_{IN} - V_{DAC}} \quad (37)$$

where t_{ON} is the UGATE turn on period, V_{IN_CORE} is the input voltage of the CORE VR, and V_{DAC} is the DAC voltage.

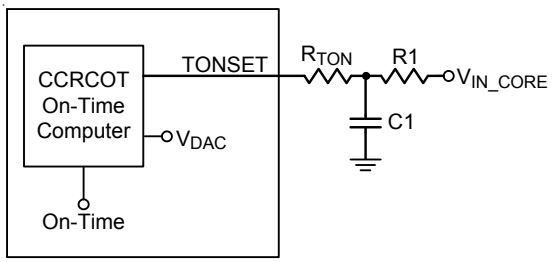


Figure 13. CORE VR : On-Time Setting with RC Filter

When V_{DAC} is larger than 1.2V, the equivalent switching frequency may be over 500kHz, and this too fast switching frequency is unacceptable. Therefore, the CORE VR implements a pseudo constant frequency technology to avoid this disadvantage of CCRCOT topology. When V_{DAC} is larger than 1.2V, the on-time equation will be modified to :

$$t_{ON}\ (V_{DAC} > 1.2V) = \frac{20.33 \times 10^{-12} \times R_{TON} \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (38)$$

On-time translates only roughly to switching frequencies. For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{SW(MAX)} \cong \frac{1}{(t_{ON} - 60ns) + \left(\frac{IccTDC}{N} \times R_{ON\_LS-FET(MAX)}\right) \times 50ns} \times \frac{V_{DAC\_PS0} + \frac{IccTDC}{N} \times \left(DCR + R_{ON\_LS-FET(MAX)} - N \times R_{DROOP}\right)}{\left[V_{IN(MAX)} + \frac{IccTDC}{N} \times \left(R_{ON\_LS-FET(MAX)} - R_{ON\_HS-FET(MAX)}\right)\right]} \quad (39)$$

where $f_{S(MAX)}$ is the maximum switching frequency, V_{DAC_PS0} is the test VID of application at PS0 for turbo mode or HFM, $V_{IN(MAX)}$ is the maximum application input voltage, IccTDC is the thermal design current of application, N is the phase number, $R_{ON\_HS-FET(MAX)}$ is the maximum equivalent high side FET $R_{DS(ON)}$, $R_{ON\_LS-FET(MAX)}$ is the maximum equivalent low side FET $R_{DS(ON)}$, DCR is the inductor DCR, and R_{DROOP} is the load line setting.

Current Sense Setting

The current sense topology of the CORE VR is continuous inductor current sensing. Therefore, the controller has less noise sensitive. Low offset amplifiers are used for current balance, loop control and over current detection. The ISENxP and ISENxN pins denote the positive and negative input of the current sense amplifier of each phase.

Users can either use a current sense resistor or the inductor's DCR for current sensing. Using the inductor's DCR allows higher efficiency as shown in Figure 14.

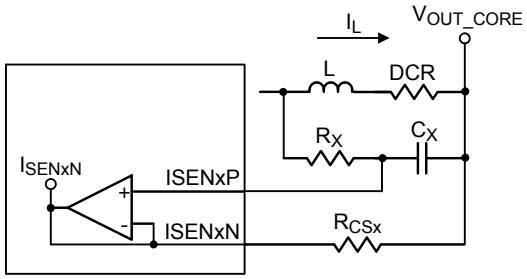


Figure 14. CORE VR : Lossless Inductor Sensing

In order to optimize transient performance, R_X and C_X must be set according to the equation below :

$$\frac{L}{DCR} = R_X \times C_X \quad (40)$$

Then the proportion between the phase current I_L and the sensed current I_{SENxN} can be described as below :

$$I_{SENxN} = I_L \times \frac{DCR}{R_{CSx}} \quad (41)$$

where R_{CSx} only an exact 680Ω sense resistor. The resistance accuracy of R_{CSx} is recommended to be 1% or higher.

In addition to considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load line requirement and the recovery is too fast causing a ring back. Vice versa, with a resistance too large the output voltage transient has only a small initial dip with a slow recovery.

Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the above mentioned inductor DCR sensing method.

Current Monitoring and Current Reporting

The RT8885A provides the current monitor function for CORE VR. IMON pin reports CORE VR inductor current.

The IMON pin outputs a high-speed analog current source that is 1 time of the summed current. Thus I_{IMON} can be described as below :

$$I_{IMON} = \sum I_{SENxN} \quad (42)$$

The RT8885A monitors the IMON pin voltage and considers that CORE VR has reached ICCMAX when IMON pin voltage is 2.392V.

As Figure 12 shows, a resistor R_{IMON} is connected between the IMON pin and VREF pin. Through the R_{IMON} to convert the IMON pin current to voltage. The voltage of IMON pin is expressed in Equation 43 :

$$V_{IMON} = I_{IMON} \times R_{IMON} + 0.6 \quad (43)$$

Rewriting Equations 41 and 42 gives Equation 44 :

$$I_{IMON} = \frac{DCR}{R_{CSx}} \times I_{LOAD} \quad (44)$$

Substitution of Equation 44 into Equation 43 gives Equation 45 :

$$V_{IMON} = \frac{DCR}{R_{CSx}} \times I_{LOAD} \times R_{IMON} + 0.6 \quad (45)$$

Rewriting Equation 45 and application of full load condition gives Equation 46 :

$$R_{IMON} = \frac{R_{CSx}}{DCR} \times \frac{(V_{IMON} - 0.6)}{I_{LOAD}} \quad (46)$$

For example, given R_{CSx} = 680Ω, DCR = 0.82mΩ, V_{IMON} = 2.392V at $I_{LOAD(MAX)}$ = 53A, Equation 46 gives R_{IMON} = 28kΩ.

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the IMON resistor network with temperature compensation for CORE VR.

Droop Setting

It's very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. This target is to have

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{DROOP} \quad (47)$$

Then solving the switching condition V_{COMP2} = V_{CS} in Figure 12 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{G_I}{R_{DROOP}} \quad (48)$$

where R_{DROOP} is the equivalent load line resistance as well as the desired static output impedance.

The summed current sense gain G_I as

$$G_I = \frac{R_{SENSE}}{R_{CSx}} \times R_{IMON} \times \frac{1}{3} \quad (49)$$

where R_{SENSE} is the current-sense resistor. If no external sense resistor present, it is the DCR of the inductor. R_{CSx} is the sense resistor. R_{IMON} is the equivalent resistance of temperature dependent resistor.

Droop Disable

Refer to the TSEN pin setting section, disabling the CORE VR droop can be set by platform users through the TSEN pin.

Loop Compensation

Optimized compensation of the CORE VR allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate

for proper compensation. Figure 12 shows the compensation circuit. Prior design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_p = \frac{1}{2\pi \times C \times R_C} \quad (50)$$

where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (51)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \quad (52)$$

Differential Remote Sense Setting

The CORE VR includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. Figure 15 shows the CORE VR differential remote voltage sense connection. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE}. Connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

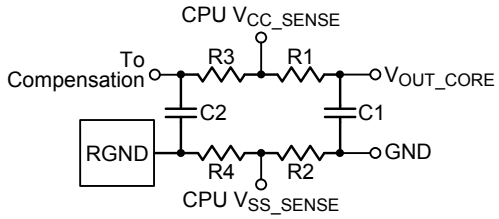


Figure 15. CORE VR : Differential Remote Voltage Sense Connection

Current Balance

The CORE VR implements internal current balance mechanism in the current loop. The CORE VR senses and compares per-phase current signal with average current. If the sensed current of any particular phase is larger than average current, the on-time of this phase will be adjusted to be shorter.

No Load Offset (SVID & Platform)

The CORE VR features no load offset function which provides the possibility of wide range positive offset of output voltage. The no-load offset function can be implemented through the SVID interface or RSET/OFS pin. Users can disable pin offset function by simply connecting RSET/OFS pin to GND. The RT8885A will latch the RSET/OFS status after EN goes high.

If pin offset function is enabled, then the output voltage is

$$V_{OUT\_CORE} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{SVID-OFS} + V_{PIN-OFS} \quad (53)$$

If not the output voltage is

$$V_{OUT\_CURE} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{SVID-OFS} \quad (54)$$

The pin offset voltage is set by the divider voltage on RSET/OFS pin. The linear range of offset pin voltage is from 1V to 1.4V. The pin offset voltage can be calculated as below:

$$V_{PIN-OFS} = V_{OFS} - 1.2V \quad (55)$$

For example, supplying 1.3V at RSET/OFS pin will achieve 100mV offset at the output.

Operation Mode Transition

The RT8885A supports operation mode transition function at the CORE VR for the SetPS command of Intel's VR12/IMVP7 CPU. The default operation mode of the CORE VR is PS0, which is full phase CCM operation. Other operation modes include PS1 (single phase CCM operation) and PS2 (single phase DEM operation).

After receiving SetPS command, the CORE VR will immediately change to the new operation state. When the CORE VR receives SetPS command of PS1 operation mode, the CORE VR operates as a single phase CCM controller, and only channel 1 is active. The CORE VR will disable phase 2 and phase 3 by disabling Internal PWM logic drivers at UGATE2 , LGATE2 and PWM3 pins (UGATE2 = 0V , LGATE2 = 0V , PWM3 = high impedance state). Therefore, the external driver which supports tri-state shutdown is required for compatibility with PS1 operation mode.

When the CORE VR receives SetPS command of PS2 operation mode, the CORE VR operates as a single phase DCM controller, and only channel 1 is active with diode emulation operation. The CORE VR will disable phase 2 and phase 3 by disabling Internal PWM logic drivers at UGATE2 , LGATE2 and PWM3 pins (UGATE2 = 0V , LGATE2 = 0V , PWM = high impedance state). Therefore, the external driver which support tri-state shutdown is required for compatibility with PS2 operation state.

If the CORE VR receives dynamic VID change command (SetVID), the CORE VR will automatically enter PS0 operation mode and all phases will be activated. After V_{OUT_CORE} reaches target voltage, the CORE VR will stay at PS0 state. VR will ignore any former SetPS command that CPU issues and asks CORE VR to be forced into PS1 or PS2 operation states during dynamic VID process.

Dynamic VID Enhancement

During a dynamic VID transition, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the setting time performance. In order to improve dynamic VID transition performance, the RT8885A provides internal™ DVID compensation function, as shown in Figure 16.

A switch (called DVID switch) turns on to observe sensed current when the controller is normal operation. During a dynamic VID transition, the switch turns off to hold sensed current to compensate the charging or discharging current effect. Therefore, the output voltage can be adjusted to the target value more quickly.

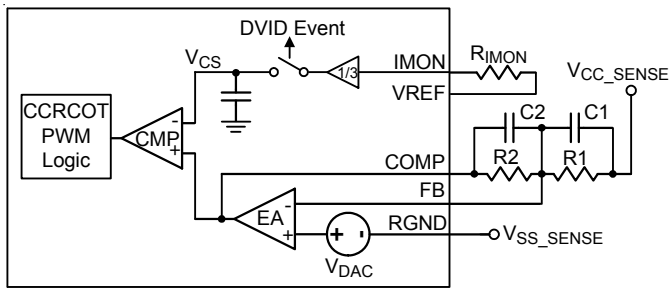


Figure 16. Internal™ DVID Compensation Function

Ramp Amplitude Adjust

When the CORE VR enters PS2 operation mode, the internal ramp of CORE VR will be modified for the reason of stability. In case of smooth transition into PS2, the CCM ramp amplitude should be designed properly. The RT8885A provides RSET pin for platform users to set the ramp amplitude of the CORE VR in CCM. The criterion is to set the ramp amplitude proportional to the on-time. The equation will be :

$$21.6\times10^{-7} = t_{ON}\times(V_{IN}-V_{DAC}) \times[1+(16-\text{Ramp Factor})\times2.95\%] \quad (56)$$

where 21.6 x 10^{-7} is an internal coefficient of analog circuit.

According to Equation 56 and Table 5, the ramp factor equation can be simplified to :

$$\text{Ramp Factor} = 16-\frac{\frac{8.85\times10^{4}}{R_{TON}}-1}{2.95\%} \quad (57)$$

Thermal Monitoring and Temperature Reporting

The CORE VR provides thermal monitoring function via sensing TSEN pin voltage. Through the voltage divider resistors, R1, R_{NTC}, R2, and R3, the voltage of TSEN will be proportional to VR temperature as shown in Figure 17. When VR temperature rises, TSEN voltage also rises. The ADC circuit of the CORE VR monitors the voltage variation at the TSEN pin from 1.4875V to 1.8725V with 55mV resolution. This voltage is then decoded into digital format and stored into Temperature_Zone register.

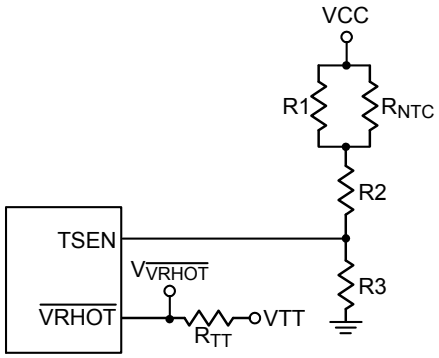


Figure 17. CORE VR : Thermal Monitoring Circuit

To meet Intel's VR12/IMVP7 specification, platform users have to set the TSEN voltage to meet the temperature variation of VR from 75% to 100% VR max temperature. For example, if the VR max temperature is 100°C, platform users have to set the TSEN voltage to be 1.5425V when VR temperature reaches 82°C and 1.8725V when VR temperature reaches 100°C. Detailed voltage setting versus temperature variation is shown in Table 8. The thermometer code is implemented in Temperature_Zone register.

Table 8. Temperature_Zone Register

$\overline{\text{VRHOT}}$	SVID Thermal Alert	Comparator Trip Points Temperatures Scaled to maximum = 100% Voltage Represents Assert bit Minimum Level					
b7	b6	b5	b4	b3	b2	b1	b0
100%	97%	94%	91%	88%	85%	82%	75%
1.8725V	1.8175V	1.7625V	1.7075V	1.6525V	1.5975V	1.5425V	1.4875V

The $\overline{\text{VRHOT}}$ pin is an open-drain structure that sends out active low $\overline{\text{VRHOT}}$ signal. When b6 of Temperature_Zone register asserts to 1 (when TSEN voltage rises above 1.8175V), the $\overline{\text{ALERT}}$ signal will be asserted to low, which is so-called SVID thermal alert. In the mean time, the CORE VR will assert bit 1 data to 1 in Status_1 register. The $\overline{\text{ALERT}}$ assertion will be de-asserted when b5 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSEN voltage falls under 1.7625V), and bit 1 of Status_1 register will also be cleared to 0. The bit 1 assertion of Status_1 is not latched and cannot be cleared by GetReg command. When b7 of Temperature_Zone register asserts to 1 (when TSEN voltage rises above 1.8725V), the $\overline{\text{VRHOT}}$ signal will be asserted to low. The $\overline{\text{VRHOT}}$ assertion will be de-asserted when b6 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSEN voltage falls under 1.8175V). It is typically recommended to connect a pull-up resistor from the $\overline{\text{VRHOT}}$ pin to a voltage source.

Quick Response

The RT8885A utilizes a quick response feature to support heavy load current demand during instantaneous load transient.

The controller monitors the abrupt VSEN pin voltage droop to trigger QR pulse generation circuit, as shown in Figure 18. At steady state, the VSEN pin voltage droop cannot trigger a quick response circuit. When this abrupt voltage droop is lower than the QR trigger threshold level, the QR circuit will be triggered. When quick response is triggered, the quick response circuit will generate a quick response pulse. The internal quick response pulse generation circuit is similar to the on-time generation circuit. After generating a quick response pulse, the pulse is then applied to the on-time generation circuit, and all the active phases' on-times will be overridden by the quick response pulse. Moreover, the quick response trigger threshold level, QR_TH, is set by VREF/QRTH pin, and the quick response pulse width, QR_TON, is set by SET1 pin. The detailed pins setting refers to the VREF/QRTH and SET1 pin setting section.

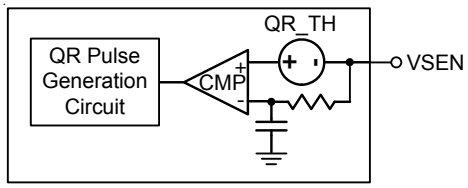


Figure 18. CORE VR : Quick Response Triggering Circuit

Over Current Protection

The RT8885A provides summed total over current and per phase over current protections.

The controller determines summed total over current protection SUM_OCP by comparing the I_{IMON} with SUM_OCP threshold whose setting refers to the OCSET pin setting section. It declares SUM_OCP when I_{IMON} is above the SUM_OCP threshold for 40µs. When I_{IMON} is above the SUM_OCP threshold for 40µs, it declares SUM_OCP. Therefore, latched SUM_OCP forces PWM into high impedance, which disables internal PWM logic drivers. Moreover, the GFX VR will also enter soft shut down sequence.

The controller monitors either phase I_{SENxN} current to determine per phase over current protection PH_OCP. If either phase I_{SENxN} current is greater than PH_OCP threshold for 100ns, the controller will declare fault and PH_OCP latches off. Therefore, latched SUM_OCP forces PWM into high impedance, which disables internal PWM logic drivers. Moreover, the GFX VR will also enter soft shut down sequence.

Over Voltage Protection (OVP)

The over voltage protection circuit of the CORE VR monitors the output voltage via the VSEN pin after EN. The supported maximum operating VID of the VR ($V_{(MAX)}$) is stored in the VOUT_Max register. If pin offset function is enabled, the OVP threshold will be VMAX value plus 450mV. If not the OVP threshold will be VMAX value plus 150mV. Once V_{OUT_CORE} exceeds OVP threshold, OVP is triggered and latched. The CORE VR will try to turn on low side MOSFETs and turn off high side MOSFETs of all active phases of the CORE VR to protect the CPU. When OVP is triggered by the CORE VR, the GFX VR will also enter soft shut down sequence. A 1μs delay is used in OVP detection circuit to prevent false trigger. OVP detection circuit will have a 1μs trigger delay which can prevent false trigger caused by any glitches. And only VCC re-power or POR reset can release OVP latch.

Negative Voltage Protection (NVP)

During OVP latch state, the CORE VR also monitors the VSEN pin for negative voltage protection. Since the OVP latch continuously turns on all low side MOSFETs of the CORE VR, the CORE VR may suffer negative output voltage which is mainly caused by negative inductor current. As a consequence, when the VSEN voltage drops below –50mV after triggering OVP, the CORE VR will trigger NVP to turn off all low side MOSFETs of the CORE VR while the high side MOSFETs still remains off. After triggering NVP, if the output voltage rises above 0V, the NVP latch will be released and turn on all low side MOSFETs due to OVP is still asserted. A 1μs trigger delay is used in NVP detection circuit to prevent false trigger.

Under Voltage Protection (UVP)

The CORE VR implements under voltage protection of V_{OUT_CORE}. If pin offset function is enabled, the UVP threshold will be VID minus 500mV. If not the OVP threshold will be VID minus 400mV. Once V_{OUT_CORE} is less than the UVP threshold, the CORE VR will trigger UVP latch. The UVP latch will turn off both high side and low side MOSFETs. When UVP is triggered by the CORE VR, the GFX VR will also enter soft shut down sequence. A 3μs trigger delay is used in UVP detection circuit to prevent false trigger. And only VCC re-power or POR reset can release UVP latch.

Under Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below POR threshold, the CORE VR will trigger UVLO. The UVLO protection forces all high side MOSFETs and low side MOSFETs off by shutting down internal PWM logic drivers. A 3μs trigger delay is used in UVLO detection circuit to prevent false trigger.

GFX VR

Active Phase Determination : Before EN

The number of active phases is determined by the internal circuitry that monitors the ISENAxN voltages during start-up. Normally, the GFX VR operates as a 2-phase PWM controller. Setting ISENA2N to VCC before power-on can program a 1-phase operation, and pulling ISENA1N, and setting ISENA2N to VCC before power-on can disable GFX VR operation. Before EN, GFX VR detects whether the voltages of ISENA1N and ISENA2N are higher than "VCC – 0.5V" respectively to decide how many phases should be active. Phase selection is only active during EN. When EN = high, the number of active phases is determined and latched. The unused ISENAxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

Loop Control

The GFX VR adopts Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The output voltage, V_{OUT_GFX} will decrease with increasing output load current. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 19.

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases, V_{CS} increases, the steady state COMPA voltage also increases and induces V_{OUT_GFX} to decrease, thus achieving AVP. A near-DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller.

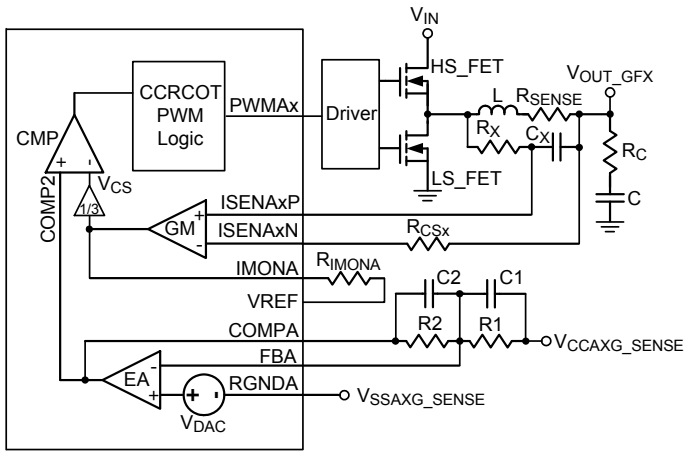


Figure 19. GFX VR : Simplified Schematic for Droop and Remote Sense in CCM

TONA Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure 20 shows the On-Time setting Circuit. Connect a resistor (R_{TONA}) between V_{IN_GFX} and TONSETA to set the on-time of UGATE :

$$t_{ON}\ (0.5V < V_{DAC} < 1.2V) = \frac{24.4 \times 10^{-12} \times R_{TONA}}{V_{IN} - V_{DAC}} \quad (58)$$

where t_{ON} is the UGATE turn on period, V_{IN_GFX} is the input voltage of the GFX VR, and V_{DAC} is the DAC voltage.

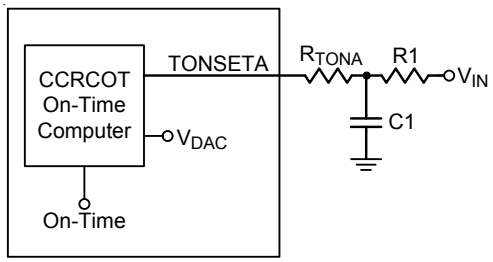


Figure 20. GFX VR : On-Time Setting with RC Filter

When V_{DAC} is larger than 1.2V, the equivalent switching frequency may be over 500kHz, and this too fast switching frequency is unacceptable. Therefore, the GFX VR implements a pseudo constant frequency technology to avoid this disadvantage of CCRCOT topology. When V_{DAC} is larger than 1.2V, the on-time equation will be modified to :

$$t_{ON}\ (V_{DAC} > 1.2V) = \frac{20.33 \times 10^{-12} \times R_{TONA} \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (59)$$

On-time translates only roughly to switching frequencies. For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{SW(MAX)} \cong \frac{1}{(t_{ON} - 60ns) + \left(\frac{IccTDC}{N} \times R_{ON\_LS-FET(MAX)}\right) \times 50ns} \times \frac{V_{DAC\_PS0} + \frac{IccTDC}{N} \times \left(DCR + R_{ON\_LS-FET(MAX)} - N \times R_{DROOP}\right)}{\left[V_{IN(MAX)} + \frac{I_{CC}TDC}{N} \times \left(R_{ON\_LS-FET(MAX)} - R_{ON\_HS-FET(MAX)}\right)\right]} \quad (60)$$

where $f_{S(MAX)}$ is the maximum switching frequency, V_{DAC_PS0} is the test VID of application at PS0 for turbo mode or HFM, $V_{IN(MAX)}$ is the maximum application input voltage, IccTDC is the thermal design current of application, N is the phase number, $R_{ON\_HS-FET(MAX)}$ is the maximum equivalent high side FET $R_{DS(ON)}$, $R_{ON\_LS-FET(MAX)}$ is the maximum equivalent low side FET $R_{DS(ON)}$, DCR is the inductor DCR, and R_{DROOP} is the load line setting.

Current Sense Setting

The current sense topology of the GFX VR is continuous inductor current sensing. Therefore, the controller has less noise sensitive. Low offset amplifiers are used for current balance, loop control and over current detection. The ISENAxP and ISENAxN pins denote the positive and negative input of the current sense amplifier of each phase.

Users can either use a current-sense resistor or the inductor's DCR for current sensing. Using the inductor's DCR allows higher efficiency as shown in Figure 21.

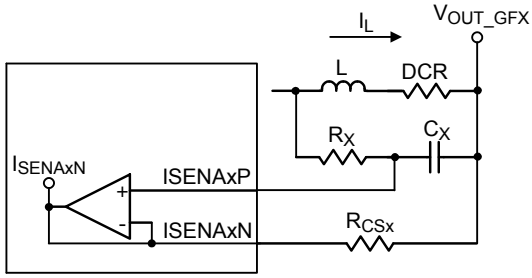


Figure 21. GFX VR : Lossless Inductor Sensing

In order to optimize transient performance, R_X and C_X must be set according to the equation below :

$$\frac{L}{DCR} = R_X \times C_X \quad (61)$$

Then the proportion between the phase current I_L and the sensed current I_{SENAxN} can be described as below :

$$I_{SENAxN} = I_L \times \frac{DCR}{R_{CSx}} \quad (62)$$

where R_{CSx} is only an exact 680Ω sense resistor. The resistance accuracy of R_{CSx} is recommended to be 1% or higher.

In addition to considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load line requirement and the recovery is too fast causing a ring back. Vice versa, with a resistance too large the output voltage transient has only a small initial dip with a slow recovery.

Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the above mentioned inductor DCR sensing method.

Current Monitoring and Current Reporting

The RT8885A provides the current monitor function for GFX VR. IMONA pin reports GFX VR inductor current.

The IMONA pin outputs a high-speed analog current source that is 1 time of the summed current. Thus I_{IMONA} can be described as below :

$$I_{IMONA} = \sum I_{SENAxN} \quad (63)$$

The RT8885A monitors the IMONA pin voltage and considers that GFX VR has reached ICCMAXA when IMONA pin voltage is 2.392V.

As Figure 19 show, a resistor R_{IMONA} is connected between the IMONA pin and VREF pin. Through the R_{IMONA} to convert the IMONA pin current to voltage. The voltage of IMONA pin is expressed in Equation 64 :

$$V_{IMONA} = I_{IMONA} \times R_{IMONA} + 0.6 \quad (64)$$

Rewriting Equations 62 and 63 gives Equation 65 :

$$I_{IMONA} = \frac{DCR}{R_{CSx}} \times I_{LOAD} \quad (65)$$

Substitution of Equation 65 into Equation 64 gives Equation 66 :

$$V_{IMONA} = \frac{DCR}{R_{CSx}} \times I_{LOAD} \times R_{IMONA} + 0.6 \quad (66)$$

Rewriting Equation 66 and application of full load condition gives Equation 67 :

$$R_{IMONA} = \frac{R_{CSx}}{DCR} \times \frac{(V_{IMONA} - 0.6)}{I_{LOAD}} \quad (67)$$

For example, given R_{CSx} = 680Ω, DCR = 0.82mΩ, V_{IMONA} = 2.392V at $I_{LOAD(MAX)}$ = 53A, Equation 65 gives R_{IMONA} = 28kΩ.

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the IMONA resistor network with temperature compensation for GFX VR.

Droop Setting

It's very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. This target is to have

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{DROOP} \quad (68)$$

Then solving the switching condition V_{COMP2} = V_{CS} in Figure 19 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{G_I}{R_{DROOP}} \quad (69)$$

where R_{DROOP} is the equivalent load line resistance as well as the desired static output impedance.

The summed current sense gain G_I as

$$G_I = \frac{R_{SENSE}}{R_{CSx}} \times R_{IMONA} \times \frac{1}{3} \quad (70)$$

where R_{SENSE} is the current-sense resistor. If no external sense resistor present, it is the DCR of the inductor. R_{CSx} is the sense resistor. R_{IMONA} is the equivalent resistance of temperature dependent resistor.

Droop Disable

Refer to the TSENA pin setting section, disabling the GFX VR droop can be set by platform users through the TSENA pin.

Loop Compensation

Optimized compensation of the GFX VR allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for proper compensation. Figure 19 shows the

compensation circuit. Prior design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_p = \frac{1}{2\pi \times C \times R_C} \quad (71)$$

where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (72)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \quad (73)$$

Differential Remote Sense Setting

The GFX VR includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. Figure 22 shows the GFX VR differential remote voltage sense connection. The CPU contains on-die sense pins, V_{CCAXG_SENSE} and V_{SSAXG_SENSE}. Connect RGNDA to V_{SSAXG_SENSE}. Connect FBA to V_{CCAXG_SENSE} with a resistor to build the negative input path of the error amplifier. The V_{DAC} and the precision voltage reference are referred to RGNDA for accurate remote sensing.

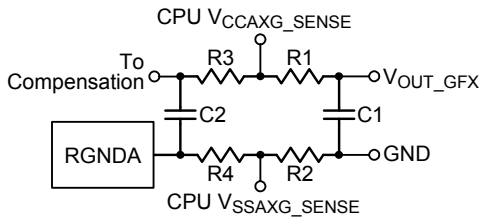


Figure 22. GFX VR : Differential Remote Voltage Sense Connection

Current Balance

The GFX VR implements internal current balance mechanism in the current loop. The GFX VR senses and compares per-phase current signal with average current. If the sensed current of any particular phase is larger than average current, the on-time of this phase will be adjusted to be shorter.

No Load Offset (SVID & Platform)

The GFX VR features no load offset function which provides the possibility of wide range positive offset of output voltage. The no-load offset function can be implemented through the SVID interface or RSETA/OFSA pin. Users can disable pin offset function by simply connecting RSETA/OFSA pin to GND. The RT8885A will latch the RSETA/OFSA status after EN goes high.

If pin offset function is enabled, then the output voltage is

$$V_{OUT\_GFX} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{SVID-OFS} + V_{PIN-OFS} \quad (74)$$

If not the output voltage is

$$V_{OUT\_GFX} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{SVID-OFS} \quad (75)$$

The pin offset voltage is set by the divider voltage on RSETA/OFSA pin. The linear range of offset pin voltage is from 1V to 1.4V. The pin offset voltage can be calculated as below :

$$V_{PIN-OFS} = V_{OFS} - 1.2V \quad (76)$$

For example, supplying 1.3V at RSETA/OFSA pin will achieve 100mV offset at the output.

Operation Mode Transition

The RT8885A supports operation mode transition function at the GFX VR for the SetPS command of Intel's VR12/ IMVP7 CPU. The default operation mode of the GFX VR is PS0, which is full phase CCM operation. Other operation modes includes PS1 (single phase CCM operation) and PS2 (single phase DEM operation).

After receiving SetPS command, the GFX VR will immediately change to the new operation state. When the GFX VR receives SetPS command of PS1 operation mode, the GFX VR operates as a single phase CCM controller, and only channel 1 is active. The GFX VR will disable PWMA2 pins. Therefore, the external driver which supports tri-state shutdown is required for compatibility with PS1 operation mode.

When the GFX VR receives SetPS command of PS2 operation mode, the GFX VR operates as a single phase

DCM controller, and only channel 1 is active with diode emulation operation. The GFX VR will disable PWMA2 pins. Therefore, the external driver which supports tri-state shutdown is required for compatibility with PS2 operation state.

If the GFX VR receives dynamic VID change command (SetVID), the GFX VR will automatically enter PS0 operation mode and all phases will be activated. After V_{OUT_GFX} reaches target voltage, the GFX VR will stay at PS0 state. VR will ignore any former SetPS command that CPU issues and asks GFX VR to be forced into PS1 or PS2 operation states during dynamic VID process.

Dynamic VID Enhancement

During a dynamic VID transition, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the setting time performance. In order to improve dynamic VID transition performance, the RT8885A provides internal™ DVID compensation function, as shown in Figure 23.

A switch (called DVID switch) turns on to observe sensed current when the controller is normal operation. During a dynamic VID transition, the switch turns off to hold sensed current to compensate the charging or discharging current effect. Therefore, the output voltage can be adjusted to the target value more quickly.

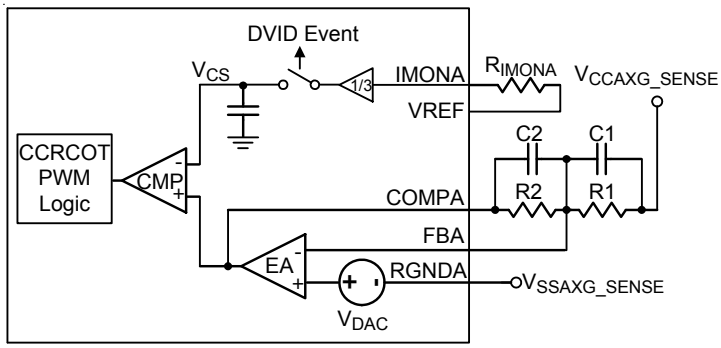


Figure 23. Internal™ DVID Compensation Function

Ramp Amplitude Adjust

When the GFX VR enters PS2 operation mode, the internal ramp of GFX VR will be modified for the reason of stability. In case of smooth transition into PS2, the CCM ramp amplitude should be designed properly. The RT8885A provides RSETA pin for platform users to set the ramp amplitude of the GFX VR in CCM. The criterion is to set the ramp amplitude proportional to the on-time. The equation will be :

$$21.6\times10^{-7} = t_{ON}\times(V_{IN}-V_{DAC}) \times[1+(16-\text{Ramp Factor})\times2.95\%] \quad (77)$$

where 21.6×10^{-7} is an internal coefficient of analog circuit.

According to Equation 77 and Table 6, the Ramp Factor equation can be simplified to :

$$\text{Ramp Factor} = 16-\frac{\frac{8.85\times10^{4}}{R_{TONA}}-1}{2.95\%} \quad (78)$$

Thermal Monitoring and Temperature Reporting

The GFX VR provides thermal monitoring function via sensing TSENA pin voltage. Through the voltage divider resistors, R1, R_{NTC}, R2, and R3, the voltage of TSENA will be proportional to VR temperature as shown in Figure 24. When VR temperature rises, TSENA voltage also rises. The ADC circuit of the GFX VR monitors the voltage variation at the TSENA pin from 1.4875V to 1.8725V with 55mV resolution. This voltage is then decoded into digital format and stored into Temperature_Zone register.

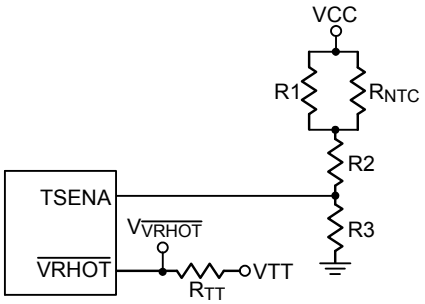


Figure 24. GFX VR : Thermal Monitoring Circuit

To meet Intel's VR12/IMVP7 specification, platform users have to set the TSENA voltage to meet the temperature variation of VR from 75% to 100% VR max temperature. For example, if the VR max temperature is 100°C, platform users have to set the TSENA voltage to be 1.5425V when VR temperature reaches 82°C and 1.8725V when VR temperature reaches 100°C. Detailed voltage setting versus temperature variation is shown in Table 9. The thermometer code is implemented in Temperature_Zone register.

Table 9. Temperature_Zone Register

$\overline{\text{VRHOT}}$	SVID Thermal Alert	Comparator Trip Points Temperatures Scaled to maximum = 100% Voltage Represents Assert bit Minimum Level					
b7	b6	b5	b4	b3	b2	b1	b0
100%	97%	94%	91%	88%	85%	82%	75%
1.8725V	1.8175V	1.7625V	1.7075V	1.6525V	1.5975V	1.5425V	1.4875V

The $\overline{\text{VRHOT}}$ pin is an open-drain structure that sends out active low $\overline{\text{VRHOT}}$ signal. When b6 of Temperature_Zone register asserts to 1 (when TSENA voltage rises above 1.8175V), the $\overline{\text{ALERT}}$ signal will be asserted to low, which is so-called SVID thermal alert. In the mean time, the GFX VR will assert bit 1 data to 1 in Status_1 register. The $\overline{\text{ALERT}}$ assertion will be de-asserted when b5 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSENA voltage falls under 1.7625V), and bit 1 of Status_1 register will also be cleared to 0. The bit 1 assertion of Status_1 is not latched and cannot be cleared by GetReg command. When b7 of Temperature_Zone register asserts to 1 (when TSENA voltage rises above 1.8725V), the $\overline{\text{VRHOT}}$ signal will be asserted to low. The $\overline{\text{VRHOT}}$ assertion will be de-asserted when b6 of Temperature_Zone register is de-asserted from 1 to 0 (which means TSENA voltage falls under 1.8175V). It is typically recommended to connect a pull-up resistor from the $\overline{\text{VRHOT}}$ pin to a voltage source.

Quick Response

The RT8885A utilizes a quick response feature to support heavy load current demand during instantaneous load transient.

The controller monitors the abrupt VSENA pin voltage droop to trigger QR pulse generation circuit, as shown in Figure 25. At steady state, the VSENA pin voltage droop cannot trigger a quick response circuit. When this abrupt voltage droop is lower than the QR trigger threshold level, the QR circuit will be triggered. When quick response is triggered, the quick response circuit will generate a quick response pulse. The internal quick response pulse generation circuit is similar to the on-time generation circuit. After generating a quick response pulse, the pulse is then applied to the on-time generation circuit, and all the active phases' on-times will be overridden by the quick response pulse. Moreover, the quick response trigger threshold level, QR_TH, is set by VREF/QRTH pin, and the quick response pulse width, QR_TON, is set by SET2 pin. The detailed pins setting refers to the VREF/QRTH and SET2 pin setting section.

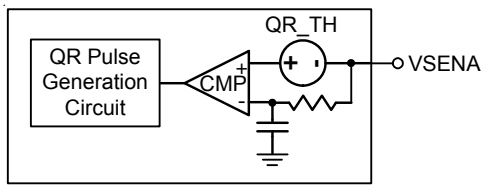


Figure 25. GFX VR : Quick Response Triggering Circuit

Over Current Protection

The RT8885A provides summed total over current and per phase over current protections.

The controller determines summed total over current protection SUM_OCP by comparing the I_{IMONA} with SUM_OCP threshold whose setting refers to the OCSET pin setting section. It declares SUM_OCP when I_{IMONA} is above the SUM_OCP threshold for 40µs. When I_{IMONA} is above the SUM_OCP threshold for 40µs, it declares SUM_OCP. Therefore, latched SUM_OCP forces PWM into high impedance, which disables internal PWM logic drivers. Moreover, the GFX VR will also enter soft shut down sequence.

The controller monitors either phase I_{SENAxN} current to determine per phase over current protection PH_OCP. If either phase I_{SENAxN} current is greater than PH_OCP threshold for 100ns, the controller will declare fault and PH_OCP latches off. Therefore, latched SUM_OCP forces PWM into high impedance, which disables internal PWM logic drivers. Moreover, the CORE VR will also enter soft shut down sequence.

Over Voltage Protection (OVP)

The over voltage protection circuit of the GFX VR monitors the output voltage via the VSENA pin after EN. The supported maximum operating VID of the VR ($V_{(MAX)}$) is

stored in the VOUT_Max register. If pin offset function is enabled, the OVP threshold will be VMAX value plus 450mV. If not the OVP threshold will be VMAX value plus 150mV. Once V_{OUT_GFX} exceeds OVP threshold, OVP is triggered and latched. The GFX VR will try to turn on low side MOSFETs and turn off high side MOSFETs of all active phases of the GFX VR to protect the CPU. When OVP is triggered by the GFX VR, the CORE VR will also enter soft shut down sequence. A 1μs delay is used in OVP detection circuit to prevent false trigger. OVP detection circuit will have a 1μs trigger delay which can prevent false trigger caused by any glitches. And only VCC re-power or POR reset can release OVP latch.

Negative Voltage Protection (NVP)

During OVP latch state, the GFX VR also monitors the VSENA pin for negative voltage protection. Since the OVP latch continuously turns on all low side MOSFETs of the GFX VR, the GFX VR may suffer negative output voltage which is mainly caused by negative inductor current. As a consequence, when the VSENA voltage drops below –50mV after triggering OVP, the GFX VR will trigger NVP to turn off all low side MOSFETs of the GFX VR while the high side MOSFETs still remains off. After triggering NVP, if the output voltage rises above 0V, the NVP latch will be released and turn on all low side MOSFETs due to OVP is still asserted. A 1μs trigger delay is used in NVP detection circuit to prevent false trigger.

Under Voltage Protection (UVP)

The GFX VR implements under voltage protection of V_{OUT_GFX}. If pin offset function is enabled, the UVP threshold will be VID minus 500mV. If not the OVP threshold will be VID minus 400mV. Once V_{OUT_GFX} is less than the UVP threshold, the GFX VR trigger UVP latch. The UVP latch will turns off both high side and low side MOSFETs. When UVP is triggered by the GFX VR, the CORE VR will also enter soft shut down sequence. A 3μs trigger delay is used in UVP detection circuit to prevent false trigger. And only VCC re-power or POR reset can release UVP latch.

Under Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below POR threshold, the GFX VR will trigger UVLO. The UVLO protection forces all high side MOSFETs and low side MOSFETs off by shutting down internal PWM logic drivers. A 3μs trigger delay is used in UVLO detection circuit to prevent false trigger.

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{I_{Ripple(MAX)}} \times T_{ON} \quad (79)$$

where t_{ON} is the UGATE turn-on period.

Higher inductance yields less ripple current and hence higher efficiency. The downside is a slower transient response of the power stage to load transients. This might increase the need for more output capacitors, thus driving up the cost. Select a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to be saturated at the peak inductor current.

Output Capacitor Selection

Output capacitors are used to obtain high bandwidth for the output voltage beyond the bandwidth of the converter itself. Usually, the CPU manufacturer recommends a capacitor configuration. Two different kinds of output capacitors are typically used : bulk capacitors closely located next to the inductors, and ceramic output capacitors in close proximity to the load. Latter ones are for mid-frequency decoupling with especially small ESR and ESL values, while the bulk capacitors have to provide stored energy enough to overcome the low frequency bandwidth gap between the regulator and the CPU.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8885A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-56L 7x7 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.226W for WQFN-56L 7x7 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance, θ_{JA}. For RT8885A package, the derating curve in Figure 26 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

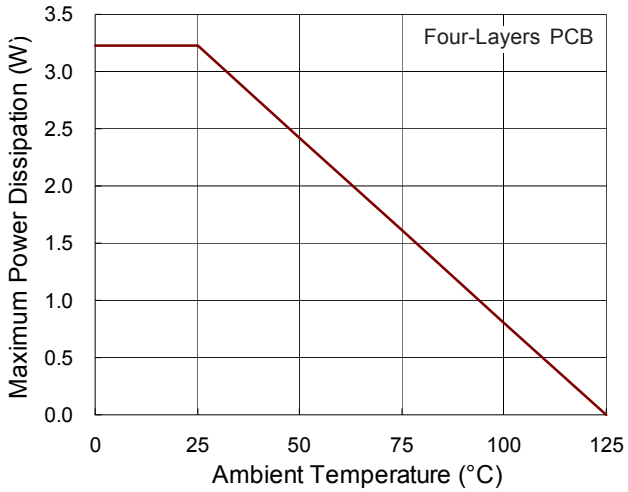


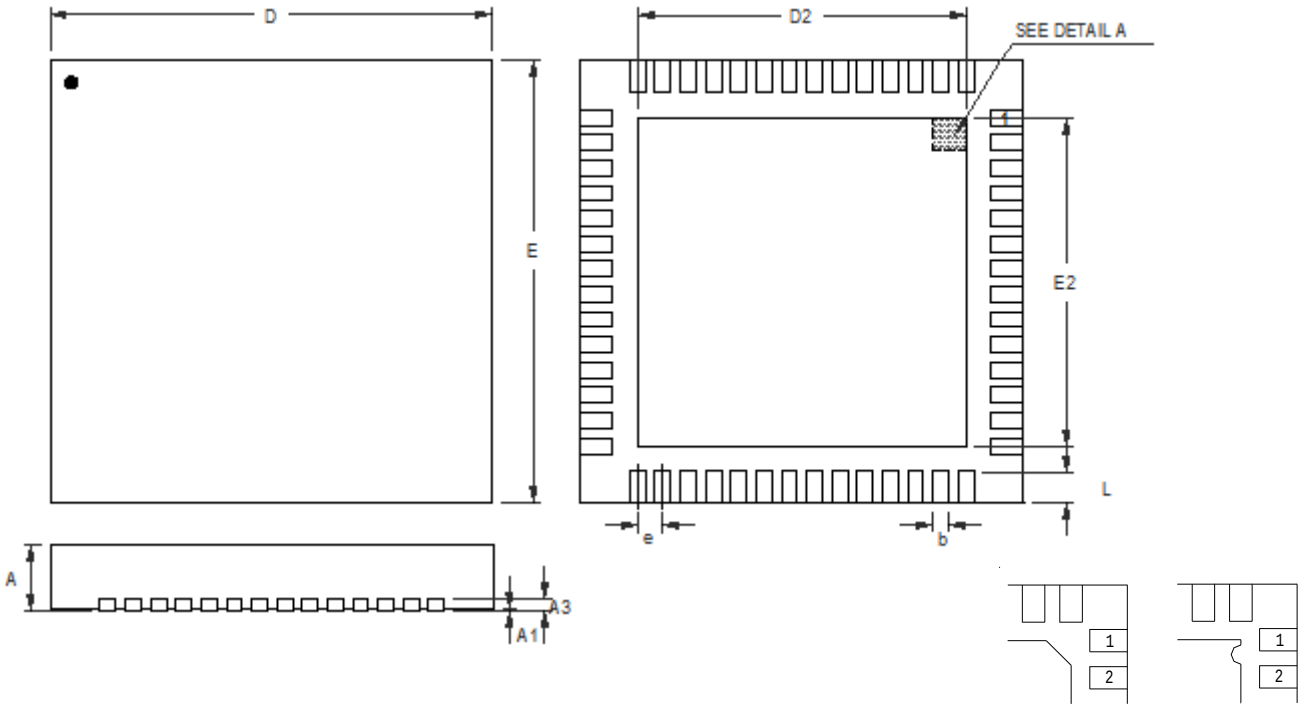
Figure 26. Derating Curve for RT8885A Package

Layout Considerations

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for optimum PC board layout :

- Keep the high current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- When trade-offs in trace lengths must be made, it's preferable to let the inductor charging path be longer than the discharging path.
- Place the current sense component close to the controller. ISENxP and ISENxN connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee current sense accuracy. The PCB trace from the sense nodes should be paralleled back to the controller.
- Route high speed switching nodes away from sensitive analog areas (COMP, FB, ISENxP, ISENxN, etc...)

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.150	5.250	0.203	0.207
E	6.900	7.100	0.272	0.280
E2	5.150	5.250	0.203	0.207
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 56L QFN 7x7 Package

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