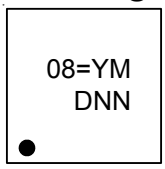
10-Channel High Voltage Level Shifter

General Description

The RT8910A provides a 10-Channel level shifter suitable for TFT-LCD row drivers. It level shifts a digital input signal to an output voltage nearly equal to its output supply voltages. The level shifter has 3 supplies : VGH1 and VGH2 are positive supplies and VGL is the negative supply. Fast rising/falling time and low propagation delay makes it suitable for driving TFT-LCD panel.

RT8910A is available in a WQFN-28L 4x5 package.

Marking Information



08= : Product Code

YMDNN : Date Code

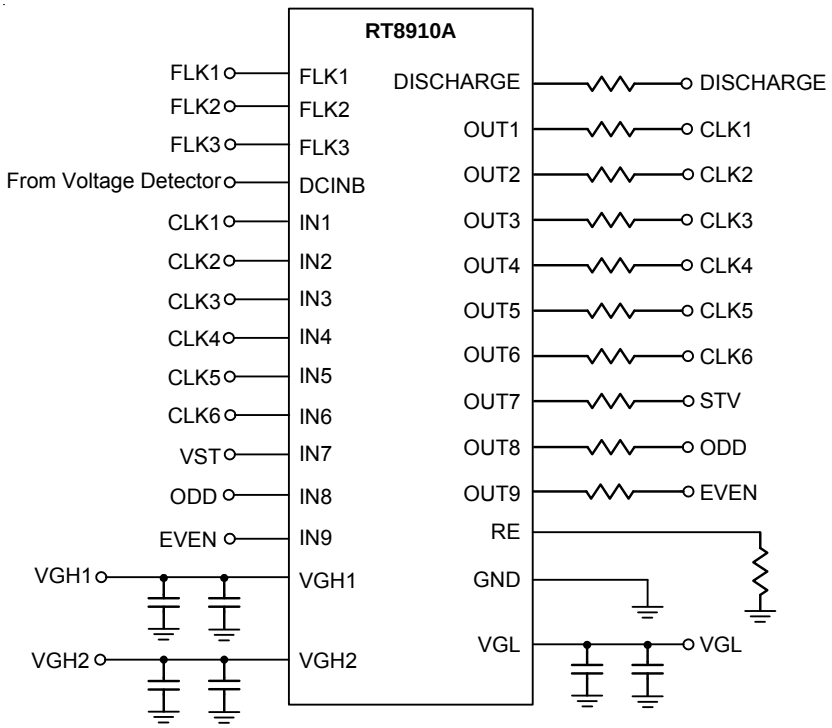
Features

- **2.5V to 5V Input Logic Level Range**
- **–12V to 38V Output Voltage Range**
- **Propagation Delay 55ns**
- **6-Channel (OUT1 to OUT6) Level Shifter with GPM Function for CLK**
- **1-Channel Level Shifter for DISCHARGE**
- **1-Channel (OUT7) Level Shifter for STV**
- **2-Channel (OUT8, OUT9) Level Shifter for ODD and EVEN**
- **Separate VGH for DISCHARGE, OUT1 to OUT7 and OUT8, OUT9**
- **Panel DISCHARGE Function**
- **Thin 28-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- IPS TFT-LCD TV Panel

Simplified Application Circuit



Ordering Information

RT8910A □ □

- Package Type
  QW : WQFN-28L 4x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

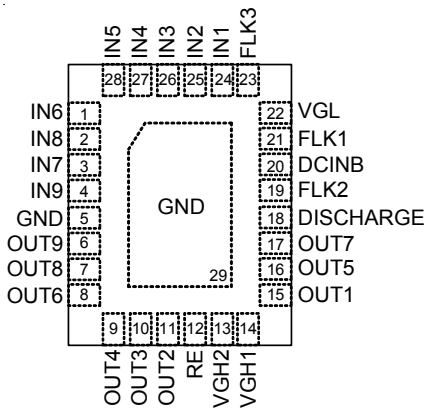
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

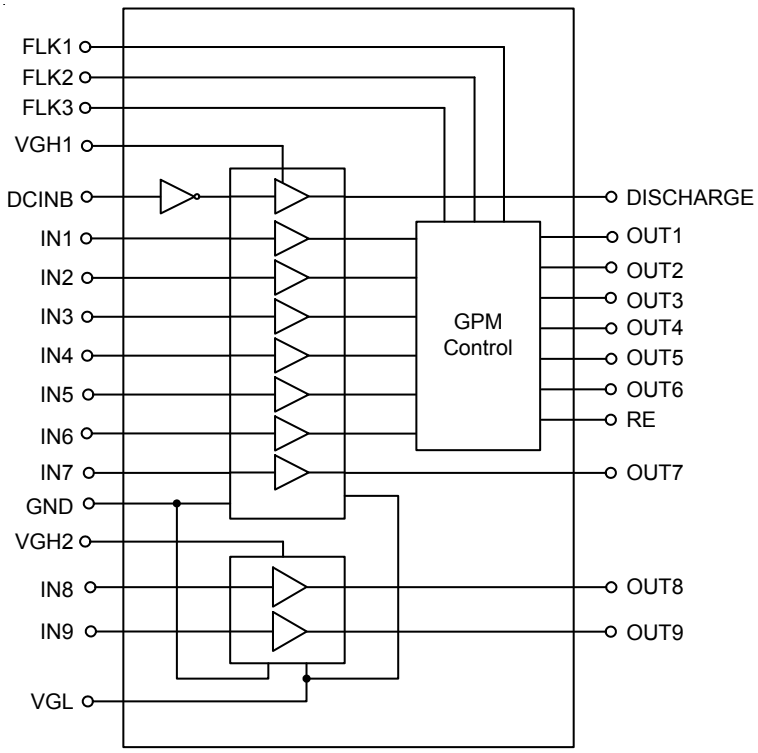


WQFN-28L 4x5

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2, 3, 4, 24 to 28	IN6, IN8, IN7, IN9, IN1 to IN5	Level Shifter Inputs for Channels 1 to 9.
5, 29 (Exposed Pad)	GND	Analog Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6, 7, 8, 9 to 11, 15, 16, 17	OUT9, OUT8, OUT6, OUT4 to OUT2, OUT1, OUT5, OUT7	Level Shifter Outputs for Channels 9 to 1.
12	RE	GPM Shaping Resistor Connection.
13	VGH2	Positive Supply Voltage for Level Shifter Channels 8 and 9.
14	VGH1	Positive Supply Voltage for Level Shifter Channels 1 to 7 and DISCHARGE.
18	DISCHARGE	Level Shifter Output for Discharging.
19	FLK2	GPM Timing Clock Input 2.
20	DCINB	Panel Discharge Voltage. Connect this pin to GND, if not used.
21	FLK1	GPM Timing Clock Input 1.
22	VGL	Negative Supply Voltage for Level Shifter All Channels.
23	FLK3	GPM Timing Clock Input 3.

Function Block Diagram



Operation

GPM Function

OUT1 to OUT6 of the level shifter support GPM function. The GPM is controlled by the three FLK signals from timing controller to modulate the Gate-On voltage. The level shifter output can be modulated from VGH to the RE voltage on the falling edge of the FLK signal if and only if the level shifter input is high. Figure 1 shows the GPM function timing diagram.

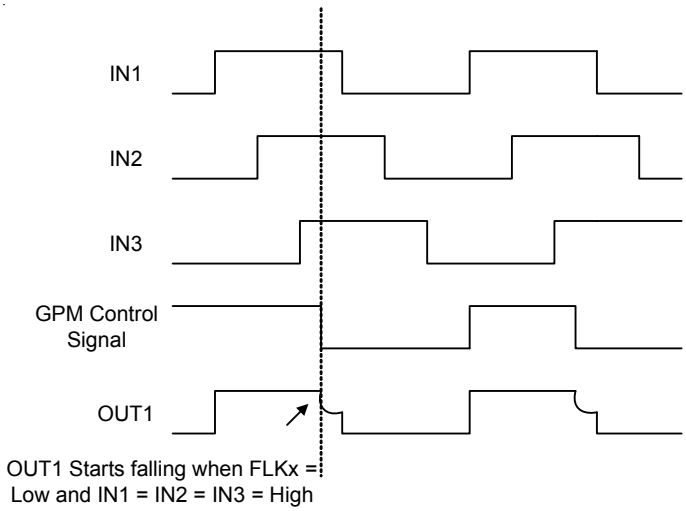


Figure 1. GPM Function Timing Diagram

Absolute Maximum Ratings (Note 1)

- VGL to GND ---------- 0.3V to –30V
- FLKx, INx, DCINB to GND ---------- –0.3V to 6V
- VGHx to VGL ---------- –0.3V to 45V
- RE to GND ---------- –0.3V to (VGH1 + 0.3V)
- OUT1 to OUT7, DISCHARGE to VGL ---------- –0.3V to (VGH1 + 0.3V)
- OUT8, OUT9 to VGL ---------- –0.3V to (VGH2 + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-28L 4x5 ---------- 3.57W
- Package Thermal Resistance (Note 2)
  WQFN-28L 4x5, θ_{JA} ---------- 28°C/W
  WQFN-28L 4x5, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{GHx} = 30V, V_{GL} = –6.2V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
High Voltage Level Shifter							
VGH1, VGH2 Operating Voltage Range				12	--	38	V
VGL Operating Voltage Range				–12	--	–2	V
(VGH1, VGH2) – VGL				–	--	40	V
Input Voltage	Logic-High	V_{IH}		1.7	--	--	V
	Logic-Low	V_{IL}		–	--	0.4	
Input Leakage Current		I_{IL}	INx = FLKx = DCINB = 0V or 5.5V	–1	--	1	μA
Propagation Delay		t_{PLH}	OUTx Rising	–	50	--	ns
		t_{PHL}	OUTx Falling	–	50	--	ns
RE to OUT1 to OUT6 Switch On-Resistance		$R_{DS(ON)}$		–	65	--	Ω
Operation Frequency				–	--	100	kHz

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VGH1 Quiescent Current		I_{VGH1}	No Load	--	720	--	μA
VGH2 Quiescent Current		I_{VGH2}	No Load	--	120	--	μA
VGL Quiescent Current		I_{VGL}	V_{IN} = 0 or 6V, No Load	--	570	--	μA
CLK (OUT1 to OUT6) Channel	Rising Time	t_R	C_{LOAD} = 4.7nF (Note5)	--	--	450	ns
	Falling Time	t_F		--	--	120	
VST (OUT7) Channel	Rising Time	t_R	C_{LOAD} = 0.22nF (Note5)	--	--	60	ns
	Falling Time	t_F		--	--	30	
VDD E/O (OUT8, OUT9) Channel	Rising Time	t_R	C_{LOAD} = 1nF (Note5)	--	--	300	ns
	Falling Time	t_F		--	--	60	
DISCHARGE Channel	Rising Time	t_R	C_{LOAD} = 560pF (Note5)	--	--	300	ns
	Falling Time	t_F		--	--	150	

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

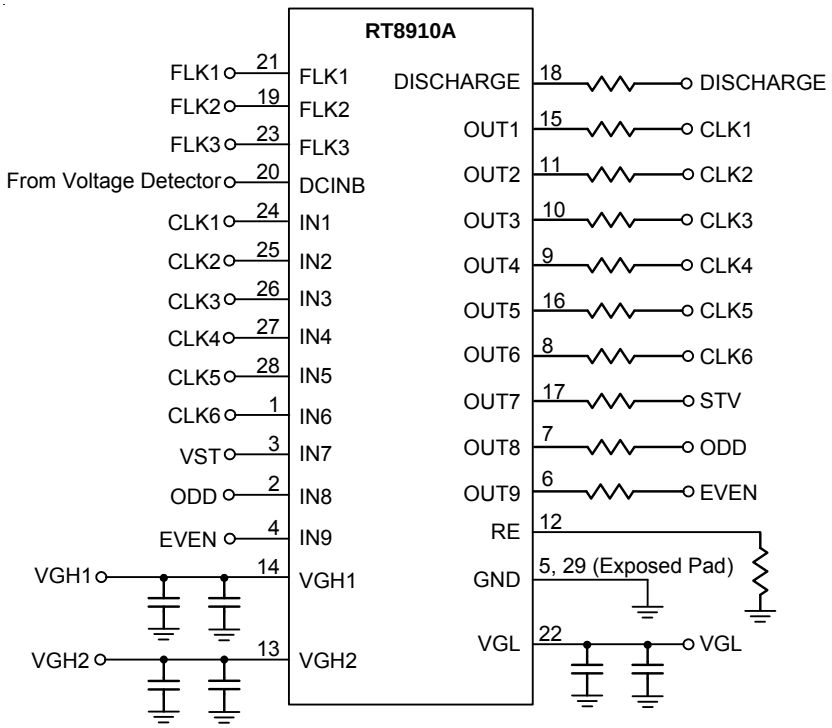
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

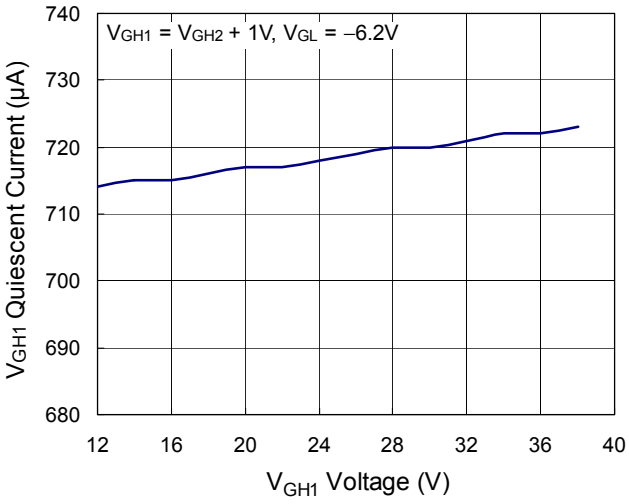
Note 5. Level shifter C_{LOAD} condition.

Typical Application Circuit

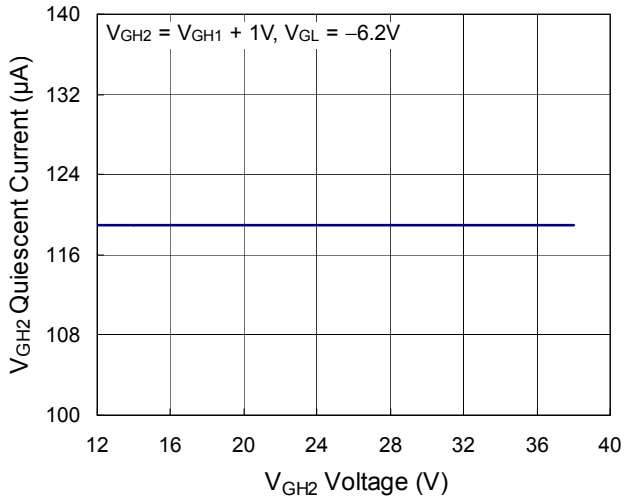


Typical Operating Characteristics

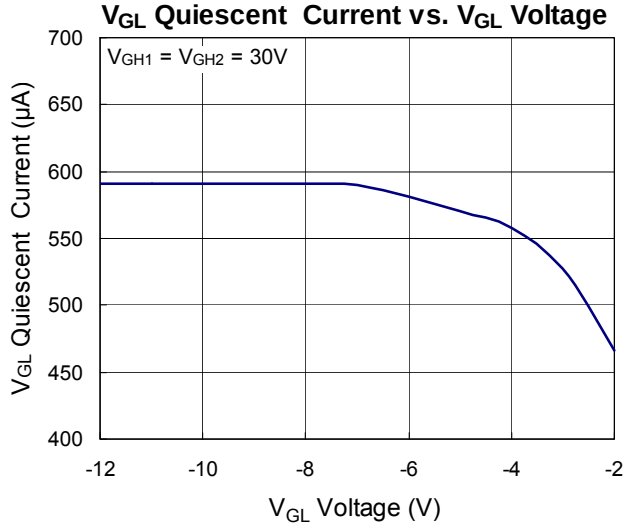
V_{GH1} Quiescent Current vs. V_{GH1} Voltage



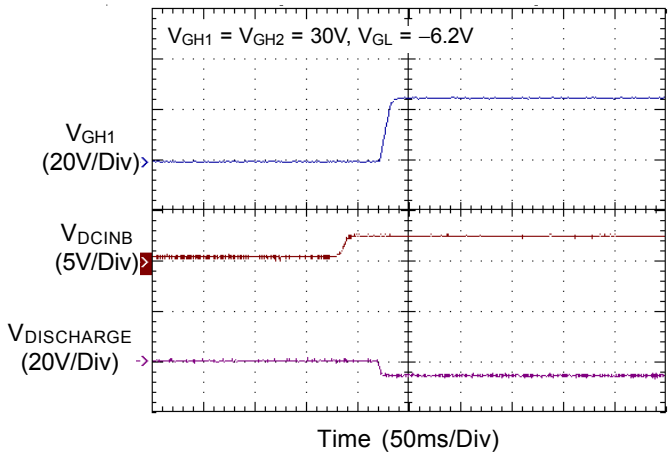
V_{GH2} Quiescent Current vs. V_{GH2} Voltage



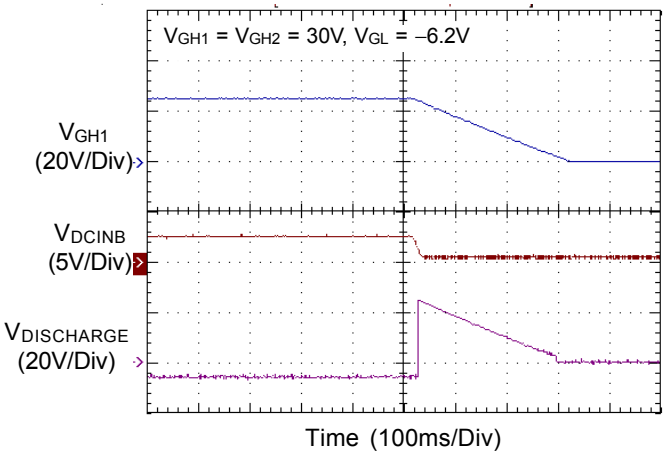
V_{GL} Quiescent Current vs. V_{GL} Voltage



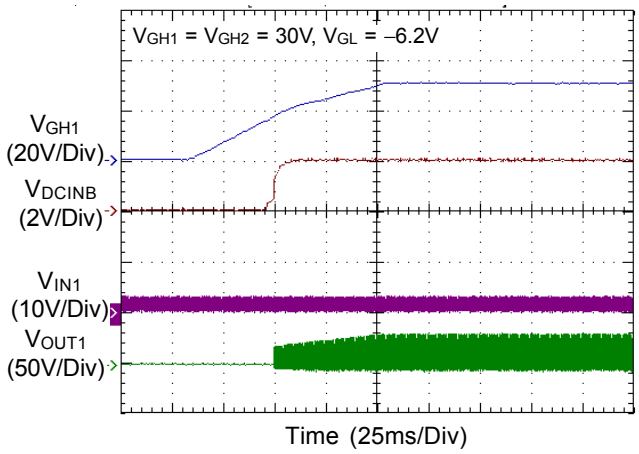
Discharge Function when Power On



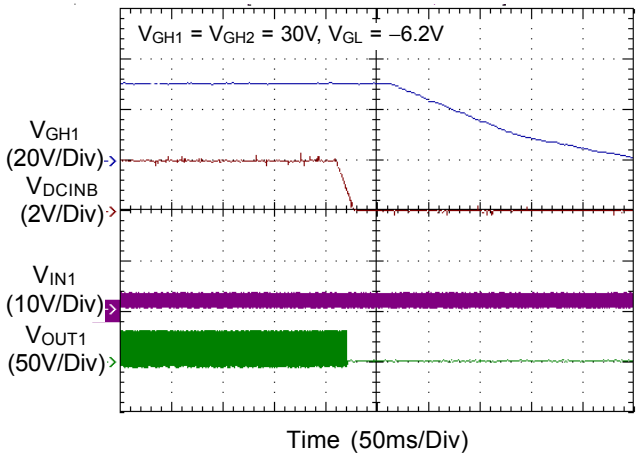
Discharge Function when Power Off



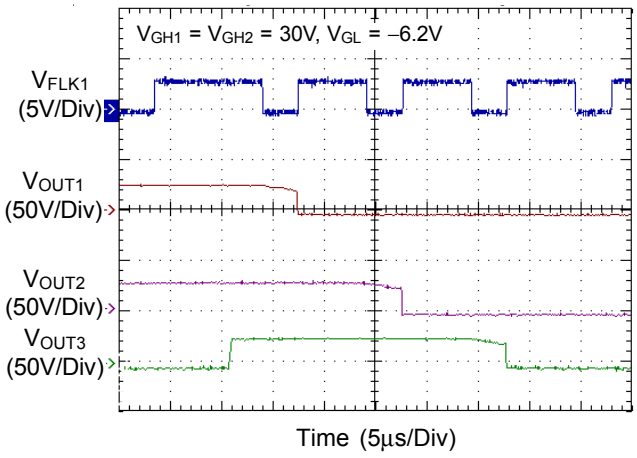
Level Shift Power On



Level Shift Power Off



V_{GPM} Function



Applications Information

The RT8910A is a ten-channel level shifter, which is designed for GIP panel. VGH1 and VGH2 are positive supplies and VGL is the negative supply. DISCHARGE and OUT1 to OUT7 channels are supplied from VGH1 and OUT8 to OUT9 channels are supplied from VGH2. VGH1 and VGH2 can be connected together. DISCHARGE is used for discharge function, OUT1 to 6 are used for clock (CLK1 to CLK6), OUT7 is used for start pulse (V_{ST}), and OUT 8 to OUT9 are used for EVEN/ODD function.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-28L 4x5 package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 3.57W for WQFN-28L 4x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

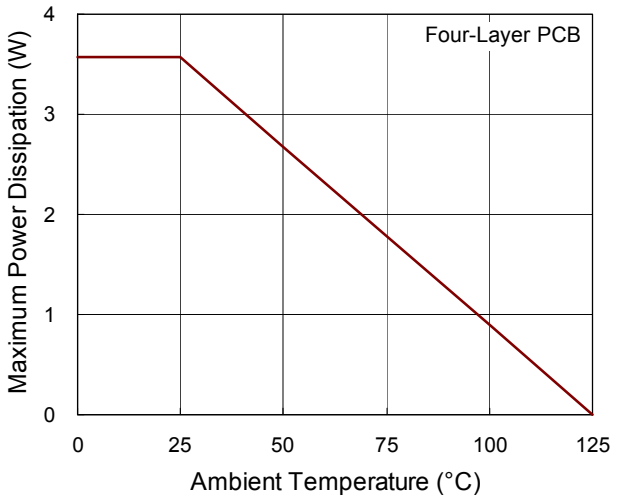


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Consideration

For best performance of the RT8910A, some recommended layout guidelines are provided just as follows :

- For good regulation, place the power components as close as possible.

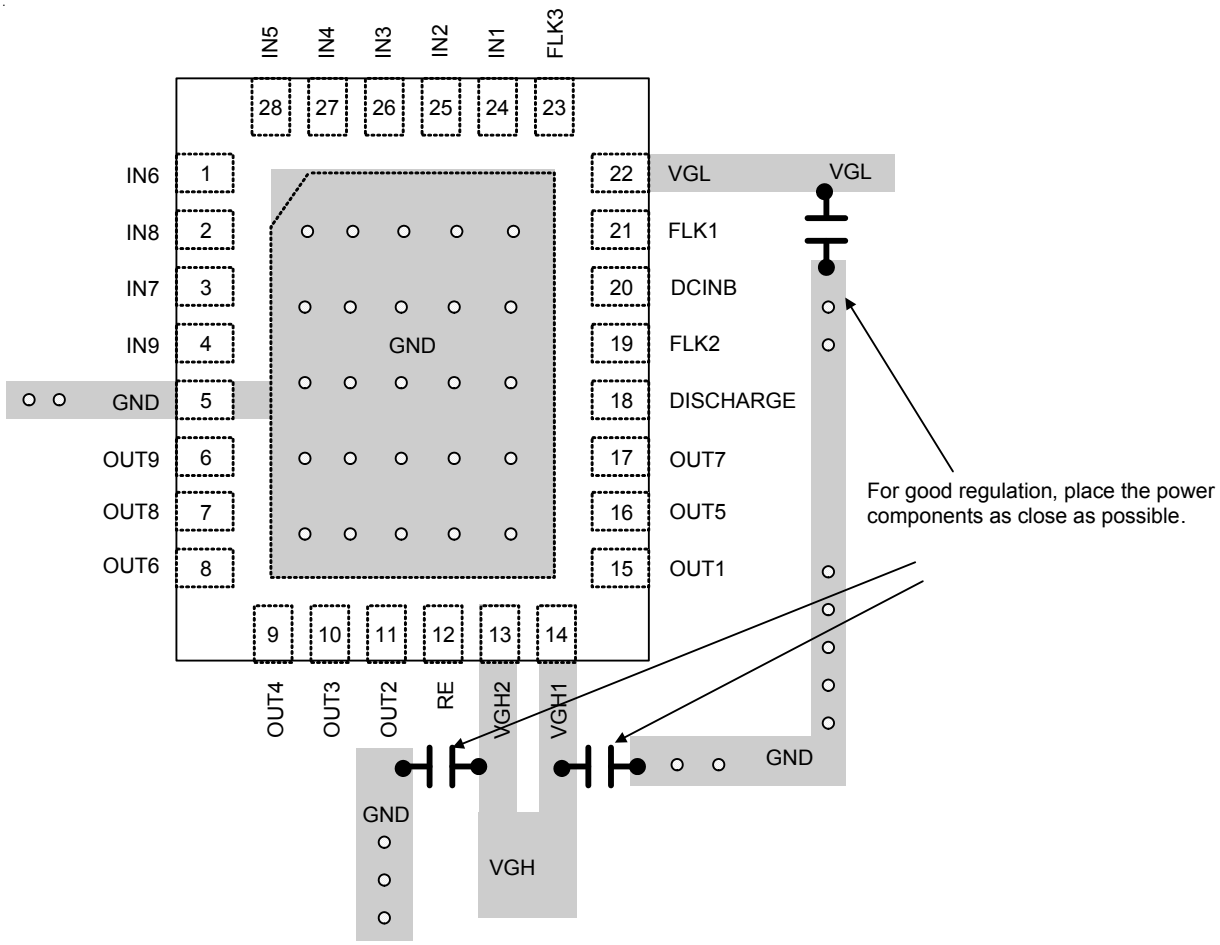
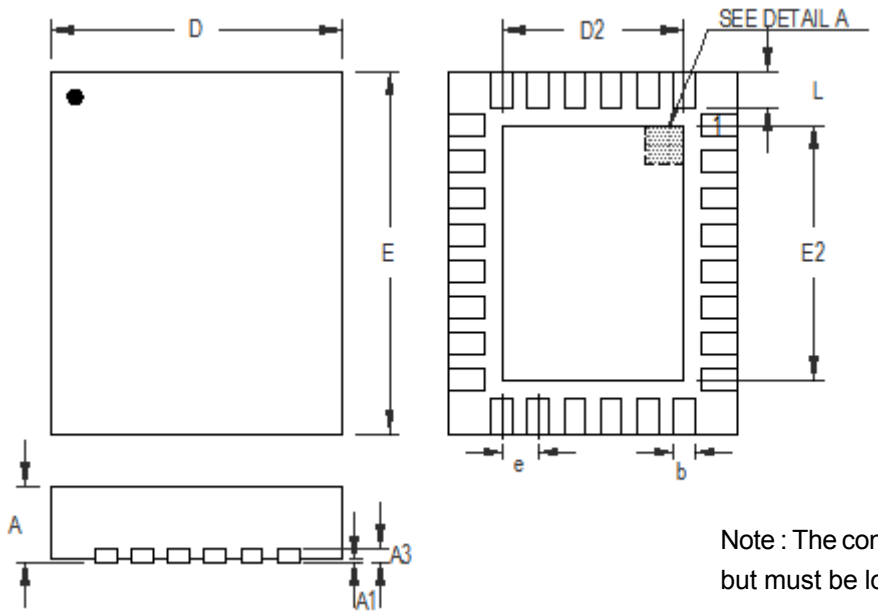
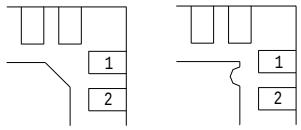


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.900	4.100	0.154	0.161
D2	2.600	2.700	0.102	0.106
E	4.900	5.100	0.193	0.201
E2	3.600	3.700	0.142	0.146
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 28L QFN 4x5 Package

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